LOW SKEW 1 TO 4 CLOCK BUFFER

ICS556-04

Description

The ICS556-04 is a low-skew, crystal input compatible clock buffer with oscillator. This device offers the lowest skew.

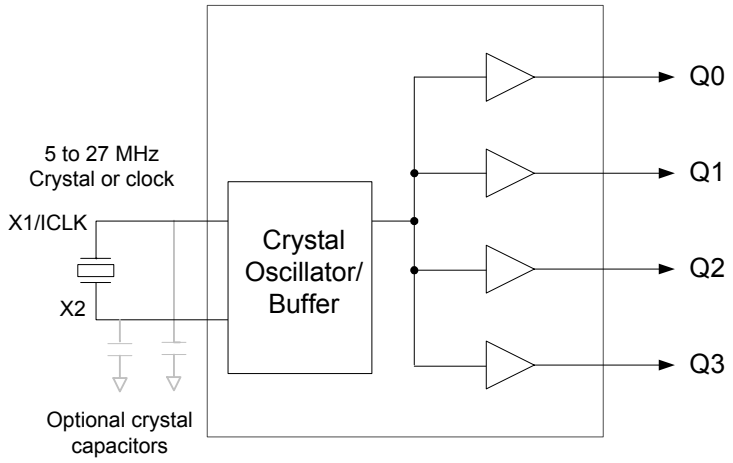
See the ICS552-02 for a 1-to-8 low skew buffer. For more than eight outputs see the MK74CBxxx Buffalo™ series of clock drivers.

IDT makes many non-PLL and PLL-based low-skew output devices. Contact IDT for all of your clocking needs.

Features

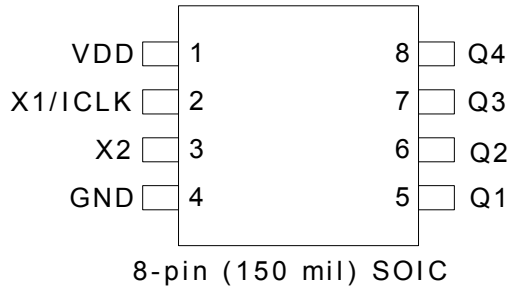
- Extremely low-skew outputs (50 ps maximum)
- Packaged in 8-pin SOIC
- Operating voltages of 2.5 to 5.0 V
- Low-power CMOS technology
- Industrial temperature range
- Pb (lead) free package

Block Diagram



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Pin Assignment



8-pin (150 mil) SOIC

Pin Descriptions

Pin Number	Pin Name	Pin Type	Pin Description
1	VDD	Power	Connect to +2.5 V, +3.3 V or +5.0 V.
2	X1/ICLK	Input	Crystal or clock input (5 V tolerant input). Connect to 5 to 27 MHz input.
3	X2	Input	Connect to a fundamental mode crystal. Leave open for clock input.
4	GND	Power	Connect to ground.
5	Q1	Output	Clock Output 1.
6	Q2	Output	Clock Output 2.
7	Q3	Output	Clock Output 3.
8	Q4	Output	Clock Output 3.

External Components

A minimum number of external components are required for proper operation. A decoupling capacitor of 0.01 µF should be connected between VDD on pin 1 and GND on pin 4, as close to the device as possible. A 33Ω series terminating resistor may be used on each clock output if the trace is longer than 1 inch.

To achieve the low output skew that the ICS556-04 is capable of, careful attention must be paid to board layout. Essentially, all four outputs must have identical terminations, identical loads, and identical trace geometries. If not, the output skew will be degraded. For example, using a 30Ω series termination on one output (with 33Ω on the others) will cause at least 15 ps of skew.

Crystal Information

The crystal used should be a fundamental mode (do not use third overtone), parallel resonant. Crystal capacitors should be connected from pins X1 to ground and X2 to ground to optimize the initial accuracy. The value of these capacitors is given by the following equation:

Crystal caps (pF) = (CL - 6) x 2

In the equation, CL is the crystal load capacitance. So, for a crystal with a 16 pF load capacitance, two 20 pF [(16-6) x 2] capacitors should be used.

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Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the ICS556-04. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Item	Rating
Supply Voltage, VDD	7 V
Output Enable and All Outputs	-0.5 V to VDD+0.5 V
ICLK	-0.5 V to 5.5 V
Ambient Operating Temperature	-40 to +85 ° C
Storage Temperature	-65 to +150° C
Junction Temperature	125° C
Soldering Temperature	260° C

Recommended Operation Conditions

Parameter	Min.	Typ.	Max.	Units
Ambient Operating Temperature	-40		+85	° C
Power Supply Voltage (measured in respect to GND)	+2.375		+5.25	V

DC Electrical Characteristics

VDD=2.5 V ±5%, Ambient temperature -40 to +85 ° C, unless stated otherwise

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Operating Voltage	VDD		2.375		2.625	V
Input High Voltage	V_{IH}		2.0			V
Input Low Voltage	V_{IL}				0.8	V
Output High Voltage	V_{OH}	I_{OH} = -12 mA	2			V
Output Low Voltage	V_{OL}	I_{OL} = 12 mA			0.4	V
Operating Supply Current	IDD	No load, 27MHz		25		mA
Nominal Output Impedance	Z_O			20		Ω
Short Circuit Current	I_{OS}			±28		mA

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DC Electrical Characteristics (continued)

VDD=3.3 V ±5% , Ambient temperature -40 to +85 °C, unless stated otherwise

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Operating Voltage	VDD		3.15		3.45	V
Input High Voltage	V_{IH}		2.0			V
Input Low Voltage	V_{IL}				0.8	V
Output High Voltage	V_{OH}	I_{OH} = -25 mA	2.4			V
Output Low Voltage	V_{OL}	I_{OL} = 25 mA			0.4	V
Output High Voltage (CMOS Level)	V_{OH}	I_{OH} = -12 mA	VDD-0.4			V
Operating Supply Current	IDD	No load, 27 MHz		35		mA
Nominal Output Impedance	Z_O			20		Ω
Short Circuit Current	I_{OS}			±50		mA

VDD=5 V ±5% , Ambient temperature -40 to +85 °C, unless stated otherwise

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Operating Voltage	VDD		4.75		5.25	V
Input High Voltage	V_{IH}		2.0			V
Input Low Voltage	V_{IL}				0.8	V
Output High Voltage	V_{OH}	I_{OH} = -35 mA	2.4			V
Output Low Voltage	V_{OL}	I_{OL} = 35 mA			0.4	V
Output High Voltage (CMOS Level)	V_{OH}	I_{OH} = -12 mA	VDD-0.4			V
Operating Supply Current	IDD	No load, 27 MHz		45		mA
Nominal Output Impedance	Z_O			20		Ω
Short Circuit Current	I_{OS}			±80		mA

Notes:
1. Nominal switching threshold is VDD/2

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AC Electrical Characteristics

VDD = 2.5 V ±5%, Ambient Temperature -40 to +85 °C, unless stated otherwise

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input Frequency			5		27	MHz
Output Rise Time	t_{OR}	0.8 to 2.0 V, C_L=15 pF		1.8	2.5	ns
Output Fall Time	t_{OF}	2.0 to 0.8 V, C_L=15 pF		1.8	2.5	ns
Output to output skew	Note 1	Rising edges at VDD/2		0	50	ps
Duty Cycle		Measured at VDD/2	45	50	55	%

VDD = 3.3 V ±5%, Ambient Temperature -40 to +85 °C, unless stated otherwise

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input Frequency			5		27	MHz
Output Rise Time	t_{OR}	0.8 to 2.0 V, C_L=15 pF		0.6	1.0	ns
Output Fall Time	t_{OF}	2.0 to 0.8 V, C_L=15 pF		0.6	1.0	ns
Output to output skew	Note 1	Rising edges at VDD/2		0	50	ps
Duty Cycle		Measured at VDD/2	45	50	55	%
Phase Noise at 1MHz from carrier				-125		dBc/Hz
Clock Jitter RMS 1KHz to 1MHz					6	ps

VDD = 5 V ±5%, Ambient Temperature -40 to +85 °C, unless stated otherwise

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input Frequency			5		27	MHz
Output Rise Time	t_{OR}	0.8 to 2.0 V, C_L=15 pF		0.3	0.7	ns
Output Fall Time	t_{OF}	2.0 to 0.8 V, C_L=15 pF		0.3	0.7	ns
Output to output skew	Note 1	Rising edges at VDD/2		0	50	ps
Duty Cycle		Measured at VDD/2	45	50	55	%

Notes: 1. Between any two outputs with equal loading.

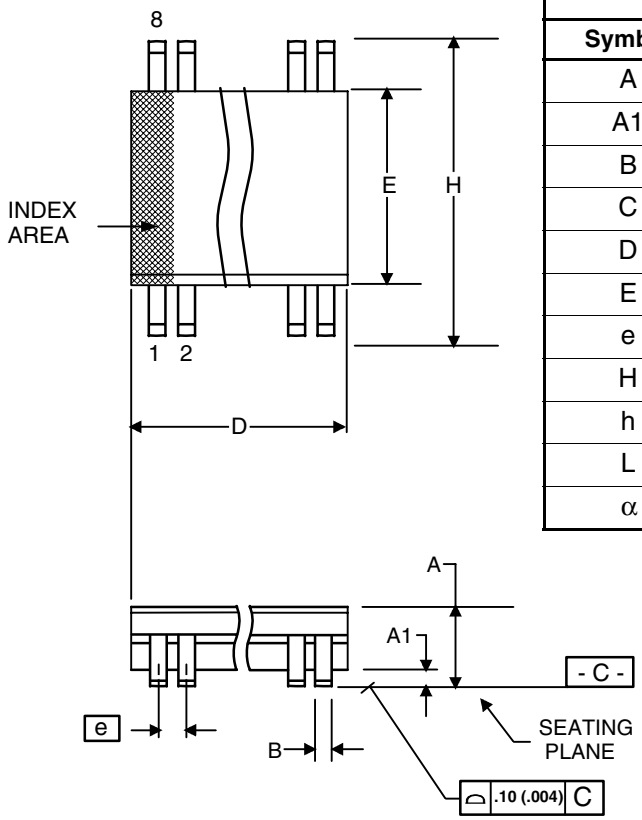
Thermal Characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Thermal Resistance Junction to Ambient	θ_{JA}	Still air		150		°C/W
	θ_{JA}	1 m/s air flow		140		°C/W
	θ_{JA}	3 m/s air flow		120		°C/W
Thermal Resistance Junction to Case	θ_{JC}			40		°C/W

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Package Outline and Package Dimensions (8-pin SOIC, 150 Mil. Narrow Body)

Package dimensions are kept current with JEDEC Publication No. 95



	Millimeters		Inches	
Symbol	**Min**	**Max**	**Min**	**Max**
A	1.35	1.75	.0532	.0688
A1	0.10	0.25	.0040	.0098
B	0.33	0.51	.013	.020
C	0.19	0.25	.0075	.0098
D	4.80	5.00	.1890	.1968
E	3.80	4.00	.1497	.1574
e	1.27 BASIC		0.050 BASIC	
H	5.80	6.20	.2284	.2440
h	0.25	0.50	.010	.020
L	0.40	1.27	.016	.050
α	0°	8°	0°	8°

Ordering Information

Part / Order Number	Marking	Shipping Packaging	Package	Temperature
556M-04ILF	556M04IL	Tubes	8-pin SOIC	-40 to +85° C
556M-04ILFT	556M04IL	Tape and Reel	8-pin SOIC	-40 to +85° C

"LF" denotes Pb free package.

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Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

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