Programmable Frequency Generator & Integrated Buffers for Pentium III Processor

Recommended Application:

Single chip clock solution for IA platform.

Output Features:

- 3 - CPU @ 2.5V
- 13 - SDRAM @ 3.3V
- 6 - PCI @3.3V,
- 2 - AGP @ 3.3V
- 1 - 48MHz, @3.3V fixed.
- 1 - 24/48MHz, @3.3V selectable by I^2C (Default is 24MHz)
- 2 - REF @3.3V, 14.318MHz.

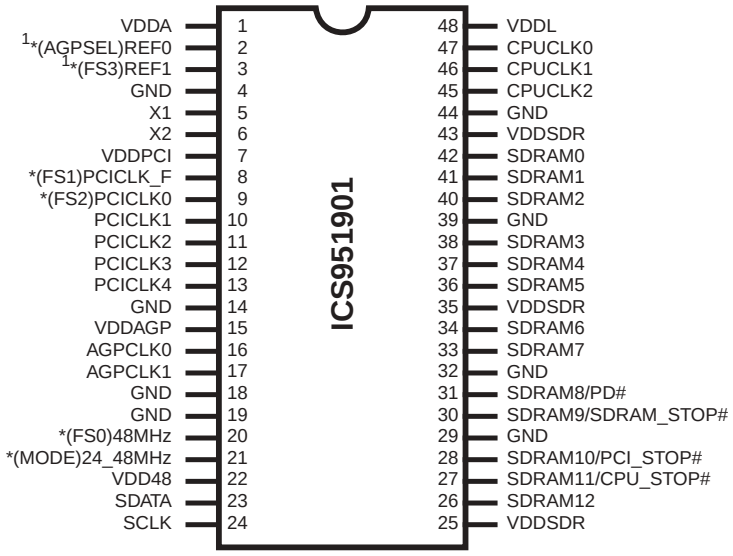
Features:

- Programmable ouput frequency.
- Programmable ouput rise/fall time.
- Programmable SDRAM and CPU skew.
- Spread spectrum for EMI control typically by 7dB to 8dB, with programmable spread percentage.
- Watchdog timer technology to reset system if over-clocking causes malfunction.
- Uses external 14.318MHz crystal.
- FS pins for frequency select

Skew Specifications:

- CPU - CPU: < 175ps
- SDRAM - SDRAM < 250ps (except SDRAM12)
- PCI - PCI: < 500ps
- CPU (early) - PCI: 1-4ns (typ. 2ns)

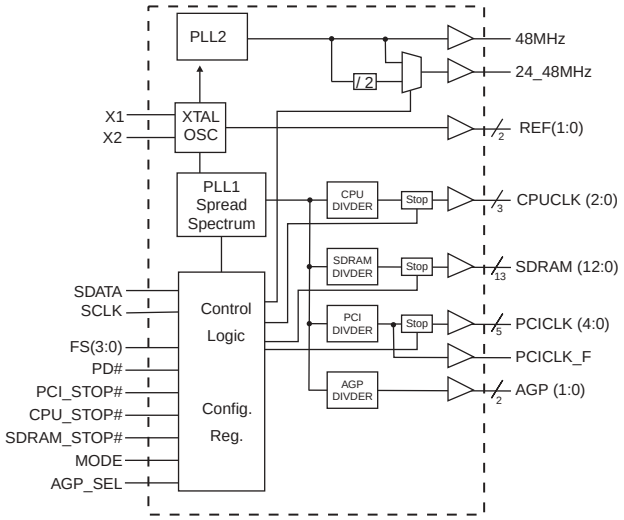
Pin Configuration



48-Pin 300mil SSOP

* These inputs have a 120K pull down to GND.
[1] These are double strength.

Block Diagram



Functionality

Bit2	FS3 Bit7	FS2 Bit6	FS1 Bit5	FS0 Bit4	CPU MHz	SDRAM MHz	PCI MHz	AGP1 SEL=1	AGP0 SEL=0
0	0	0	0	0	66.67	66.67	33.33	66.67	64
0	0	0	0	1	66.67	100.00	33.33	66.67	64
0	0	0	1	0	66.67	133.34	33.33	66.67	64
0	0	0	1	1	75.00	75.00	37.50	75.00	64
0	0	1	0	0	83.31	83.31	33.32	66.64	64
0	0	1	0	1	90.00	90.00	30.00	60.00	64
0	0	1	1	0	95.00	95.00	31.67	63.33	64
0	0	1	1	1	100.00	66.67	33.33	66.67	64
0	1	0	0	0	100.00	100.00	33.33	66.67	64
0	1	0	0	1	100.00	133.34	33.33	66.67	64
0	1	0	1	0	105.00	105.00	35.00	70.00	64
0	1	0	1	1	112.00	112.00	33.60	67.20	64
0	1	1	0	0	117.99	117.99	35.40	70.80	64
0	1	1	0	1	124.09	124.09	31.02	62.05	64
0	1	1	1	0	133.34	100.00	33.33	66.67	64
0	1	1	1	1	133.34	133.34	33.33	66.67	64

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General Description

The **ICS951901** is a single chip clock solution for desktop designs using 630S chipsets. It provides all necessary clock signals for such a system.

The **ICS951901** belongs to ICS new generation of programmable system clock generators. It employs serial programming I^2C interface as a vehicle for changing output functions, changing output frequency, configuring output strength, configuring output to output skew, changing spread spectrum amount, changing group divider ratio and dis/enabling individual clocks. This device also has ICS propriety 'Watchdog Timer' technology which will reset the frequency to a safe setting if the system becomes unstable from over clocking.

Power Groups

Analog
VDDA = X1, X2, Core, PLL
VDD48 = 48MHz, 24MHz, fixed PLL
Digital
VDDPCI = PCICLK_F, PCICLK
VDDSDR = SDRAM
VDDAGP=AGP, REF

MODE Pin Power Management Control Input

MODE Pin 21	Pin 27	Pin 28	Pin 30	Pin 31
0	SDRAM11	SDRAM10	SDRAM9	SDRAM8
1	CPU_STOP#	PCI_STOP#	SDRAM_STOP#	PD#

Pin Configuration

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
1, 7, 15, 22, 25, 35, 43	VDD	PWR	3.3V Power supply for SDRAM output buffers, PCI output buffers, reference output buffers and 48MHz output
2	AGPSEL	IN	AGP frequency select pin.
	REF0	OUT	14.318 MHz reference clock.
3	FS3	IN	Frequency select pin.
	REF1	OUT	14.318 MHz reference clock.
4, 14, 18, 19, 29, 32, 39, 44	GND	PWR	Ground pin for 3V outputs.
5	X1	IN	Crystal input,nominally 14.318MHz.
6	X2	OUT	Crystal output, nominally 14.318MHz.
8	FS1	IN	Frequency select pin.
	PCICLK_F	OUT	PCI clock output, not affected by PCI_STOP#
9	FS2	IN	Frequency select pin.
	PCICLK0	OUT	PCI clock output.
13, 12, 11, 10	PCICLK (4:1)	OUT	PCI clock outputs.
17, 16,	AGP (1:0)	OUT	AGP outputs defined as 2X PCI. These may not be stopped.
20	FS0	IN	Frequency select pin.
	48MHz	OUT	48MHz output clock
21	MODE	IN	Pin 27, 28, 30, & 31 function select pin 0=Desktop 1=Mobile mode
	24_48MHz	OUT	Clock output for super I/O/USB default is 24MHz
23	SDATA	I/O	Data pin for I^2C circuitry 5V tolerant
24	SCLK	IN	Clock pin of I^2C circuitry 5V tolerant
27	CPU_STOP#	IN	Stops all PCICLKs besides the PCICLK_F clocks at logic 0 level, when input is low and MODE pin is in Mobile mode
	SDRAM11	OUT	SDRAM clock output
28	PCI_STOP#	IN	Stops all CPUCLKs clocks at logic 0 level, when input is low and MODE pin is in Mobile mode
	SDRAM10	OUT	SDRAM clock output
30	SDRAM9	OUT	SDRAM clock output
	SDRAM_STOP#	IN	Stops all SDRAM clocks at logic 0 level, when input is low and MODE pin is in Mobile mode
31	PD#	IN	Asynchronous active low input pin used to power down the device into a low power state. The internal clocks are disabled and the VCO and the crystal are stopped. The latency of the power down will not be greater than 3ms
	SDRAM8	OUT	SDRAM clock output
26 33, 34, 36, 37, 38, 40, 41, 42	SDRAM (12, 7:0)	OUT	SDRAM clock outputs
45, 46, 47	CPUCLK (2:0)	OUT	CPU clock outputs.
48	VDDL	PWR	Power pin for the CPUCLKs. 2.5V

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Serial Configuration Command Bitmap

Byte0: Functionality and Frequency Select Register (default = 0)

		Description										
Bit	Bit2	FS3 Bit7	FS2 Bit6	FS1 Bit5	FS0 Bit4	CPU MHz	SDRAM MHz	PCI MHz	AGP1 SEL=1	AGP0 SEL=0	Spread %	PWD
	0	0	0	0	0	66.67	66.67	33.33	66.67	64	± 0.35% center spread	
	0	0	0	0	1	66.67	100.00	33.33	66.67	64	± 0.35% center spread	
	0	0	0	1	0	66.67	133.34	33.33	66.67	64	± 0.35% center spread	
	0	0	0	1	1	75.00	75.00	37.50	75.00	64	± 0.35% center spread	
	0	0	1	0	0	83.31	83.31	33.32	66.64	64	± 0.35% center spread	
	0	0	1	0	1	90.00	90.00	30.00	60.00	64	± 0.35% center spread	
	0	0	1	1	0	95.00	95.00	31.67	63.33	64	± 0.35% center spread	
	0	0	1	1	1	100.00	66.67	33.33	66.67	64	± 0.35% center spread	
	0	1	0	0	0	100.00	100.00	33.33	66.67	64	± 0.35% center spread	
	0	1	0	0	1	100.00	133.34	33.33	66.67	64	± 0.35% center spread	
	0	1	0	1	0	105.00	105.00	35.00	70.00	64	± 0.35% center spread	
	0	1	0	1	1	112.00	112.00	33.60	67.20	64	± 0.35% center spread	
	0	1	1	0	0	117.99	117.99	35.40	70.80	64	± 0.35% center spread	
	0	1	1	0	1	124.09	124.09	31.02	62.05	64	± 0.35% center spread	
Bit 2	0	1	1	1	0	133.34	100.00	33.33	66.67	64	± 0.35% center spread	00000
Bit 7:4	0	1	1	1	1	133.34	133.34	33.33	66.67	64	± 0.35% center spread	Note1
	1	0	0	0	0	75.00	100.00	37.50	75.00	64	± 0.35% center spread	
	1	0	0	0	1	75.00	112.50	32.14	64.29	64	± 0.35% center spread	
	1	0	0	1	0	75.00	150.00	32.14	64.29	64	± 0.35% center spread	
	1	0	0	1	1	83.31	111.07	33.32	66.64	64	± 0.35% center spread	
	1	0	1	0	0	83.32	166.65	31.25	62.49	64	± 0.35% center spread	
	1	0	1	0	1	90.00	60.00	30.00	60.00	64	± 0.35% center spread	
	1	0	1	1	0	90.00	120.00	30.00	60.00	64	± 0.35% center spread	
	1	0	1	1	1	95.00	63.33	31.67	63.33	64	± 0.35% center spread	
	1	1	0	0	0	95.00	126.66	31.67	63.33	64	± 0.35% center spread	
	1	1	0	0	1	105.00	70.00	35.00	70.00	64	± 0.35% center spread	
	1	1	0	1	0	105.00	140.00	35.00	70.00	64	± 0.35% center spread	
	1	1	0	1	1	112.00	84.00	33.60	67.20	64	± 0.35% center spread	
	1	1	1	0	0	117.99	88.49	35.40	70.80	64	± 0.35% center spread	
	1	1	1	0	1	124.09	93.07	31.02	62.05	64	± 0.35% center spread	
	1	1	1	1	0	129.99	97.49	32.50	64.99	64	± 0.35% center spread	
	1	1	1	1	1	140.00	105.00	35.00	70.00	64	± 0.35% center spread	
Bit 3	0 - Frequency is selected by hardware select, Latched inputs 1 - Frequency is selected by Bit, 2 7:4											0
Bit 1	0 - Normal 1 - Spread Spectrum Enabled											1
Bit 0	0 - Running 1 - Tristate all outputs											0

Note1:
Default at power-up will be for latched logic inputs to define frequency, as displayed by Bit 3.

Note: PWD = Power-Up Default

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Byte 1: CPU, Active/Inactive Register (1= enable, 0 = disable)

BIT	PIN#	PWD	DESCRIPTION
Bit 7	-	1	Sel24_48 (1:24MHz, 0:48MHz)
Bit 6	-	1	Reserved
Bit 5	-	1	Reserved
Bit 4	-	1	Reserved
Bit 3	47	1	CPUCLK0
Bit 2	46	1	CPUCLK1
Bit 1	45	1	CPUCLK2
Bit 0	-	1	Reserved

Byte 2: PCI, Active/Inactive Register (1= enable, 0 = disable)

BIT	PIN#	PWD	DESCRIPTION
Bit 7	-	1	Reserved
Bit 6	-	1	Reserved
Bit 5	13	1	PCICLK4
Bit 4	12	1	PCICLK3
Bit 3	11	1	PCICLK2
Bit 2	10	1	PCICLK1
Bit 1	9	1	PCICLK0
Bit 0	8	1	PCICLK_F

Byte 3: SDRAM, Active/Inactive Register (1= enable, 0 = disable)

BIT	PIN#	PWD	DESCRIPTION
Bit 7	33	1	SDRAM7
Bit 6	34	1	SDRAM6
Bit 5	36	1	SDRAM5
Bit 4	37	1	SDRAM4
Bit 3	38	1	SDRAM3
Bit 2	40	1	SDRAM2
Bit 1	41	1	SDRAM1
Bit 0	42	1	SDRAM0

Byte 4: SDRAM , Active/Inactive Register (1= enable, 0 = disable)

BIT	PIN#	PWD	DESCRIPTION
Bit 7	-	1	Reserved
Bit 6	21	1	24_48MHz
Bit 5	20	1	48MHz
Bit 4	26	1	SDRAM12
Bit 3	27	1	SDRAM11
Bit 2	28	1	SDRAM10
Bit 1	30	1	SDRAM9
Bit 0	31	1	SDRAM8

Byte 5: AGP, Active/Inactive Register (1= enable, 0 = disable)

BIT	PIN#	PWD	DESCRIPTION
Bit 7	-	X	FS3 (Readback)
Bit 6	-	X	FS2 (Readback)
Bit 5	-	X	FS1 (Readback)
Bit 4	-	X	FS0 (Readback)
Bit 3	3	1	REF0
Bit 2	2	1	REF1
Bit 1	17	1	AGPCLK1
Bit 0	16	1	AGPCLK0

Notes:

1. Inactive means outputs are held LOW and are disabled from switching.
2. Latched Frequency Selects (FS#) will be inverted logic load of the input frequency select pin conditions.

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Byte 6: Control , Active/Inactive Register
(1= enable, 0 = disable)

BIT	PIN#	PWD	DESCRIPTION
Bit7	2,3	0	REF strength 0=1X, 1=2X
Bit6	45	0	CPUCLK2 - Stop - Control 0=CPU_STOP# will control CPUCLK2, 1=CPUCLK2 is free running even if CPU_STOP# is low
Bit5	-	X	AGPSEL (Readback)
Bit4	-	X	MODE (Readback)
Bit3	-	X	CPU_STOP# (Readback)
Bit2	-	X	PCI_STOP# (Readback)
Bit1	-	X	SDRAM_STOP# (Readback)
Bit0	-	0	AGP Speed Toggle 0=AGPSEL (pin2) will be determined by latch input setting, 1=AGPSEL will be opposite of latch input setting

Byte 7: Vendor ID Register
(1= enable, 0 = disable)

BIT	PIN#	PWD	DESCRIPTION
Bit 7	-	0	Reserved
Bit 6	-	0	Reserved
Bit 5	-	1	Reserved
Bit 4	-	0	Reserved
Bit 3	-	1	Reserved
Bit 2	-	0	Reserved
Bit 1	-	0	Reserved
Bit 0	-	1	Reserved

Byte 8: Byte Count and Read Back Register
(1= enable, 0 = disable)

BIT	PIN#	PWD	DESCRIPTION
Bit 7	-	0	Reserved
Bit 6	-	0	Reserved
Bit 5	-	0	Reserved
Bit 4	-	0	Reserved
Bit 3	-	0	Reserved
Bit 2	-	1	Reserved
Bit 1	-	0	Reserved
Bit 0	-	0	Reserved

Byte 9: Watchdog Timer Count Register

Bit	PWD	Description
Bit 7	0	The decimal representation of these 8 bits correspond to 290ms or 1ms the watchdog timer will wait before it goes to alarm mode and reset the frequency to the safe setting. Default at power up is 16X 290ms = 4.6 seconds.
Bit 6	0	
Bit 5	0	
Bit 4	1	
Bit 3	0	
Bit 2	0	
Bit 1	0	
Bit 0	0	

Byte 10: VCO Control Selection Bit &
Watchdog Timer Control Register

Bit	PWD	Description
Bit 7	0	0=Hw/B0 freq / 1=B11 & 12 freq
Bit 6	0	WD Enable 0=disable / 1=enable
Bit 5	0	WD Status 0=normal / 1=alarm
Bit 4	0	WD Safe Frequency, Byte 0 bit 2
Bit 3	0	WD Safe Frequency, FS3
Bit 2	0	WD Safe Frequency, FS2
Bit 1	0	WD Safe Frequency, FS1
Bit 0	0	WD Safe Frequency, FS0

Note: FS values in bit [0:4] will correspond to Byte 0 FS values. Default safe frequency is same as 00000 entry in byte0.

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Byte 11: VCO Frequency Control Register

Bit	PWD	Description
Bit 7	X	VCO Divider Bit0
Bit 6	X	REF Divider Bit6
Bit 5	X	REF Divider Bit5
Bit 4	X	REF Divider Bit4
Bit 3	X	REF Divider Bit3
Bit 2	X	REF Divider Bit2
Bit 1	X	REF Divider Bit1
Bit 0	X	REF Divider Bit0

Note: The decimal representation of these 7 bits (Byte 11 [6:0]) + 2 is equal to the REF divider value .

Notes:

1. PWD = Power on Default

Byte 12: VCO Frequency Control Register

Bit	PWD	Description
Bit 7	X	VCO Divider Bit8
Bit 6	X	VCO Divider Bit7
Bit 5	X	VCO Divider Bit6
Bit 4	X	VCO Divider Bit5
Bit 3	X	VCO Divider Bit4
Bit 2	X	VCO Divider Bit3
Bit 1	X	VCO Divider Bit2
Bit 0	X	VCO Divider Bit1

Note: The decimal representation of these 9 bits (Byte 12 bit [7:0] & Byte 11 bit [7]) + 8 is equal to the VCO divider value. For example if VCO divider value of 36 is desired, user need to program 36 - 8 = 28, namely, 0, 00011100 into byte 12 bit & byte 11 bit 7.

Byte 13: Spread Sectrum Control Register

Bit	PWD	Description
Bit 7	X	Spread Spectrum Bit7
Bit 6	X	Spread Spectrum Bit6
Bit 5	X	Spread Spectrum Bit5
Bit 4	X	Spread Spectrum Bit4
Bit 3	X	Spread Spectrum Bit3
Bit 2	X	Spread Spectrum Bit2
Bit 1	X	Spread Spectrum Bit1
Bit 0	X	Spread Spectrum Bit0

Note: Please utilize software utility provided by ICS Application Engineering to configure spread spectrum. Incorrect spread percentage may cause system failure.

Byte 14: Spread Sectrum Control Register

Bit	PWD	Description
Bit 7	X	Reserved
Bit 6	X	Reserved
Bit 5	X	Reserved
Bit 4	X	Spread Spectrum Bit12
Bit 3	X	Spread Spectrum Bit11
Bit 2	X	Spread Spectrum Bit10
Bit 1	X	Spread Spectrum Bi 9
Bit 0	X	Spread Spectrum Bit8

Note: Please utilize software utility provided by ICS Application Engineering to configure spread spectrum. Incorrect spread percentage may cause system failure.

Byte 15: Output Skew Control

Bit	PWD	Description
Bit 7	1	SDRAM 12 Skew Control
Bit 6	0	
Bit 5	0	SDRAM (11:0) Skew Control
Bit 4	1	
Bit 3	1	CPUCLK2 Skew Control
Bit 2	1	
Bit 1	1	CPUCLK (1:0) Skew Control
Bit 0	0	

Byte 16: Output Skew Control

Bit	PWD	Description
Bit 7	X	Reserved
Bit 6	X	Reserved
Bit 5	X	Reserved
Bit 4	X	Reserved
Bit 3	X	Reserved
Bit 2	X	Reserved
Bit 1	X	Reserved
Bit 0	X	Reserved

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Byte 17: Output Rise/Fall Time Select Register

Bit	PWD	Description
Bit 7	1	PCI (3:0) Slew Rate Control
Bit 6	0	
Bit 5	1	PCI_F Slew Rate Control
Bit 4	0	
Bit 3	1	CPUCLK2 Slew Rate Control
Bit 2	0	
Bit 1	0	CPUCLK1 Slew rate Control
Bit 0		

Byte 18: Output Rise/Fall Time Select Register

Bit	PWD	Description
Bit 7	1	SDRAM12: Slew Rate Control
Bit 6	0	
Bit 5	1	AGPCLK1: Slew Rate Control
Bit 4	0	
Bit 3	1	AGPCLK0: Slew Rate Control
Bit 2	0	
Bit 1	1	PCICLK4: Slew Rate Control
Bit 0	0	

Byte 19: Output Rise/Fall Time Select Register

Bit	PWD	Description
Bit 7	1	48MHz: Slew Rate Control
Bit 6	0	
Bit 5	1	24_48MHz: Slew Rate Control
Bit 4	0	
Bit 3	1	REF1: Slew Rate Control
Bit 2	0	REF0: Slew Rate Control
Bit 1	1	SDRAM (11:0): Slew Rate Control
Bit 0	0	

Byte 20: Output Rise/Fall Time Select Register

Bit	PWD	Description
Bit 7	0	Reserved
Bit 6	0	Reserved
Bit 5	0	Reserved
Bit 4	0	Reserved
Bit 3	0	Reserved
Bit 2	0	Reserved
Bit 1	0	CPUCLK0 Slew Rate Control
Bit 0		

VCO Programming Constrains

VCO Frequency ..... 150MHz to 500MHz
VCO Divider Range ..... 8 to 519
REF Divider Range ..... 2 to 129
Phase Detector Stability ..... 0.3536 to 1.4142

Useful Formula

VCO Frequency = 14.31818 x VCO/REF divider value

Phase Detector Stabiliy = 14.038 x (VCO divider value)$^{-0.5}$

To program the VCO frequency for over-clocking.

0. Before trying to program our clock manually, consider using ICS provided software utilities for easy programming.

1. Select the frequency you want to over-clock from with the desire gear ratio (i.e. CPU:SDRAM:3V66:PCI ratio) by writing to byte 0, or using initial hardware power up frequency.

2. Write 0001, 1001 (19_H) to byte 8 for readback of 21 bytes (byte 0-20).

3. Read back byte 11-20 and copy values in these registers.

4. Re-initialize the write sequence.

5. Write a '1' to byte 9 bit 7 and write to byte 11 & 12 with the desired VCO & REF divider values.

6. Write to byte 13 to 20 with the values you copy from step 3. This maintains the output spread, skew and slew rate.

7. The above procedure is only needed when changing the VCO for the 1st pass. If VCO frequency needed to be changed again, user only needs to write to byte 11 and 12 unless the system is to reboot.

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Absolute Maximum Ratings

Supply Voltage . . . . . 5.5 V
Logic Inputs . . . . . GND –0.5 V to V_{DD} +0.5 V
Ambient Operating Temperature . . . . . 0°C to +70°C
Case Temperature . . . . . 115°C
Storage Temperature . . . . . –65°C to +150°C

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Electrical Characteristics - Input/Supply/Common Output Parameters

TA = 0 - 70°C; Supply Volt age VDD = 3.3 V +/-5%VDDL = 2.5 V +/-5% (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input High Voltage	V_{IH}		2		V_{DD} + 0.3	V
Input Low Voltage	V_{IL}		V_{SS} - 0.3		0.8	V
Supply Current	I_{DD}	C_L=30 pF, CPU @ 66, 100 MHz		390	400	mA
Power Down	PD			300	600	mA
Input frequency	Fi	V_{DD} = 3.3 V;	12	14.32	16	MHz
Input Capacitance[1]	C_{IN}	Logic Inputs			5	pF
	C_{INX}	X1 & X2 pins	27		45	pF
Transition Time	T_{trans}	To 1st crossing of target Freq.			3	
Settling Time	T_S	From 1st crossing to 1% target Freq.				
Clk Stabilization[1]	T_{STAB}	From V_{DD}= 3.3 V to 1% target Freq.			3	ms
Skew	$T_{CPU-PCI}$	CPUV_T= 1.5 V PCI V_T=1.25V	1	1.9	4	ns
Skew	$T_{CPU-SDRAM}$	CPUV_T= 1.5 V SDRAM V_T=1.25	-500	-300	0	ps

[1] Guaranteed by design, not 100% tested in production.

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Electrical Characteristics - CPU

T_A = 0 - 70°C; V_{DDL} = 2.5 V +/-5%; VDDL = 2.5 V +/-5%; C_L = 10-20 pF (unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance[1]	R_{DSP2B}	$V_O = V_{DD}*(0.5)$	10		20	
Output Impedance[1]	R_{DSN2B}	$V_O = V_{DD}*(0.5)$	10		20	
Output High Voltage	V_{OH2B}	I_{OH} = -12.0 mA	2			V
Output Low Voltage	V_{OL2B}	I_{OL} = 12 mA			0.4	V
Output High Current	I_{OH2B}	V_{OH} = 1.7 V			-19	mA
Output Low Current	I_{OL2B}	V_{OL} = 0.7 V	19			mA
Rise Time[1]	t_{r2B}	V_{OL} = 0.4 V, V_{OH} = 2.0 V	0.4	1.2	1.6	ns
Fall Time[1]	t_{f2B}	V_{OH} = 2.0 V, V_{OL} = 0.4 V	0.4	1.1	1.6	ns
Duty Cycle[1]	d_{t2B}	V_T = 1.25 V	45	46.9	55	%
Skew window[0:1]	t_{sk2B}	V_T = 1.25 V		43	175	ps
Skew window[0:2]	t_{sk2B}	V_T = 1.25 V		142	375	ps
Jitter, Cycle-to-cycle[1]	$t_{jcyc-cyc}$	V_T = 1.25 V, CPU=66 MHz		177	250	ps

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - 24-48MHz

T_A = 0 - 70°C; V_{DD} = 3.3 V +/-5%;VDDL = 2.5 V +/-5%; C_L = 10-20 pF (unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance	R_{DSP5B}[1]	$V_O = V_{DD}*(0.5)$	20		60	
Output Impedance	R_{DSN5B}[1]	$V_O = V_{DD}*(0.5)$	20		60	
Output High Voltage	V_{OH15}	I_{OH} = -14 mA	2.4			V
Output Low Voltage	V_{OL5}	I_{OL} = 6.0 mA			0.4	V
Output High Current	I_{OH5}	V_{OH} = 2.0 V			-20	mA
Output Low Current	I_{OL5}	V_{OL} = 0.8 V	10			mA
Rise Time[1]	t_{r5}	V_{OL} = 0.4 V, V_{OH} = 2.4 V	0.4	1.45	4	ns
Fall Time[1]	t_{f5}	V_{OH} = 2.4 V, V_{OL} = 0.4 V	0.4	1.5	4	ns
Duty Cycle[1]	d_{t5}	V_T = 1.5 V	45	52.5	55	%
Jitter	$t_{cycle\ to\ cycle}$	V_T = 1.5 V		210	500	ps

[1]Guaranteed by design, not 100% tested in production.

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Electrical Characteristics - PCI

T_A = 0 - 70°C; V_{DD} = 3.3 V +/-5%; VDDL = 2.5 V +/-5%; C_L = 10-30 pF (unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance	R_{DSP1B}[1]	$V_O = V_{DD}*(0.5)$	12		55	
Output Impedance	R_{DSN1B}[1]	$V_O = V_{DD}*(0.5)$	12		55	
Output High Voltage	V_{OH1}	I_{OH} = -1 mA	2.4			V
Output Low Voltage	V_{OL1}	I_{OL} = 1 mA			0.55	V
Output High Current	I_{OH1}	$V_{OH @ MIN}$ = 1.0 V			-29	mA
Output Low Current	I_{OL1}	$V_{OL @ MIN}$ = 1.95 V	29			mA
Rise Time[1]	t_{r1}	V_{OL} = 0.4 V, V_{OH} = 2.4 V	0.5	2.3	2.5	ns
Fall Time[1]	t_{f1}	V_{OH} = 2.4 V, V_{OL} = 0.4 V	0.5	2.3	2.5	ns
Duty Cycle[1]	d_{t1}	V_T = 1.5 V	45	51.2	55	%
Skew window[1]	t_{sk1}	V_T = 1.5 V		108	500	ps
Jitter, Cycle-to-cycle[1]	$t_{jcyc-cyc1}$	V_T = 1.5 V		353	500	ps

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - SDRAM

T_A = 0 - 70°C; V_{DD} = 3.3 V +/-5%;VDDL = 2.5 V +/-5%; C_L = 20-30 pF (unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance	R_{DSP3B}[1]	$V_O = V_{DD}*(0.5)$	10		24	
Output Impedance	R_{DSN3B}[1]	$V_O = V_{DD}*(0.5)$	10		24	
Output High Voltage	V_{OH3}	I_{OH} = -18 mA	2.4			V
Output Low Voltage	V_{OL3}	I_{OL} = 9.4 mA			0.4	V
Output High Current	I_{OH3}	V_{OH} = 2.0 V			-46	mA
Output Low Current	I_{OL3}	V_{OL} = 0.8V				mA
Rise Time[1]	t_{r3}	V_{OL} = 0.4 V, V_{OH} = 2.4 V		0.8	1.6	ns
Fall Time[1]	t_{f3}	V_{OH} = 2.4 V, V_{OL} = 0.4 V		0.8	1.6	ns
Duty Cycle[1]	d_{t3}	V_T = 1.5 V	45	48.5	55	%
Skew window[1(0:11)]	t_{sk3}	V_T = 1.5 V		192	250	ps
Skew window[1(0:12)]	t_{sk3}	V_T = 1.5 V		290	500	ps
Jitter, Cycle-to-cycle[1]	$t_{jcyc-cyc3}$	V_T = 1.5 V, CPU=66,100,133 MHz		173	250	ps

[1]Guaranteed by design, not 100% tested in production.

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Electrical Characteristics - AGP

T_A = 0 - 70°C; V_{DD}=3.3V +/-5%; C_L = 20 pF (unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance	R_{DSP4B}[1]	$V_O=V_{DD}*(0.5)$	12		55	
Output Impedance	R_{DSN4B}[1]	$V_O=V_{DD}*(0.5)$	12		55	
Output High Voltage	V_{OH4B}	I_{OH} = -18 mA	2			V
Output Low Voltage	V_{OL4B}	I_{OL} = 18 mA			0.4	V
Output High Current	I_{OH4B}	V_{OH} = 2.0 V			-19	mA
Output Low Current	I_{OL4B}	V_{OL} = 0.8 V	19			mA
Rise Time[1]	t_{r4B}	V_{OL} = 0.4 V, V_{OH} = 2.4 V	0.5	1.5	2	ns
Fall Time[1]	t_{f4B}	V_{OH} = 2.4 V, V_{OL} = 0.4 V	0.5	1.6	2	ns
Duty Cycle[1]	d_{t4B}	V_T = 1.5 V	45	52.3	55	%
Skew window1	tsk[1]	V_T = 1.5 V		55.5	175	ps
Jitter Cyc-Cyc	tjcyc-cyc[1]	V_T = 1.5 V		239	500	ps

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - REF

TA = 0 - 70°C; VDD = 3.3 V +/-5%;VDDL = 2.5 V +/-5%; CL = 20 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	V_{OH5}	I_{OH} = -12 mA	2.4			V
Output Low Voltage	V_{OL5}	I_{OL} = 9 mA			0.4	V
Output High Current	I_{OH5}	V_{OH} = 2.0 V			-22	mA
Output Low Current	I_{OL5}	V_{OL} = 0.8 V	16			mA
Rise Time[1]	t_{r5}	V_{OL} = 0.4 V, VOH = 2.4 V		1.8	4	ns
Fall Time[1]	t_{f5}	V_{OH} = 2.4 V, VOL = 0.4 V		1.9	4	ns
Duty Cycle[1]	d_{t5}	V_T = 50%	45	54.5	55	%

[1]Guaranteed by design, not 100% tested in production.

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General I²C serial interface information for the ICS951901

How to Write:

- Controller (host) sends a start bit.
- Controller (host) sends the write address D2 (H)
- ICS clock will ***acknowledge***
- Controller (host) sends a dummy command code
- ICS clock will ***acknowledge***
- Controller (host) sends a dummy byte count
- ICS clock will ***acknowledge***
- Controller (host) starts sending ***Byte 0 through Byte 28*** (see Note 2)
- ICS clock will ***acknowledge*** each byte ***one at a time***
- Controller (host) sends a Stop bit

How to Write:	
Controller (Host)	**ICS (Slave/Receiver)**
Start Bit	
Address D2(H)	
	ACK
Dummy Command Code	
	ACK
Dummy Byte Count	
	ACK
Byte 0	
	ACK
Byte 1	
	ACK
Byte 2	
	ACK
Byte 3	
	ACK
Byte 4	
	ACK
Byte 5	
	ACK
Byte 6	
	ACK
○	
○	○
○	○
	○
Byte 18	
	ACK
Byte 19	
	ACK
Byte 20	
	ACK
Stop Bit	

*See notes on the following page.

How to Read:

- Controller (host) will send start bit.
- Controller (host) sends the read address D3 (H)
- ICS clock will ***acknowledge***
- ICS clock will send the ***byte count***
- Controller (host) acknowledges
- ICS clock sends ***Byte 0 through byte 6 (default)***
- ICS clock sends ***Byte 0 through byte X (if $X_{(H)}$ was written to byte 6).***
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a stop bit

How to Read:	
Controller (Host)	**ICS (Slave/Receiver)**
Start Bit	
Address D3(H)	
	ACK
	Byte Count
ACK	
	Byte 0
ACK	
	Byte 1
ACK	
	Byte 2
ACK	
	Byte 3
ACK	
	Byte 4
ACK	
	Byte 5
ACK	
	Byte 6
ACK	
If 7_H has been written to B6	***Byte 7***
ACK	
○	○
○	○
○	○
If $1A_H$ has been written to B6	***Byte18***
ACK	
If $1B_H$ has been written to B6	***Byte 19***
ACK	
If $1C_H$ has been written to B6	***Byte 20***
ACK	
Stop Bit	

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Brief I²C registers description for ICS951901 Programmable System Frequency Generator

Register Name	Byte	Description	PWD Default
Functionality & Frequency Select Register	0	Output frequency, hardware / I²C frequency select, spread spectrum & output enable control register.	See individual byte description
Output Control Registers	1-6	Active / inactive output control registers/latch inputs read back.	See individual byte description
Vendor ID & Revision ID Registers	7	Byte 11 bit[7:4] is ICS vendor id - 1001. Other bits in this register designate device revision ID of this part.	See individual byte description
Byte Count Read Back Register	8	Writing to this register will configure byte count and how many byte will be read back. Do not write 00_H to this byte.	08_H
Watchdog Timer Count Register	9	Writing to this register will configure the number of seconds for the watchdog timer to reset.	10_H
Watchdog Control Registers	10 Bit [6:0]	Watchdog enable, watchdog status and programmable 'safe' frequency' can be configured in this register.	000,0000
VCO Control Selection Bit	10 Bit [7]	This bit select whether the output frequency is control by hardware/byte 0 configurations or byte 11&12 programming.	0
VCO Frequency Control Registers	11-12	These registers control the dividers ratio into the phase detector and thus control the VCO output frequency.	Depended on hardware/byte 0 configuration
Spread Spectrum Control Registers	13-14	These registers control the spread percentage amount.	Depended on hardware/byte 0 configuration
Group Skews Control Registers	15-16	Increment or decrement the group skew amount as compared to the initial skew.	See individual byte description
Output Rise/Fall Time Select Registers	17-20	These registers will control the output rise and fall time.	See individual byte description

Notes:

1. The ICS clock generator is a slave/receiver, I²C component. It can read back the data stored in the latches for verification. Readback will support standard SMBUS controller protocol. **The number of bytes to readback is defined by writing to byte 8.**
2. **When writing to byte 11 - 12, and byte 13 - 14, they must be written as a set.** If for example, only byte 14 is written but not 15, neither byte 14 or 15 will load into the receiver.
3. The data transfer rate supported by this clock generator is 100K bits/sec or less (standard mode)
4. The input is operating at 3.3V logic levels.
5. The data byte format is 8 bit bytes.
6. To simplify the clock generator I²C interface, the protocol is set to use only Block-Writes from the controller. The bytes must be accessed in sequential order from lowest to highest byte with the ability to stop after any complete byte has been transferred. The Command code and Byte count shown above must be sent, but the data is ignored for those two bytes. The data is loaded until a Stop sequence is issued.
7. At power-on, all registers are set to a default condition, as shown.

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Shared Pin Operation - Input/Output Pins

The I/O pins designated by (input/output) on the ICS951901 serve as dual signal functions to the device. During initial power-up, they act as input pins. The logic level (voltage) that is present on these pins at this time is read and stored into a 5-bit internal data latch. At the end of Power-On reset, (see AC characteristics for timing values), the device changes the mode of operations for these pins to an output function. In this mode the pins produce the specified buffered clocks to external loads.

To program (load) the internal configuration register for these pins, a resistor is connected to either the VDD (logic 1) power supply or the GND (logic 0) voltage potential. A 10 Kilohm (10K) resistor is used to provide both the solid CMOS programming voltage needed during the power-up programming period and to provide an insignificant load on the output clock during the subsequent operating period.

Figure 1 shows a means of implementing this function when a switch or 2 pin header is used. With no jumper is installed the pin will be pulled high. With the jumper in place the pin will be pulled low. If programmability is not necessary, than only a single resistor is necessary. The programming resistors should be located close to the series termination resistor to minimize the current loop area. It is more important to locate the series termination resistor close to the driver than the programming resistor.

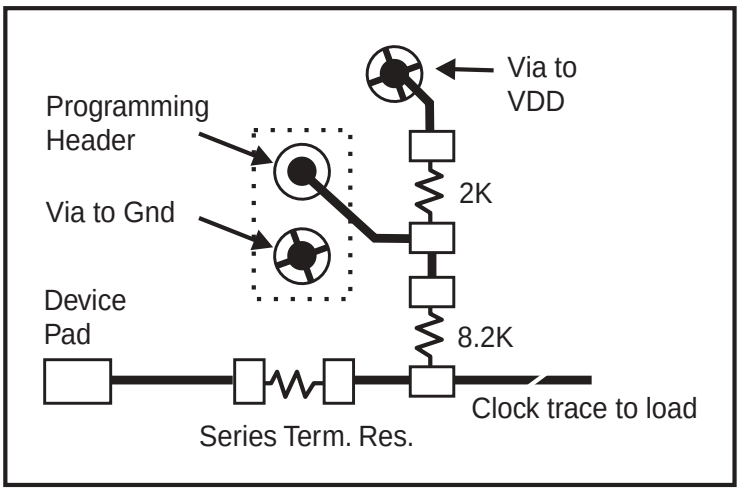
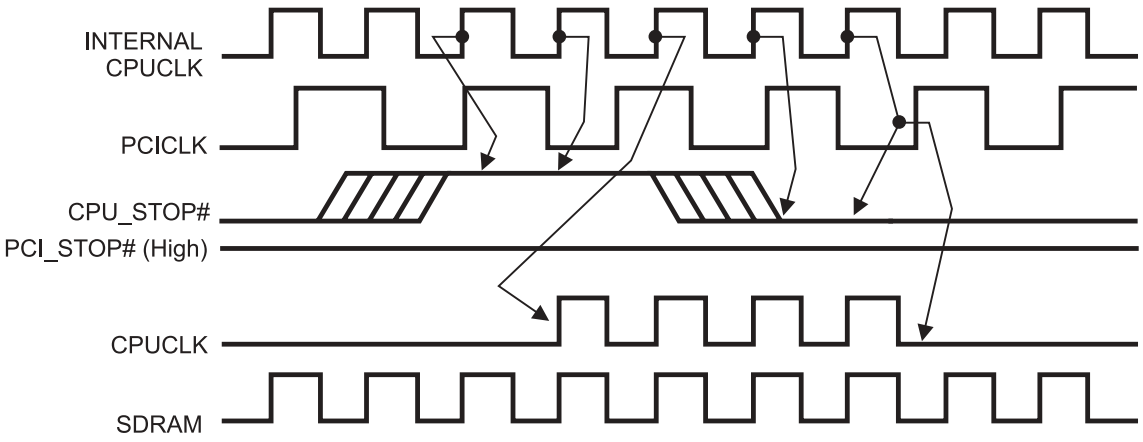


Fig. 1

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CPU_STOP# Timing Diagram

CPU_STOP# is an asychronous input to the clock synthesizer. It is used to turn off the CPU clocks for low power operation. CPU_STOP# is synchronized by the **ICS94209**. The minimum that the CPU clock is enabled (CPU_STOP# high pulse) is 100 CPU clocks. All other clocks will continue to run while the CPU clocks are disabled. The CPU clocks will always be stopped in a low state and start in such a manner that guarantees the high pulse width is a full pulse. CPU clock on latency is less than 4 CPU clocks and CPU clock off latency is less than 4 CPU clocks.



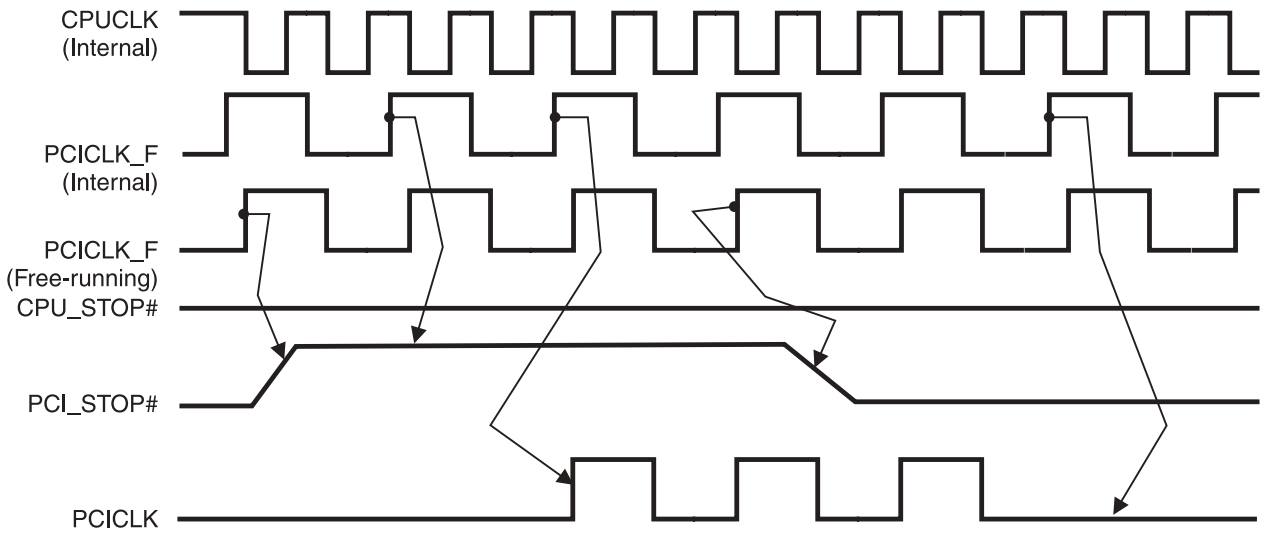
Notes:

1. All timing is referenced to the internal CPU clock.
2. CPU_STOP# is an asynchronous input and metastable conditions may exist. This signal is synchronized to the CPU clocks inside the ICS94209.
3. All other clocks continue to run undisturbed. (including SDRAM outputs).

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PCI_STOP# Timing Diagram

PCI_STOP# is an asynchronous input to the **ICS94209**. It is used to turn off the PCICLK clocks for low power operation. PCI_STOP# is synchronized by the **ICS94209** internally. The minimum that the PCICLK clocks are enabled (PCI_STOP# high pulse) is at least 10 PCICLK clocks. PCICLK clocks are stopped in a low state and started with a full high pulse width guaranteed. PCICLK clock on latency cycles are only one rising PCICLK clock off latency is one PCICLK clock.



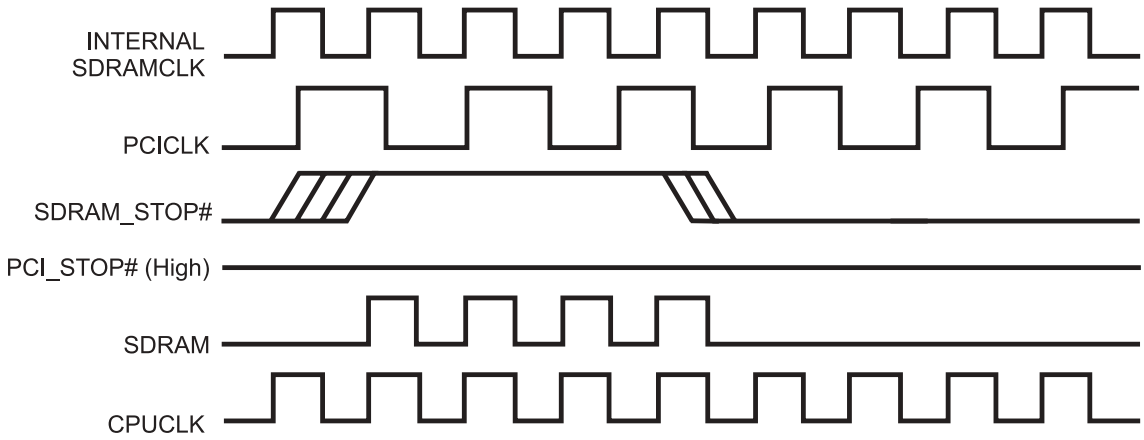
Notes:

1. All timing is referenced to the Internal CPUCLK (defined as inside the ICS94209 device.)
2. PCI_STOP# is an asynchronous input, and metastable conditions may exist. This signal is required to be synchronized inside the ICS94209.
3. All other clocks continue to run undisturbed.
4. CPU_STOP# is shown in a high (true) state.

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SDRAM_STOP# Timing Diagram

SDRAM_STOP# is an asychronous input to the clock synthesizer. It is used to stop SDRAM clocks for low power operation. SDRAM_STOP# is synchronized to complete it's current cycle, by the **ICS94209**. All other clocks will continue to run while the SDRAM clocks are disabled. The SDRAM clocks will always be stopped in a low state and start in such a manner that guarantees the high pulse width is a full pulse.



Notes:

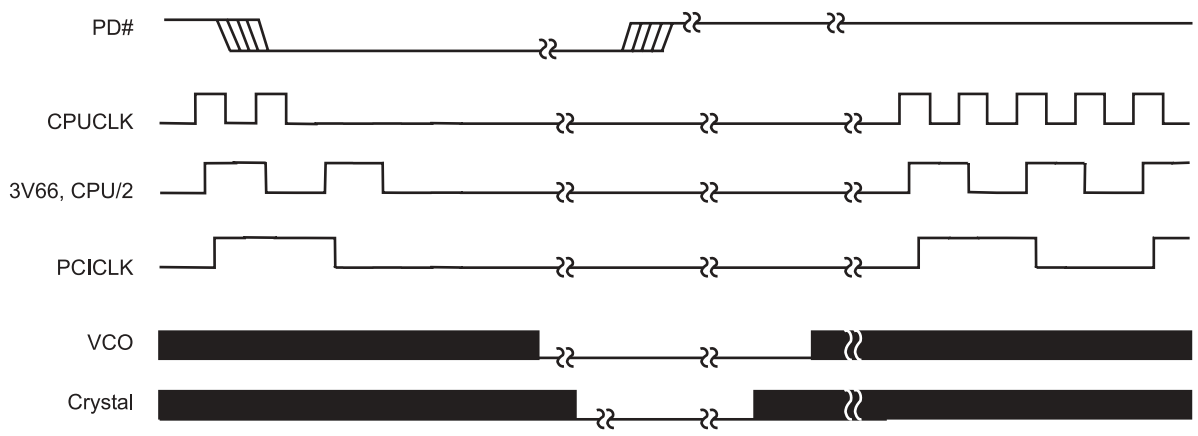
1. All timing is referenced to the internal CPU clock.
2. SDRAM is an asynchronous input and metastable conditions may exist. This signal is synchronized to the SDRAM clocks inside the ICS94209.
3. All other clocks continue to run undisturbed.

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PD# Timing Diagram

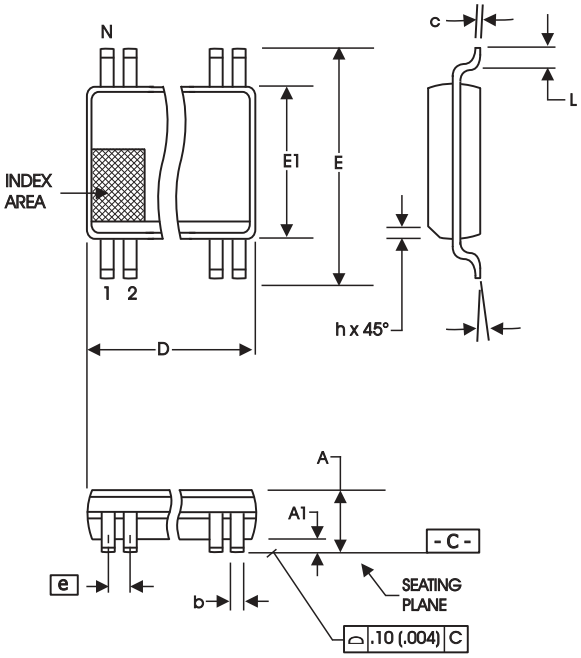
The power down selection is used to put the part into a very low power state without turning off the power to the part. PD# is an asynchronous active low input. This signal needs to be synchronized internal to the device prior to powering down the clock synthesizer.

Internal clocks are not running after the device is put in power down. When PD# is active low all clocks need to be driven to a low value and held prior to turning off the VCOs and crystal. The power up latency needs to be less than 3 mS. The power down latency should be as short as possible but conforming to the sequence requirements shown below. PCI_STOP# and CPU_STOP# are considered to be don't cares during the power down operations. The REF and 48MHz clocks are expected to be stopped in the LOW state as soon as possible. Due to the state of the internal logic, stopping and holding the REF clock outputs in the LOW state may require more than one clock cycle to complete.



Notes:
1. All timing is referenced to the Internal CPUCLK (defined as inside the ICS94209 device).
2. As shown, the outputs Stop Low on the next falling edge after PD# goes low.
3. PD# is an asynchronous input and metastable conditions may exist. This signal is synchronized inside this part.
4. The shaded sections on the VCO and the Crystal signals indicate an active clock.
5. Diagrams shown with respect to 133MHz. Similar operation when CPU is 100MHz.

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300 mil SSOP Package

SYMBOL	In Millimeters COMMON DIMENSIONS		In Inches COMMON DIMENSIONS	
	MIN	MAX	MIN	MAX
A	2.41	2.80	.095	.110
A1	0.20	0.40	.008	.016
b	0.20	0.34	.008	.0135
c	0.13	0.25	.005	.010
D	SEE VARIATIONS		SEE VARIATIONS	
E	10.03	10.68	.395	.420
E1	7.40	7.60	.291	.299
e	0.635 BASIC		0.025 BASIC	
h	0.38	0.64	.015	.025
L	0.50	1.02	.020	.040
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°

VARIATIONS

N	D mm.		D (inch)	
	MIN	MAX	MIN	MAX
48	15.75	16.00	.620	.630

Reference Doc.: JEDEC Publication 95, MO-118

10-0034

Ordering Information

ICS951901yFLF-T

Example:

ICS XXXXXX y F LF- T

- **Designation for tape and reel packaging**
- **Lead Free (Optional)**
- **Package Type**
  F = SSOP
- **Revision Designator** (will not correlate with datasheet revision)
- **Device Type**
- **Prefix**
  ICS = Standard Device

0670B—07/15/04

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