Programmable Timing Control Hub™ for Mobile P4™ Systems

Recommended Application:

Supports CK410M with additional SRC clock support

Output Features:

- 2 - 0.7V current-mode differential CPU pairs
- 9 - 0.7V current-mode differential SRC pair for SATA and PCI Express*
- 1 - 0.7V current-mode differential CPU/SRC selectable pair
- 4 - PCI (33MHz)
- 1 - PCICLK_F, (33MHz) free-running
- 1 - USB, 48MHz
- 1 - DOT, 96MHz, 0.7V current differential pair
- 1 - REF, double-strength 14.318MHz

Key Specifications:

- CPU outputs cycle-cycle jitter < 85ps
- SRC outputs cycle-cycle jitter < 125ps
- PCI outputs cycle-cycle jitter < 500ps
- +/- 100ppm frequency accuracy on USB

Features/Benefits:

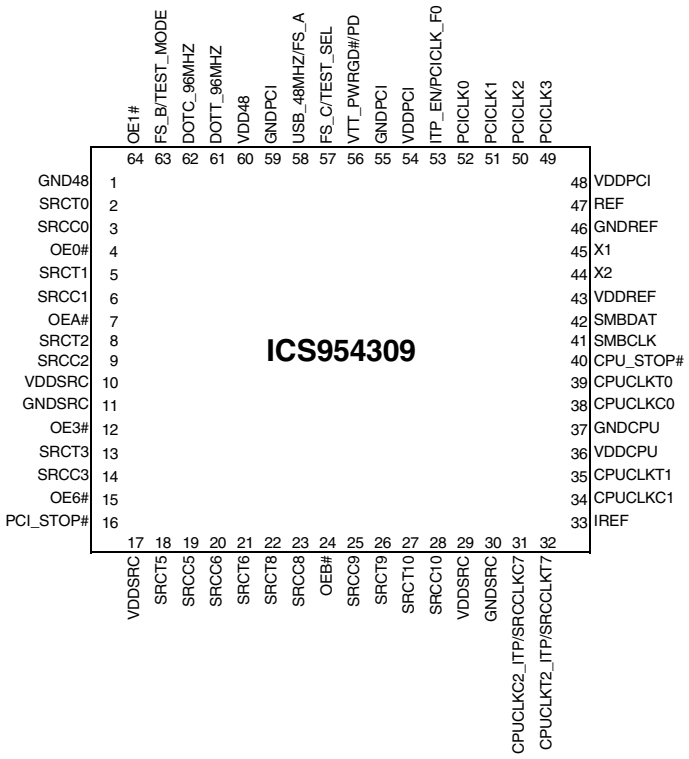
- +/- 300 ppm accuracy clocks for Serial-ATA and PCI Express and CPU clocks
- Supports spread spectrum modulation, 0 to -0.5% down spread for CPU, SRC and PCI clocks
- Supports CPU clocks up to 400MHz
- Uses external 14.318MHz crystal, external crystal load caps are required for frequency tuning
- Supports undriven differential CPU, SRC pair in PD# for power management.

Functionality

FS_C[1]	FS_B[2]	FS_A[2]	CPU MHz	SRC MHz	PCI MHz	REF MHz	USB MHz	DOT MHz
0	0	0	266.66	100.00	33.33	14.318	48.00	96.00
0	0	1	133.33	100.00	33.33	14.318	48.00	96.00
0	1	0	200.00	100.00	33.33	14.318	48.00	96.00
0	1	1	166.66	100.00	33.33	14.318	48.00	96.00
1	0	0	333.33	100.00	33.33	14.318	48.00	96.00
1	0	1	100.00	100.00	33.33	14.318	48.00	96.00
1	1	0	400.00	100.00	33.33	14.318	48.00	96.00
1	1	1	RESERVED			14.318	48.00	96.00

1. FS_C is a three-level input. Please see V_{IL_FS} and V_{IH_FS} specifications in the Input/Supply/Common Output Parameters Table for correct values. Also refer to the Test Clarification Table.
2. FS_B and FS_A are low-threshold inputs. Please see the V_{IL_FS} and V_{IH_FS} specifications in the Input/Supply/Common Output Parameters Table for correct values.

Pin Configuration



64-pin MLF

*Other names and brands may be claimed as the property of others.

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Pin Description

PIN #	PIN NAME	PIN TYPE	DESCRIPTION
1	GND48	PWR	Ground pin for the 48MHz outputs
2	SRCT0	OUT	True clock of differential SRC clock pair.
3	SRCC0	OUT	Complement clock of differential SRC clock pair.
4	OE0#	IN	Active low input for enabling DIF pair 0. 1 = tri-state outputs, 0 = enable outputs
5	SRCT1	OUT	True clock of differential SRC clock pair.
6	SRCC1	OUT	Complement clock of differential SRC clock pair.
7	OEA#	IN	Active low input for enabling outputs. 1 = tri-state outputs, 0 = enable outputs
8	SRCT2	OUT	True clock of differential SRC clock pair.
9	SRCC2	OUT	Complement clock of differential SRC clock pair.
10	VDDSRC	PWR	Supply for SRC clocks, 3.3V nominal
11	GNDSRC	PWR	Ground pin for the SRC outputs
12	OE3#	IN	Active low input for enabling DIF pair 3. 1 = tri-state outputs, 0 = enable outputs
13	SRCT3	OUT	True clock of differential SRC clock pair.
14	SRCC3	OUT	Complement clock of differential SRC clock pair.
15	OE6#	IN	Active low input for enabling DIF pair 6. 1 = tri-state outputs, 0 = enable outputs
16	PCI_STOP#	IN	Stops all PCICLKs at logic 0 level, when low. Free running PCICLKs are not effected by this input.
17	VDDSRC	PWR	Supply for SRC clocks, 3.3V nominal
18	SRCT5	OUT	True clock of differential SRC clock pair.
19	SRCC5	OUT	Complement clock of differential SRC clock pair.
20	SRCC6	OUT	Complement clock of differential push-pull SRC clock pair.
21	SRCT6	OUT	True clock of differential push-pull SRC clock pair.
22	SRCT8	OUT	True clock of differential SRC clock pair.
23	SRCC8	OUT	Complement clock of differential SRC clock pair.
24	OEB#	IN	Active low input for enabling outputs. 1 = tri-state outputs, 0 = enable outputs
25	SRCC9	OUT	Complement clock of differential SRC clock pair.
26	SRCT9	OUT	True clock of differential push-pull SRC clock pair.
27	SRCT10	OUT	True clock of differential push-pull SRC clock pair.
28	SRCC10	OUT	Complement clock of differential SRC clock pair.
29	VDDSRC	PWR	Supply for SRC clocks, 3.3V nominal
30	GNDSRC	PWR	Ground pin for the SRC outputs
31	CPUCLKC2_ITP/SRCCLKC7	OUT	Complementary clock of CPU_ITP/SRC differential pair CPU_ITP/SRC output. These are current mode outputs. External resistors are required for voltage bias. Selected by ITP_EN input.
32	CPUCLKT2_ITP/SRCCLKT7	OUT	True clock of CPU_ITP/SRC differential pair CPU_ITP/SRC output. These are current mode outputs. External resistors are required for voltage bias. Selected by ITP_EN input.

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Pin Description (Continued)

PIN #	PIN NAME	PIN TYPE	DESCRIPTION
33	IREF	OUT	This pin establishes the reference current for the differential current-mode output pairs. This pin requires a fixed precision resistor tied to ground in order to establish the appropriate current. 475 ohms is the standard value.
34	CPUCLKC1	OUT	Complementary clock of differential pair CPU outputs. These are current mode outputs. External resistors are required for voltage bias.
35	CPUCLKT1	OUT	True clock of differential pair CPU outputs. These are current mode outputs. External resistors are required for voltage bias.
36	VDDCPU	PWR	Supply for CPU clocks, 3.3V nominal
37	GNDCPU	PWR	Ground pin for the CPU outputs
38	CPUCLKC0	OUT	Complementary clock of differential pair CPU outputs. These are current mode outputs. External resistors are required for voltage bias.
39	CPUCLKT0	OUT	True clock of differential pair CPU outputs. These are current mode outputs. External resistors are required for voltage bias.
40	CPU_STOP#	IN	Stops all CPUCLK, except those set to be free running clocks
41	SMBCLK	IN	Clock pin of SMBUS circuitry, 5V tolerant
42	SMBDAT	I/O	Data pin of SMBUS circuitry, 5V tolerant
43	VDDREF	PWR	Ref, XTAL power supply, nominal 3.3V
44	X2	OUT	Crystal output, Nominally 14.318MHz
45	X1	IN	Crystal input, Nominally 14.318MHz.
46	GNDREF	PWR	Ground pin for the REF outputs.
47	REF	OUT	14.318 MHz reference clock.
48	VDDPCI	PWR	Power supply for PCI clocks, nominal 3.3V
49	PCICLK3	OUT	PCI clock output.
50	PCICLK2	OUT	PCI clock output.
51	PCICLK1	OUT	PCI clock output.
52	PCICLK0	OUT	PCI clock output.
53	ITP_EN/PCICLK_F0	I/O	Free running PCI clock not affected by PCI_STOP#. ITP_EN: latched input to select pin functionality 1 = CPU_ITP pair 0 = SRC pair
54	VDDPCI	PWR	Power supply for PCI clocks, nominal 3.3V
55	GNDPCI	PWR	Ground pin for the PCI outputs
56	VTT_PWRGD#/PD	IN	Vtt_PwrGd# is an active low input used to determine when latched inputs are ready to be sampled. PD is an asynchronous active high input pin used to put the device into a low power state. The internal clocks, PLLs and the crystal oscillator are stopped.
57	FS_C/TEST_SEL	IN	3.3V tolerant input for CPU frequency selection. Low voltage threshold inputs, see input electrical characteristics for Vil_FS and Vih_FS values. TEST_Sel: 3-level latched input to enable test mode. Refer to Test Clarification Table
58	USB_48MHZ/FS_A	I/O	Frequency select latch input pin / Fixed 48MHz USB clock output. 3.3V.
59	GNDPCI	PWR	Ground pin for the PCI outputs
60	VDD48	PWR	Power pin for the 48MHz output.3.3V
61	DOTT_96MHZ	OUT	True clock of differential pair for 96.00MHz DOT clock.
62	DOTC_96MHZ	OUT	Complement clock of differential pair for 96.00MHz DOT clock.
63	FS_B/TEST_MODE	IN	3.3V tolerant input for CPU frequency selection. Refer to input electrical characteristics for Vil_FS and Vih_FS values. TEST_MODE is a real time input to select between Hi-Z and REF/N divider mode while in test mode. Refer to Test Clarification Table.
64	OE1#	IN	Active low input for enabling DIF pair 1. 1 = tri-state outputs, 0 = enable outputs

NOTE: Only OE# pins have internal pull-up resistors. No other inputs have pull-up or pull-down resistors.

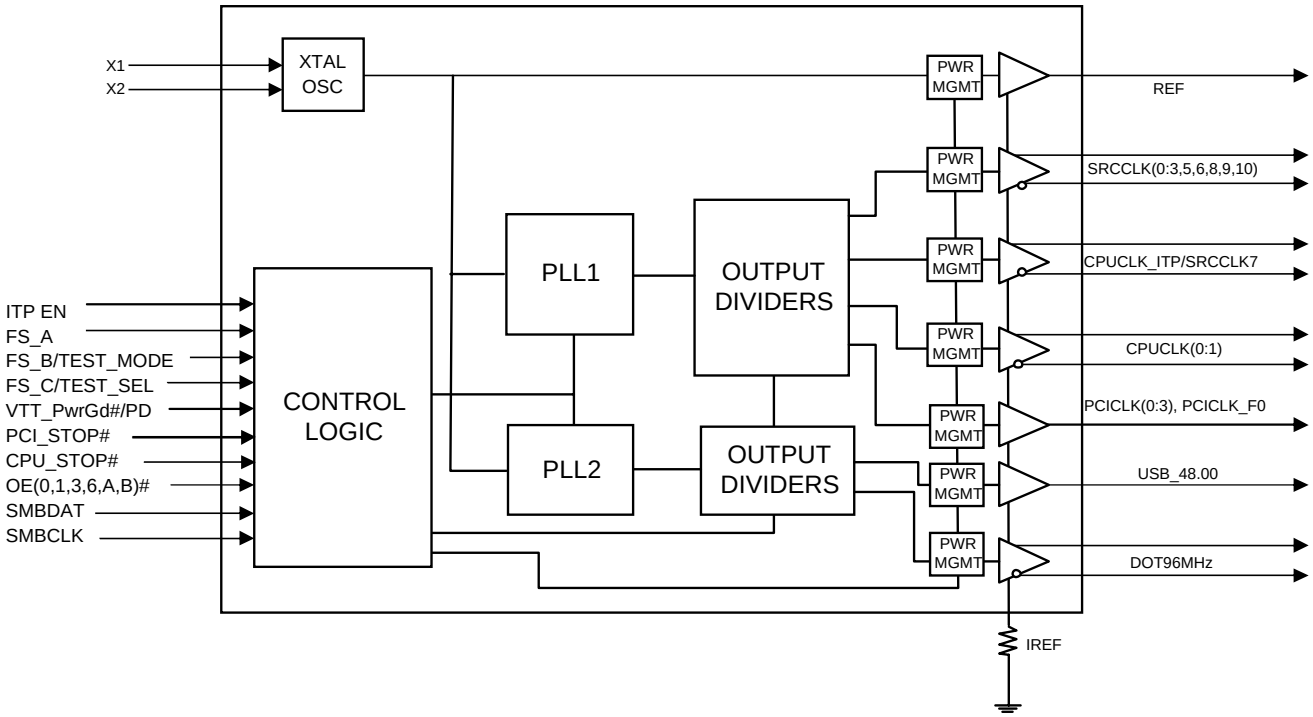
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General Description

The **ICS954309** is a CK410M clock synthesizer with additional SRC clock support. The **ICS954309** provides a single-chip solution for mobile systems built with Intel P4-M processors and Intel mobile chipsets. The **ICS954309** is driven with a 14.318MHz crystal and generates CPU outputs up to 400MHz.

Block Diagram



Power Groups

Pin Number		Description
VDD	GND	
43	46	Xtal, REF
54, 48	59, 55	PCICLK outputs
29, 17, 10	30, 11	SRCCLK outputs
60	1	DOT_96, USB_48
36	37	CPUCLK outputs, Analog

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General SMBus serial interface information for the ICS954309

How to Write:

- Controller (host) sends a start bit.
- Controller (host) sends the write address D2 (H)
- ICS clock will ***acknowledge***
- Controller (host) sends the begining byte location = N
- ICS clock will ***acknowledge***
- Controller (host) sends the data byte count = X
- ICS clock will ***acknowledge***
- Controller (host) starts sending ***Byte N through Byte N + X -1***
  (see Note 2)
- ICS clock will ***acknowledge*** each byte ***one at a time***
- Controller (host) sends a Stop bit

How to Read:

- Controller (host) will send start bit.
- Controller (host) sends the write address D2 (H)
- ICS clock will ***acknowledge***
- Controller (host) sends the begining byte location = N
- ICS clock will ***acknowledge***
- Controller (host) will send a separate start bit.
- Controller (host) sends the read address D3 (H)
- ICS clock will ***acknowledge***
- ICS clock will send the data byte count = X
- ICS clock sends ***Byte N + X -1***
- Controller (host) will need to acknowledge each byte
- Controllor (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

Index Block Write Operation

Controller (Host)		ICS (Slave/Receiver)
T	starT bit	
Slave Address D2(H)		
WR	WRite	
		ACK
Beginning Byte = N		
		ACK
Data Byte Count = X		
		ACK
Beginning Byte N	X Byte	
		ACK
O		
O		O
O		O
		O
Byte N + X - 1		
		ACK
P	stoP bit	

Index Block Read Operation

Controller (Host)		ICS (Slave/Receiver)	
T	starT bit		
Slave Address D2(H)			
WR	WRite		
		ACK	
Beginning Byte = N			
		ACK	
RT	Repeat starT		
Slave Address D3(H)			
RD	ReaD		
		ACK	
		Data Byte Count = X	
ACK			
	X Byte	Beginning Byte N	
ACK			
		O	
O		O	
O		O	
O			
		Byte N + X - 1	
N	Not acknowledge		
P	stoP bit		

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Absolute Max

Symbol	Parameter	Min	Max	Units
VDD_A	3.3V Core Supply Voltage		V_{DD} + 0.5V	V
VDD_In	3.3V Logic Input Supply Voltage	GND - 0.5	V_{DD} + 0.5V	V
Ts	Storage Temperature	-65	150	˚C
Tambient	Ambient Operating Temp	0	70	°C
Tcase	Case Temperature		115	°C
ESD prot	Input ESD protection human body model	2000		V

Electrical Characteristics - Input/Supply/Common Output Parameters

T_A = 0 - 70°C; Supply Voltage V_{DD} = 3.3 V +/-5%

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	Notes
Input High Voltage	V_{IH}	3.3 V +/-5%	2		V_{DD} + 0.3	V	1
Input Low Voltage	V_{IL}	3.3 V +/-5%	V_{SS} - 0.3		0.8	V	1
Input High Current	I_{IH}	V_{IN} = V_{DD}	-5		5	uA	1
Input Low Current	I_{IL1}	V_{IN} = 0 V; Inputs with no pull-up resistors	-5			uA	1
	I_{IL2}	V_{IN} = 0 V; Inputs with pull-up resistors	-200			uA	1
Low Threshold Input-High Voltage	V_{IH_FS}	3.3 V +/-5%	0.7		V_{DD} + 0.3	V	1
Low Threshold Input-Low Voltage	V_{IL_FS}	3.3 V +/-5%	V_{SS} - 0.3		0.35	V	1
Operating Current	$I_{DD3.3OP}$	All outputs driven, Full Active			500	mA	1
Powerdown Current	$I_{DD3.3PD}$	all diff pairs driven			70	mA	1
		all differential pairs tri-stated			12	mA	1
Input Frequency	F_i	V_{DD} = 3.3 V		14.31818		MHz	2
Pin Inductance	L_{pin}				7	nH	1
Input Capacitance	C_{IN}	Logic Inputs			5	pF	1
	C_{OUT}	Output pin capacitance			6	pF	1
	C_{INX}	X1 & X2 pins			5	pF	1
Clk Stabilization	T_{STAB}	From VDD Power-Up or de-assertion of PD to 1st clock			1.8	ms	1
Modulation Frequency		Triangular Modulation	30	32.540	33	kHz	1
Tdrive_PD		CPU output enable after PD de-assertion			300	us	1
Tfall_PD		PD fall time of			5	ns	1
Trise_PD		PD rise time of			5	ns	1
Tdrive_CPU_STOP		CPU output enable after CPU_STOP de-assertion			10	ns	1
Tfall_CPU_STOP		CPU_STOP fall time of			5	ns	1
Trise_CPU_STOP#		CPU_STOP rise time of			5	ns	1
SMBus Voltage	V_{DD}		2.7		5.5	V	1
Low-level Output Voltage	V_{OL}	@ I_{PULLUP}			0.4	V	1
Current sinking at V_{OL} = 0.4 V	I_{PULLUP}		4			mA	1
SCLK/SDATA Clock/Data Rise Time	T_{RI2C}	(Max VIL - 0.15) to (Min VIH + 0.15)			1000	ns	1
SCLK/SDATA Clock/Data Fall Time	T_{FI2C}	(Min VIH + 0.15) to (Max VIL - 0.15)			300	ns	1

[1]Guaranteed by design and characterization, not 100% tested in production.

[2] Input frequency should be measured at the REFOUT pin and tuned to ideal 14.31818MHz to meet ppm frequency accuracy on PLL outputs.

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Electrical Characteristics - SRC 0.7V Current Mode Differential Pair

T_A = 0 - 70°C; V_{DD} = 3.3 V +/-5%; C_L =2pF, R_S=33.2Ω, R_P=49.9Ω, I_{REF} = 475Ω

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	Notes
Current Source Output Impedance	Zo	$V_O = V_x$	3000			Ω	1
Voltage High	VHigh	Statistical measurement on single ended signal using oscilloscope	660		850	mV	1,3
Voltage Low	VLow		-150		150		1,3
Max Voltage	Vovs	Measurement on single ended signal using absolute value.			1150	mV	1
Min Voltage	Vuds		-300				1
Crossing Voltage (abs)	Vcross(abs)		250	350	550	mV	1
Crossing Voltage (var)	d-Vcross	Variation of crossing over all edges		12	140	mV	1
Long Accuracy	ppm	see Tperiod min-max values	-300		300	ppm	1,2
Average period	T_{period}	100.00MHz nominal	9.9970		10.0030	ns	2
		100.00MHz spread	9.9970		10.0533	ns	2
Absolute min/max period	T_{abs}	100.00MHz nominal	9.8720		10.1280	ns	1,2
		100.00MHz spread	9.8720		10.1783	ns	1,2
Rise Time	t_r	V_{OL} = 0.175V, V_{OH} = 0.525V	175		700	ps	1
Fall Time	t_f	V_{OH} = 0.525V V_{OL} = 0.175V	175		700	ps	1
Rise Time Variation	d-t_r			30	125	ps	1
Fall Time Variation	d-t_f			30	125	ps	1
Duty Cycle	d_{t3}	Measurement from differential wavefrom	45		55	%	1
Skew	t_{sk3}	V_T = 50%			250	ps	1
Jitter, Cycle to cycle	$t_{jcyc-cyc}$	Measurement from differential wavefrom			125	ps	1

[1]Guaranteed by design and characterization, not 100% tested in production.

[2] All Long Term Accuracy and Clock Period specifications are guaranteed assuming that REFOUT is at 14.31818MHz

[3]$I_{REF} = V_{DD}/(3xR_R)$. For R_R = 475Ω (1%), I_{REF} = 2.32mA. I_{OH} = 6 x I_{REF} and V_{OH} = 0.7V @ Z_O=50Ω.

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Electrical Characteristics - CPU 0.7V Current Mode Differential Pair

T_A = 0 - 70°C; V_{DD} = 3.3 V +/-5%; C_L =2pF, R_S=33.2Ω, R_P=49.9Ω, I_{REF} = 475Ω

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Current Source Output Impedance	Zo	$V_O = V_x$	3000			Ω	1
Voltage High	VHigh	Statistical measurement on single ended signal using oscilloscope math function.	660		850	mV	1,3
Voltage Low	VLow		-150		150		1,3
Max Voltage	Vovs	Measurement on single ended signal using absolute value.			1150	mV	1
Min Voltage	Vuds		-300				1
Crossing Voltage (abs)	Vcross(abs)		250		550	mV	1
Crossing Voltage (var)	d-Vcross	Variation of crossing over all edges			140	mV	1
Long Accuracy	ppm	see Tperiod min-max values	-300		300	ppm	1,2
Average period	T_{period}	400MHz nominal	2.4993		2.5008	ns	2
		400MHz spread	2.4993		2.5133	ns	2
		333.33MHz nominal	2.9991		3.0009	ns	2
		333.33MHz spread	2.9991		3.0160	ns	2
		266.66MHz nominal	3.7489		3.7511	ns	2
		266.66MHz spread	3.7489		3.7700	ns	2
		200MHz nominal	4.9985		5.0015	ns	2
		200MHz spread	4.9985		5.0266	ns	2
		166.66MHz nominal	5.9982		6.0018	ns	2
		166.66MHz spread	5.9982		6.0320	ns	2
		133.33MHz nominal	7.4978		7.5023	ns	2
		133.33MHz spread	7.4978		7.5400	ns	2
		100.00MHz nominal	9.9970		10.0030	ns	2
		100.00MHz spread	9.9970		10.0533	ns	2
Absolute min/max period	T_{abs}	400MHz nominal	2.4993		2.5008	ns	1,2
		400MHz spread	2.4993		2.5133	ns	1,2
		333.33MHz nominal	2.9991		3.0009	ns	1,2
		333.33MHz spread	2.9991		3.0160	ns	1,2
		266.66MHz nominal	3.7489		3.7511	ns	1,2
		266.66MHz spread	3.7489		3.7700	ns	1,2
		200MHz nominal	4.9985		5.0015	ns	1,2
		200MHz spread	4.9985		5.0266	ns	1,2
		166.66MHz nominal	5.9982		6.0018	ns	1,2
		166.66MHz spread	5.9982		6.0320	ns	1,2
		133.33MHz nominal	7.4978		7.5023	ns	1,2
		133.33MHz spread	7.4978		7.5400	ns	1,2
		100.00MHz nominal	9.9970		10.0030	ns	1,2
		100.00MHz spread	9.9970		10.0533	ns	1,2
Rise Time	t_r	V_{OL} = 0.175V, V_{OH} = 0.525V	175		700	ps	1
Fall Time	t_f	V_{OH} = 0.525V V_{OL} = 0.175V	175		700	ps	1
Rise Time Variation	d-t_r				125	ps	1
Fall Time Variation	d-t_f				125	ps	1
Duty Cycle	d_{t3}	Measurement from differential wavefrom	45		55	%	1
Skew	t_{sk3}	CPU(1:0), V_T = 50%			100	ps	1
	t_{sk4}	CPU(1:0) to CPU2_ITP, V_T = 50%			150	ps	1
Jitter, Cycle to cycle	$t_{jcyc-cycITP}$	Measurement from differential wavefrom (CPU2_ITP)			125	ps	1
	$t_{jcyc-cyc}$	Measurement from differential wavefrom, (CPU(1:0))			85	ps	1

[1]Guaranteed by design and characterization, not 100% tested in production.

[2] All Long Term Accuracy and Clock Period specifications are guaranteed assuming that REFOUT is at 14.31818MHz

[3]$I_{REF} = V_{DD}/(3xR_R)$. For R_R = 475Ω (1%), I_{REF} = 2.32mA. I_{OH} = 6 x I_{REF} and V_{OH} = 0.7V @ Z_O=50Ω.

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Electrical Characteristics - DOT_96MHz 0.7V Current Mode Differential Pair

T_A = 0 - 70°C; V_{DD} = 3.3 V +/-5%; C_L =2pF, R_S=33.2Ω, R_P=49.9Ω, I_{REF} = 475Ω

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	Notes
Current Source Output Impedance	Zo	$V_O = V_x$	3000			Ω	1
Voltage High	VHigh	Statistical measurement on single ended signal using	660		850	mV	1,3
Voltage Low	VLow		-150		150		1,3
Max Voltage	Vovs	Measurement on single ended signal using absolute value.			1150	mV	1
Min Voltage	Vuds		-300				1
Crossing Voltage (abs)	Vcross(abs)		250		550	mV	1
Crossing Voltage (var)	d-Vcross	Variation of crossing over all edges			140	mV	1
Long Accuracy	ppm	see Tperiod min-max values			300	ppm	1,2
Average period	T_{period}	96.00MHz nominal	10.4156	10.4167	10.4177	ns	2
Absolute min/max period	T_{abs}	96.00MHz nominal	10.1656		10.6677	ns	1,2
Rise Time	t_r	V_{OL} = 0.175V, V_{OH} = 0.525V	175		700	ps	1
Fall Time	t_f	V_{OH} = 0.525V V_{OL} = 0.175V	175		700	ps	1
Rise Time Variation	d-t_r				125	ps	1
Fall Time Variation	d-t_f				125	ps	1
Duty Cycle	d_{t3}	Measurement from differential wavefrom	45		55	%	1
Jitter, Cycle to cycle	$t_{jcyc-cyc}$	Measurement from differential wavefrom			250	ps	1

[1]Guaranteed by design and characterization, not 100% tested in production.

[2] All Long Term Accuracy and Clock Period specifications are guaranteed assuming that REFOUT is at 14.31818MHz

[3]$I_{REF} = V_{DD}/(3xR_R)$. For R_R = 475Ω (1%), I_{REF} = 2.32mA. I_{OH} = 6 x I_{REF} and V_{OH} = 0.7V @ Z_O=50Ω.

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Electrical Characteristics - PCICLK/PCICLK_F

T_A = 0 - 70°C; V_{DD} = 3.3 V +/-5%; C_L = 10-20 pF (unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	Notes
Long Accuracy	ppm	see Tperiod min-max values	-300		300	ppm	1,2
Clock period	T_{period}	33.33MHz output non-spread	29.9910		30.0090	ns	2
		33.33MHz output spread			30.1598	ns	2
Absolute min/max period	T_{abs}	33.33MHz output non-spread	29.4910		30.5090	ns	1,2
		33.33MHz output spread			30.6598	ns	1,2
Output High Voltage	V_{OH}	I_{OH} = -1 mA	2.4			V	1
Output Low Voltage	V_{OL}	I_{OL} = 1 mA			0.55	V	1
Output High Current	I_{OH}	V_{OH} = 1.0 V	-33			mA	1
		V_{OH} = 3.135 V			-33	mA	1
Output Low Current	I_{OL}	V_{OL} = 1.95 V	30			mA	1
		V_{OL} = 0.4 V			38	mA	1
Edge Rate		Rising edge rate	1		4	V/ns	1
Edge Rate		Falling edge rate	1		4	V/ns	1
Rise Time	t_{r1}	V_{OL} = 0.4 V, V_{OH} = 2.4 V	0.5		2	ns	1
Fall Time	t_{f1}	V_{OH} = 2.4 V, V_{OL} = 0.4 V	0.5		2	ns	1
Duty Cycle	d_{t1}	V_T = 1.5 V	45		55	%	1
Skew	t_{sk1}	V_T = 1.5 V			500	ps	1
Jitter	$t_{jcyc-cyc}$	V_T = 1.5 V			500	ps	1

[1]Guaranteed by design and characterization, not 100% tested in production.

[2] All Long Term Accuracy and Clock Period specifications are guaranteed assuming that REFOUT is at 14.31818MHz

Electrical Characteristics - 48MHz, USB

T_A = 0 - 70°C; V_{DD} = 3.3 V +/-5%; C_L = 10-20 pF (unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	Notes
Long Accuracy	ppm	see Tperiod min-max values	-100		100	ppm	1,2
Clock period	T_{period}	48.00MHz output nominal	20.8313		20.8354	ns	2
Absolute min/max period	T_{abs}	48.00MHz output nominal	20.4813		21.1854	ns	2
Output High Voltage	V_{OH}	I_{OH} = -1 mA	2.4			V	1
Output Low Voltage	V_{OL}	I_{OL} = 1 mA			0.55	V	1
Output High Current	I_{OH}	V_{OH} = 1.0 V	-29			mA	1
		V_{OH} = 3.135 V			-23	mA	1
Output Low Current	I_{OL}	V_{OL} = 1.95 V	29			mA	1
		V_{OL} = 0.4 V			27	mA	1
Edge Rate		Rising edge rate	1		2	V/ns	1
Edge Rate		Falling edge rate	1		2	V/ns	1
Duty Cycle	d_{t1}	V_T = 1.5 V	45		55	%	1
Jitter, Cycle to cycle	$t_{jcyc-cyc}$	V_T = 1.5 V			350	ps	1

[1]Guaranteed by design and characterization, not 100% tested in production.

[2] All Long Term Accuracy and Clock Period specifications are guaranteed assuming that REFOUT is at 14.31818MHz

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Electrical Characteristics - REF-14.318MHz

T_A = 0 - 70°C; V_{DD} = 3.3 V +/-5%; C_L = 10-20 pF (unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	Notes
Long Accuracy	ppm	see Tperiod min-max values	-300		300	ppm	1
Clock period	T_{period}	14.318MHz output nominal	69.8203		69.8622	ns	1
Clock period	T_{abs}	14.318MHz output nominal	69.8203		70.8622	ns	1
Output High Voltage	V_{OH}	I_{OH} = -1 mA	2.4			V	1
Output Low Voltage	V_{OL}	I_{OL} = 1 mA			0.55	V	1
Output High Current	I_{OH}	V_{OH} = 1.0 V	-33			mA	1
		V_{OH} = 3.135 V			-33	mA	1
Output Low Current	I_{OL}	V_{OL} = 1.95 V	30			mA	1
		V_{OL} = 0.4 V			38	mA	1
Edge Rate		Rising edge rate	1		4	V/ns	1
Edge Rate		Falling edge rate	1		4	V/ns	1
Duty Cycle	d_{t1}	V_T = 1.5 V	45		55	%	1,2
Jitter	$t_{jcyc-cyc}$	V_T = 1.5 V			1000	ps	1

[1]Guaranteed by design and characterization, not 100% tested in production.

[2] All Long Term Accuracy and Clock Period specifications are guaranteed assuming that REFOUT is at 14.31818MHz

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SMBus Table: Output Enable Control Register

Byte 0	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	CPUCLK2_ITP/SRCCLK7 EN	Output Enable	RW	Disabled (Hi-Z)	Enabled	1
Bit 6	-	SRCCLK6 EN	Output Enable	RW	Disabled (Hi-Z)	Enabled	1
Bit 5	-	SRCCLK5 EN	Output Enable	RW	Disabled (Hi-Z)	Enabled	1
Bit 4	-	Reserved					0
Bit 3	-	SRCCLK3 EN	Output Enable	RW	Disabled (Hi-Z)	Enabled	1
Bit 2	-	SRCCLK2 EN	Output Enable	RW	Disabled (Hi-Z)	Enabled	1
Bit 1	-	SRCCLK1 EN	Output Enable	RW	Disabled (Hi-Z)	Enabled	1
Bit 0	-	SRCCLK0 EN	Output Enable	RW	Disabled (Hi-Z)	Enabled	1

SMBus Table: Spreading and Output Enable Control Register

Byte 1	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7		PCI_F0 EN	Output Enable	RW	Disabled	Enabled	1
Bit 6		DOT_96MHz EN	Output Enable	RW	Disabled (Hi-Z)	Enabled	1
Bit 5		USB_48MHz EN	Output Enable	RW	Disabled	Enabled	1
Bit 4		REFCLK EN	Output Enable	RW	Disabled	Enabled	1
Bit 3		Reserved					1
Bit 2		CPUCLK1 EN	Output Enable	RW	Disabled (Hi-Z)	Enabled	1
Bit 1		CPUCLK0 EN	Output Enable	RW	Disabled (Hi-Z)	Enabled	1
Bit 0		SS_EN for CPU, SRC and PCI Outputs	Spread Spectrum Enable	RW	Spread Off	Spread On	0

SMBus Table: Output Enable Control Register

Byte 2	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7		Reserved					1
Bit 6		Reserved					1
Bit 5		PCICLK3 EN	Output Enable	RW	Disabled	Enabled	1
Bit 4		PCICLK2 EN	Output Enable	RW	Disabled	Enabled	1
Bit 3		PCICLK1 EN	Output Enable	RW	Disabled	Enabled	1
Bit 2		PCICLK0 EN	Output Enable	RW	Disabled	Enabled	1
Bit 1		Reserved					1
Bit 0		Reserved					1

SMBus Table: SRC Output Enable Control Register

Byte 3	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7		SRCCLK7 OEB# Select	Selects OEB# Control	RW	Not Controlled	Controlled	0
Bit 6		Reserved					0
Bit 5		SRCCLK5 OEB# Select	Selects OEB# Control	RW	Not Controlled	Controlled	0
Bit 4		Reserved					0
Bit 3		Reserved					0
Bit 2		SRCCLK2 OEB# Select	Selects OEB# Control	RW	Not Controlled	Controlled	0
Bit 1		Reserved					0
Bit 0		Reserved					0

Note: Please refer to CPU and SRC Clock Control Truth Tables

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SMBus Table: Stop and Output Control Register

Byte 4	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7		Reserved					X
Bit 6		DOT96MHz	PD Drive Mode	RW	Driven	Hi-Z	0
Bit 5		Reserved					0
Bit 4		Reserved					0
Bit 3		PCICLK_F0 Stop EN	Allow assertion of PCI_STOP# or setting of PCI_STOP control bit in SMBus register to stop PCICLK_F output	RW	Free-Running	Stoppable	0
Bit 2		CPUCLK2 Stop	Allow assertion of CPU_STOP# to stop CPUCLK outputs	RW	Free-Running	Stoppable	0
Bit 1		CPUCLK1 Stop		RW	Free-Running	Stoppable	0
Bit 0		CPUCLK0 Stop		RW	Free-Running	Stoppable	0

SMBus Table: CPU and SRC Stop and Power Down Drive Mode Control Register

Byte 5	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7		Reserved					0
Bit 6		CPUCLK2 STOP Drive Mode	Driven in CPU_STOP#	RW	Driven	Hi-Z	0
Bit 5		CPUCLK1 STOP Drive Mode		RW	Driven	Hi-Z	0
Bit 4		CPUCLK0 STOP Drive Mode		RW	Driven	Hi-Z	0
Bit 3		SRCCLK PD Drive Mode	Driven in Powerdown (PD)	RW	Driven	Hi-Z	0
Bit 2		CPUCLK2 PD Drive Mode	Driven in Powerdown (PD)	RW	Driven	Hi-Z	0
Bit 1		CPUCLK1 PD Drive Mode		RW	Driven	Hi-Z	0
Bit 0		CPUCLK0 PDDrive Mode		RW	Driven	Hi-Z	0

SMBus Table: Test Mode Control and FS Readback Register

Byte 6	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	Test Mode Selection	Test Mode Selection	RW	Hi-Z	REF/N	0
Bit 6	-	Test Clock Mode Entry	Test Mode Entry	RW	Normal Operation	Test Mode	0
Bit 5		Reserved					0
Bit 4	-	REFCLK Strength	Output Drive Strength	RW	1X	2X	1
Bit 3	-	PCI_STOP# Configure	Stops all PCI clocks except PCICLK_F0 if it is set to free-running.	RW	Stopped	Normal Operation	1
Bit 2	-	FS_C	FS_C Readback	R	-	-	Latched
Bit 1	-	FS_B	FS_B Readback	R	-	-	Latched
Bit 0	-	FS_A	FS_A Readback	R	-	-	Latched

SMBus Table: Vendor & Revision ID Register

Byte 7	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	RID3	REVISION ID	R	-	-	X
Bit 6	-	RID2		R	-	-	X
Bit 5	-	RID1		R	-	-	X
Bit 4	-	RID0		R	-	-	X
Bit 3	-	VID3	VENDOR ID	R	-	-	0
Bit 2	-	VID2		R	-	-	0
Bit 1	-	VID1		R	-	-	0
Bit 0	-	VID0		R	-	-	1

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SMBus Table: SRC Output Enable Control Register

Byte 8	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7		Reserved					0
Bit 6		SRCCLK10 EN	Output Enable	RW	Disabled (Hi-Z)	Enabled	1
Bit 5		SRCCLK9 EN	Output Enable	RW	Disabled (Hi-Z)	Enabled	1
Bit 4		SRCCLK8 EN	Output Enable	RW	Disabled (Hi-Z)	Enable	1
Bit 3		Reserved					0
Bit 2		SRCCLK10 OEA# Select	Selects OEA# Control	RW	Not Controlled	Controlled	0
Bit 1		SRCCLK9 OEB# Select	Selects OEA# Control	RW	Not Controlled	Controlled	0
Bit 0		SRCCLK8 OEA# Select	Selects OEA# Control	RW	Not Controlled	Controlled	0

SMBus Table: Output Strength Register

Byte 9	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	PCICLK3	OUTPUT DRIVE STRENGTH	RW	0.75x	1x	1
Bit 6	-	PCICLK2		RW	0.75x	1x	1
Bit 5	-	PCICLK1		RW	0.75x	1x	1
Bit 4	-	PCICLK0		RW	0.75x	1x	1
Bit 3	-	PCICLK_F0		RW	0.75x	1x	1
Bit 2	-	CPUCLK2		RW	0.75x	1x	1
Bit 1	-	CPUCLK1		RW	0.75x	1x	1
Bit 0	-	CPUCLK0		RW	0.75x	1x	1

SMBus Table: Output Strength Register

Byte 10	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	SRC7	OUTPUT DRIVE STRENGTH	RW	0.75x	1x	1
Bit 6	-	SRC6		RW	0.75x	1x	1
Bit 5	-	SRC5		RW	0.75x	1x	1
Bit 4	-	Reserved		Reserved			1
Bit 3	-	SRC3		RW	0.75x	1x	1
Bit 2	-	SRC2		RW	0.75x	1x	1
Bit 1	-	SRC1		RW	0.75x	1x	1
Bit 0	-	SRC0		RW	0.75x	1x	1

SMBus Table: Output Strength Register

Byte 11	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	Reserved						X
Bit 6	Reserved						X
Bit 5	Reserved						X
Bit 4	Reserved						X
Bit 3	Reserved						X
Bit 2	-	SRC10	OUTPUT DRIVE STRENGTH	RW	0.75x	1x	1
Bit 1	-	SRC9		RW	0.75x	1x	1
Bit 0	-	SRC8		RW	0.75x	1x	1

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Test Clarification Table

Comments	HW		SW		
	FS_C/TEST_SEL HW PIN	FS_B/TEST_MODE HW PIN	TEST ENTRY BIT W6b6	REF/N or HI-Z W6b7	OUTPUT
	0	X	0	X	NORMAL
Power-up w/ TEST_SEL = 1 to enter test mode Cycle power to disable test mode FS_C./TEST_SEL -->3-level latched input If power-up w/ V>2.0V (-0.3V) then use TEST_SEL If power-up w/ V<2.0V (-0.3V) then use FS_C FS_B/TEST_MODE -->low Vth input TEST_MODE is a real time input	1	0	X	0	HI-Z
	1	0	X	1	REF/N
	1	1	X	0	REF/N
	1	1	X	1	REF/N
If TEST_SEL HW pin is 0 during power-up, test mode can be invoked through W6b6. If test mode is invoked by W6b6, **only** W6b7 is used to select HI-Z or REF/N FS_B/TEST_Mode pin is not used. Cycle power to disable test mode, one shot control	0	X	1	0	HI-Z
	0	X	1	1	REF/N
W6b6: 1= ENTER TEST MODE, Default = 0 (NORMAL OPERATION)					
W6b7: 1= REF/N, Default = 0 (HI-Z)					

Table 7: Tristate CPU Clock Control Truth Table

Signal	PD	CPU_STOP#	CPU_STOP Tristate BIT	PD Tristate BIT	NON-STOP OUTPUTS	STOPPABLE OUTPUTS
	56	40	B5b[6, 5, 4]	B5b[2,1,0]		
CPU[2:0]	0	1	X	X	Running	Running
CPU[2:0]	0	0	0	X	Running	Driven @ I_{REF} X6
CPU[2:0]	0	0	1	X	Running	Tristate
CPU[2:0]	1	X	X	0	Driven @ I_{REF} X2	Driven @ I_{REF} X2
CPU[2:0]	1	X	X	1	Tristate	Tristate

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Table 8: Tristate SRC Clock Control Truth Table

Signal	PD	PD Tristate BIT	NON-STOP OUTPUTS	STOPPABLE OUTPUTS
	56	B5b3		
SRC	0	X	Running	Running
SRC	1	0	Driven @ I_{REF} X2	Driven @ I_{REF} X2
SRC	1	1	Tristate	Tristate

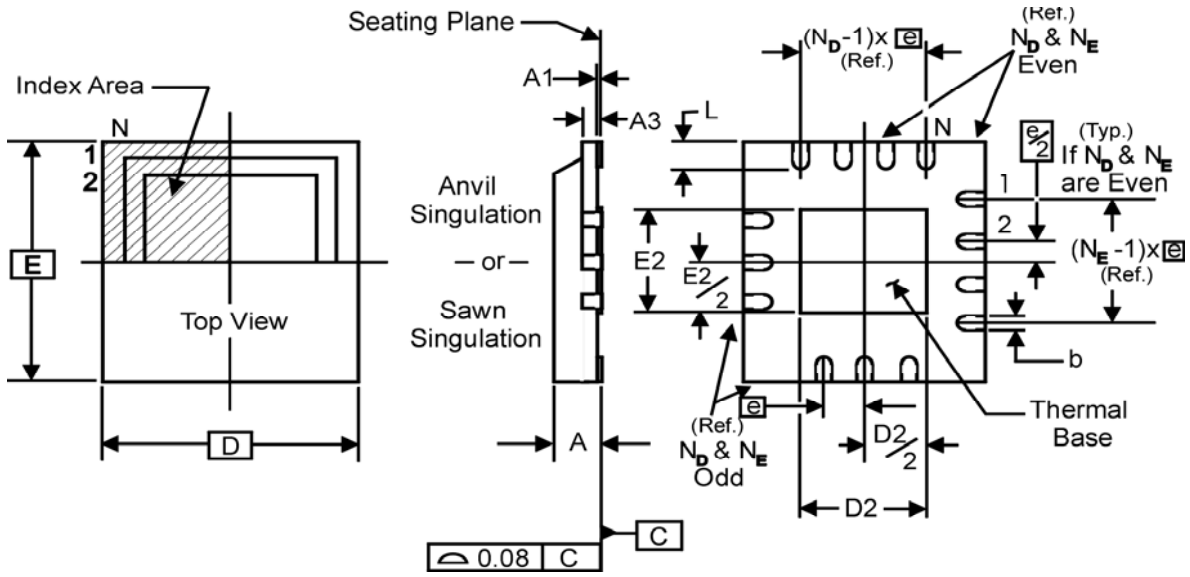
Table 9: Tristate DOT Clock Control Truth Table

Signal	PD	PD Tristate BIT	STOPPABLE OUTPUTS
	56	B4b6	
DOT_96	0	X	Running
DOT_96	1	0	Driven @ I_{REF} X2
DOT_96	1	1	Tristate

Table10: CLKREQ# Clock Control Truth Table

Signal	PD	OEx#	SELECTED OUTPUTS
	56	4,7,12,15,24,64	
SRCx	0	0	Running
SRCx	0	1	Tristate
SRCx	1	X	Stopped per B5b3

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THERMALLY ENHANCED, VERY THIN, FINE PITCH
QUAD FLAT / NO LEAD PLASTIC PACKAGE

DIMENSIONS

SYMBOL	64L
N	64
N_D	16
N_E	16

OPTION 1 DIMENSIONS (mm)

SYMBOL	MIN.	MAX.
A	0.8	1.0
A1	0	0.05
A3	0.25 Reference	
b	0.18	0.3
e	0.50 BASIC	
D x E BASIC	9.00 x 9.00	
D2 MIN. / MAX.	7.00	7.25
E2 MIN. / MAX.	7.00	7.25
L MIN. / MAX.	0.30	0.50

OPTION 2 DIMENSIONS (mm)

SYMBOL	MIN.	MAX.
A	0.8	1.0
A1	0	0.05
A3	0.25 Reference	
b	0.18	0.3
e	0.50 BASIC	
D x E BASIC	9.00 x 9.00	
D2 MIN. / MAX.	6.00	6.25
E2 MIN. / MAX.	6.00	6.25
L MIN. / MAX.	0.30	0.50

Ordering Information

ICS954309yKLFT

Example:

ICS XXXX y K LF T

- **Designation for tape and reel packaging**
- **Annealed Lead Free (optional)**
- **Package Type**
  K = MLF
- **Revision Designator** (will not correlate with datasheet revision)
- **Device Type (consists of 3 or 4 digit numbers)**
- **Prefix**
  ICS, AV = Standard Device

1044A—02/20/07

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Revision History

Rev.	Issue Date	Description	Page #
A	2/20/2007	Initial Release	-

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