PROGRAMMABLE FLEXPC™ CLOCK FOR AMD K8 PROCESSOR ATI RS480

IDTCV137

FEATURES:

- **One high precision N and SSC programmable PLL for CPU**
- **One high precision N and SSC programmable PLL for SRC[2:1]**
- **One high precision N and SSC programmable PLL for SRC0 [7:3] (PCI Express)**
- **One high precision PLL for 48MHz**
- **Band-gap circuit for differential outputs**
- **Support multiple spread spectrum modulation, down and center**
- **Support SMBus block read/write, index read/write**
- **Selectable output strength for REF, PCI, 48MHz, HTT66**
- **Available in SSOP and TSSOP packages**

KEY SPECIFICATION:

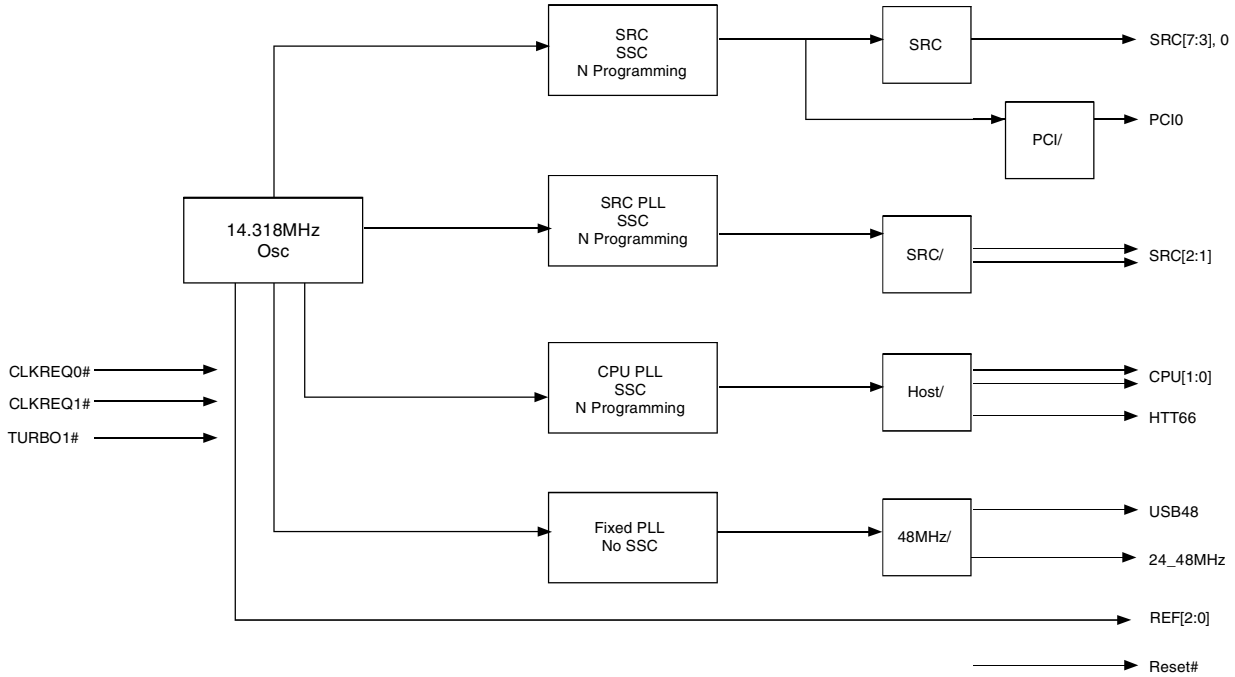
- **CPU CLK cycle to cycle jitter < 85ps**
- **SRC CLK cycle to cycle jitter < 100ps**

DESCRIPTION:

IDTCV137 is a 56 pin clock device for AMD advance K8 processors. The CPU output buffer is designed to support up to 400MHz processor. This device also implements Band-gap referenced I_{REF} to reduce the impact of V_{DD} variation on differential outputs, which can provide more robust system performance.

Each CPU/SRC clock has its own Spread Spectrum selection, which allows for isolated changes instead of affecting other clock groups.

FUNCTIONAL BLOCK DIAGRAM



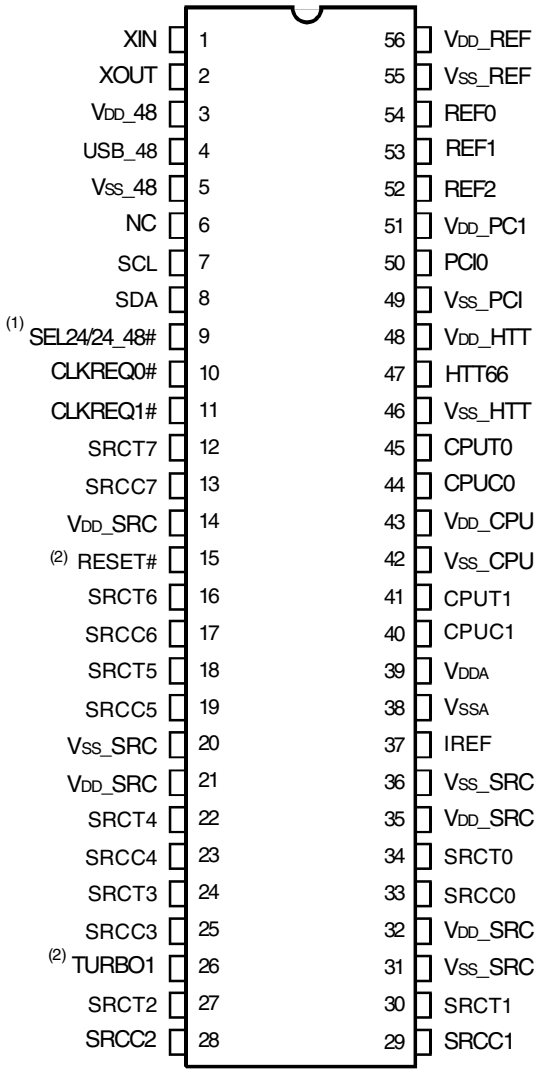
OUTPUT TABLE

CPU	CLKREQ	SRC	HTT66	PCI	TURBO	USB48	24_48	REF	RESET#
2	2	8	1	1	1	1	1	3	1

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PIN CONFIGURATION



NOTES:
1. Internal 130KΩ pull-down resistor.
2. Tristate at power on to be compatible with ATI pin definition.

SSOP/ TSSOP
TOP VIEW

CPU AND SRC SPREAD SPECTRUM MAGNITUDE CONTROL

SMC[2:0]	%
000	OFF
001	-0.25
010	-0.5
011	-0.75
100	±0.125
101	±0.25
110	±0.375
111	±0.5

SE SIGNAL STRENGTH SELECTION

Str[1:0]	Strength
00	0.6x
01	0.8x
10	1x
11	1.2x

PCI (BASED ON SRC = 100MHz)

PCIS[1:0]	PCI
00	33.33
01	36.36
10	40
11	30.77

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PIN DESCRIPTION

Pin Name	Type	Pin #	Description
XIN	IN	1	XTAL in
XOUT	OUT	2	XTAL out
PCI0	OUT	50	PCI clock
HTT66	OUT	47	66.66 MHz
USB48	OUT	4	48MHz
Turbo1	IN	26	Turbo frequency select
CPUC[1:0] CPUT[1:0]	OUT	40, 41, 44, 45	Differential clock
SRCC[7:0] SRCT[7:0]	OUT	12, 13, 16, 17, 18, 19, 22, 23, 24, 25, 27, 28, 29, 30, 33, 34	Differential clock
IREF	OUT	37	Differential clock reference current
REF[0:1]	I/O	53, 54	14.318MHz
REF2	OUT	52	14.318MHz
CLKREQ0#	IN	10	SRC OE control, see bytes 3, 4
CLKREQ1#	IN	11	SRC OE control, see bytes 3, 4
SDA	I/O	8	SMBus data
SCL	IN	7	SMBus clock
SEL24/24_48#	IN	9	Latched select input for 24 or 48MHz output. 1 = 24MHz, 0 = 48MHz.
RESET#	OUT, OD	15	Reset output signal, Open Drain

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SM PROTOCOL

INDEX BLOCK WRITE PROTOCOL

Bit	# of bits	From	Description
1	1	Master	Start
2-9	8	Master	D2h
10	1	Slave	Ack (Acknowledge)
11-18	8	Master	Register offset byte (starting byte)
19	1	Slave	Ack (Acknowledge)
20-27	8	Master	Byte count, N (0 is not valid)
28	1	Slave	Ack (Acknowledge)
29-36	8	Master	first data byte (Offset data byte)
37	1	Slave	Ack (Acknowledge)
38-45	8	Master	2nd data byte
46	1	Slave	Ack (Acknowledge)
			:
		Master	Nth data byte
		Slave	Acknowledge
		Master	Stop

INDEX BLOCK READ PROTOCOL

Master can stop reading any time by issuing the stop bit without waiting until Nth byte (byte count bit30-37).

Bit	# of bits	From	Description
1	1	Master	Start
2-9	8	Master	D2h
10	1	Slave	Ack (Acknowledge)
11-18	8	Master	Register offset byte (starting byte)
19	1	Slave	Ack (Acknowledge)
20	1	Master	Repeated Start
21-28	8	Master	D3h
29	1	Slave	Ack (Acknowledge)
30-37	8	Slave	Byte count, N (block read back of N bytes), power on is 8
38	1	Master	Ack (Acknowledge)
39-46	8	Slave	first data byte (Offset data byte)
47	1	Master	Ack (Acknowledge)
48-55	8	Slave	2nd data byte
			Ack (Acknowledge)
			:
		Master	Ack (Acknowledge)
		Slave	Nth data byte
			Not acknowledge
		Master	Stop

INDEX BYTE WRITE

Setting bit[11:18] = starting address, bit[20:27] = 01h.

INDEX BYTE READ

Setting bit[11:18] = starting address. After reading back the first data byte, master issues Stop bit.

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BYTE 0

Bit	Output(s) Affected	Description/Function	0	1	Type	Power On
7	SRCT7, SRCC7	Output enable	Tristate	Enable	RW	1
6	SRCT6, SRCC6	Output enable	Tristate	Enable	RW	1
5	SRCT5, SRCC5	Output enable	Tristate	Enable	RW	1
4	SRCT4, SRCC4	Output enable	Tristate	Enable	RW	1
3	SRCT3, SRCC3	Output enable	Tristate	Enable	RW	1
2	SRCT2, SRCC2	Output enable	Tristate	Enable	RW	1
1	SRCT1, SRCC1	Output enable	Tristate	Enable	RW	1
0	SRCT0, SRCT0	Output enable	Tristate	Enable	RW	1

BYTE 1

Bit	Output(s) Affected	Description/Function	0	1	Type	Power On
7	USB48	Output enable	Tristate	Enable	RW	1
6	REF2	Output enable	Tristate	Enable	RW	1
5	REF1	Output enable	Tristate	Enable	RW	1
4	REF0	Output enable	Tristate	Enable	RW	1
3	24_48MHz	Output enable	Tristate	Enable	RW	1
2	CPUT1, CPUC1	Output enable	Tristate	Enable	RW	1
1	CPUT0, CPUC0	Output enable	Tristate	Enable	RW	1
0	HTT66	Output enable	Tristate	Enable	RW	1

BYTE 2

Bit	Output(s) Affected	Description / Function	0	1	Type	Power On
7	Reserved				RW	1
6	Reserved				RW	0
5	PCI0 SEL1	see PCI select table			RW	0
4	PCI0 SEL0				RW	0
3	Reserved				RW	0
2	Reserved				RW	0
1	Reserved				RW	0
0	Reserved				RW	0

BYTE 3

Bit	Output(s) Affected	Description / Function	0	1	Type	Power On
7	SRC7	Controlled by CLKREQB# or CLKREQA#	CLKREQ0#	CLKREQ1#	RW	0
6	SRC6		CLKREQ0#	CLKREQ1#	RW	0
5	SRC5		CLKREQ0#	CLKREQ1#	RW	0
4	SRC4		CLKREQ0#	CLKREQ1#	RW	0
3	SRC3		CLKREQ0#	CLKREQ1#	RW	0
2	Reserved				RW	0
1	Reserved				RW	0
0	SRC0	Controlled by CLKREQB# or CLKREQA#	CLKREQ0#	CLKREQ1#	RW	0

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BYTE 4

Bit	Output(s) Affected	Description / Function	0	1	Type	Power On
7	SRC7	When CLKREQ is HIGH, Output is Hi-Z	Not Controlled	Controlled	RW	0
6	SRC6		Not Controlled	Controlled	RW	0
5	SRC5		Not Controlled	Controlled	RW	0
4	SRC4		Not Controlled	Controlled	RW	0
3	SRC3		Not Controlled	Controlled	RW	0
2	Reserved				RW	0
1	Reserved				RW	0
0	SRC0	When CLKREQ is HIGH, Output is Hi-Z	Not Controlled	Controlled	RW	0

BYTE 5

Bit	Output(s) Affected	Description / Function	0	1	Type	Power On
7	HTT66	HTT66 strength selection			RW	1
6	HTT66				RW	0
5	PCIStrC1	PCI strength selection			RW	1
4	PCIStrC0				RW	0
3	REFStr1	REF strength selection			RW	1
2	REFStr0				RW	0
1	48MHStr1	USB48MHz strength selection			RW	1
0	48MHzStr0				RW	0

BYTE 6

Bit	Output(s) Affected	Description / Function	0	1	Type	Power On
7	Reserve				RW	0
6	SRC0, SR[7:3], SMC2	SRC0, SRC[7:3] SSC control (see SMC table)			RW	0
5	SRC0, SR[7:3], SMC1				RW	0
4	SRC0, SR[7:3], SMC0				RW	0
3	Reserved				RW	0
2	SRC[2:1], SMC2	SRC[2:1] control (see SMC table)			RW	0
1	SRC[2:1], SMC1				RW	0
0	SRC[2:1], SMC0				RW	0

BYTE 7

Bit	Output(s) Affected	Description / Function	0	1	Type	Power On
7		Revision ID			R	0
6		Revision ID			R	0
5		Revision ID			R	0
4		Revision ID			R	0
3		Vendor ID			R	0
2		Vendor ID			R	1
1		Vendor ID			R	0
0		Vendor ID			R	1

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BYTE 8 (INDEX BLOCK READ BYTE COUNT)

Bit	Output(s) Affected	Description / Function	0	1	Type	Power On
7					RW	0
6					RW	0
5					RW	0
4					RW	1
3					RW	0
2					RW	1
1					RW	1
0					RW	0

BYTE 9

Bit	Output(s) Affected	Description / Function	0	1	Type	Power On
7	Reserved				RW	0
6	Reserved				RW	0
5	Reserved				RW	0
4	Reserved				RW	0
3	Reserved				RW	0
2	CPU_SMC2	CPU PLL SSC control (see SMC table)			RW	0
1	CPU_SMC1				RW	0
0	CPU_SMC0				RW	0

BYTE 10

Bit	Output(s) Affected	Description / Function	0	1	Type	Power On
7	WD_1_Timer7	WatchDog_1_Alarm timer Default is 11*290ms			RW	0
6	WD_1_Timer6				RW	0
5	WD_1_Timer5				RW	0
4	WD_1_Timer4				RW	0
3	WD_1_Timer3				RW	1
2	WD_1_Timer2				RW	0
1	WD_1_Timer1				RW	1
0	WD_1_Timer0				RW	1

BYTE 11

Bit	Output(s) Affected	Description / Function	0	1	Type	Power On
7	CPU_N8				RW	0
6	Reserved				RW	0
5	Reserved				RW	0
4	Reserved				RW	0
3	WDRB	Alarm read back, reset by WD disable		Alarm	R	0
2	RESET#(1)	Reset Enable	Disable	Reset Enable	RW	0
1	Reserved				RW	0
0	Watch Dog Enable	Watch Dog Enable	Disable	Enable	RW	0

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BYTE 12

Bit	Output(s) Affected	Description / Function	0	1	Type	Power On
7	CPU_N7	CPU CLK = N*Resolution Resolution = 1.3333			RW	1
6	CPU_N6				RW	0
5	CPU_N5				RW	0
4	CPU_N4				RW	1
3	CPU_N3				RW	0
2	CPU_N2				RW	1
1	CPU_N1				RW	1
0	CPU_N0, LSB				RW	0

BYTE 13

Bit	Output(s) Affected	Description / Function	0	1	Type	Power On
7	SRC1_N7, MSB	SRC2, SRC1 SRC CLK = N*Resolution Resolution = 0.66667			RW	1
6	SRC1_N6				RW	0
5	SRC1_N5				RW	0
4	SRC1_N4				RW	1
3	SRC1_N3				RW	0
2	SRC1_N2				RW	1
1	SRC1_N1				RW	1
0	SRC1_N0, LSB				RW	0

BYTE 14

Bit	Output(s) Affected	Description / Function	0	1	Type	Power On
7	SRC0_N7, MSB	SRC[7:3], SRC0 SRC CLK = N*Resolution Resolution = 0.66667			RW	1
6	SRC0_N6				RW	0
5	SRC0_N5				RW	0
4	SRC0_N4				RW	1
3	SRC0_N3				RW	0
2	SRC0_N2				RW	1
1	SRC0_N1				RW	1
0	SRC0_N0, LSB				RW	0

BYTE 15

Bit	Output(s) Affected	Description / Function	0	1	Type	Power On
7			Disable	Enable	RW	0
6	CPU N programming enable		Disable	Enable	RW	0
5	SRC1, SRC2 N Programming enable		Disable	Enable	RW	0
4	SRC0, SRC[7:3] N Programming enable		Disable	Enable	RW	0
3	Turbo1 enable		Disable	Enable	RW	0
2	Turbo	Turbo Active Selection	Active HIGH	Active LOW	RW	0
1	Reserved				RW	0
0	T1CN8				RW	0

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BYTE 16

Bit	Output(s) Affected	Description / Function	0	1	Type	Power On
7	T1CN7	Turbo1 CPU PLL N setting CLK = N*Resolution Resolution = 1.3333			RW	1
6	T1CN6				RW	0
5	T1CN5				RW	0
4	T1CN4				RW	1
3	T1CN3				RW	0
2	T1CN2				RW	1
1	T1CN1				RW	1
0	T1CN0				RW	0

BYTE 17

Bit	Output(s) Affected	Description / Function	0	1	Type	Power On
7	TSRC1_N7, MSB	Turbo1 SRC2, SRC1 SRC CLK = N*Resolution Resolution = 0.66667			RW	1
6	TSRC1_N6				RW	0
5	TSRC1_N5				RW	0
4	TSRC1_N4				RW	1
3	TSRC1_N3				RW	0
2	TSRC1_N2				RW	1
1	TSRC1_N1				RW	1
0	TSRC1_N0, LSB				RW	0

BYTE 18 (RESERVED FOR USER)

Bit	Output(s) Affected	Description / Function	0	1	Type	Power On
7					RW	0
6					RW	0
5					RW	0
4					RW	0
3					RW	0
2					RW	0
1					RW	0
0					RW	0

BYTE 19 (RESERVED FOR USER)

Bit	Output(s) Affected	Description / Function	0	1	Type	Power On
7					RW	0
6					RW	0
5					RW	0
4					RW	0
3					RW	0
2					RW	0
1					RW	0
0					RW	0

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BYTE 20 (RESERVED FOR USER)

Bit	Output(s) Affected	Description / Function	0	1	Type	Power On
7					RW	0
6					RW	0
5					RW	0
4					RW	0
3					RW	0
2					RW	0
1					RW	0
0					RW	0

BYTE 21

Bit	Output(s) Affected	Description / Function	0	1	Type	Power On
7	Reserved				RW	0
6	Reserved				RW	0
5	Reserved				RW	0
4	Reserved				RW	0
3	Reserved				RW	0
2	Reserved				RW	0
1	Test_scl	On chip test mode enable	Normal	SCLK = 1, CLK outputs = 1 SCLK = 0, CLK outputs = 0	RW	0
0	Test_hiz	CLK outputs enable	Normal	CLK outputs = Tristate	RW	0

BYTE 62 = 70h

BYTE 63 = 13h

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Description	Min	Max	Unit
V_{DDA}	3.3V Core Supply Voltage		4.6	V
V_{DD}	3.3V I/O Supply Voltage		4.6	V
V_{IH}	3.3V Input HIGH		4.6	V
V_{ID}	3.3V Input LOW	–0.5		V
T_S	Storage Temperature	–65	+150	°C
ESD Prot	Input ESD Protection Human Body Model	2000		V

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

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ELECTRICAL CHARACTERISTICS - INPUT / SUPPLY / COMMON OUTPUT PARAMETERS

Following Conditions Apply Unless Otherwise Specified:
Operating Condition: T_A = 0°C to +70°C, Supply Voltage: V_{DD} = 3.3V ± 5%

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{IH}	Input HIGH Voltage	3.3V ± 5%	2	—	V_{DD} + 0.3	V
V_{IL}	Input LOW Voltage	3.3V ± 5%	V_{SS} - 0.3	—	0.8	V
V_{IH_FS}	3.3V Input HIGH Voltage	V_{DD}	0.7	—	V_{DD} + 0.3	V
V_{IL_FS}	3.3V Input LOW Voltage		V_{SS} - 0.3	—	0.35	V
I_{IH}	Input HIGH Current	V_{IN} = V_{DD}	–5	—	5	µA
I_{IL1}	Input LOW Current	V_{IN} = 0V, inputs with no pull-up resistors	–5	—	—	µA
I_{IL2}	Input LOW Current	V_{IN} = 0V, inputs with pull-up resistors	–200	—	—	µA
$I_{DD3.3OP}$	Operating Supply Current	Full active, C_L = full load	—	—	400	mA
F_I	Input Frequency(1)	V_{DD} = 3.3V	—	14.31818	—	MHz
L_{PIN}	Pin Inductance(2)		—	—	7	nH
C_{IN}	Input Capacitance(2)	Logic inputs	—	—	5	pF
C_{OUT}		Output pin capacitance	—	—	6	
C_{INX}		X1 and X2 pins	—	—	5	
T_{STAB}	Clock Stabilization(2,3)	From V_{DD} power-up	—	—	1.8	ms
	Modulation Frequency(2)	Triangular modulation	30	—	33	KHz

NOTES:
1. Input frequency should be measured at the REF output pin and tuned to ideal 14.31818MHz to meet ppm frequency accuracy on PLL outputs.
2. This parameter is guaranteed by design, but not 100% production tested.
3. See TIMING DIAGRAMS for timing requirements.

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ELECTRICAL CHARACTERISTICS - SRC 0.7 CURRENT MODE DIFFERENTIAL PAIR

Following Conditions Apply Unless Otherwise Specified:
Operating Condition: T_A = 0°C to +70°C, Supply Voltage: V_{DD} = 3.3V ± 5%; C_L = 2pF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Z_O	Current Source Output Impedance(1)	$V_O = V_X$	3000	—	—	Ω
V_{OH3}	Output HIGH Voltage	I_{OH} = -1mA	2.4	—	—	V
V_{OL3}	Output LOW Voltage	I_{OL} = 1mA	—	—	0.4	V
V_{HIGH}	Voltage HIGH(1)	Statistical measurement on single-ended signal using	660	—	1150	mV
V_{LOW}	Voltage LOW(1)	oscilloscope math function	–300	—	150	
V_{OVS}	Max Voltage(1)	Measurement on single-ended signal using absolute value	—	—	1150	mV
V_{UDS}	Min Voltage(1)		–300	—	—	
$V_{CROSS(ABS)}$	Crossing Voltage (abs)(1)		250	—	550	mV
d - V_{CROSS}	Crossing Voltage (var)(1)	Variation of crossing over all edges	—	—	140	mV
ppm	Long Accuracy(1,2)	See T_{PERIOD} Min. - Max. values	–300	—	300	ppm
T_{PERIOD}	Average Period(2)	100MHz nominal	9.997	—	10.003	ns
T_{ABSMIN}	Absolute Min Period(1,2)	100MHz nominal	9.912	—	—	ns
t_R	Rise Time(1)	V_{OL} = 0.175V, V_{OH} = 0.525V	175	—	700	ps
t_F	Fall Time(1)	V_{OL} = 0.175V, V_{OH} = 0.525V	175	—	700	ps
d-t_R	Rise Time Variation(1)		—	—	125	ps
d-t_F	Fall Time Variation(1)		—	—	125	ps
d_{T3}	Duty Cycle(1)	Measurement from differential waveform	45	—	55	%
$t_{JCYC-CYC}$	Jitter, Cycle to Cycle(1)	Measurement from differential waveform	—	—	125	ps
S_{KEW}	Pin-to-Pin Skew(1)	V_T = 50%	—	—	250	ps
	T_{SU}_SRC(1,3)	SRC STOP response to CLKREQ#	—	—	60	ns
	T_{DRIVE}_SRC(1,3)	SRC START response to CLKREQ#	—	—	60	ns

NOTES:
1. This parameter is guaranteed by design, but not 100% production tested.
2. All long term accuracy and clock period specifications are guaranteed with the assumption that the REF output is at 14.31818MHz.
3. See TIMING DIAGRAMS for timing requirements.

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ELECTRICAL CHARACTERISTICS - CPU DIFFERENTIAL PAIR (SSC ENABLE AND DISABLE)

Following Conditions Apply Unless Otherwise Specified:
Operating Condition: T_A = 0°C to +70°C, Supply Voltage: V_{DD} = 3.3V ± 5%; C_L = 2pF

Symbol	Parameter[1]	Test Conditions	Min.	Typ.	Max.	Unit
t_R	Rise Edge Rate		2	—	10	V/ns
t_F	Fall Edge Rate		2	—	10	V/ns
V_{DIFF}	Differential Voltage (single end)		0.4	1.25	2.3	V
ΔV_{DIFF}	Change in V_{DIFF_DC} Magnitude		–150	—	+150	mV
V_{CM}	Common Mode Voltage		1.05	1.25	1.45	V
ΔV_{CM}	Change in Common Mode Voltage		–200	—	+200	mV
$t_{CCJITTER}$	Jitter, Cycle to Cycle		—	—	200	ps
t_{JA}	Jitter Accumulated		–1000	—	+1000	ps
t_{FS}	Frequency Stabilization from Power-Up		—	—	3	ms
R_{ON}	Output Impedance		15	35	55	Ω
Duty Cycle	Duty Cycle		47	50	53	%
ppm	Long Accuracy[2]	See T_{PERIOD} Min. - Max. values	–300	—	+300	ppm
T_{PERIOD}	Average Period[2]	200MHz nominal	4.9985	—	5.0015	ns
		250MHz nominal	3.9988	—	4.0012	

NOTES:
1. Parameters guaranteed by design, but not 100% production tested.
2. All long term accuracy and clock period specifications are guaranteed with the assumption that the REF output is at 14.31818MHz.

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ELECTRICAL CHARACTERISTICS - PCICLK / PCICLK_F, HTT66

Following Conditions Apply Unless Otherwise Specified:
Operating Condition: T_A = 0°C to +70°C, Supply Voltage: V_{DD} = 3.3V ± 5%; C_L = 10 - 30pF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
ppm	Long Accuracy(1,2)	See Tperiod Min. - Max. values	—	—	300	ppm
T_{PERIOD}	Clock Period(2)	33.33MHz output nominal	29.991	—	30.009	ns
		33.33MHz output spread	29.991	—	30.1598	
V_{OH}	Output HIGH Voltage	I_{OH} = -1mA	2.4	—	—	V
V_{OL}	Output LOW Voltage	I_{OL} = 1mA	—	—	0.55	V
I_{OH}	Output HIGH Current	V_{OH} at Min. = 1V	-33	—	—	mA
		V_{OH} at Max. = 3.135V	—	—	-33	
I_{OL}	Output LOW Current	V_{OL} at Min. = 1.95V	30	—	—	mA
		V_{OL} at Max. = 0.4V	—	—	38	
	Edge Rate(1)	Rising edge rate	1	—	4	V/ns
	Edge Rate(1)	Falling edge rate	1	—	4	V/ns
t_{R1}	Rise Time(1)	V_{OL} = 0.8V, V_{OH} = 2V	0.3	—	1.2	ns
t_{F1}	Fall Time(1)	V_{OL} = 0.8V, V_{OH} = 2V	0.3	—	1.2	ns
d_{T1}	Duty Cycle(1)	V_T = 1.5V	45	—	55	%
$t_{JCYC-CYC}$	Jitter, Cycle to Cycle(1)	V_T = 1.5V	—	—	500	ps

NOTES:
1. This parameter is guaranteed by design, but not 100% production tested.
2. All long term accuracy and clock period specifications are guaranteed with the assumption that the REF output is at 14.31818MHz.

ELECTRICAL CHARACTERISTICS - 24_48MHZ, 48MHZ, USB

Following Conditions Apply Unless Otherwise Specified:
Operating Condition: T_A = 0°C to +70°C, Supply Voltage: V_{DD} = 3.3V ± 5%; C_L = 10 - 20pF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
ppm	Long Accuracy(1,2)	See Tperiod Min. - Max. values	—	—	300	ppm
T_{PERIOD}	Clock Period(2)	48MHz output nominal	20.8257	—	20.834	ns
V_{OH}	Output HIGH Voltage	I_{OH} = -1mA	2.4	—	—	V
V_{OL}	Output LOW Voltage	I_{OL} = 1mA	—	—	0.55	V
I_{OH}	Output HIGH Current	V_{OH} at Min. = 1V	-29	—	—	mA
		V_{OH} at Max. = 3.135V	—	—	-23	
I_{OL}	Output LOW Current	V_{OL} at Min. = 1.95V	29	—	—	mA
		V_{OL} at Max. = 0.4V	—	—	27	
	Edge Rate(1)	Rising edge rate	1	—	2	V/ns
	Edge Rate(1)	Falling edge rate	1	—	2	V/ns
t_{R1}	Rise Time(1)	V_{OL} = 0.8V, V_{OH} = 2V	0.5	—	1.2	ns
t_{F1}	Fall Time(1)	V_{OL} = 0.8V, V_{OH} = 2V	0.5	—	1.2	ns
d_{T1}	Duty Cycle(1)	V_T = 1.5V	45	—	55	%
$t_{JCYC-CYC}$	Jitter, Cycle to Cycle(1)	V_T = 1.5V	—	—	350	ps

NOTES:
1. This parameter is guaranteed by design, but not 100% production tested.
2. All long term accuracy and clock period specifications are guaranteed with the assumption that the REF output is at 14.31818MHz.

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ELECTRICAL CHARACTERISTICS - REF-14.318MHZ

Following Conditions Apply Unless Otherwise Specified:
Operating Condition: T_A = 0°C to +70°C, Supply Voltage: V_{DD} = 3.3V ± 5%; C_L = 10 - 20pF

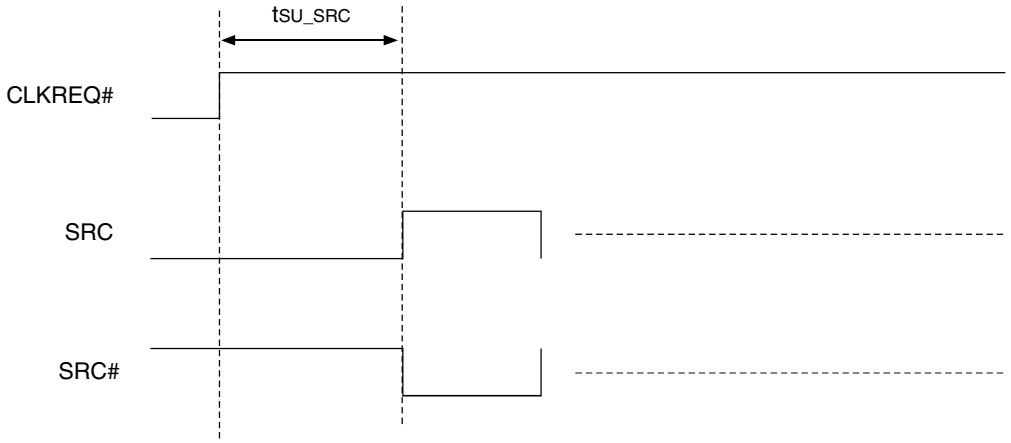
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
ppm	Long Accuracy(1)	See Tperiod Min. - Max. values	—	—	0	ppm
T_{PERIOD}	Clock Period	14.318MHz output nominal	69.827	—	69.855	ns
V_{OH}	Output HIGH Voltage(1)	I_{OH} = -1mA	2.4	—	—	V
V_{OL}	Output LOW Voltage(1)	I_{OL} = 1mA	—	—	0.4	V
I_{OH}	Output HIGH Current	V_{OH} at Min. = 1V	-33	—	—	mA
		V_{OH} at Max. = 3.135V	—	—	-33	
I_{OL}	Output LOW Current	V_{OL} at Min. = 1.95V	30	—	—	mA
		V_{OL} at Max. = 0.4V	—	—	38	
	Edge Rate(1)	Rising edge rate	1	—	4	V/ns
	Edge Rate(1)	Falling edge rate	1	—	4	V/ns
t_{R1}	Rise Time(1)	V_{OL} = 0.8V, V_{OH} = 2V	0.3	—	1.2	ns
t_{F1}	Fall Time(1)	V_{OL} = 0.8V, V_{OH} = 2V	0.3	—	1.2	ns
d_{T1}	Duty Cycle(1)	V_T = 1.5V	45	—	55	%
$t_{JCYC-CYC}$	Jitter, Cycle to Cycle(1)	V_T = 1.5V	—	—	1000	ps

NOTE:
1. This parameter is guaranteed by design, but not 100% production tested.

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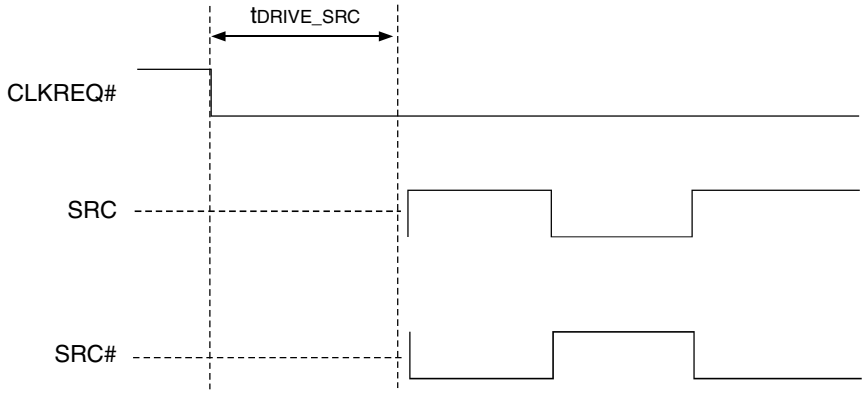
CLKREQ# ASSERTION

The clock samples the CLKREQ# signal on a rising edge of SRC clock. After detecting the CLKREQ# assertion low, all controlled SRC clocks will be tristate on their next high to low transition.



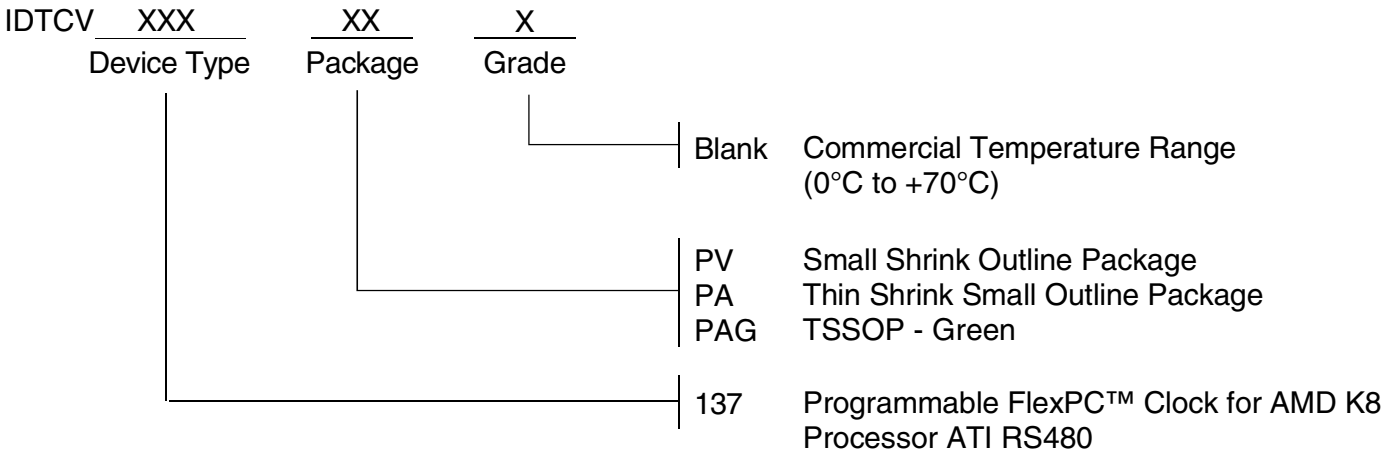
CLKREQ# - DE-ASSERTION

The de-assertion of the CLKREQ# signal is to be sampled on the rising edge of the SRC free running clock domain. After detecting CLKREQ# de-assertion, all controlled SRC clocks will resume in a glitch free manner.



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ORDERING INFORMATION



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