1-TO-19 DIFFERENTIAL CLOCK BUFFER

IDTCV145

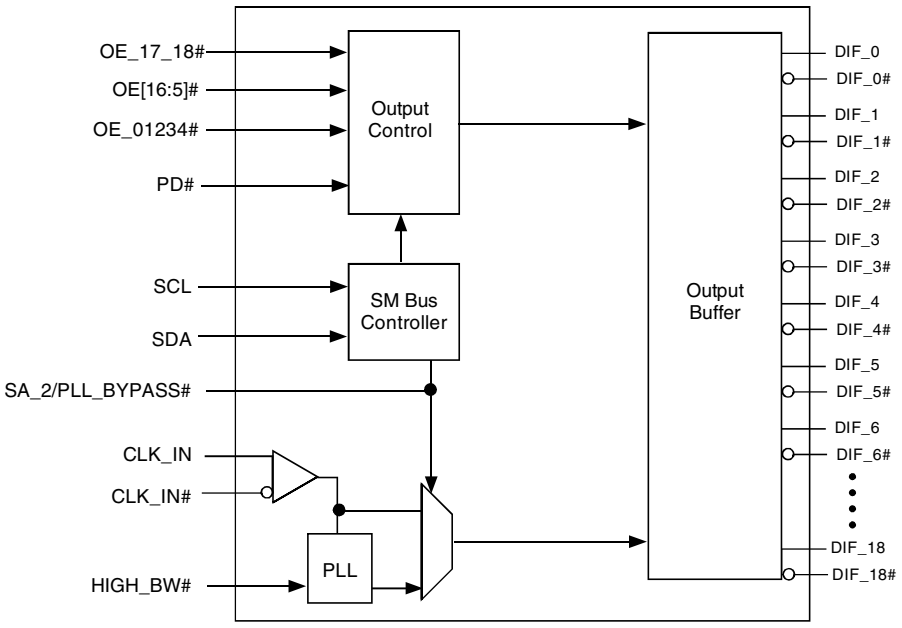
FEATURES:

- **Compliant with Intel DB1900G**
- **DIF Clock Support**
  - *19 differential clock output pairs @ 0.7 V*
  - *150 ps skew performance across all outputs*
- **OE pin Control of All Outputs**
- **3.3 V Operation**
- **Gear Ratio supporting generation of clocks at a different frequency ratioed from the input.**
- **Split outputs supporting options of 2 outputs @1:1 and remaining 17 pairs at an alternate gear**
- **Pin level OE control of individual outputs**
- **Multiple output frequency options up to 400Mhz as a gear ratio of input clocks of 100-400Mhz**
- **Output is HCSL compatible**
- **SMBus Programmable configurations**
- **PLL Bypass Configurable**
- **SMBus address configurable to allow multiple buffer control in a single control network**
- **Programmable Bandwidth**
- **Glitchfree transition between frequency states**
- **Available in 72-pin VFQPFN package**

DESCRIPTION:

The CV145 differential buffer complies with Intel DB1900G , and is designed to work in conjunction with the main clock of CK409, CK410/CK410M and CK410B etc., PLL is off in bypass mode and no clock detect.

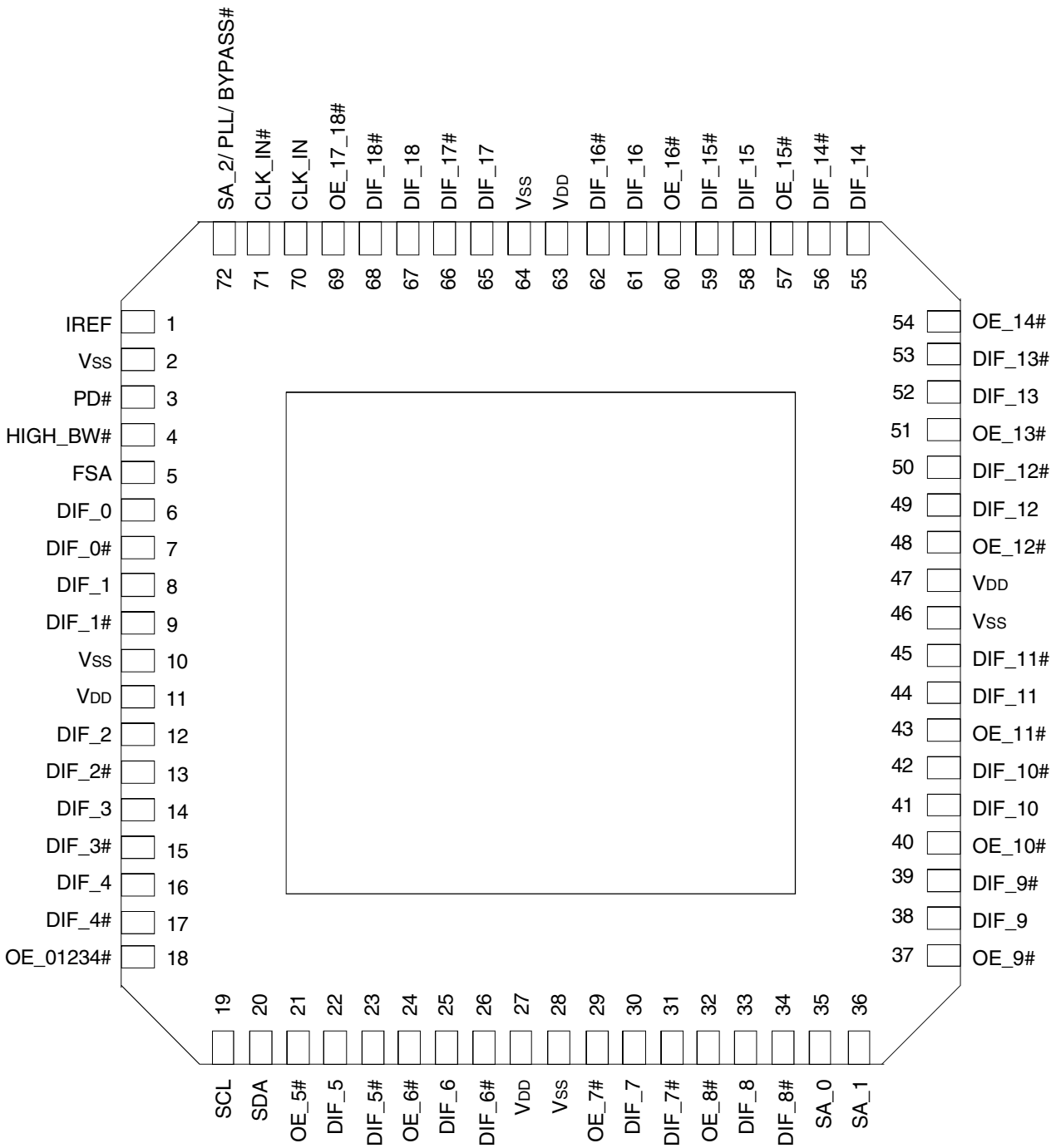
FUNCTIONAL BLOCK DIAGRAM



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PIN CONFIGURATION



VFQFPN
TOP VIEW

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ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Description	Min.	Max.	Unit
V_{DDA}	3.3V Core Supply Voltage		4.6	V
V_{DDIN}	3.3V Logic Input Supply Voltage	GND - 0.5	4.6	V
T_{STG}	Storage Temperature	–65	+150	°C
$T_{AMBIENT}$	Ambient Operating Temperature	0	+70	°C
T_{CASE}	Case Temperature		+115	°C
ESD Prot	Input ESD Protection Human Body Model	2000		V

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OE FUNCTIONALITY

OE# - Pin	OE# - SMBus bit	DIF	DIFF]#
0	1	Normal	Normal
0	0	Tristate	Tristate
1	1	Tristate	Tristate
1	0	Tristate	Tristate

PD FUNCTIONALITY

Inputs		Outputs		
PD# / V_{DDA}	CLK_IN / CLK_IN#	DIF	DIF#	PLL State
3.3V (Nom)	Running	Running		ON
GND	X	Hi-Z		OFF

PIN DESCRIPTION

Pin Name	Type	Pin #	Description
CLK_IN, CLK_IN#	IN	70, 71	0.7v Differential input
DIF_[16:0] & DIF_[16:0]#	OUT	6 - 9, 12 - 17, 22, 23, 25, 26, 30, 31, 33, 34, 38, 39, 41, 42, 44, 45, 49, 50, 52, 53, 55, 56, 58, 59, 61, 62	0.7 V Differential clock outputs, geared to a ratio of the input clock
DIF & DIF# [18:17]	OUT	65 - 68	0.7 V Differential clock outputs, which can be configured to be 1:1 instead of geared. Default is geared same as 0-9 outputs.
OE_[16:5]#	IN	21, 24, 29, 32, 37, 40, 43, 48, 51, 54, 57, 60	3.3 V LVTTL active LOW input for enabling corresponding differential output clock. Clocks also can be disabled via SMBus registers
OE_17_18#	IN	69	3.3 V LVTTL active low input for enabling both DIF10 and 11 differential output clocks. Clocks also can be disabled via SMBus registers individually.
OE_01234#	IN	18	3.3V LVTTL input
HIGH_BW#	IN	4	3.3 V LVTTL input for selecting the PLL bandwidth. 0 = HIGH BW, 1 = LOW BW.
SCL	IN	19	SMBus slave clock input
SDA	I/O, OC	20	Open collector SMBus data
IREF	IN	1	A precision resistor is attached to this pin to set the differential output current
SA_[1:0]	IN	35, 36	3.3V LVTTL input selecting the address. SA_[2:0] set device SMBus address.
SA_2/PLL_BYPASS#	IN	72	3.3 V LVTTL input for PLL bypass and SMBus address
FS_A	IN	5	3.3V LVTTL input to establish a HIGH (>200Mhz) or LOW frequency(<200Mhz) range
PD#	IN	3	3.3 V LVTTL input to power up or power down the device (see PD Functionality table).

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INDEX BLOCK WRITE PROTOCOL

Bit	# of bits	From	Description
1	1	Master	Start
2-9	8	Master	See SMBus Address Mode table
10	1	Slave	Ack (Acknowledge)
11-18	8	Master	Register offset byte (starting byte)
19	1	Slave	Ack (Acknowledge)
20-27	8	Master	Byte count, N (0 is not valid)
28	1	Slave	Ack (Acknowledge)
29-36	8	Master	first data byte (Offset data byte)
37	1	Slave	Ack (Acknowledge)
38-45	8	Master	2nd data byte
46	1	Slave	Ack (Acknowledge)
			:
		Master	Nth data byte
		Slave	Acknowledge
		Master	Stop

INDEX BLOCK READ PROTOCOL

Master can stop reading any time by issuing the stop bit without waiting until Nth byte (byte count bit30-37).

Bit	# of bits	From	Description
1	1	Master	Start
2-9	8	Master	See SMBus Address Mode table
10	1	Slave	Ack (Acknowledge)
11-18	8	Master	Register offset byte (starting byte)
19	1	Slave	Ack (Acknowledge)
20	1	Master	Repeated Start
21-28	8	Master	See SMBus Address Mode table
29	1	Slave	Ack (Acknowledge)
30-37	8	Slave	Byte count, N (block read back of N bytes)
38	1	Master	Ack (Acknowledge)
39-46	8	Slave	first data byte (Offset data byte)
47	1	Master	Ack (Acknowledge)
48-55	8	Slave	2nd data byte
			Ack (Acknowledge)
			:
		Master	Ack (Acknowledge)
		Slave	Nth data byte
			Not acknowledge
		Master	Stop

INDEX BYTE WRITE

Setting bit[11:18] = starting address, bit[20:27] = 01h.

INDEX BYTE READ

Setting bit[11:18] = starting address. After reading back the first data byte, master issues Stop bit.

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GEAR RATIOS

Select FSA	SMBus3	SMBus2	SMBus1	SMBus0	m	n	Gear n/m
0	0	0	0	0	3	1	0.333
0	0	0	0	1	5	2	0.400
0	0	0	1	0	12	5	0.417
0	0	0	1	1	2	1	0.500
0	0	1	0	0	5	3	0.600
0	0	1	0	1	8	5	0.625
0	0	1	1	0	3	2	0.667
0	0	1	1	1	4	3	0.750
0	1	0	0	0	6	5	0.833
0	1	0	0	1	1	1	1.000
0	1	0	1	0	5	6	1.200
0	1	0	1	1	4	5	1.250
0	1	1	0	0	3	4	1.333
0	1	1	0	1	2	3	1.500
0	1	1	1	0	3	5	1.667
0	1	1	1	1	1	2	2.000
1	0	0	0	0	3	1	0.333
1	0	0	0	1	5	2	0.400
1	0	0	1	0	12	5	0.417
1	0	0	1	1	2	1	0.500
1	0	1	0	0	5	3	0.600
1	0	1	0	1	8	5	0.625
1	0	1	1	0	3	2	0.667
1	0	1	1	1	5	4	0.800
1	1	0	0	0	6	5	0.833
1	1	0	0	1	1	1	1.000
1	1	0	1	0	5	6	1.200
1	1	0	1	1	4	5	1.250
1	1	1	0	0	3	4	1.333
1	1	1	0	1	2	3	1.500
1	1	1	1	0	3	5	1.667
1	1	1	1	1	1	2	2.000

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TARGETED INPUT AND OUTPUT FREQUENCIES

Input (MHz)	Output (MHz)	m:n	
200	200	1:1	
267	133	2:1	
160	320	1:2	
333	167	2:1	
200	400	1:2	
400	200	2:1	
200	133	3:2	
133	200	2:3	
400	133	3:1	
133	167	4:5	
167	133	5:4	
333	133	5:2	
200	267	3:4	
267	200	4:3	
400	160	5:2	
167	200	5:6	
200	167	6:5	
200	333	3:5	
333	200	5:3	
267	167	8:5	Targeted

SMBUS ADDRESS MODE SELECTION

SA_[2:0]	Buffer Address
000	D0h (write) D1h (read)
001	D2h, D3h
010	D4h, D5h
011	D6h, D7h
100	D8h, D9h
101	DAh, DBh
110	DCh, DDh
111	Deh, DFh

FUNCTIONALITY AT POWER-UP(1)

FSA	CLK_IN (CPU FSB)	DIF[9:0] Output	DIF[11:10] Output
1	100MHz	100MHz	100MHz
1	133MHz	133MHz	133MHz
1	166MHz	166MHz	166MHz
1	RESERVED	RESERVED	RESERVED
0	200MHz	200MHz	200MHz
0	266.66MHz	266.66MHz	266.66MHz
0	333.33MHz	333.33MHz	333.33MHz
0	400MHz	400MHz	400MHz

NOTE:
1. FSA is a low-threshold input. Please see the V_{IL_FS} and V_{IH_FS} specifications in the DC OPERATING CHARACTERISTICS table.

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CONTROL REGISTERS

BYTE 0

Bit	Output(s) Affected	Description/Function	0	1	Type	Power On
7	Group of 17 gear # DIF[16:0] Speed selection		GR selection	1:1 = In	RW	1
6	Group of 2 gear # DIF[18:17] Speed selection		GR selection	1:1 = In	RW	1
5	Reserved				RW	1
4	FSA latched input				RW	
3	SMBus3				RW	
2	SMBus2				RW	
1	SMBus1				RW	
0	SMBus0				RW	

BYTE 1

Bit	Output(s) Affected	Description/Function	0	1	Type	Power On
7	DIF_7	Output Enable	Tristate	Enable	RW	1
6	DIF_6	Output Enable	Tristate	Enable	RW	1
5	DIF_5	Output Enable	Tristate	Enable	RW	1
4	DIF_4	Output Enable	Tristate	Enable	RW	1
3	DIF_3	Output Enable	Tristate	Enable	RW	1
2	DIF_2	Output Enable	Tristate	Enable	RW	1
1	DIF_1	Output Enable	Tristate	Enable	RW	1
0	DIF_0	Output Enable	Tristate	Enable	RW	1

BYTE 2

Bit	Output(s) Affected	Description/Function	0	1	Type	Power On
7	PLL_BW# adjust		HIGH BW	LOW BW	RW	1
6	BYPASS# test mode / PLL		Bypass	PLL	RW	1
5	DIF_13	Output Enable	Tristate	Enable	RW	1
4	DIF_12	Output Enable	Tristate	Enable	RW	1
3	DIF_11	Output Enable	Tristate	Enable	RW	1
2	DIF_10	Output Enable	Tristate	Enable	RW	1
1	DIF_9	Output Enable	Tristate	Enable	RW	1
0	DIF_8	Output Enable	Tristate	Enable	RW	1

BYTE 3

Bit	Output(s) Affected	Description / Function	0	1	Type	Power On
7	Readback - OE#_9 Input	Depends on the state of the pin			R	
6	Readback - OE#_8 Input				R	
5	Readback - OE#_7 Input				R	
4	Readback - OE#_6 Input				R	
3	Readback - OE#_5 Input				R	
2	Readback - OE#_01234 Input				R	
1	Readback - HIGHBW# Input	Latch value of pin at power-up			R	
0	Readback - SA2/PLL/BYPASS# Input	Latch value of pin at power-up			R	

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BYTE 4

Bit	Output(s) Affected	Description / Function	0	1	Type	Power On
7	Readback - OE#_17_18 Input	Depends on the state of the pin			R	
6	Readback - OE#_16 Input				R	
5	Readback - OE#_15 Input				R	
4	Readback - OE#_14 Input				R	
3	Readback - OE#_13 Input				R	
2	Readback - OE#_12 Input				R	
1	Readback - OE#_11 Input				R	
0	Readback - OE#_10 Input				R	

BYTE 5

Bit	Output(s) Affected	Description / Function	0	1	Type	Power On
7		Revision ID			R	0
6		Revision ID			R	0
5		Revision ID			R	0
4		Revision ID			R	0
3		Vendor ID			R	0
2		Vendor ID			R	1
1		Vendor ID			R	0
0		Vendor ID			R	1

BYTE 6 - DEVICE ID

BYTE 7 - BYTE COUNT

BYTE 8

Bit	Output(s) Affected	Description / Function	0	1	Type	Power On
7	Readback - FSA Input	Latch Value of pin at power-up			R	
6	Reserved				R	
5	Reserved				R	
4	DIF_18	Output Enable	Tristate	Enable	RW	1
3	DIF_17	Output Enable	Tristate	Enable	RW	1
2	DIF_16	Output Enable	Tristate	Enable	RW	1
1	DIF_15	Output Enable	Tristate	Enable	RW	1
0	DIF_14	Output Enable	Tristate	Enable	RW	1

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DC OPERATING CHARACTERISTICS

Following Conditions Apply Unless Otherwise Specified:
Operating Condition: V_{DD}/V_{DDA} = 3.3V ± 5%

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{DDA}	3.3 V Core Supply Voltage	3.3 V ±5%	3.135	-	3.465	V
V_{DD}	3.3 V I/O Supply Voltage	3.3 V ±5%	3.135	-	3.465	V
I_{DD}	3.3 V Supply Current	3.3 V ±5%, 0 to 70C	-	450	600	mA
I_{DDPD}	3.3 V Power Down Supply Current	3.3 V ±5%, 0 to 70C	-	20	36	mA
V_{IH}	3.3 V Input High Voltage	Vdd	2.0	-	Vdd+0.3	V
V_{IL}	3.3 V Input Low Voltage		Vss-0.3	-	0.8	V
I_{IL}	Input Leakage Current	0 < Vin < Vdd	-5	-	5	µA
Cin	Input Pin Capacitance		1.5	-	5	pF
Cout	Output Pin Capacitance		-	-	6	pF
Lpin	Pin Inductance		-	-	7	nH
Ta	Ambient Temperature	No Airflow	0	-	70	°C

OUTPUT RELATIONAL TIMING PARAMETERS

Group	Parameter	Min.	Typ.	Max.
CLK_IN, DIF [x:0]	Input to Output Skew in PLL mode (1:1 only)	-500ps	0	+500ps
CLK_IN, DIF [x:0]	Input to Output Skew in non PLL mode (1:1 only)	2.5ns	4	4.5ns
DIF	DIFF[x:0] Pin-to-Pin Skew (output within same group)	0ps	115	125ps
DIF	DIFF[x:0] Pin-to-Pin Skew (across all outputs)	0ps	115	150ps
DIF	Accumulated Differential Phase Jitter	-100ps	0	+100ps

PLL BANDWIDTH AND PEAKING

Group	Parameter	Min.	Typ.	Max.	Unit
DIF	PLL Peaking (HIGH_BW# = 0)	0	1	2.5	dB
DIF	PLL Peaking (HIGH_BW# = 1)	0	1	2	dB
DIF	PLL Bandwidth (HIGH_BW# = 0)	2	3.8	4	MHz
DIF	PLL Bandwidth (HIGH_BW# = 1)	0.7	0.9	1.4	MHz
DIF	Output phase jitter impact (PCIe: including BW 1.5-22Mhz)	-	99	108	ps
	Output phase jitter impact (FBD/CSI: including BW 11-33Mhz)	-	3	3	ps Rms

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DIF TIMING CHARACTERISTICS (NON SSC CLOCK INPUT)

DIF 0.7 V AC Timing Characteristics (Non-Spread Spectrum Mode)

Symbol	Parameter	CLK - 100Mhz, 133.3Mhz, 166.6Mhz, 200Mhz, 233.3Mhz, 266.6Mhz, 333Mhz, 400Mhz			Unit
		Min.	Typ.	Max.	
Laccuracy	Long Accuracy	-	-	0	ppm
Tperiod	Average Period	-0.30%	-	0.30%	ns
Tabsmin	Absolute Minimum Host CLK Period	-2.50%	-	-	ns
Trise	Rise Time	125	-	700	ps
Tfall	Fall Time	125	-	700	ps
ΔTrise	Rise Time Variation	-	-	75	ps
ΔTfall	Fall Time Variation	-	-	75	ps
Rise/Fall Matching		-	-	20%	
Vhigh	Voltage HIGH (typ 0.7 Volts)	660	-	850	mV
Vlow	Voltage LOW (typ 0 Volts)	-300	-	150	mV
Vcross absolute	Absolute Crossing Point Voltages	250	-	550	mV
Total Δ Vcross	Total Variation of Vcross Over All Edges	-	-	140	mV
Tccjitter	PLL Mode Cycle-to-Cycle Jitter Fin = 100, 166,67, 200, 266.67, 333.33 MHz	-	-	50	ps
Tccjitter	PLL Mode Cycle-to-Cycle Jitter Fin = 133.33, 400.00 MHz	-	-	75	ps
Tccjitter	Bypass Mode Cycle-to-Cycle Jitter (Additive)	-	-	50	ps
Duty Cycle		45	-	55	%
Vovs	Maximum Voltage (Overshoot)	-	-	Vh + 0.3V	
Vuds	Minimum Voltage (Undershoot)	-	-	-0.3	
Vrb	Ringback Voltage	0.2	-	N/A	Volt

DIF TIMING CHARACTERISTICS (SSC CLOCK INPUT)

DIF 0.7 V AC Timing Characteristics (-0.5% Spread Spectrum Mode)

Symbol	Parameter	CLK - 100Mhz, 133.3Mhz, 166.6Mhz, 200Mhz, 233.3Mhz, 266.6Mhz, 333Mhz, 400Mhz			Unit
		Min.	Typ.	Max.	
Laccuracy	Long Accuracy	---	-	0	ppm
Tperiod	Average Period	-0.30%	-	0.53%	ns
Tabsmin	Absolute Minimum Host CLK Period	(period - 0.125ns)	-	-	ns
Trise	Rise Time	125	-	700	ps
Tfall	Fall Time	125	-	700	ps
ΔTrise	Rise Time Variation	-	-	75	ps
ΔTfall	Fall Time Variation	-	-	75	ps
Rise/Fall Matching		-	-	20%	
Vhigh	Voltage HIGH (typ 0.7 Volts)	660	-	850	mV
Vlow	Voltage LOW (typ 0 Volts)	-300	-	150	mV
Vcross absolute	Absolute Crossing Point Voltages	250	-	550	mV
Vcross relative	Relative Crossing Point Voltages	Calc	-	Calc	
Total Δ Vcross	Total Variation of Vcross Over All Edges	-	-	140	mV
Tccjitter	PLL Mode Cycle-to-Cycle Jitter Fin = 100, 166,67, 200, 266.67, 333.33 MHz	-	-	50	ps
Tccjitter	PLL Mode Cycle-to-Cycle Jitter Fin = 133.33, 400.00 MHz	-	-	75	ps
Tccjitter	Bypass Mode Cycle-to-Cycle Jitter (Additive)	-	-	50	ps
Duty Cycle		45	-	55	%
Vovs	Maximum Voltage (Overshoot)	-	-	Vh + 0.3V	
Vuds	Minimum Voltage (Undershoot)	-	-	-0.3	
Vrb	Ringback Voltage	Vx ± 0.2	-	N/A	Volt

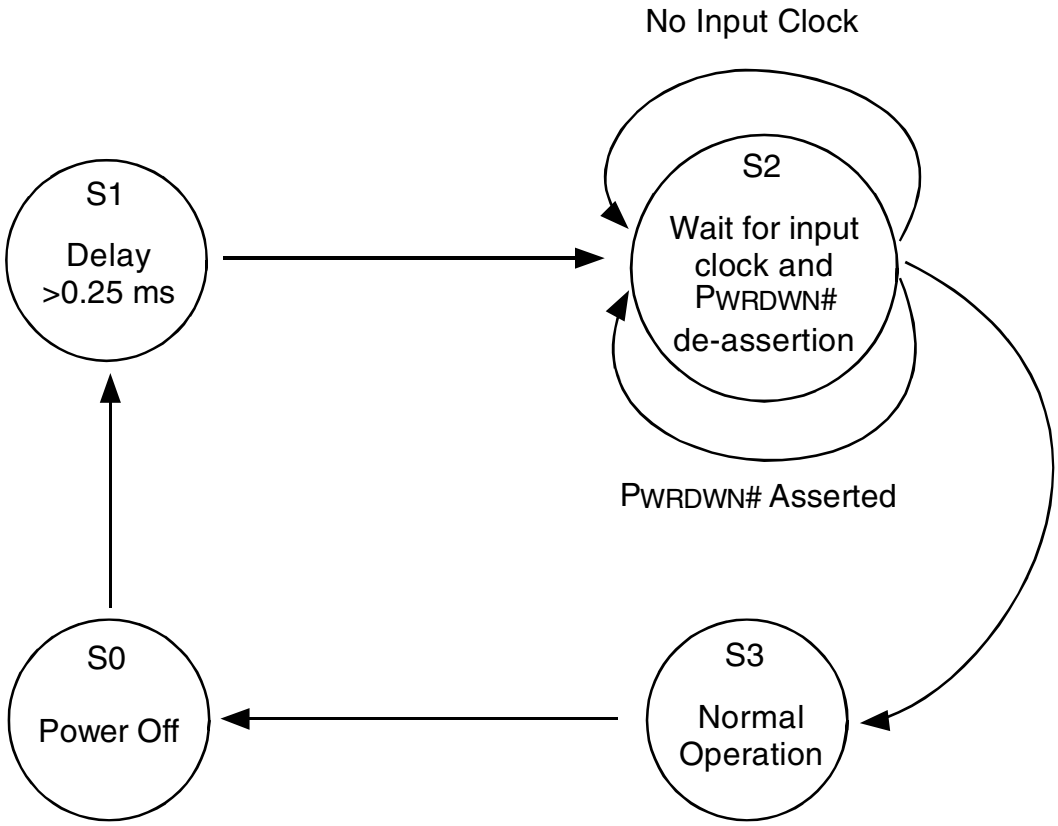
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BUFFER POWER-UP STATE MACHINE(1)

State	Description
State0	Power off
State1	After 3.3V supply is detected to rise above 1.8-2V, the buffer enters state1 and initiates a 0.2ms-0.3ms delay. The total power up latency from power on to all outputs active must be less than 1ms (assume SRC_IN is available)
State2	Buffer waits for a valid clock on the SRC_IN input and PD de-assertion.
State3	Only after SRC_IN and power valid, PD de-asserted with the current mirror stable, or PLL lock, the DIF outputs are enabled

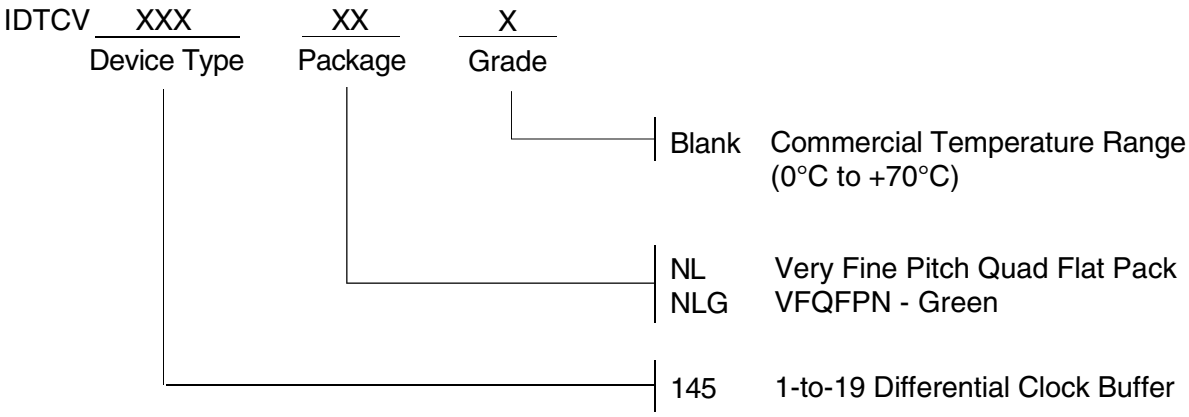
NOTE:
1. The total power up latency from power on to all outputs active must be less than 1ms (assuming a valid clock is present on CLK_IN input). If power is valid and PWRDWN is de-asserted but no input clocks are present on the CLK_IN input, DIF clocks must remain disabled. Only after valid input clocks are detected, valid power, PWRDWN# de-asserted with the PLL locked/stable and the DIF outputs enabled (doesn't apply to bypass mode).

BUFFER POWER-UP STATE DIAGRAM



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ORDERING INFORMATION



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REVISION HISTORY

JUNE 08, 2006 **Updated Electrical Characteristics pages (9-10).**

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