8×8/7×9 MATRIX LED DRIVER

May 2022

GENERAL DESCRIPTION

The IS31FL3717 is a general purpose 7×9 or 8×8 LED Matrix programmed via 1MHz I2C compatible interface. All LED can be turned on and off individually, and all of the LED can be dimmed individually with 8-bit PWM data, all LED has a global 7-bit DC data which allowing 128 steps of linear DC current adjustable level for all LED.

Additionally each LED open and short state can be detected, IS31FL3717 store the open or short information in Open-Short Registers. The Open-Short Registers allowing MCU to read out via I2C compatible interface. Inform MCU whether there are LEDs open or short and the locations of open or short LEDs.

The IS31FL3717 operates from 2.7V to 5.5V and features a very low shutdown and operational current.

IS31FL3739 is available in SOP-24 package. It operates from 2.7V to 5.5V over the full temperature range of -40°C to +125°C.

FEATURES

- Supply voltage range: 2.7V to 5.5V
- Pin compatible with IS31FL3739 (7×9 and 8×8 mode)
- 8 current sinks
- Support 8×n (n=1~8) or 7×9 LED matrix configurations
- Individual 256 PWM control steps for 8×8/9×7 LEDs
- 128 global current steps
- SDB rising edge reset I2C module
- 256kHz PWM frequency or 28.4kHz scanning rate when n=9
- 1MHz I2C-compatible interface
- Individual open and short error detect function
- PWM 180 degree phase shift
- De-ghost
- SOP-24 package

APPLICATIONS

- White goods LED display panel
- Gaming device
- IOT device

TYPICAL APPLICATION CIRCUIT

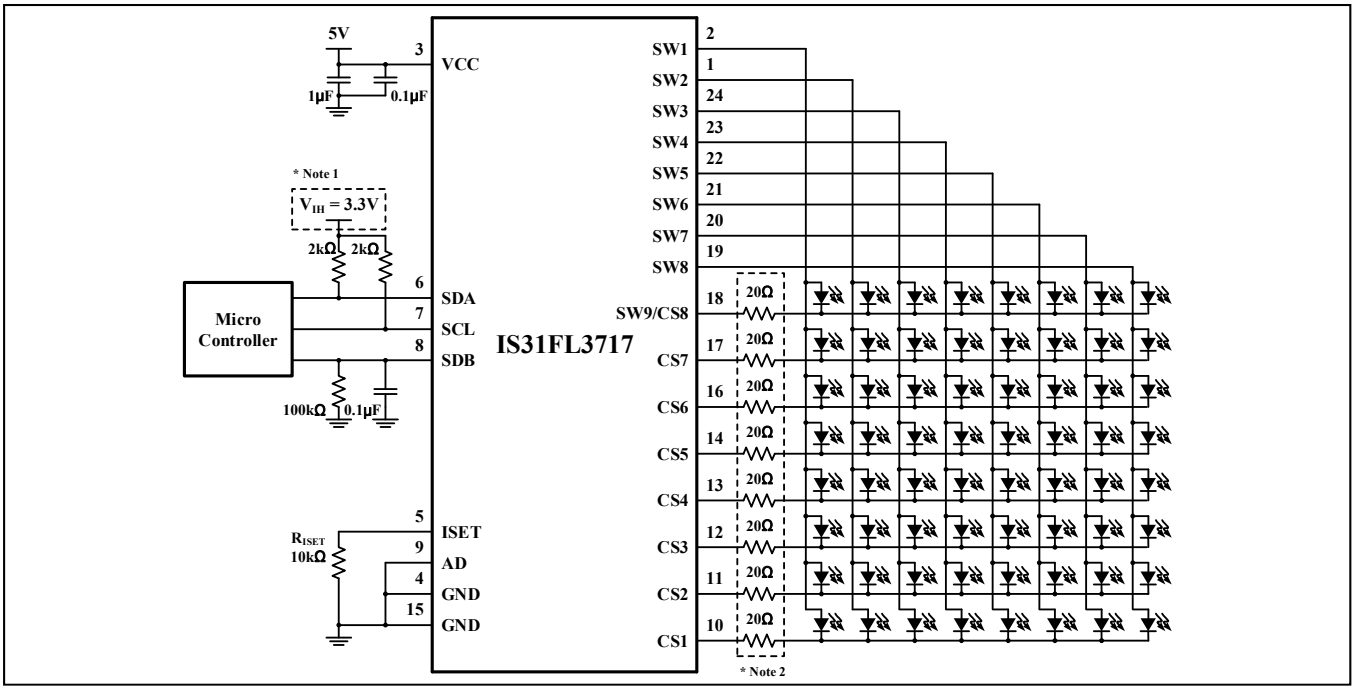


Figure 1 Typical Application Circuit (8×8)

Note 1: The VIH of I2C bus should be not higher than VCC. And if VIH is lower than 3.0V, it is recommended add a level shift circuit to avoid extra shutdown current.

Note 2: These optional resistors are for offloading the thermal dissipation ($P=I^2R$) away from the IS31FL3717, for mono red/yellow/orange LED, if $PV_{CC}=V_{CC}=3.3V$, don't need these resistors.

TYPICAL APPLICATION CIRCUIT (CONTINUED)

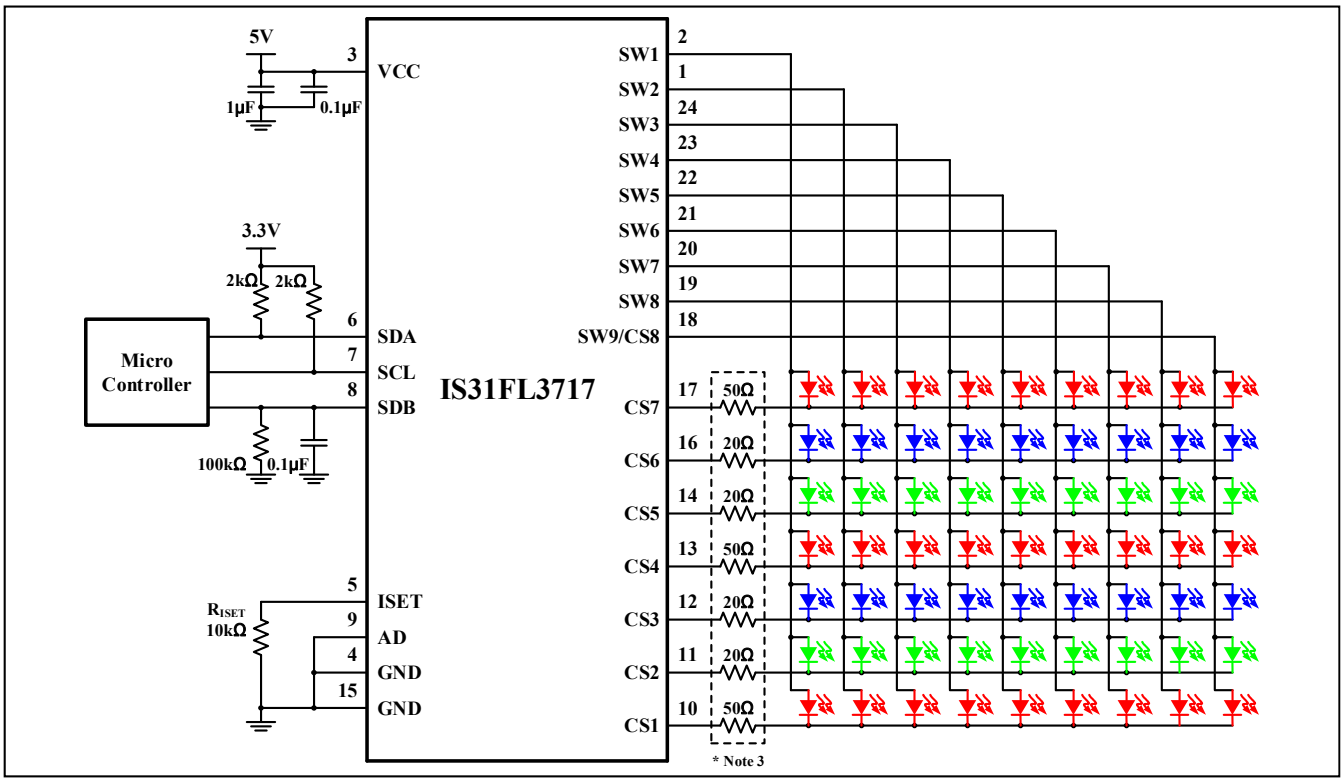


Figure 2 Typical Application Circuit (7×9, RGB)

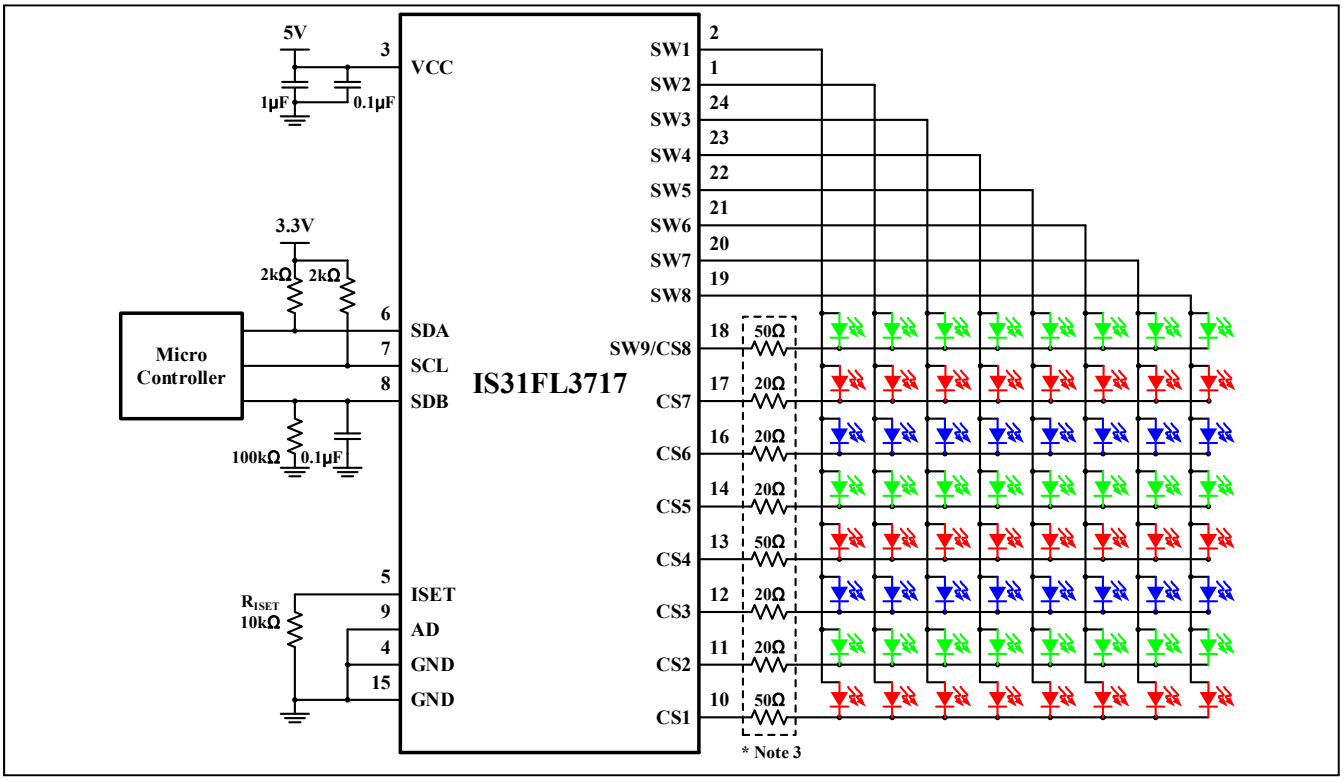
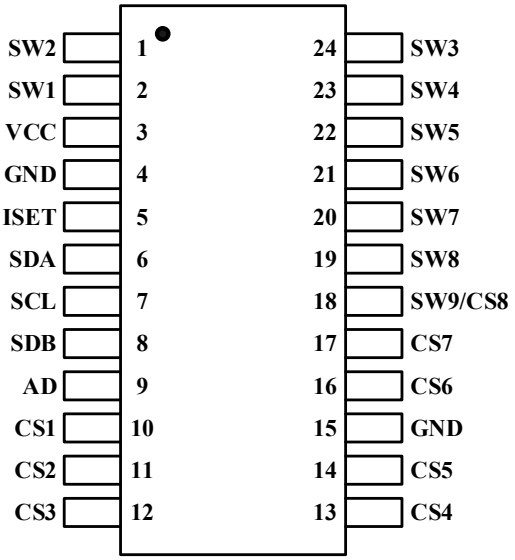


Figure 3 Typical Application Circuit (8×8, RGB)

Note 3: These optional resistors are for offloading the thermal dissipation ($P=I^2R$) away from the IS31FL3717, for red LED, it is recommended to use about 30Ω more than blue/green LED, to offload more extra voltage due to lower forward voltage of red LED.

PIN CONFIGURATION

Package	Pin Configuration (Top View)
SOP-24	

PIN DESCRIPTION

No.	Pin	Description
1, 2	SW2, SW1	Switch power source.
3	VCC	Power supply.
4, 15	GND	Ground.
5	ISET	Current setting pin.
6	SDA	Serial data.
7	SCL	Serial clock.
8	SDB	Shutdown the chip when pull to low.
9	AD	I2C Address setting.
10~14	CS1~CS5	Current sinks output.
16, 17	CS6, CS7	Current sinks output.
18	SW9/CS8	Switch power source or current sink output.
19~24	SW8~SW3	Switch power source.

ORDERING INFORMATION
Industrial Range: -40°C to +125°C

Order Part No.	Package	QTY/Reel
IS31FL3717-GRLS4-TR	SOP-24, Lead-free	1500

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ABSOLUTE MAXIMUM RATINGS

Supply voltage, V_{CC}	-0.3V ~+6.0V
Voltage at any input pin	-0.3V ~ V_{CC}+0.3V
Maximum junction temperature, T_{JMAX}	+150°C
Storage temperature range, T_{STG}	-65°C ~+150°C
Operating temperature range, T_A=T_J	-40°C ~ +125°C
Package thermal resistance, junction to ambient (4-layer standard test PCB based on JESD 51-2A), θ_{JA}	40.7°C/W
ESD (HBM) ESD (CDM)	±8kV ±750V

Note 4: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

The following specifications apply for V_{CC}= 5V, T_A= 25°C, unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{CC}	Supply voltage		2.7		5.5	V
I_{CC}	Quiescent power supply current	V_{SDB}= V_{CC}= 5V, 8-bit mode, All LEDs PWM= 0x00, OSC= 8MHz		1.29	1.9	mA
		V_{SDB}= V_{CC}= 3.6V, 8-bit mode, All LEDs PWM= 0x00, OSC= 8MHz		0.82	1.3	
I_{SD}	Shutdown current	V_{SDB}= 0V		0.6	2	µA
		V_{SDB}= V_{CC}= 5V, software shutdown mode		0.7	2	
		V_{SDB}= 0V		0.43	2	
		V_{SDB}= V_{CC}= 3.6V, software shutdown mode		0.43	2	
I_{OUT}	Peak current of CSy	R_{ISET}= 10kΩ, I_{OUT}= 34.6mA	31.8	34.6	37.4	mA
ΔI_{MAT}	Sink current between channels	I_{OUT}= 34.6mA (Note 5)	-6		6	%
ΔI_{ACC}	Sink current Between device to device	I_{OUT}= 34.6mA (Note 6)	-6		6	%
I_{LED}	Average current on each LED I_{LED}= $I_{OUT(PEAK)}$/Duty	R_{ISET}= 10kΩ, n= 8, Duty=1/8.205		4.21		mA
V_{HR}	Current switch headroom voltage SWx	I_{SW}= 600mA		500	780	mV
	Current sink headroom voltage CSy	I_{OUT}= 34.6mA		450	600	
t_{SCAN}	Period of scanning of single SWx	8-bit PWM mode		32	40	µs
		6+2-bit PWM mode		4	5	
t_{NOL1}	Non-overlap blanking time during scan, the SWx and CSy are all off during this time	8-bit PWM mode		0.55	0.7	µs
		6+2-bit PWM mode		0.25	0.35	
t_{NOL2}	Delay total time for CS1 to CS8, during this time, the SWx is on but CSy is not all turned on	8-bit PWM mode, 32kHz (Note 7)		0.27		µs
		16MHz OSC, 6+2-bit PWM mode (Note 7)		0.1		
V_{OD}	CSy pin open detect threshold	V_{CC}= 5V, R_{ISET}= 10kΩ, I_{OUT}≥0.1mA, measured at CSy	0.12	0.24		V
V_{SD}	LED short detect threshold	V_{CC}= 5V, R_{ISET}= 10kΩ, I_{OUT}≥ 0.1mA, measured at (V_{CC}-V_{CSy})	0.6	1.0	1.4	V

ELECTRICAL CHARACTERISTICS (CONTINUE)

The following specifications apply for V_{CC}= 5V, T_A= 25°C, unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Logic Electrical Characteristics (SDA, SCL, AD, SDB)						
V_{IL}	Logic “0” input voltage	V_{CC}= 2.7V~5.5V	GND		0.3V_{CC}	V
V_{IH}	Logic “1” input voltage	V_{CC}= 2.7V~5.5V	0.7V_{CC}		V_{CC}	V
V_{IL}	Logic “0” input voltage	V_{CC}= 4.5V~5.5V	GND		0.3V_{CC}	V
V_{IH}	Logic “1” input voltage	V_{CC}= 4.5V~5.5V	0.5V_{CC}		V_{CC}	V
V_{HYS}	Input schmitt trigger hysteresis	V_{CC}= 5V (Note 7)		0.35		V
I_{IL}	Logic “0” input current	SDB= L, V_{INPUT}= L (Note 7)		5		nA
I_{IH}	Logic “1” input current	SDB= L, V_{INPUT}= H (Note 7)		5		nA

DIGITAL INPUT I2C SWITCHING CHARACTERISTICS (NOTE 7)

Symbol	Parameter	Fast Mode			Fast Mode Plus			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
f_{SCL}	Serial-clock frequency	-		400	-		1000	kHz
t_{BUF}	Bus free time between a STOP and a START condition	1.3		-	0.5		-	µs
$t_{HD, STA}$	Hold time (repeated) START condition	0.6		-	0.26		-	µs
$t_{SU, STA}$	Repeated START condition setup time	0.6		-	0.26		-	µs
$t_{SU, STO}$	STOP condition setup time	0.6		-	0.26		-	µs
$t_{HD, DAT}$	Data hold time	-		-	-		-	µs
$t_{SU, DAT}$	Data setup time	100		-	50		-	ns
t_{LOW}	SCL clock low period	1.3		-	0.5		-	µs
t_{HIGH}	SCL clock high period	0.7		-	0.26		-	µs
t_R	Rise time of both SDA and SCL signals, receiving	-		300	-		120	ns
t_F	Fall time of both SDA and SCL signals, receiving	-		300	-		120	ns

Note 5: I_{OUT} mismatch (bit to bit) $\triangle I_{MAT}$ is calculated:

$$\Delta I_{MAT} = \pm \left(\frac{I_{OUT(MAX)} - I_{OUT(MIN)}}{\left(\frac{I_{OUT0} + I_{OUT1} + ... + I_{OUT23}}{24} \times 2 \right)} \right) \times 100\%$$

Note 6: I_{OUT} accuracy (device to device) $\triangle I_{ACC}$ is calculated:

$$\Delta I_{ACC} = \pm MAX \left(\frac{I_{OUT(MIN)} - I_{OUT(IDEAL)}}{I_{OUT(IDEAL)}} \right) \times 100\%$$

Where $I_{OUT(IDEAL)}$= 34.6mA when R_{ISET}= 10kΩ.

Note 7: Guaranteed by design.

DETAILED DESCRIPTION

I2C INTERFACE

IS31FL3717 uses a serial bus, which conforms to the I2C protocol, to control the chip's functions with two wires: SCL and SDA. The IS31FL3717 has a 7-bit slave address (A7:A1), followed by the R/W bit, A0. Set A0 to "0" for a write command and set A0 to "1" for a read command. The value of bits A1 and A2 are decided by the connection of the AD pin.

Table 1 Slave Address

AD	A7:A3	A2:A1	A0
GND	01101	00	0/1
SCL		01	
SDA		10	
VCC		11	

AD connected to GND, A2:A1=00;
AD connected to VCC, A2:A1=11;
AD connected to SCL, A2:A1=01;
AD connected to SDA, A2:A1=10;

The SCL line is uni-directional. The SDA line is bi-directional (open-drain) with a pull-up resistor (typically 400kHz I2C with 4.7kΩ, 1MHz I2C with 2kΩ). The maximum clock frequency specified by the I2C standard is 1MHz. In this discussion, the master is the microcontroller and the slave is the IS31FL3717.

The timing diagram for the I2C is shown in Figure 4. The SDA is latched in on the stable high level of the SCL. When there is no interface activity, the SDA line should be held high.

The "START" signal is generated by lowering the SDA signal while the SCL signal is high. The start signal will alert all devices attached to the I2C bus to check the incoming address against their own chip address.

The 8-bit chip address is sent next, most significant bit first. Each address bit must be stable while the SCL level is high.

After the last bit of the chip address is sent, the master checks for the IS31FL3717's acknowledge. The master releases the SDA line high (through a pull-up resistor). Then the master sends an SCL pulse. If the IS31FL3717 has received the address correctly, then it holds the SDA line low during the SCL pulse. If the SDA line is not low, then the master should send a "STOP" signal (discussed later) and abort the transfer.

Following acknowledge of IS31FL3717, the register address byte is sent, most significant bit first. IS31FL3717 must generate another acknowledge indicating that the register address has been received.

Then 8-bit of data byte are sent next, most significant bit first. Each data bit should be valid while the SCL level is stable high. After the data byte is sent, the IS31FL3717 must generate another acknowledge to indicate that the data was received.

The "STOP" signal ends the transfer. To signal "STOP", the SDA signal goes high while the SCL signal is high.

ADDRESS AUTO INCREMENT

To write multiple bytes of data into IS31FL3717, load the address of the data register that the first data byte is intended for. During the IS31FL3717 acknowledge of receiving the data byte, the internal address pointer will increment by one. The next data byte sent to IS31FL3717 will be placed in the new address, and so on. The auto increment of the address will continue as long as data continues to be written to IS31FL3717 (Figure 7).

READING OPERATION

Most of the registers can be read.

To read the register, after I2C start condition, the bus master must send the IS31FL3717 device address with the R/$\overline{W}$ bit set to "0", followed by the register address which determines which register is accessed. Then restart I2C, the bus master should send the IS31FL3717 device address with the R/$\overline{W}$ bit set to "1". Data from the register defined by the command byte is then sent from the IS31FL3717 to the master (Figure 8).

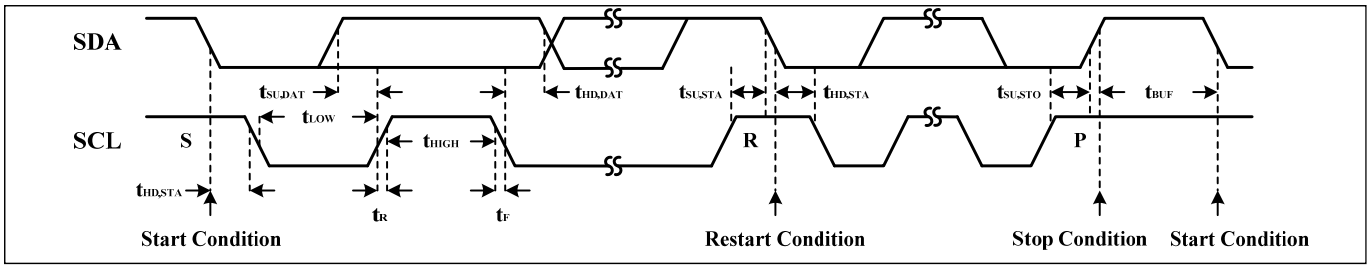


Figure 4 I2C Interface Timing

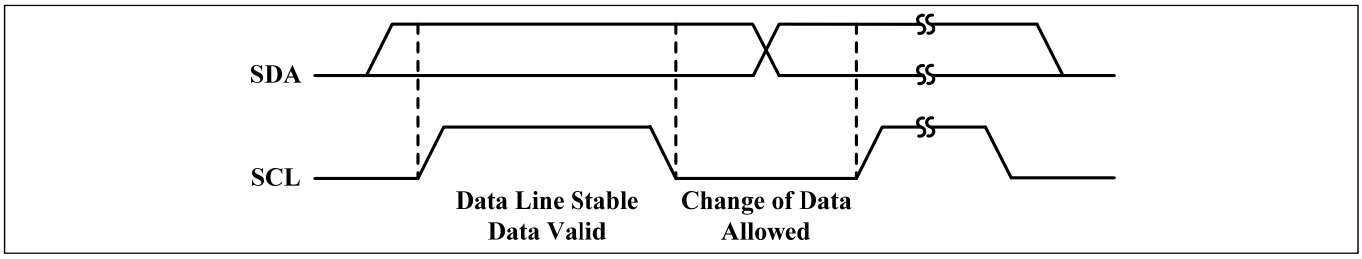


Figure 5 I2C Bit Transfer

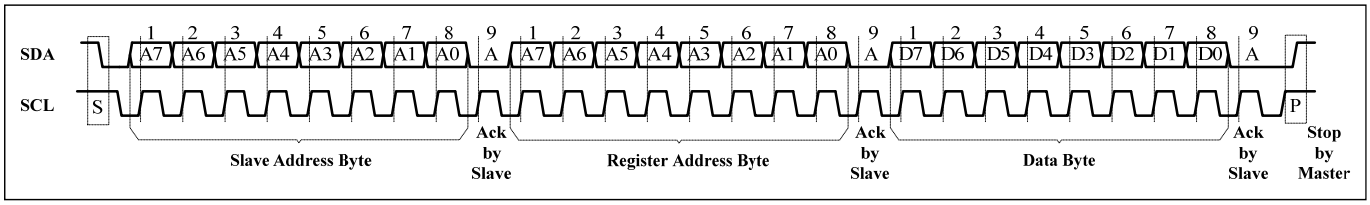


Figure 6 I2C Writing to IS31FL3717 (Typical)

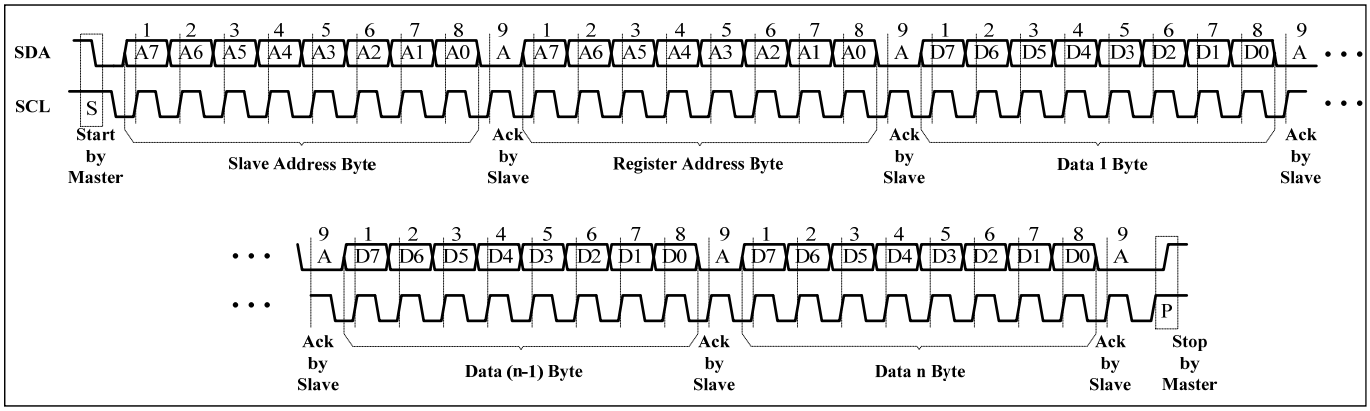


Figure 7 I2C Writing to IS31FL3717 (Automatic Address Increment)

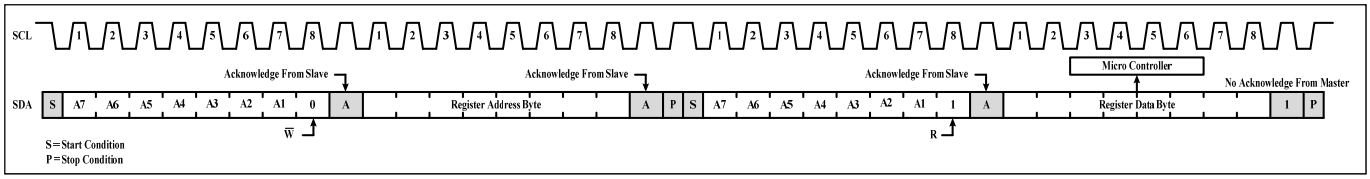


Figure 8 I2C Reading from IS31FL3717

Table 2 Register Definition

Address	Name	Function	Table	R/W	Default
01h~56h	PWM Register	Set PWM value for LED	3	R/W	0000 0000
A0h	Configuration Register	Configure the operation mode	4	R/W	0001 0000
A1h	Global Current Control Register	Set the global current	5	R/W	0000 0000
A2h	PWM Frequency Register	Set PWM frequency	6	R/W	0000 0001
A4h	Pull Down/Up Level Selection Register	Set the pull down for SWx and pull up for CSy	7	R/W	0011 0011
B0h	Open/short enable register	Enable open/short function with position	8	W	0000 0000
B1h	Open/short register	Store the open/short information	9	R	0000 0000
EFh	Reset Register	Reset the registers value to default	-	W	0000 0000

PWM Register

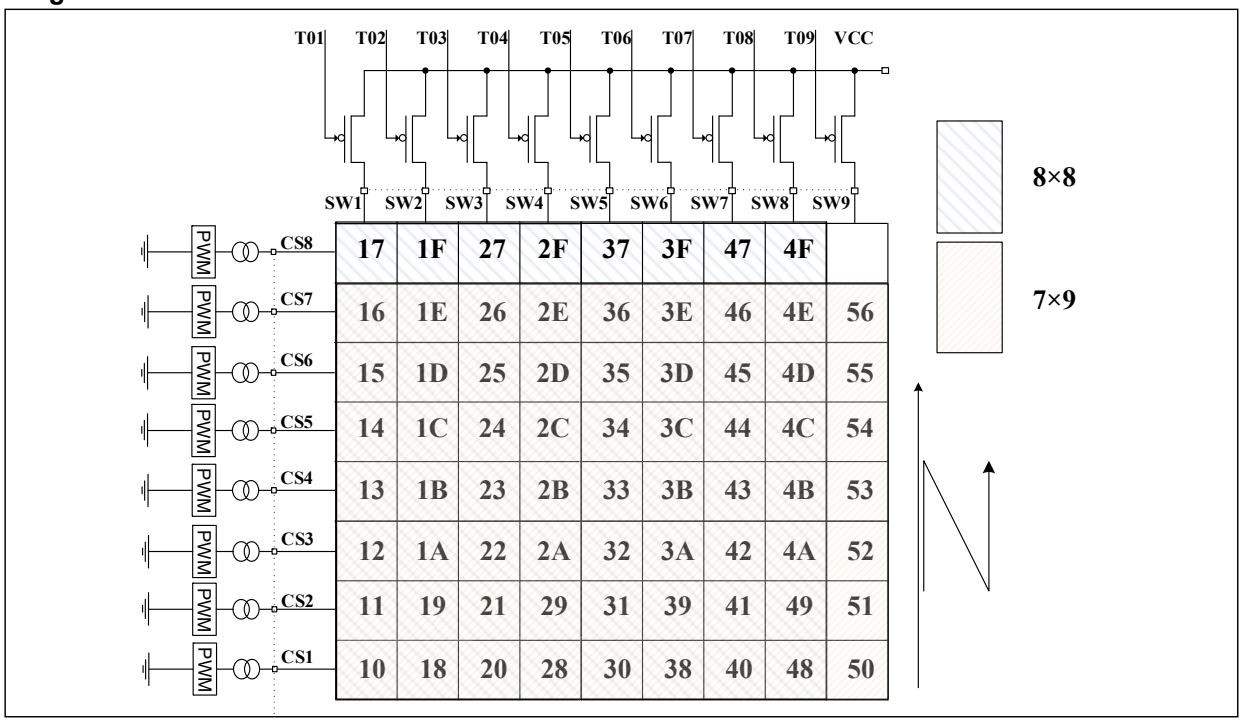


Figure 9 PWM Register

Table 3 10h~56h PWM Register

Bit	D7:D0
Name	PWM
Default	0000 0000

Each LED dot has a byte to modulate the PWM duty in 256 steps. The PWM clock frequency is set by the PWM Frequency Register (A2h). The following calculations assume A2h is configured for 32kHz PWM, A2h= "0x01" for t_{SCAN}= 32μs, the period of scanning and 0.55μs is t_{NOL1}, the non-overlap time and 0.27μs is the CSy delay time.

The value of the PWM Registers decides the average current of each LED noted I_{LED}.

I_{LED} computed by Formula (1):

$$I_{LED} = \frac{PWM}{256} \times I_{OUT(PEAK)} \times Duty \qquad (1)$$

$$PWM = \sum_{n=0}^{7} D[n] \cdot 2^n$$

Where Duty is the duty cycle of SWx, when n=9,

8-bit PWM mode:

$$Duty = \frac{32\mu s}{(32\mu s + 0.55\mu s + 0.27\mu s)} \times \frac{1}{9} = \frac{1}{9.23} \qquad (2)$$

6+2-bit PWM mode:

$$Duty = \frac{4\mu s}{(4\mu s + 0.25\mu s + 0.1\mu s)} \times \frac{1}{9} = \frac{1}{9.7875} \qquad (2)$$

When n=8,

8-bit PWM mode:

$$Duty = \frac{32\mu s}{(32\mu s + 0.55\mu s + 0.27\mu s)} \times \frac{1}{8} = \frac{1}{8.205} \qquad (2)$$

6+2-bit PWM mode:

$$Duty = \frac{4\mu s}{(4\mu s + 0.25\mu s + 0.1\mu s)} \times \frac{1}{8} = \frac{1}{8.7} \qquad (2)$$

I_{OUT} is the output current of CSy (y=1~8),

$$I_{OUT(PEAK)} = \frac{350}{R_{ISET}} \times \frac{GCC}{128} \qquad (3)$$

GCC is the Global Current Control Register (A1h) value, R_{ISET} is the external resistor of ISET pin. D[n] stands for the individual bit value, 1 or 0, in location n.

For example: if D7:D0=1011 0101 (0xB5, 181), GCC= 111 1111, 8-bit PWM mode, n=9, R_{ISET}=10kΩ:

$$I_{LED} = \frac{181}{256} \times \frac{350}{10\,k\Omega} \times \frac{127}{128} \times \frac{1}{9.23}$$

if D7:D0=1001 0100 (0x94, 148), GCC= 111 1111, 6+2-bit PWM mode, n=8, R_{ISET}=10kΩ:

$$I_{LED} = \frac{148}{256} \times \frac{350}{10\,k\Omega} \times \frac{127}{128} \times \frac{1}{8.7}$$

Table 4 A0h Configuration Register

Bit	D7:D4	D3	D2:D1	D0
Name	SWS	PMS	-	SSD
Default	0001	0	00	0

The Configuration Register sets operating mode of IS31FL3719.

When SSD is “0”, IS31FL3717 works in software shutdown mode and for normal operation the SSD bit should set to “1”.

PMS select the PWM mode.

SWS control the duty cycle of the SWx, default mode is 1/8.

When PWM Mode is 6+2 mode, the PWMF bits should be set to “1001” (256kHz, 16MHz OCS).

SSD Software Shutdown Control
0 Software shutdown
1 Normal operation

PMS PWM Mode Select
0 8-bit mode
1 6+2-bit mode

SWS SWx Setting
0000 n=9, SW1~SW9, 9SW×7CS matrix
0001 n=8, SW1~SW8, 8SW×8CS matrix
0010 n=7, SW1~SW7, 7SW×8CS matrix, SW8 no-active
0011 n=6, SW1~SW6, 6SW×8CS matrix, SW7~SW8 no-active
0100 n=5, SW1~SW5, 5SW×8CS matrix, SW6~SW8 no-active
0101 n=4, SW1~SW4, 4SW×8CS matrix, SW5~SW8 no-active
0110 n=3, SW1~SW3, 3SW×8CS matrix, SW4~SW8 no-active
0111 n=2, SW1~SW2, 2SW×8CS matrix, SW3~SW8 no-active
1000 SW1~SW9 with same phase, all on.
Others SW1~SW9, SW1~SW9, 9SW×7CS matrix

Table 5 A1h Global Current Control Register

Bit	D7	D6:D0
Name	-	GCC
Default	0	000 0000

The Global Current Control Register modulates all CSy (y=1~16) DC current which is noted as I_{OUT} in 128 steps, maximum GCC is “111 1111”.

I_{OUT} is computed by the Formula (3):

$$I_{OUT(PEAK)} = \frac{350}{R_{ISET}} \times \frac{GCC}{128}$$

$$GCC = \sum_{n=0}^{6} D[n] \times 2^n$$

Where D[n] stands for the individual bit value 1 or 0, in location n.

Table 6 A2h PWM Frequency

Bit	D7:D4	D3:D0
Name	-	PWMF
Default	0000	0001

Set the PWM frequency, default setting is 32kHz, 8MHz OSC. When PWM Mode is 6+2 mode, the PWMF bits should be set to “1001” (256kHz, 16MHz OCS).

PWMF PWM frequency setting
0001 32kHz
(when n=9, scanning rate is 32/9=3.5kHz)
0010 8kHz (8MHz OCS)
0011 2kHz (8MHz OCS)
0100 1kHz (8MHz OCS)
0101 500Hz (8MHz OCS)
0110 250Hz (8MHz OCS)
0111 125Hz (8MHz OCS)
1001 256kHz (16MHz OCS)
(when n=9, scanning rate is 256/9=28.4kHz)

Table 7 A4h Pull Down/Up Voltage Selection Register

Bit	D7	D6:D4	D3	D2:D0
Name	PHC	CSPUL	DGEN	SWPDL
Default	1	010	0	010

The Pull Down/Up Voltage Selection Register sets phase choice and deghost options of IS31FL3717.

When PHC is “1”, IS31FL3717 enables 180-degree phase delay function.

When DGEN is “1”, IS31FL3717 enables deghost function. The CSPUL sets the CSy pull up voltage level and SWPDL sets the SWx pull down voltage level.

PHC Phase choice
0 0 degree phase delay
1 180 degree phase delay

DGEN De-ghost Enable Control
0 Disable
1 Enable

SWPDL	SWx Pull Down Level Section Bit
000	No pull
001	2.8V
010	2.4V
011	2.0V
100	1.6V
101	1.2V
110	0.8V
111	GND

CSPUL	CSy Pull up Level Selection Bit
000	No pull
001	V_{CC}-2.8V
010	V_{CC}-2.4V
011	V_{CC}-2.0V
100	V_{CC}-1.6V
101	V_{CC}-1.2V
110	V_{CC}-0.8V
111	V_{CC}

If CSPUL sets to “111” (pull to VCC) and SWPDL sets to “111” (pull to GND), there will be large reverse voltage like -5V on LED and may break down the LED.

Table 8 B0h Open Short Enable Register

Bit	D7	D6:D5	D4	D3:D0
Name	-	OSDE	-	SWC
Default	0	00	0	0000

When OSDE set to “01”, open detection will be trigger once, the user could trigger open detection again by set OSDE from “00” to “01”.

When OSDE set “10”, short detection will be trigger once, the user could trigger short detection again by set OSDE from “00” to “10”.

Set the SWC bits to choose one SWx in the LED matrix, and the open/short detect result of the CS8: CS1 on this SWx will be stored in the Open/Short Register (B1h).

OSDE	Open or Short Detect Enable
00	Disable
01/11	Enable open detect
10	Enable short detect

SWC	Choose the SWx
0001	SW1 line
0010	SW2 line
0011	SW3 line
0100	SW4 line
0101	SW5 line
0110	SW6 line
0111	SW7 line
1000	SW8 line
1001	SW9 line

Table 9 B1h Open/Short Register (Read Only)

Bit	D7:D0
Name	CS8:CS1
Default	0000 0000

When OSDE (B0) is set to “01”, open detection will be trigger once, and the open information will be stored at B1h.

When OSDE (B0) is set to “10”, short detection will be trigger once, and the open information will be stored at B1h.

Before set OSDE, the GCC recommend to set to 0x0F

EFh Reset Register

Once the Reset Register is updated with 0xAE, all the IS31FL3717 registers will be reset to their default values. Upon initial power-up, the IS31FL3717 registers will also reset to their default values for a blank display.

APPLICATION INFORMATION

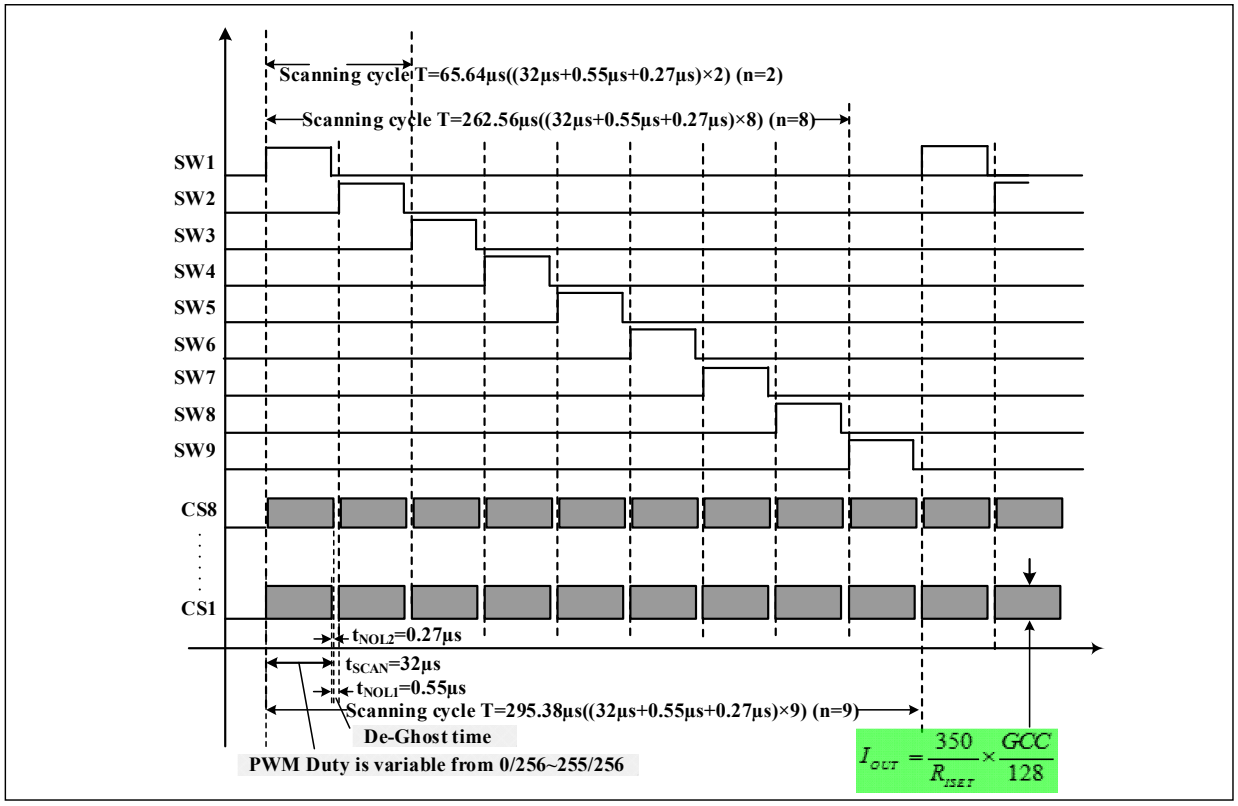


Figure 10 Scanning Timing (8-bit Mode, 32kHz)

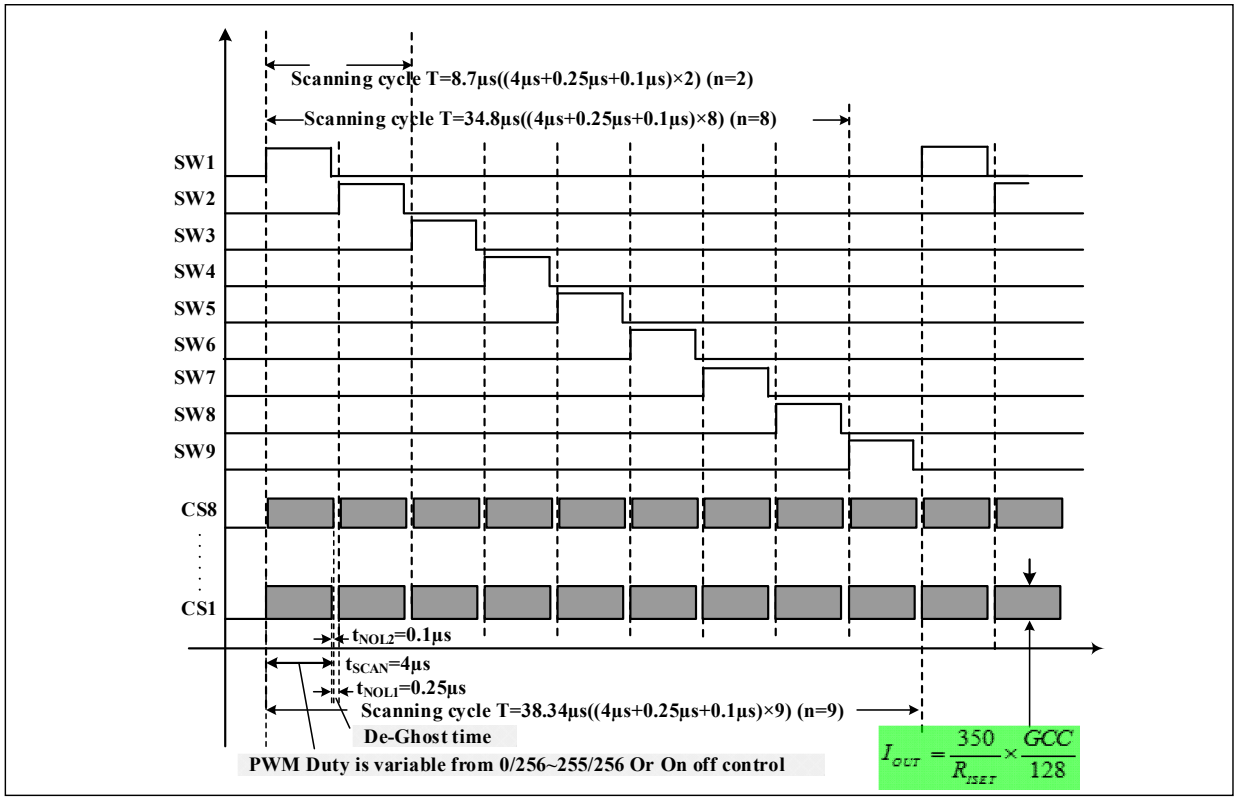


Figure 11 Scanning Timing (6+2-bit Mode, 32kHz)

SCANNING TIMING

As shown in Figure above, the SW1~SW9 is turned on by serial, LED is driven 7 by 9 within the SWx (x=1~9) on time (SWx, x=1~9 is source and it is high when LED on), including the non-overlap blanking time during scan, the duty cycle of SWx (active high, x=1~9) is (n=9):

8bit PWM mode:

$$Duty=\frac{32\mu s}{(32\mu s+0.55\mu s+0.27\mu s)}\times\frac{1}{9}=\frac{1}{9.23} \qquad (2)$$

6+2bit PWM mode:

$$Duty=\frac{4\mu s}{(4\mu s+0.25\mu s+0.1\mu s)}\times\frac{1}{9}=\frac{1}{9.7875} \qquad (2)$$

Or (n=8):

8bit PWM mode:

$$Duty=\frac{32\mu s}{(32\mu s+0.55s+0.27\mu s)}\times\frac{1}{8}=\frac{1}{8.205} \qquad (2)$$

6+2bit PWM mode:

$$Duty=\frac{4\mu s}{(4\mu s+0.25\mu s+0.1\mu s)}\times\frac{1}{8}=\frac{1}{8.7} \qquad (2)$$

Where PMS bit in A0h is "0" (8-bit mode) and PWM Frequency Register A2h= "0x01" (PWM frequency= 32kHz) for t_{SCAN}= 32μs, the period of scanning and 0.55μs is t_{NOL1}, the non-overlap time and 0.27μs is the CSy delay time. Where PMS bit in A0h is "1" (6+2-bit mode) and PWM Frequency Register A2h= "0x05" (PWM frequency= 256kHz) for t_{SCAN}= 4μs, the period of scanning and 0.25μs is t_{NOL1}, the non-overlap time and 0.1μs is the CSy delay time.

POWER ON SEQUENCE

The IS31FL3717 integrates a power-on reset (POR) feature associated with the input supply voltage VCC. The IS31FL3719 will be initialized when VCC exceeds 2.4V (Typ., 2.7V max.) until then all the control circuits and configuration registers will be held in reset while the internal voltage stabilizes (≥2.4V).

The IS31FL3717 enters a hardware shutdown mode when the SDB pin is pulled low. During hardware shutdown the state Function Registers can be accessed but all analog circuits are disabled to conserve power. Once VCC stabilizes > 2.4V, a rising edge of the SDB signal will reset the I2C bus and cause the chip to exit hardware shutdown mode. Since there could be I2C bus transactions prior to the rising edge of the SDB pin, it is recommended to allow 10us prior to and after the rising edge before beginning any I2C bus transaction.

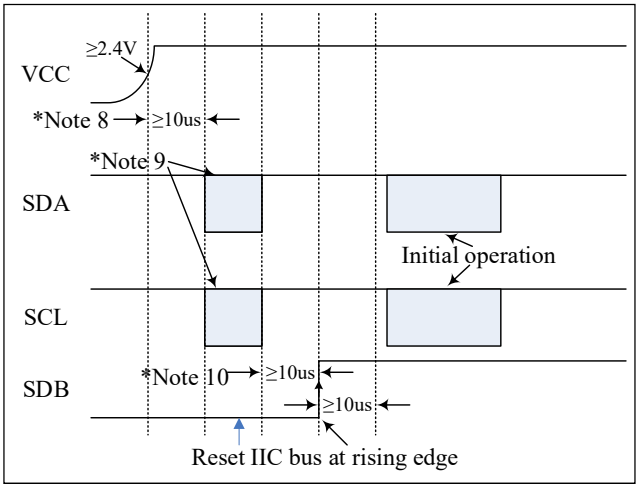


Figure 12 SDB Pin Sequence

Note 8: There should be no I2C operation 10μs before V_{CC} remain ≥2.4V.

Note 9: I2C operation is allowed while SDB is low and V_{CC} ≥2.4V.

Note 10: There should be no I2C operation 10μs before and after SDB rising edge.

PWM CONTROL

After setting the I_{OUT} and GCC, the brightness of each LEDs (LED average current (I_{LED})) can be modulated with 256 steps by PWM Register, as described in Formula (1).

$$I_{LED}=\frac{PWM}{256}\times I_{OUT\ (PEAK\ )}\times Duty \qquad (1)$$

Where PWM is PWM Registers' (10h~56h) data showing in Table 3.

For example, in Figure 1, if R_{ISET}= 10kΩ, PWM= 1011 0101 (0xB5, 181), and GCC= 111 1111, 8-bit PWM mode, then,

$$I_{OUT(PEAK)}=\frac{350}{R_{ISET}}\times\frac{GCC}{128}$$

$$I_{LED}=\frac{181}{256}\times\frac{350}{10k\Omega}\times\frac{127}{128}\times\frac{1}{9.23} \quad (n=9)$$

if D7:D0=1001 0100 (0x94, 148), GCC= 111 1111, 6+2-bit PWM mode, R_{ISET}=10kΩ:

$$I_{LED}=\frac{148}{256}\times\frac{350}{10k\Omega}\times\frac{127}{128}\times\frac{1}{8.7} \quad (n=8)$$

Writing new data continuously to the registers can modulate the brightness of the LEDs to achieve a breathing effect.

GAMMA CORRECTION

In order to perform a better visual LED breathing effect we recommend using a gamma corrected PWM value to set the LED intensity. This results in a reduced number of steps for the LED intensity setting, but causes the change in intensity to appear more linear to the human eye.

Gamma correction, also known as gamma compression or encoding, is used to encode linear luminance to match the non-linear characteristics of display. Since the IS31FL3717 can modulate the brightness of the LEDs with 256 steps, a gamma correction function can be applied when computing each subsequent LED intensity setting such that the changes in brightness matches the human eye's brightness curve.

Table 10 32 Gamma Steps with 256 PWM Steps

C(0)	C(1)	C(2)	C(3)	C(4)	C(5)	C(6)	C(7)
0	1	2	4	6	10	13	18
C(8)	C(9)	C(10)	C(11)	C(12)	C(13)	C(14)	C(15)
22	28	33	39	46	53	61	69
C(16)	C(17)	C(18)	C(19)	C(20)	C(21)	C(22)	C(23)
78	86	96	106	116	126	138	149
C(24)	C(25)	C(26)	C(27)	C(28)	C(29)	C(30)	C(31)
161	173	186	199	212	226	240	255

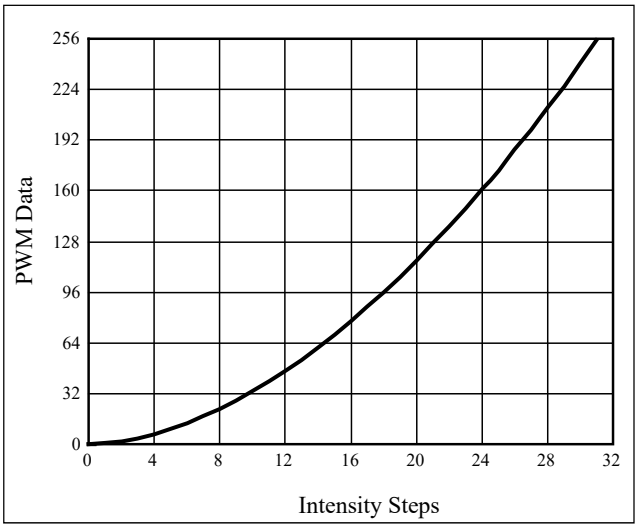


Figure 13 Gamma Correction (32 Steps)

Choosing more gamma steps provides for a more continuous looking breathing effect. This is useful for very long breathing cycles. The recommended configuration is defined by the breath cycle T. When T=1s, choose 32 gamma steps, when T=2s, choose 64 gamma steps. The user must decide the final number of gamma steps not only by the LED itself, but also based on the visual performance of the finished product.

Table 11 64 Gamma Steps with 256 PWM Steps

C(0)	C(1)	C(2)	C(3)	C(4)	C(5)	C(6)	C(7)
0	1	2	3	4	5	6	7
C(8)	C(9)	C(10)	C(11)	C(12)	C(13)	C(14)	C(15)
8	10	12	14	16	18	20	22
C(16)	C(17)	C(18)	C(19)	C(20)	C(21)	C(22)	C(23)
24	26	29	32	35	38	41	44
C(24)	C(25)	C(26)	C(27)	C(28)	C(29)	C(30)	C(31)
47	50	53	57	61	65	69	73
C(32)	C(33)	C(34)	C(35)	C(36)	C(37)	C(38)	C(39)
77	81	85	89	94	99	104	109
C(40)	C(41)	C(42)	C(43)	C(44)	C(45)	C(46)	C(47)
114	119	124	129	134	140	146	152
C(48)	C(49)	C(50)	C(51)	C(52)	C(53)	C(54)	C(55)
158	164	170	176	182	188	195	202
C(56)	C(57)	C(58)	C(59)	C(60)	C(61)	C(62)	C(63)
209	216	223	230	237	244	251	255

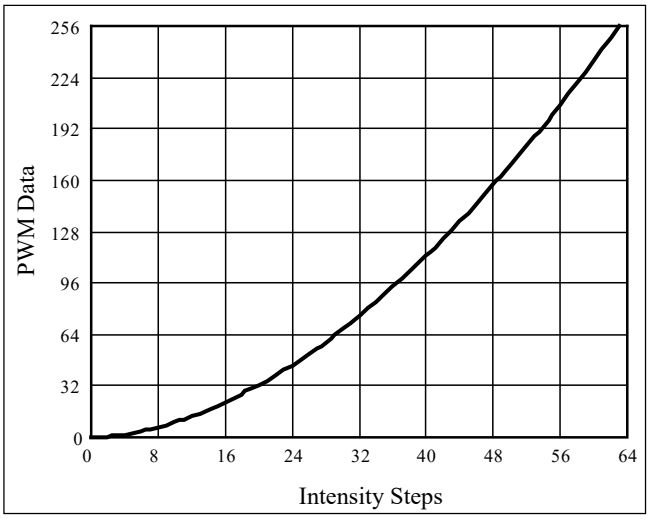


Figure 14 Gamma Correction (64 Steps)

Note: The data of 32 gamma steps is the standard value and the data of 64 gamma steps is the recommended value.

OPERATING MODE

IS31FL3717 can only operate in PWM Mode. The brightness of each LED can be modulated with 256 steps by PWM registers. For example, if the data in PWM Register is “0000 0100”, then the PWM is the fourth step.

Writing new data continuously to the registers can modulate the brightness of the LEDs to achieve a breathing effect.

OPEN/SHORT DETECT FUNCTION

IS31FL3717 has individual LED open and short detection capability.

By setting the SWC bits of the Open Short Enable Register, 8 LEDs in the matrix can be selected for the open and short detection. By setting the OSDE bits of the Open Short Enable Register (B0h) from “00” to “01” or “10”, the LED Open/short Register will begin storing the open/short information. After 2 scan cycles, the MCU can read the open/short information stored in registers B1h. The open/short data will not get refreshed while setting the OSDE bit of the Open Short Enable Register.

There are two configurations which need to be set prior to configuring the the OSDE bits:

1) 0x0F≤A1h≤0x7F adjust LED current
2) A4h=0x00, disable pullup/pulldown resistors

Where A1h is Global Current Control Register and A4h is the Pull Down/Up Resistor Selection Register.

The detect action is one-time event, so each time before reading out the open/short information, the OSDE bit of the Open Short Enable Register (B0h) needs to be set from “0” to “1” (clear before set operation).

DE-GHOST FUNCTION

The “ghost” term is used to describe the behavior of an LED that should be OFF but instead glows dimly when another LED is turned ON. A ghosting effect typically can occur when multiplexing LEDs. In matrix architecture any parasitic capacitance found in the constant-current outputs or the PCB traces to the LEDs may provide sufficient current to dimly light an LED to create a ghosting effect.

To prevent this LED ghost effect, the IS31FL3717 has integrated Pull down resistors for each SWx (x=1~9) and Pull up resistors for each CSy (y=1~8). Select the Pull Down/Up Resistor Selection Register (A4h) which eliminates the ghost LED for a particular matrix layout configuration.

Typically, selecting the 2.4V will be sufficient to eliminate the LED ghost phenomenon.

The SWx Pull down resistors and CSy Pull up resistors are active only when the CSy/SWx output working the OFF state and therefore no power is lost through these resistors.

SHUTDOWN MODE

Shutdown mode can be used as a means of reducing power consumption. During shutdown mode all registers retain their data.

Software Shutdown

By setting SSD bit of the Configuration Register (A0h) to “0”, the IS31FL3717 will operate in software shutdown mode. When the IS31FL3717 is in software shutdown, all current sources are switched off, so that the matrix is blanked. All registers can be operated. Typical current consumption is 0.7μA.

Hardware Shutdown

The chip enters hardware shutdown when the SDB pin is pulled low. When the IS31FL3717 is in hardware shutdown, all current sources are switched off, so that the matrix is blanked. All registers can be operated. Typical current consumption is 0.7μA.

The chip releases hardware shutdown when the SDB pin is pulled high.

If V_{CC} has a risk of dropping below 1.75V but remain above 0.1V while the SDB pin is pulled low, please re-initialize all Function Registers before SDB is pulled high.

LAYOUT

As described previously, depending on the current set resistor (R_{ISET}) value and current register settings, the chip can consumes lots of power. Please consider the below factors during the PCB layout phase.

1. The V_{CC} capacitors need to be close to the VCC pin 23 with their ground pins well connected to the GND of the chip.

2. R_{ISET} should be close to the chip and the ground side should well connect to the GND of the chip.

3. The CSy pins will have a maximum current of 35mA (R_{ISET}=10kΩ). However, the SWx pins maximum current is larger since it is the combined current of the CSy pins. Therefore, the width of the SWx trace needs to be much wider than the CSy trace.

CLASSIFICATION REFLOW PROFILES

Profile Feature	Pb-Free Assembly
Preheat & Soak Temperature min (Tsmin) Temperature max (Tsmax) Time (Tsmin to Tsmax) (ts)	150°C 200°C 60-120 seconds
Average ramp-up rate (Tsmax to Tp)	3°C/second max.
Liquidous temperature (TL) Time at liquidous (tL)	217°C 60-150 seconds
Peak package body temperature (Tp)*	Max 260°C
Time (tp)** within 5°C of the specified classification temperature (Tc)	Max 30 seconds
Average ramp-down rate (Tp to Tsmax)	6°C/second max.
Time 25°C to peak temperature	8 minutes max.

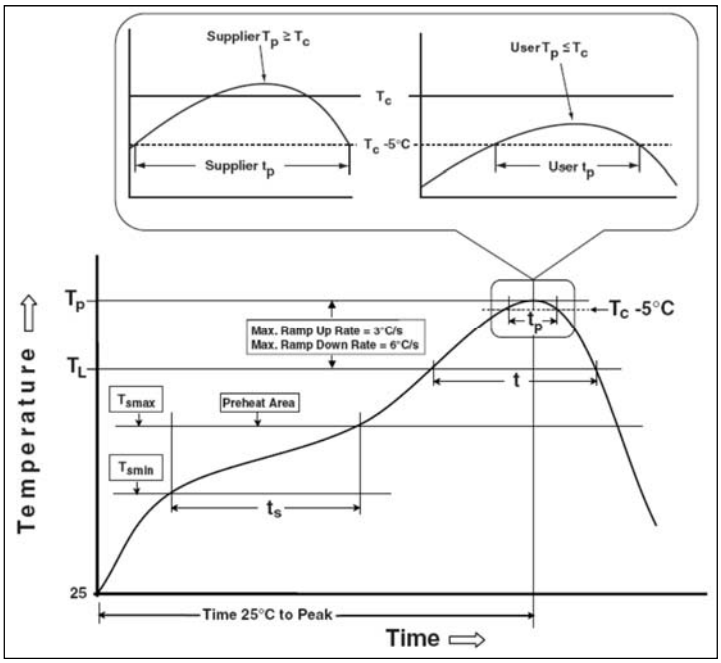
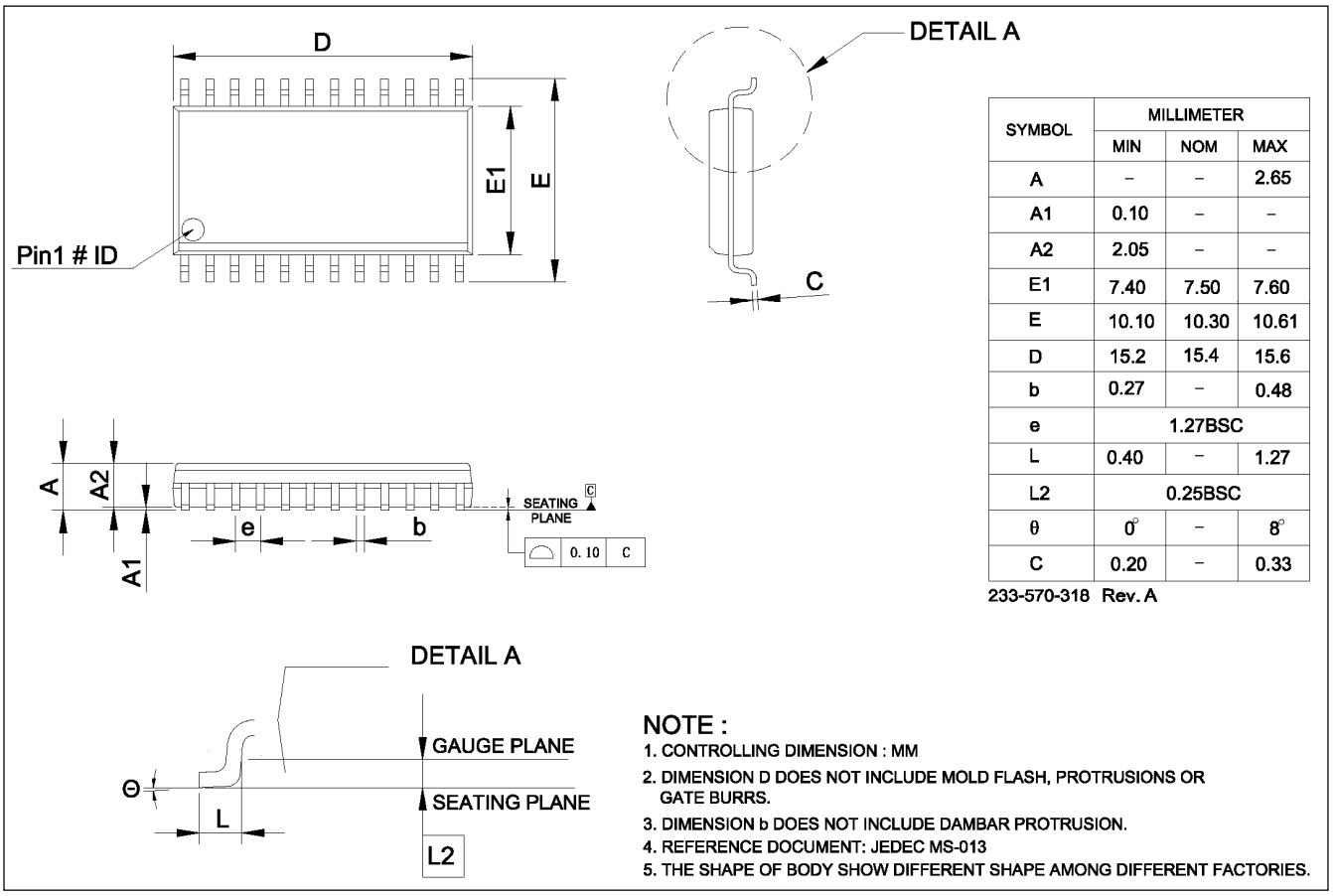


Figure 15 Classification Profile

PACKAGE INFORMATION

SOP-24



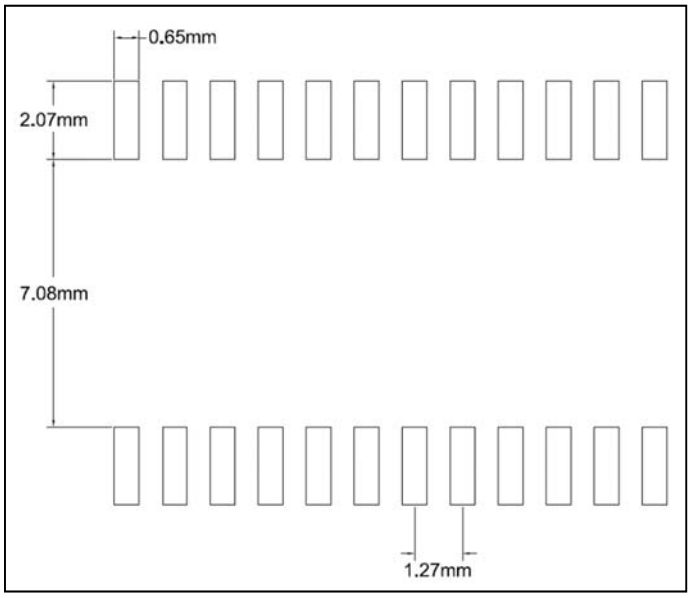
SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	–	–	2.65
A1	0.10	–	–
A2	2.05	–	–
E1	7.40	7.50	7.60
E	10.10	10.30	10.61
D	15.2	15.4	15.6
b	0.27	–	0.48
e	1.27BSC		
L	0.40	–	1.27
L2	0.25BSC		
θ	0°	–	8°
C	0.20	–	0.33

233-570-318 Rev. A

NOTE :
1. CONTROLLING DIMENSION : MM
2. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION.
4. REFERENCE DOCUMENT: JEDEC MS-013
5. THE SHAPE OF BODY SHOW DIFFERENT SHAPE AMONG DIFFERENT FACTORIES.

RECOMMENDED LAND PATTERN

SOP-24



Note:

1. Land pattern complies to IPC-7351.
2. All dimensions in MM.
3. This document (including dimensions, notes & specs) is a recommendation based on typical circuit board manufacturing parameters. Since land pattern design depends on many factors unknown (eg. User's board manufacturing specs), user must determine suitability for use.

REVISION HISTORY

Revision	Detail Information	Date
A	Release to mass product	2022.03.22
B	Update the EC table	2022.05.09