IS31LT3361

INTEGRATED NMOS SWITCH 40V/1.3A LED DRIVER WITH FAULT PROTECTION

May 2021

GENERAL DESCRIPTION

The IS31LT3361 is a continuous mode inductive step-down converter, designed for driving a single LED or multiple series connected LEDs efficiently from a voltage source higher than the LED voltage. The chip operates from an input supply between 6V and 40V and provides an externally adjustable output current of up to 1.3A.

The IS31LT3361 includes an integrated low-side output NMOS switch and a high-side output current sensing circuit, which uses an external resistor to set the nominal average output current.

Output current can be adjusted linearly by applying an external control signal to the ADJ pin. The ADJ pin will accept either a DC voltage or a PWM waveform. This will provide either a continuous or a gated output current. Applying a voltage less than 0.6V to the ADJ pin turns the output off and switches the chip into a low current standby state.

IS31LT3361 also features robust protections to ensure reliable operation.

The chip is assembled in a thermally enhanced SOT89-5 package and operates over the temperature range of -40°C to +125°C.

FEATURES

- Wide input voltage range: 6V~40V
- Integrated 40V NMOS switch
- Up to 1.3A output current
- High efficiency (up to 98%)
- Simple low parts count
- ±5% output current accuracy over -40°C to +125°C temperature
- Single pin on/off and brightness control using DC voltage or PWM
- Up to 2000: 1 dimming ratio at 100Hz PWM
- Up to 1MHz switching frequency
- Robust fault protections
  - ✓ Inherent LED string open/short protection
  - ✓ Integrated NMOS over current protection
  - ✓ Diode open/short protection
  - ✓ Thermal shutdown protection

APPLICATIONS

- Avionic lighting
- Fog lights
- Daytime running lights
- Combination tail lights
- Courtesy lights
- Other LED lighting

TYPICAL APPLICATION CIRCUIT

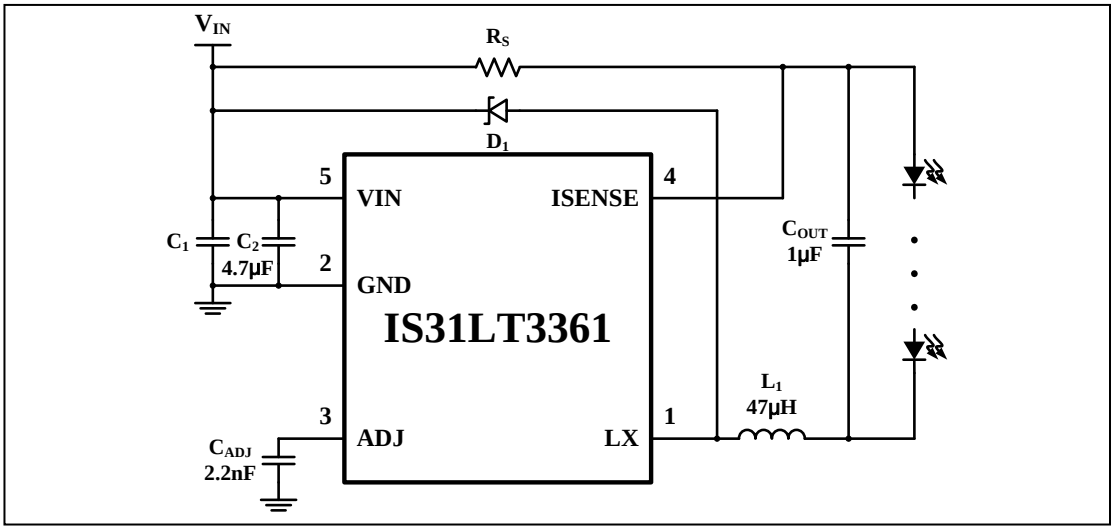
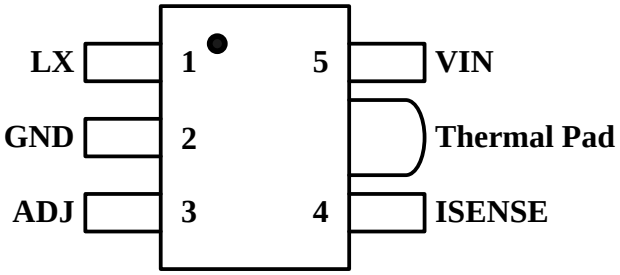


Figure 1 Typical Application Circuit

Note 1: The capacitor, C_2, can't be removed. And it MUST be placed as close as possible to the VIN and GND pins, otherwise the operation might be abnormal.

Note 2: R_S must be placed as close as possible to VIN and ISENSE pins to avoid noise interference.

PIN CONFIGURATION

Package	Pin Configuration
SOT89-5	

PIN DESCRIPTION

No.	Pin	Description
1	LX	Drain of NMOS switch.
2	GND	Ground pin.
3	ADJ	Multi-function On/Off and brightness control pin: * Leave floating for normal operation. (V_{ADJ}= V_{REF}= 2.5V giving nominal average output current I_{OUT_NOM} = 0.1V/R_S) * Drive to below 0.6V to turn off output current. Keep low for over t_{SD} to enter low current standby mode * Drive with DC voltage (0.81V <V_{ADJ} <2.5V) to adjust output current from 6% to 100% of I_{OUT_NOM} * When driving the ADJ pin above 2.5V, the current will be clamped to 100% brightness automatically. * Drive with PWM signal (low level < 0.6V and high level >2.5V) to adjust output current.
4	ISENSE	Connect resistor R_S from this pin to V_{IN} to define nominal average output current I_{OUT_NOM}= 0.1V/R_S
5	VIN	Input voltage (6V ~ 40V). Decouple to ground with ≥ 4.7μF X7R ceramic capacitor as close to device as possible.
	Thermal Pad	Must be connected to GND.

ORDERING INFORMATION
Industrial Range: -40°C to +125°C

Order Part No.	Package	QTY/Reel
IS31LT3361-SDLS4-TR	SOT89-5, Lead-free	2500

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a.) the risk of injury or damage has been minimized;
b.) the user assume all such risks; and
c.) potential liability of Lumissil Microsystems is adequately protected under the circumstances

ABSOLUTE MAXIMUM RATINGS (NOTE 3)

VIN, LX pins	-0.3V ~ +45V
ISENSE pin	V_{IN}-5V ~ V_{IN}+0.3V, V_{IN}≥5V
	-0.3V ~ V_{IN}+0.3V, V_{IN}<5V
ADJ pin	-0.3V ~ +6.0V
Maximum output current, I_{LX}	1.5A
Recommended maximum operating frequency	1MHz
Power dissipation, $P_{D(MAX)}$ (Note 4)	1.77W
Operating temperature, $T_A = T_J$	-40°C ~ +150°C
Storage temperature, T_{STG}	-65°C ~ +150°C
Junction temperature, T_{JMAX}	150°C
Package thermal resistance, junction to ambient (4 layer standard test PCB based on JESD 51-2A), θ_{JA}	56.5°C/W
Package thermal resistance, junction to thermal PAD (4 layer standard test PCB based on JESD 51-8), θ_{JP}	4.18°C/W
ESD (HBM) ESD (CDM)	±4kV ±750V

Note 3: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 4: Detail information please refer to package thermal de-rating curve on Page 15.

ELECTRICAL CHARACTERISTICS

Valid are at V_{IN}= 12V, T_A= T_J= 25°C, unless otherwise noted.
Limits apply over the junction temperature (T_J) range of -40°C to +125°C, unless otherwise stated. Minimum and maximum limits are specified through test, design or statistical correlation (Note 5).

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{IN}	Input voltage		6		40	V
V_{IN_UVLO}	VIN under voltage locked out threshold	V_{IN} rising	5.0	5.25	5.5	V
$V_{IN_UVLO_HY}$	Hysteresis of V_{IN_UVLO}			200		mV
I_{SD}	Shutdown current	ADJ pin grounded for >20ms		15	25	μA
I_{INQ_ON}	Quiescent supply current with output not switching	ADJ and LX pins floating		1.5	2	mA
V_{SENSE}	Mean current sense threshold voltage		95	100	105	mV
$V_{SENSEHYS}$	Sense threshold hysteresis			±15		%
I_{ISENSE}	ISENSE pin input current	V_{ISENSE} =V_{IN}-0.1V	16	20	24	μA
V_{REF}	Internal reference voltage	Measured on ADJ pin with pin floating		2.5		V
V_{ADJ_RG}	External control voltage range on ADJ pin for DC brightness control		0.81		2.5	V
V_{ADJ_OFF}	Threshold voltage on ADJ pin to switch chip from active (on) state to quiescent (off) state	V_{ADJ} falling	0.6	0.65		V
V_{ADJ_ON}	Threshold voltage on ADJ pin to switch chip from quiescent (off) state to active (on) state	V_{ADJ} rising		0.7	0.8	V

ELECTRICAL CHARACTERISTICS (CONTINUED)

Valid are at V_{IN} =12V, T_A=T_J= 25°C, unless otherwise noted.

Limits apply over the junction temperature (T_J) range of -40°C to +125°C, unless otherwise stated. Minimum and maximum limits are specified through test, design or statistical correlation. (Note 5).

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
t_{PWM}	Delay time between PWM rising edge to 10% of I_{OUT} during PWM dimming	f_{PWM}>100Hz			1.5	µs
t_{SD}	The low voltage persist time on ADJ pin to shutdown IC	V_{ADJ}<0.6V	14	17	20	ms
R_{ADJ}	Internal pullup resistor between ADJ pin and V_{REF} (2.5V)		480	580	680	kΩ
I_{LX_LEAK}	LX switch leakage current				1	µA
I_{LX_MEAN}	Continuous LX switch current	(Note 6)			1.3	A
I_{LX_LIMIT}	LX switch current limit		2.1	2.5	2.9	A
t_{SKIP}	Current limit reset time	(Note 6)	26	30	34	ms
R_{LX}	LX switch “ON” resistance			0.25	0.40	Ω
V_{OD_TH}	Open diode detection threshold	Test on LX pin	41	43	46	V
t_{ON_MIN}	Minimum switch “ON” time	LX switch “ON” (Note 6)		110	150	ns
t_{OFF_MIN}	Minimum switch “OFF” time	LX switch “OFF” (Note 6)		110	150	ns
t_{PD}	Internal comparator propagation delay	(Note 6)		50		ns
T_{SD}	Thermal shutdown temperature	(Note 6)		165		°C
T_{SD_HYS}	Thermal shutdown hysteresis	(Note 6)		15		°C

Note 5: Limits are 100% production tested at 25ºC. Limits over the operating temperature range verified through either bench and/or tester testing and correlation using Statistical methods.

Note 6: Guaranteed by design.

TYPICAL PERFORMANCE CHARACTERISTICS

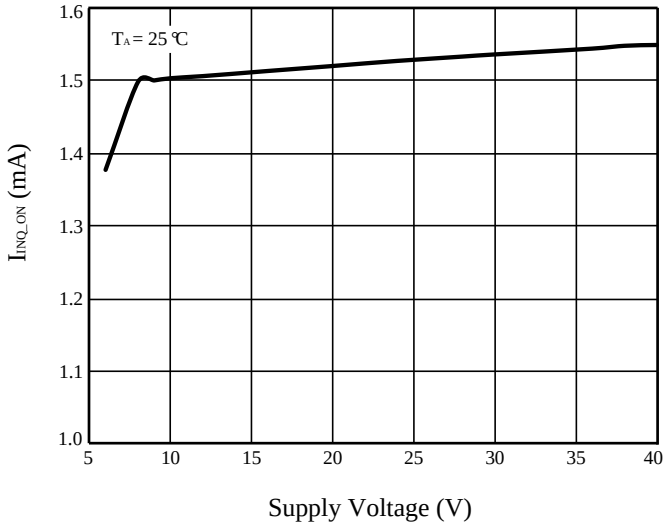


Figure 2 I_{INQ_ON} vs. Supply Voltage

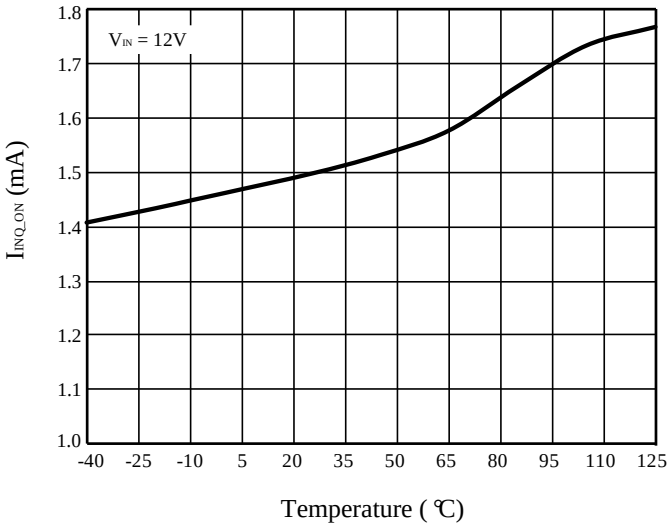


Figure 3 I_{INQ_ON} vs. Temperature

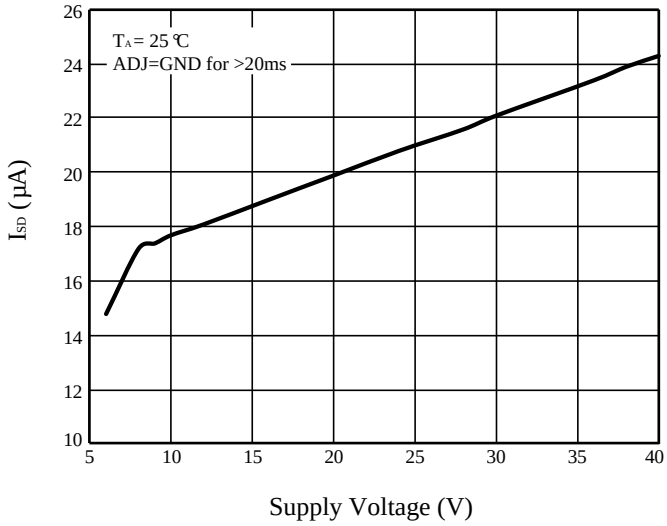


Figure 4 I_{SD} vs. Supply Voltage

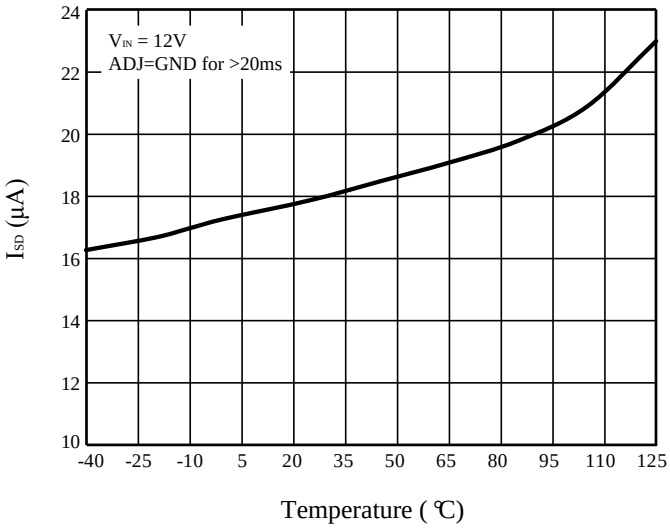


Figure 5 I_{SD} vs. Temperature

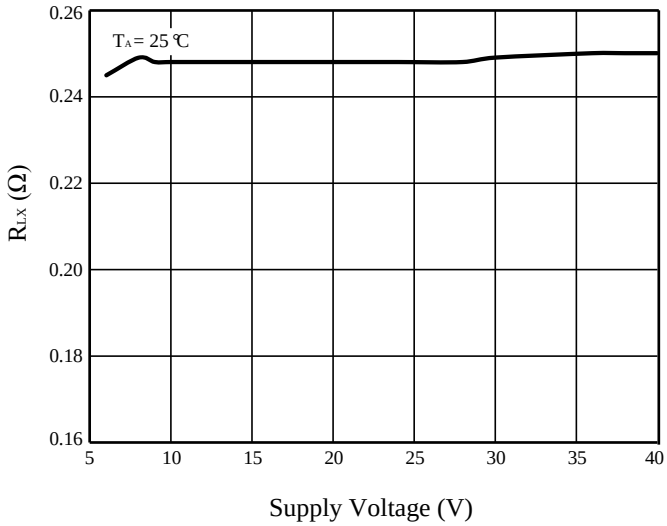


Figure 6 R_{LX} vs. Supply Voltage

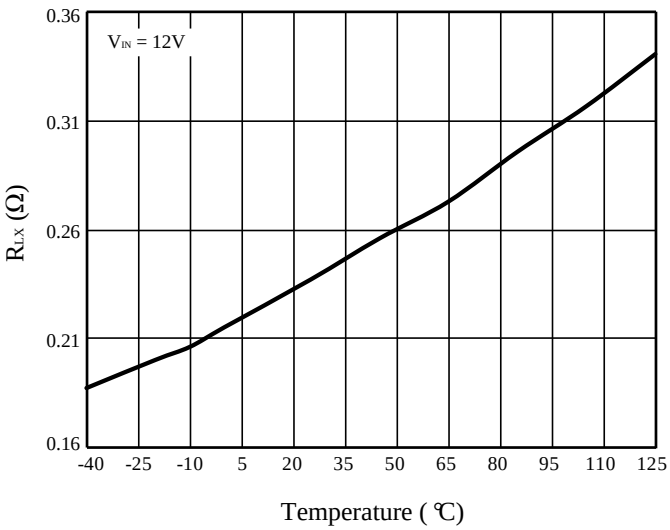


Figure 7 R_{LX} vs. Temperature

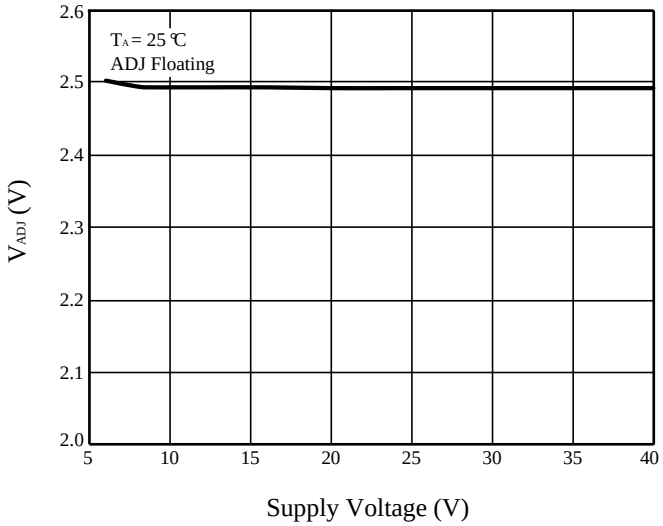


Figure 8 V_{ADJ} vs. Supply Voltage

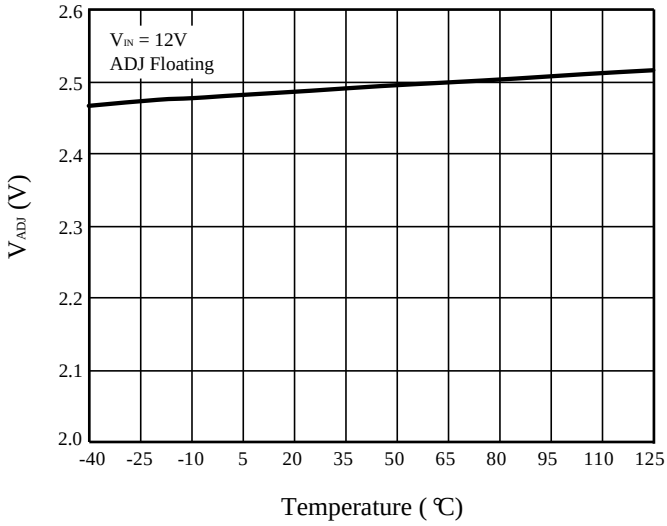


Figure 9 V_{ADJ} vs. Temperature

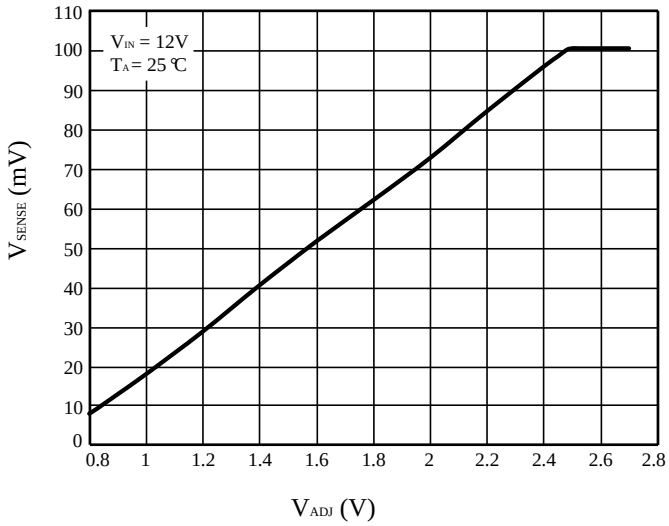


Figure 10 V_{SENSE} vs. V_{ADJ}

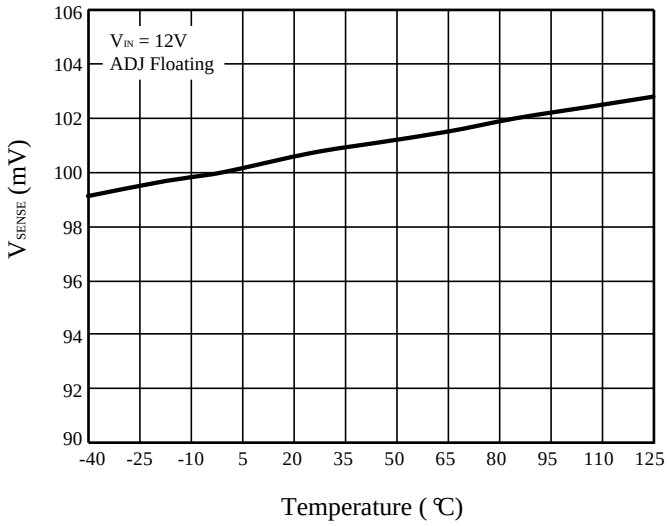


Figure 11 V_{SENSE} vs. Temperature

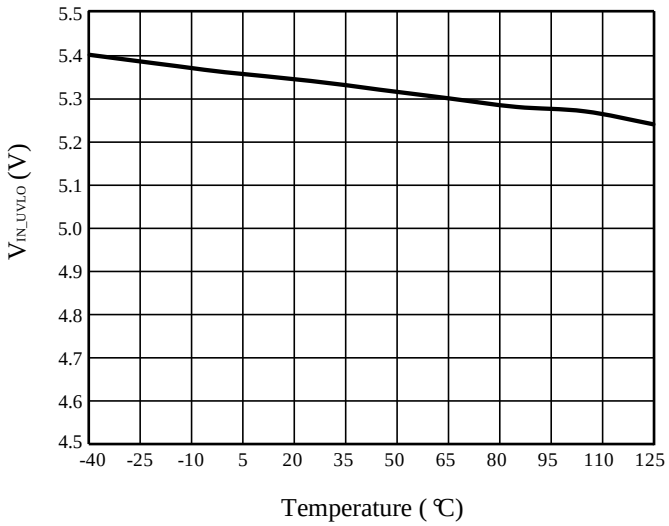


Figure 12 V_{IN_UVLO} vs. Temperature

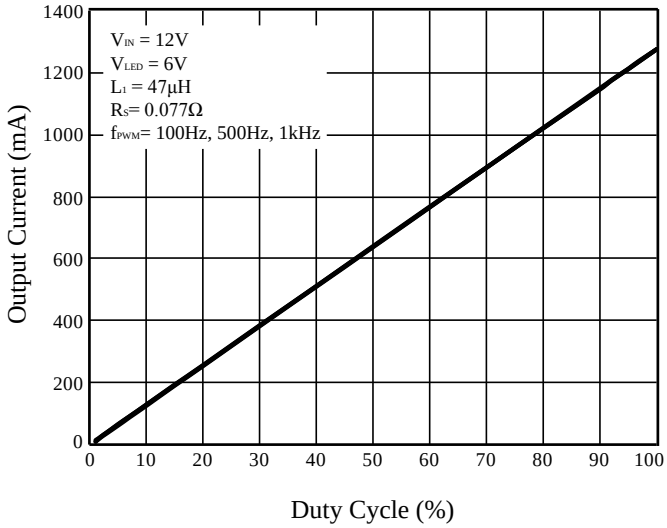


Figure 13 PWM Dimming

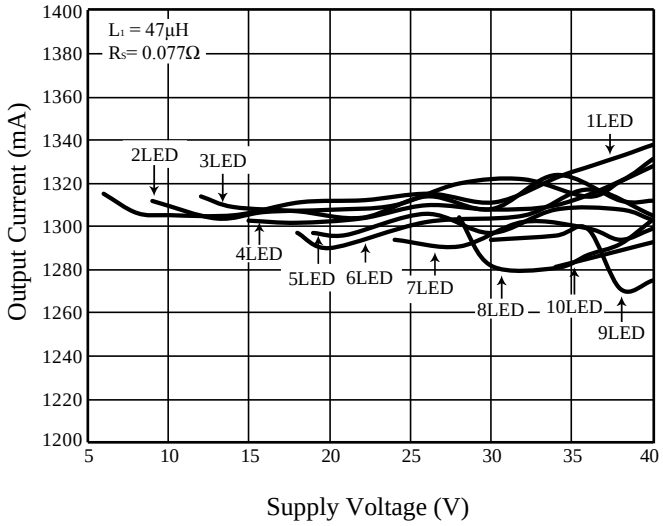


Figure 14 Output Current vs. Supply Voltage

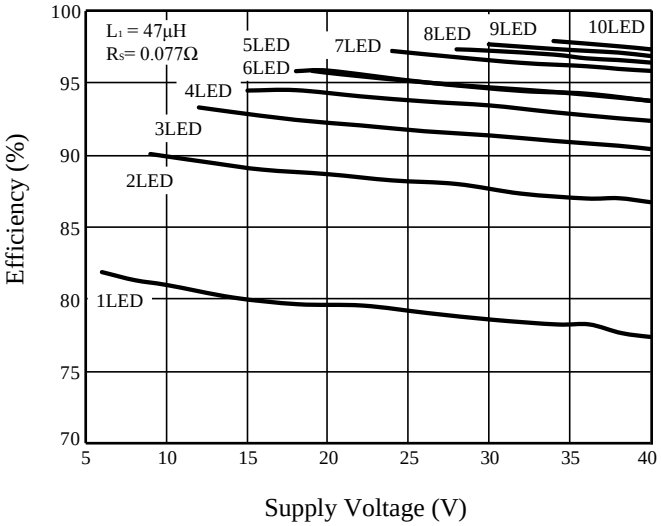


Figure 15 Efficiency vs. Supply Voltage

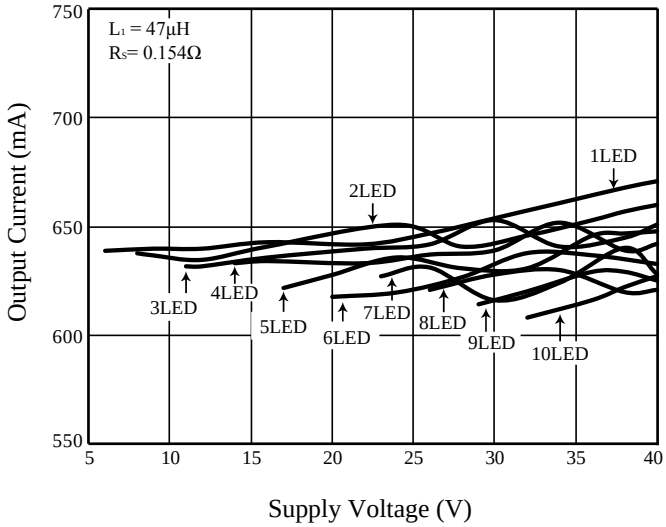


Figure 16 Output Current vs. Supply Voltage

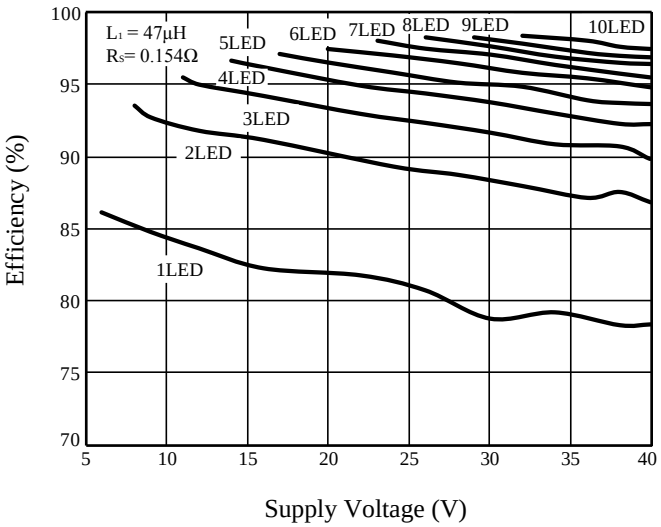


Figure 17 Efficiency vs. Supply Voltage

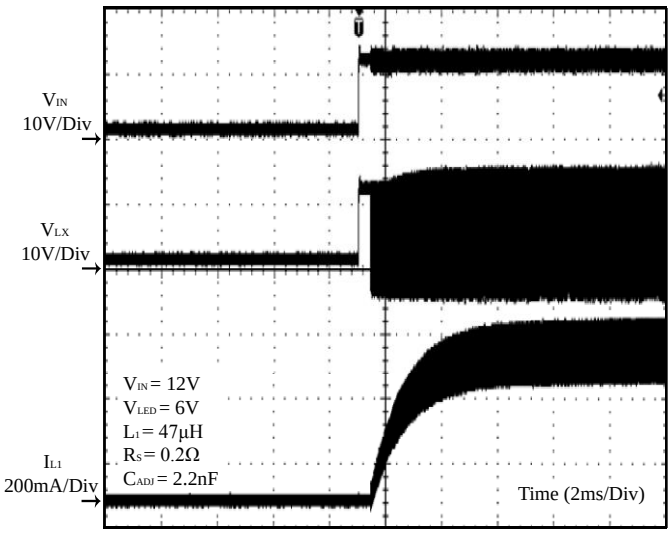


Figure 18 Power Up

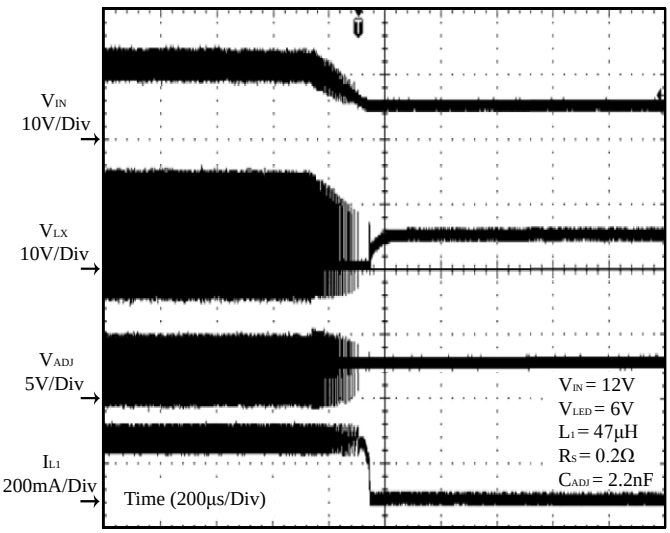


Figure 19 Power Down

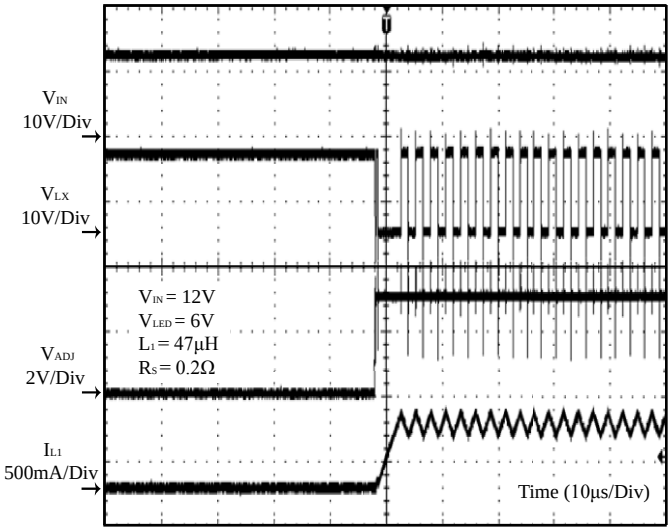


Figure 20 PWM On

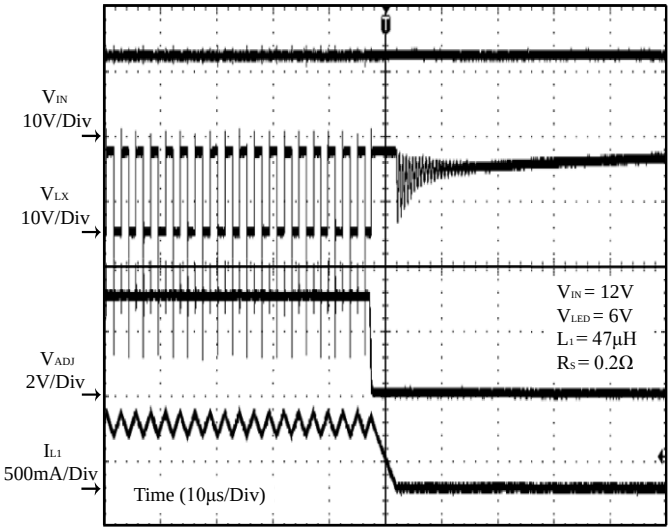


Figure 21 PWM Off

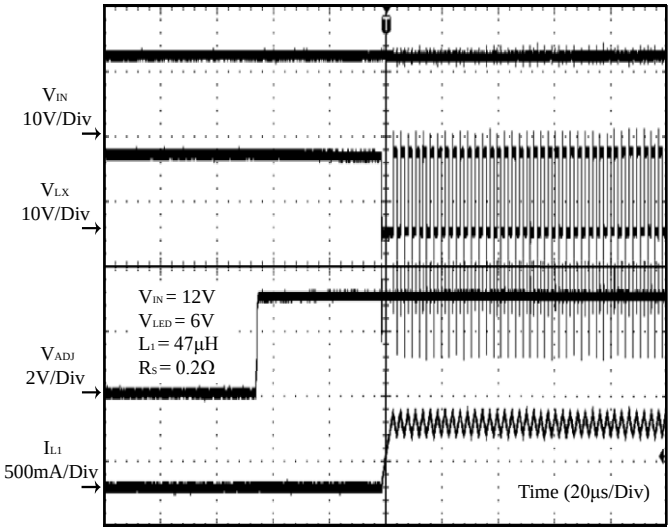


Figure 22 Enabling from Shutdown Mode

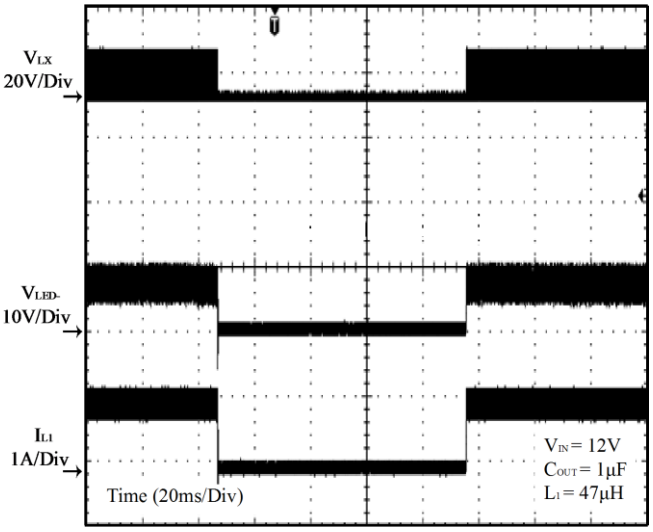


Figure 23 LED Open and Recovery

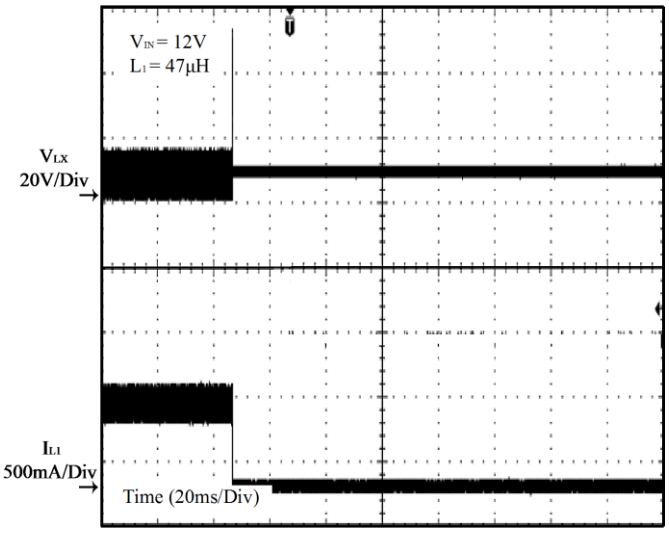


Figure 24 Diode Open

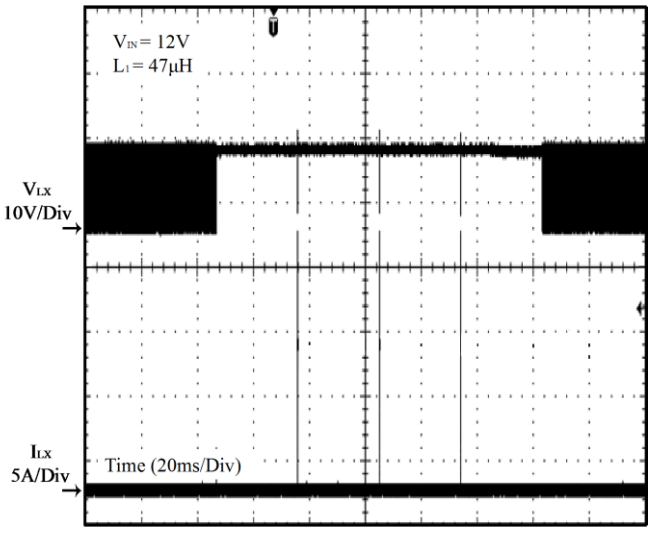
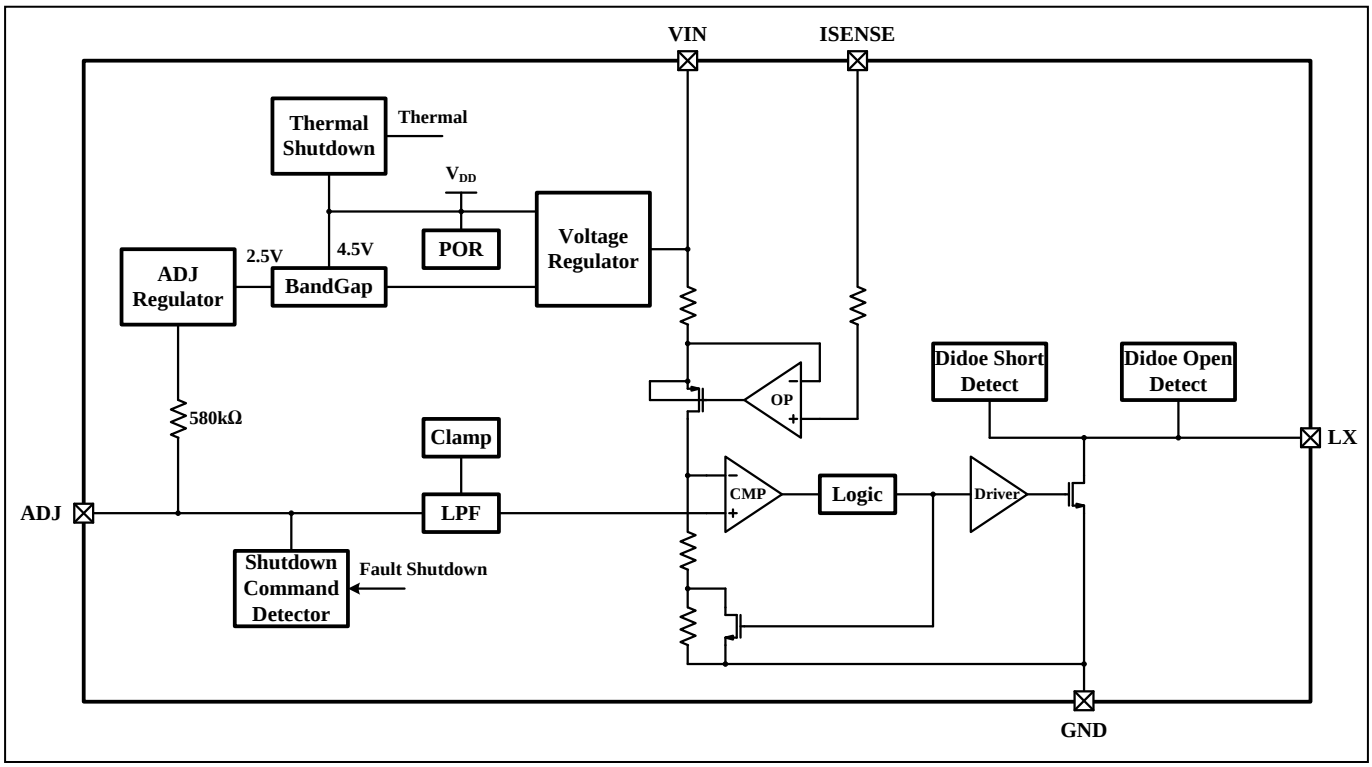


Figure 25 Diode Short and Recovery

FUNCTIONAL BLOCK DIAGRAM



APPLICATION INFORMATION

The IS31LT3361 is a current hysteresis control LED buck driver with integrated NMOS switch. When power is applied, the integrated NMOS switch is turned on and the current starts to flow through the sense resistor R_S, the LED string, the inductor L_1 and internal NMOS switch to ground. The current ramps up linearly and its ramp up rate is determined by the supply voltage, LED string voltage and inductor L_1 value. The device monitors the voltage across the sense resistor R_S, which is produced by R_S x I_{OUT}. Once the voltage reaches the internal upper threshold (about +15% over V_{SENSE}), the integrated NMOS switch is turned off and the current in the inductor L_1 continues to flow through the Schottky diode D_1, sense resistor R_S, LED string and back into the inductor. The current linearly ramps down and its ramp down rate is determined by the Schottky diode D_1 forward voltage, the LED string voltage and inductor L_1 value. When the voltage reaches the internal lower threshold (about -15% below V_{SENSE}), the integrated NMOS switch is turned on again. Therefore the on/off of the NMOS switch maintains an average current in the LED string set by sense resistor R_S.

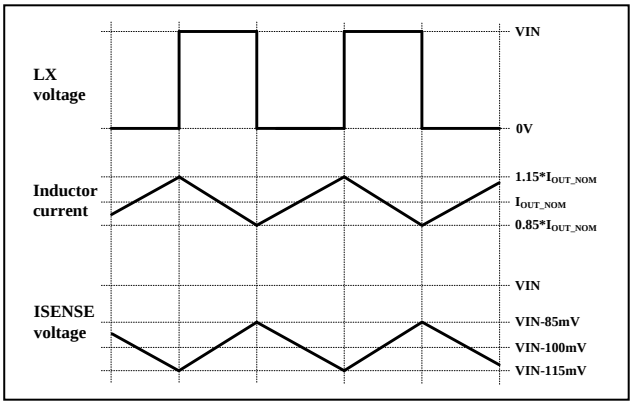


Figure 26 Operation Waveforms

UNDER VOLTAGE LOCKOUT (UVLO)

The device features an under voltage lockout (UVLO) function on VIN pin. This is a fixed value which cannot be adjusted. The device is enabled when the VIN voltage rises to exceed V_{IN_UVLO} (Typ. 5.25V), and disabled when the VIN voltage falls below (V_{IN_VLO} – $V_{IN_UVLO_HY}$) (Typ. 5.05V).

OUTPUT CURRENT SETTING

The nominal average output current in the LED(s) is determined by the value of the external current sense resistor (R_S) connected between VIN and ISENSE pins and is given by Equation (1):

$$I_{OUT_NOM} = \frac{0.1V}{R_S} \qquad (1)$$

Note that R_S=0.077Ω is the minimum allowed value for the sense resistor to maintain a switch current below the specified maximum value of 1.3A.

Table 1 gives values of nominal average output current for several values of current setting resistor (R_S) in the typical application circuit Figure 1:

Table 1 Output Current Setting

R_S (Ω)	Nominal Average Output Current (mA)
0.077	1300
0.15	667
0.3	333

The above values assume that the ADJ pin is floating and at a nominal voltage of V_{REF} = 2.5V.

R_S needs to be a 1% accuracy resistor with enough power tolerance and good temperature characteristic to ensure a stable output current. On PCB layout, this resistor MUST be placed as close to VIN and ISENSE pins as possible to avoid the EMI noise interference.

ENABLE AND PWM DIMMING

A high logic signal (>2.5V) on the ADJ pin will enable the IC. The buck converter ramps up the LED current to a target level which is set by current sense resistor, R_S.

When the ADJ pin goes from high to low (<0.6V), the buck converter will turn off, but the IC remains in standby mode for up to t_{SD}. When the ADJ pin goes high within this period, the LED current will turn on immediately. A Pulse-Width Modulated (PWM) signal with duty cycle D_{PWM} can be applied to the ADJ pin, as shown in Figure 27, to adjust the output current to a value below the nominal average value set by resistor R_S, the signal range is from 0V~5V. The logic "HIGH" must be higher than 2.5V, the logic "LOW" must be lower than 0.6V. The PWM signal must have the driving ability to drive the internal pull-up resistor R_{ADJ} (580kΩ Typ.). A practical range for PWM dimming frequency is between 100Hz and 20kHz.

There is an inherent PWM turn on delay time t_{PWM} (1.5μs max.) during continuous PWM dimming. A high frequency PWM signal has a shorter period time that will degrade the PWM dimming linearity. Therefore, a low frequency PWM signal is good for achieving better dimming contrast ratio. At a 200Hz PWM frequency, the dimming duty cycle can be varied from 100% down to 1% or lower.

If the ADJ pin is kept low for over t_{SD}, the IC enters shutdown mode to reduce power consumption. The next high signal on ADJ will initialize a full startup sequence, which takes about 50μs (Typ.). This startup sequence does not exist in a typical 100Hz to

20kHz PWM operation.

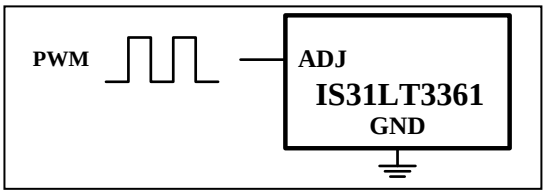


Figure 27 PWM Dimming Control Via ADJ Pin

ANALOG DIMMING

The ADJ pin can be driven by an external DC voltage within the range of 0.81V ~ 2.5V, as shown in Figure 28, to adjust the output current to a value below the nominal average value defined by R_S.

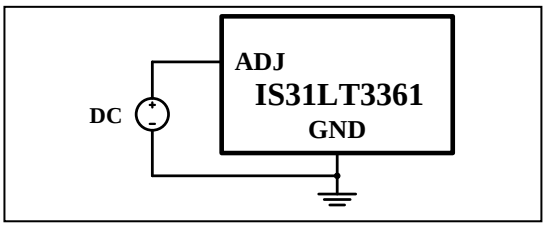


Figure 28 Dimming by External DC Voltage

The nominal average output current in this case is given by Equation (2):

$$I_{OUT_DC} = \frac{0.1V}{R_S} \times \frac{V_{ADJ} - 0.7V}{1.8V} \qquad (2)$$

For 0.81V< V_{ADJ} < 2.5V.

Note that 100% brightness setting corresponds to V_{ADJ} = V_{REF} =2.5V. When driving the ADJ pin above 2.5V, the current will be clamped to 100% brightness automatically.

The input pullup impedance of the ADJ pin is 580kΩ (Typ.).

SOFT START

To optimize the dimming accuracy at high frequency PWM, IS31LT3361 doesn't have a built-in soft start function. However, connecting an external capacitor C_{ADJ} from the ADJ pin to ground can provide a soft start delay. When power up, the internal reference voltage V_{REF} charges C_{ADJ} through the pull-up resistor R_{ADJ}. C_{ADJ} increases the V_{ADJ} rising time of reaching the turn-on threshold and 100% brightness to provide the soft start function. The larger the capacitor value the longer the soft start time. The soft start time can be roughly calculated using the following Equation:

$$t_{SS} = 1.5 \times 10^6 \times C_{ADJ} \qquad (3)$$

A 2.2nF ceramic capacitor can create about 3.3ms soft start time.

CAPACITOR SELECTION

A low ESR capacitor should be used for input decoupling, as the ESR of this capacitor appears in series with the supply source impedance and lowers overall efficiency. This capacitor needs to supply the relatively high peak current to the inductor and smooth out the resulting feedback current ripple on the input supply.

The capacitor value is selected based on the acceptable ripple at the source, and is calculated by Equation (4):

$$C_{MIN} = \frac{I_{OUT_NOM} \times t_{ON}}{\Delta U_{MAX}} \qquad (4)$$

I_{OUT_NOM} is the value of output current，ΔU_{MAX} is the acceptable ripple of power supply. T_{ON} is the "ON" time of LX.

The selected value must be higher than the calculated minimum value. Typically, a ≥10μF capacitor is recommended. Besides that, a 4.7μF X7R ceramic capacitor MUST be added and placed as close to VIN and GND pins as possible to decouple the high frequency ground bounce, otherwise the operation might be abnormal.

INDUCTOR SELECTION

The IS31LT3361 is a current hysteresis buck controller, which has a fixed inductor current ripple. For a given current, the higher inductor value results in a lower operating frequency. Selecting the inductor value involves trade-offs in performance. A larger inductance reduces operating frequency, and it also introduces unwanted parasitic resistance that lowers the efficiency. A smaller inductor value has a compact size and a lower cost, but introduces a higher operating frequency which results in more AC switching loss on the internal NMOS switch. The recommended inductor values are in the range of 47μH to 220μH.

Higher inductor values are recommended for high supply voltages and low output current in order to minimize errors due to switching delays, which results in increased ripple and lower efficiency. Higher value inductance also results in a smaller change in output current over the supply voltage range. The inductor should be mounted as close to the chip as possible with low resistance connections to the LX and VIN pins.

The chosen inductor should have a saturation current higher than the peak output current and a continuous current rating above the required mean output current. It is recommended to use inductors with a saturation current greater than 2.2A for a 1.3A output current or a saturation current greater than 1.2A for a 750mA output current.

The inductor value should be chosen to maintain an operating frequency (recommended Max. 1Mhz) with operating duty cycle and switch "on/off" times within the specified limits over the supply voltage and load

current range.

The following equations can be used as a guide.

LX Switch "ON" time:

$$t_{ON} = \frac{L \times \Delta I}{V_{IN} - V_{LED} - I_{AVG}(R_S + R_L + R_{LX})} \quad (5)$$

Note: t_{ON_MIN} > 150ns.

LX Switch "OFF" time:

$$t_{OFF} = \frac{L \times \Delta I}{V_{LED} + V_D + I_{AVG}(R_L + R_S)} \quad (6)$$

Note: t_{OFF_MIN} > 150ns.

Where:

L is the inductor inductance (H)

R_L is the inductor resistance (Ω)

I_{AVG} is the required LED current (A)

ΔI is the inductor peak-peak ripple current (A) [Internally set to 0.3 × I_{AVG}]

V_{IN} is the supply voltage (V)

V_{LED} is the total LED forward voltage (V)

R_{LX} is the NMOS switch resistance (Ω)

V_D is the diode forward voltage at the required load current (V)

Example:

For V_{IN}=12V, L=47μH, R_L=0.26Ω, V_{LED}=3.4V, I_{AVG} =333mA, V_D =0.36V, R_S = 0.3Ω, R_{LX}=0.25Ω:

$$t_{ON} = \frac{47 \times 0.3 \times 0.333}{12 - 3.4 - 0.333 \times (0.3 + 0.26 + 0.25)} \approx 0.564\mu s$$

$$t_{OFF} = \frac{47 \times 0.3 \times 0.333}{3.4 + 0.36 + 0.333 \times (0.26 + 0.3)} \approx 1.19\mu s$$

This gives an operating frequency of 570kHz and a duty cycle of 32%.

Optimum performance will be achieved by setting the duty cycle close to 50% at the nominal supply voltage. This helps to equalize the undershoot and overshoot and improves temperature stability of the output current.

DIODE SELECTION

For maximum efficiency and performance, the rectifier (D_1) should be a fast and low capacitance Schottky diode with low reverse leakage at the maximum operating voltage and temperature.

If alternative diodes are used, it is important to select diodes with a peak current rating above the peak inductor current and a continuous current rating higher than the maximum output load current. It is very important to consider the reverse leakage of the diode when operating at high temperature. Excess leakage will increase the power dissipation in the device.

The higher forward voltage and overshoot due to reverse recovery time in silicon diodes will increase the peak voltage on the LX output. If a silicon diode is used, care should be taken to ensure that the total voltage appearing on the LX pin including supply ripple, does not exceed the specified maximum value.

REDUCING LED CURRENT RIPPLE

In a buck architecture, the output current is identical with the inductor current. For the IS31LT3361, the output current ripple is fixed at about ±15%. Connecting an output capacitor in parallel with LED string will further reduce the current ripple in the LED string. A value of 1μF will reduce nominal ripple current by a factor of three (approx.). Proportionally lower ripple can be achieved with higher capacitor values. Note that the capacitor will not affect operating frequency or efficiency, but it will increase start-up delay, by reducing the rate of rise of LED voltage.

INHERENT LED STRING OPEN PROTECTION

The LED string open detection is enabled after the VIN voltage rises above the internally fixed threshold, V_{FT_UVLO}, which is to prevent insufficient VIN voltage falsely triggering an open detection. If the connection to the LED(s) is open, the loop current flow is cut off, the voltage cross the sense resistor R_S will never reach the internal upper threshold, preventing switching operation (the NMOS switch stays in the ON state). This prevents damage to the IS31LT3361, unlike in many boost converters, where the back EMF may damage the internal switch by forcing the drain above its breakdown voltage. Once the open fault condition is removed, the device will recover to normal operation.

INHERENT LED SHORT PROTECTION

If the LED string is shorted by a low impedance wire, the system will continue operation with the set current but at a very low duty cycle, however it will not cause any damage to system.

DIODE SHORT PROTECTION

Should the Schottky diode be shorted by a low impedance wire, the power supply is directly connected to the drain of the integrated NMOS switch and will be shorted to ground when the NMOS switch turns on. That triggers the NMOS switch current limit protection and the integrated NMOS switch will immediately turn off. The device enters a hiccup mode of t_{SKIP} cycle time until the fault condition is removed.

DIODE OPEN PROTECTION

In the event the Schottky diode fails open and once the integrated NMOS switch turns off, the voltage on LX pin will increase due to the back EMF of the inductor. When the LX pin voltage exceeds the open diode detection threshold, V_{OD_TH}, the IS31LT3361 latches at the off state (stop switching). The back EMF is discharged by the breakdown of the integrated NMOS switch, which is overstressed and may cause permanent damage to the device. Therefore the protection is not auto recoverable but needs a power cycle. Note that even though the diode open protection is able to latch the switching off, the back EMF still might cause permanent damage to the NMOS switch. To avoid an open diode condition, it is recommended that the soldering reliability of the Schottky diode must be ensured during the mass-production.

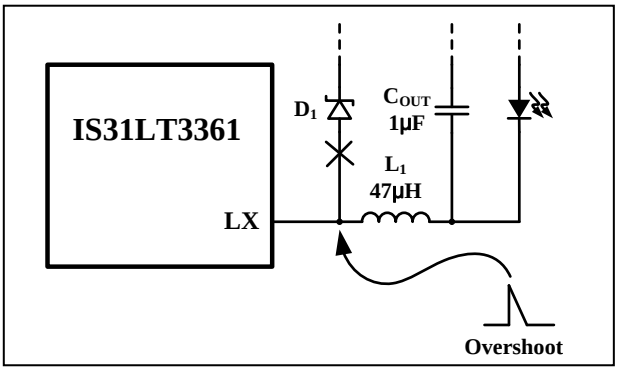


Figure 29 Schottky Diode Open

THERMAL SHUTDOWN PROTECTION

To protect the device from damage due to high power dissipation, the junction temperature is monitored. If the junction temperature exceeds the thermal shutdown temperature of 165°C (Typ.) then the device will shut down immediately, and the output current is shut off. After a thermal shutdown event, the IS31LT3361 will not try to restart until its temperature has reduced to less than 150°C (Typ.).

Table 2 Fault Conditions

Fault Type	Detection Condition	Driver Action	Fault Recovering
Diode Short	NMOS switch current exceeds I_{LX_LIMIT}	NMOS switch turns off immediately and retrys after every t_{SKIP} cycle time	NMOS switch current drops below I_{LX_LIMIT}
Diode Open	LX pin voltage exceeds V_{OD_TH} for 1 switching cycles time	Latch at off state immediately	Power cycle
Thermal Shutdown	The junction temperature exceeds 165°C	NMOS switch turns off immediately	The junction temperature falls below 150°C.

THERMAL CONSIDERATIONS

The package thermal resistance, θ_{JA}, determines the amount of heat that can pass from the silicon die to the surrounding ambient environment. The θ_{JA} is a measure of the temperature rise created by power dissipation and is usually measured in degree Celsius per watt (°C/W).

When operating the chip at high ambient temperatures, or when driving maximum load current, care must be taken to avoid exceeding the package power dissipation limits. The maximum power dissipation can be calculated using the following Equation:

$$P_{D(MAX)} = \frac{T_{J(MAX)} - T_A}{\theta_{JA}} \qquad (7)$$

So, $$P_{D(MAX)} = \frac{125°C - 25°C}{56.5°C/W} \approx 1.77W$$

Figure 30, shows the power derating of the IS31LT3361 on a JEDEC boards (in accordance with JESD 51-5 and JESD 51-7) standing in still air.

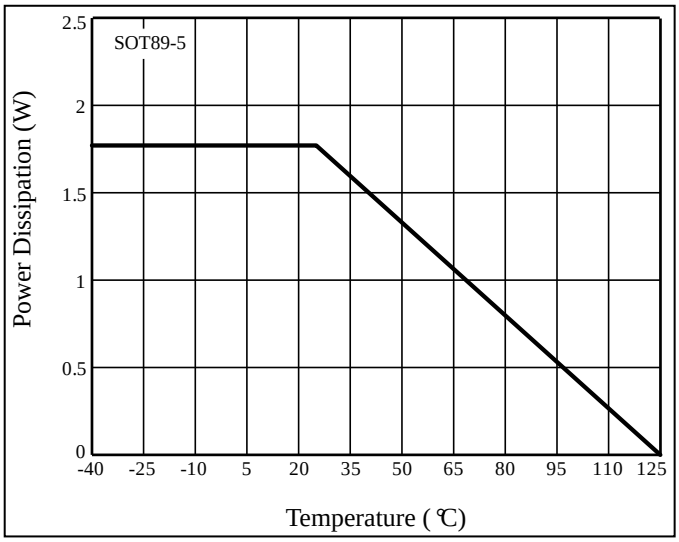


Figure 30 Dissipation Curve

The thermal resistance is achieved by mounting the IS31LT3361 on a standard FR4 double-sided printed circuit board (PCB) with a copper area of a few square inches on each side of the board under the IS31LT3361. Multiple thermal vias, as shown in Figure 31, help to conduct the heat from the exposed pad of the IS31LT3361 to the copper on each side of the board. The thermal resistance can be reduced by using a metal substrate or by adding a heatsink.

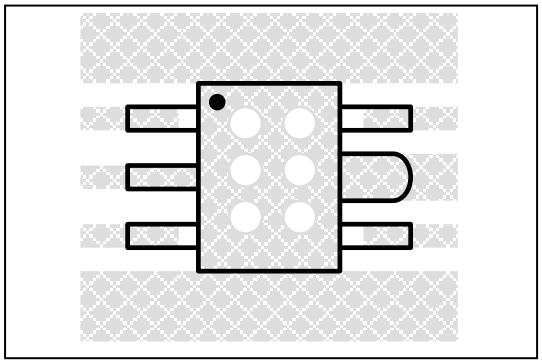


Figure 31 Board Via Layout For Thermal Dissipation

LAYOUT CONSIDERATIONS

As for all switching power supplies, especially those providing high current and using high switching frequencies, layout is an important design step. If layout is not carefully handled, the operation could show instability as well as EMI problems.

The high dV/dt surface and dI/dt loops are a big noise emission source. To optimize the EMI performance, maintain a compact PCB layout for all high switching frequency points with a high voltage. Meantime, keep all traces carrying high current as short as possible to minimize the loops.

VIN Pin

The capacitor C_1 and C_2 should be placed as close as possible to VIN and GND pins for good filtering. Especially the C_2 (4.7μF), it must be right next to the IS31LT3361 to prevent ground bounce, otherwise the device operation may be abnormal.

R_S Resistor

To avoid ground jitter, the current monitoring resistor, R_S, should be placed close to the device with short trace length to the device pins. To prevent noise coupling, the R_S traces should either be far away or be isolated from high-current paths and high-speed switching nodes. These practices are essential for improved accuracy and stability.

LX Pin

Keep the traces of the switching points short. The inductor L_1, LX and free wheeling Schottky diode D_1 should be placed as close to each other as possible and the traces of connection between them kept as short and wide as possible.

ADJ Pin

The ADJ pin is a high impedance input, so when left floating, PCB traces to this pin should be as short as possible to reduce noise pickup. A small nanofarad capacitor is recommended for soft start and noise decoupling.

Thermal Pad

The thermal pad under the IS31LT3361 package must be soldered to a sufficient size of copper ground plane with sufficient vias to conduct the heat to opposite side PCB for adequate cooling.

CLASSIFICATION REFLOW PROFILES

Profile Feature	Pb-Free Assembly
Preheat & Soak Temperature min (Tsmin) Temperature max (Tsmax) Time (Tsmin to Tsmax) (ts)	150°C 200°C 60-120 seconds
Average ramp-up rate (Tsmax to Tp)	3°C/second max.
Liquidous temperature (TL) Time at liquidous (tL)	217°C 60-150 seconds
Peak package body temperature (Tp)*	Max 260°C
Time (tp)** within 5°C of the specified classification temperature (Tc)	Max 30 seconds
Average ramp-down rate (Tp to Tsmax)	6°C/second max.
Time 25°C to peak temperature	8 minutes max.

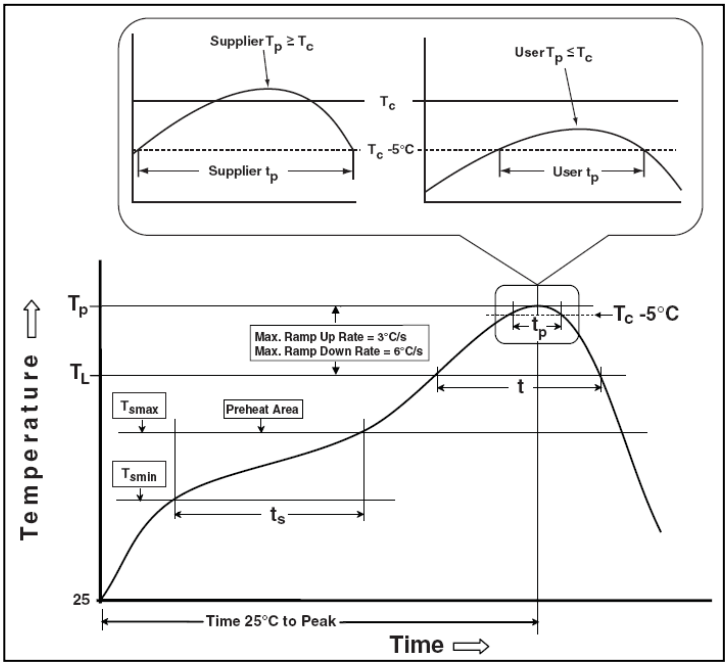
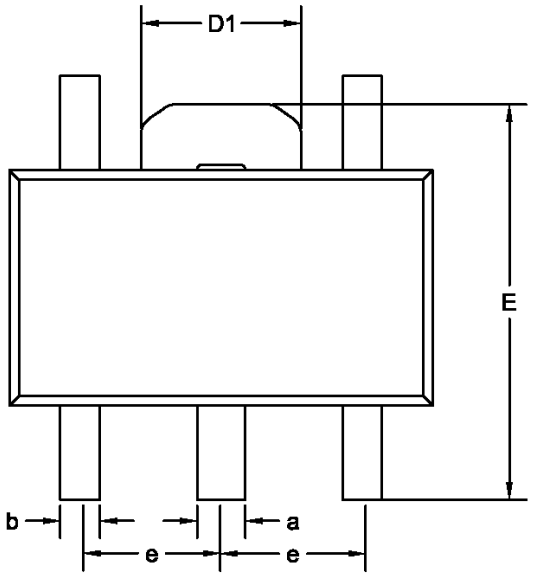


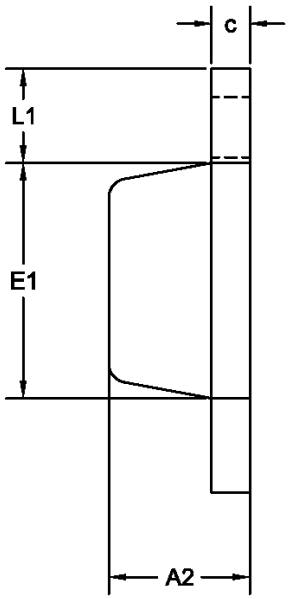
Figure 32 Classification Profile

PACKAGE INFORMATION

SOT89-5

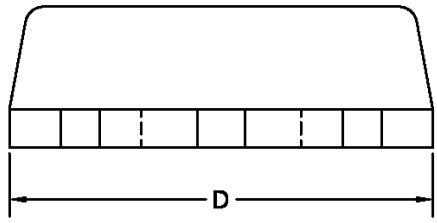


Top View



Side View

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A2	1.40	—	1.60
D	4.30	—	4.70
D1	1.55	—	1.83
E	3.94	—	4.40
E1	2.13	—	2.70
a	0.38	—	0.58
e	1.50BSC		
b	0.32	—	0.52
L1	0.80	—	1.20
c	0.35	—	0.44



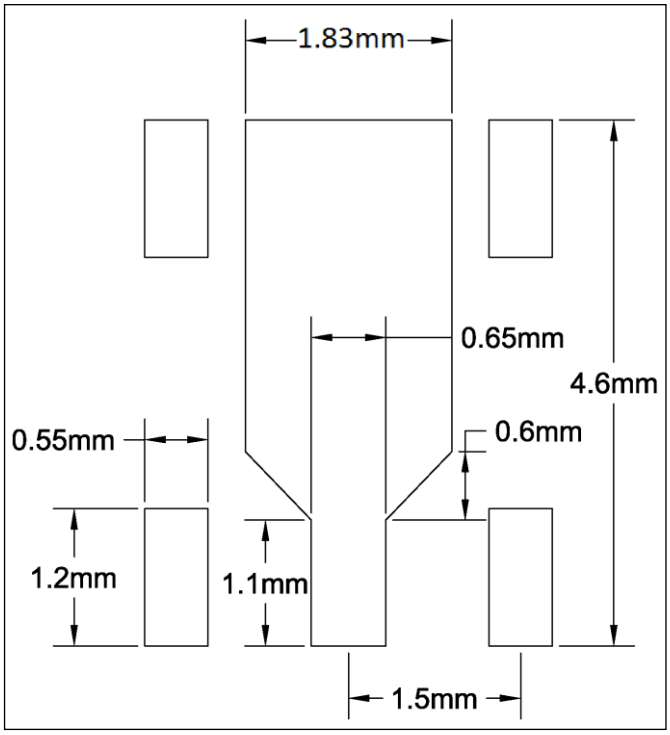
End View

NOTE :

1. CONTROLLING DIMENSION : MM
2. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
3. DIMENSION a,b DOES NOT INCLUDE DAMBAR PROTRUSION.
4. REFERENCE DOCUMENT: JEDEC TO-243C
5. THE SHAPE THERAMAL PAD SHOW DIFFERENT SHAPE AMONG DIFFERENT FACTORIES.

RECOMMENDED LAND PATTERN

SOT89-5



Note:

1. Land pattern complies to IPC-7351.
2. All dimensions in MM.
3. This document (including dimensions, notes & specs) is a recommendation based on typical circuit board manufacturing parameters. Since land pattern design depends on many factors unknown (eg. User's board manufacturing specs), user must determine suitability for use.

REVISION HISTORY

Revision	Detail Information	Date
0A	Initial release	2021.01.18
A	Update to final version	2021.05.11