IS32LT3128A

TRIPLE CHANNEL LINEAR LED DRIVER WITH FADE ON/OFF AND PWM DIMMING

February 2022

GENERAL DESCRIPTION

The IS32LT3128A is a programmable triple channel linear current regulator; two channels of up to 150mA each for LED lighting and a single channel of up to 30mA for illuminating switches. The device operates as a fully configurable theatrical dimming LED driver; no microcontroller is required. External resistors will program the current levels as well as the LED fade ON/OFF ramp rate. Additional configuration such as PWM source (internal or external), polarity (positive or negative) and switch type (momentary contact or latched) are selectable via the MODE1/2 pins.

An integrated debounce and latch circuit on the channel enable pin (EN1/2) is enabled when the device is configured for a momentary contact switch interface. The other option is to configure the EN pins to accept a static level signal for operation with latched switches. A VCC level PWM dimming signal can be connected to the PWM input pin to directly drive both LED channels. If configured for Internal-PWM-Dimming mode, the integrated PWM source will be triggered by a PWM pin voltage level. This enables LED dimming without the need for an external PWM input. The PWM input have a higher priority and will override the EN inputs. See Figure 60~66 for the details.

The device integrates a 63 step fade ON/OFF algorithm (Gamma correction) which causes the output LED brightness to gradually ramp up to the full source value after the EN1/2 or PWM (when configured for Internal-PWM-Dimming mode) pins are triggered. The same controller causes the LED brightness to gradually ramp down to zero if the EN1/2 or PWM (when configured for Internal-PWM-Dimming mode) pins are triggered while the output channel is ON. The fade ramp can be interrupted mid-cycle before completion of the ramp cycle.

The IS32LT3128A is targeted at the automotive market with end applications to include map and dome lighting as well as exterior accent lighting. For 12V automotive applications the low dropout driver can support 1 to 3 LEDs per channel. It is offered in a small thermally enhanced eTSSOP-20 package.

FEATURES

- Operating voltage range, 5V to 42V
- Dual channel current sources
  - Individual programmable current via a single external resistor
  - Configurable from 20mA to 150mA
- Single channel 30mA (Max.) current source for switch illumination
- EN input supports either momentary contact or latched switch
  - Input is debounced and latched
  - Lower priority than PWM input
  - Gamma corrected Fade ON/OFF algorithm
  - Pull down resistors set independent fade ON and OFF ramp time
- Selectable external or internal PWM source
  - External PWM directly drives the current source
  - Internal 220Hz PWM source with Gamma corrected algorithm for automatic dimming the current source
  - Support both positive and negative polarity PWM
- Fault Protection:
  - Fault Reporting
    - ✓ LED strings short
    - ✓ Over temperature thermal shutdown
  - ISET pin shorted to GND
  - Over temperature current roll off
- AEC-Q100 Qualified
- Operating temperature range from -40°C ~ +125°C

APPLICATIONS

- Automotive Interior:
  - Map/Dome light
  - Puddle lamp in doors
  - Glove box light
  - Vanity mirror light

TYPICAL APPLICATION CIRCUIT

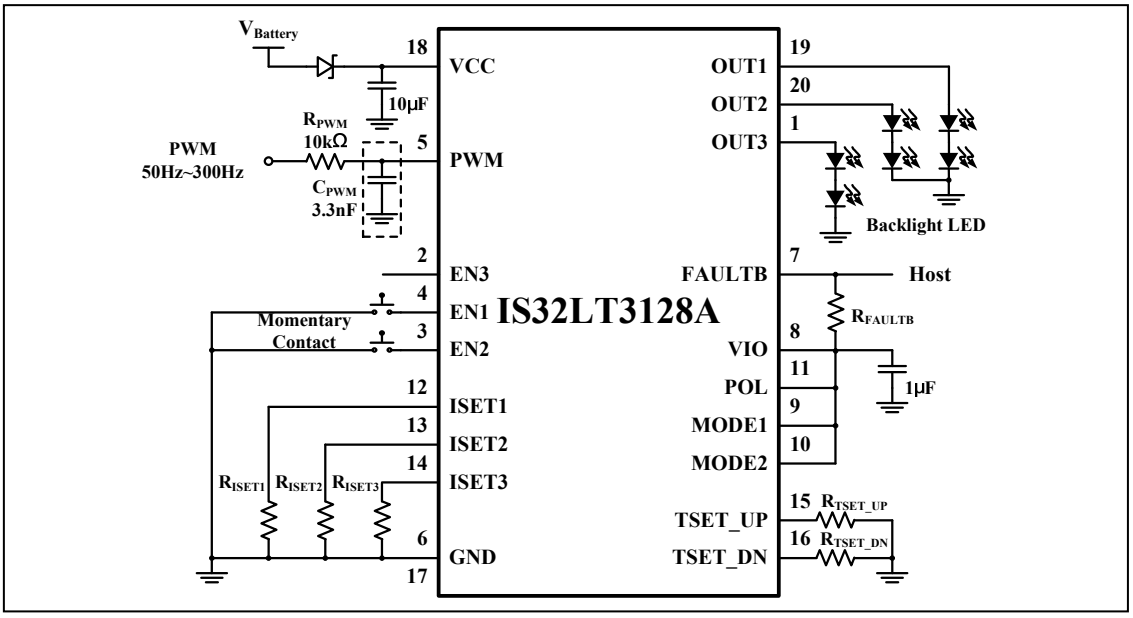


Figure 1 Typical Application Circuit Configured for Momentary Contact Switch And External PWM Dimming

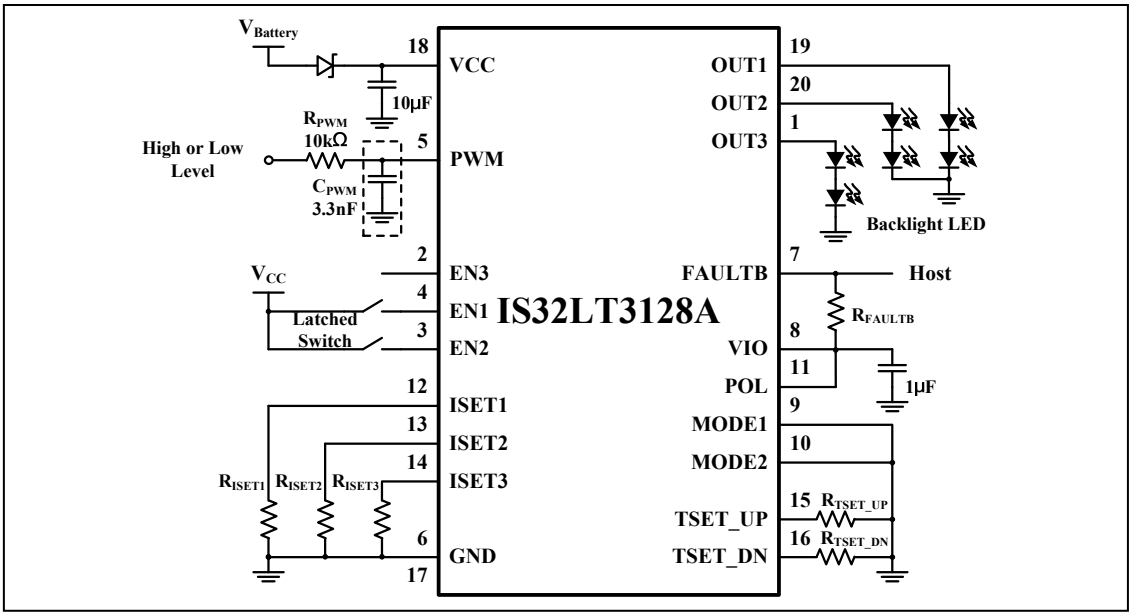
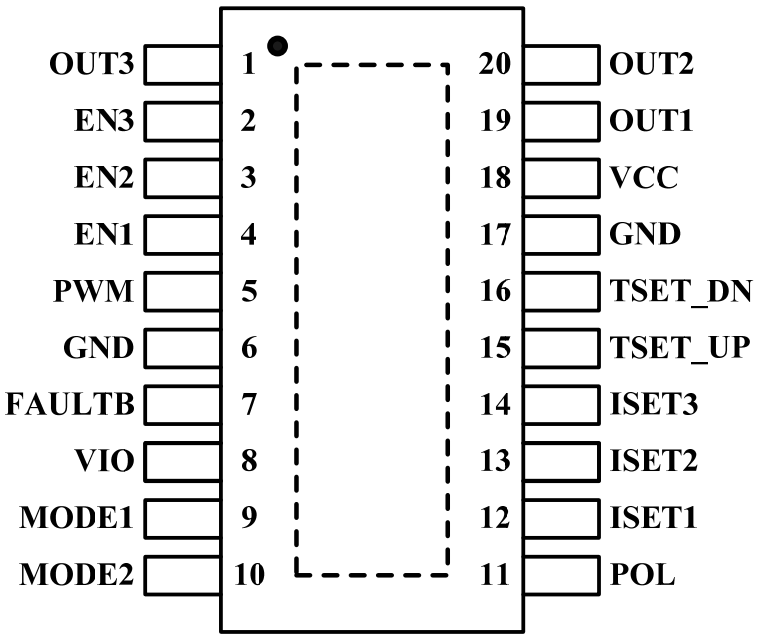


Figure 2 Typical Application Circuit Configured for Latched Switch And Internal PWM Dimming

Note 1: The resistor R_{PWM} is a fixed 10kΩ, do not change value. C_{PWM} is optional to minimize electromagnetic susceptibility.

PIN CONFIGURATION

Package	Pin Configuration (Top View)
eTSSOP-20	

PIN DESCRIPTION

No.	Pin	Description
1	OUT3	Max 30mA output current source for switch backlight LEDs.
2	EN3	Internally deglitch input pin for control of OUT3 current. Pull high (>V_{IH}) to enable OUT3 current. Pull low (<V_{IL}) to disable OUT3 current.
3,4	EN2, EN1	Internally debounced input pin for control of OUT1/2 current. When configured for Low Pulse Mode: EN1/2 pins are internally pulled up to internal 4V LDO by 50kΩ resistors. A low going pulse on either of these two pins will toggle the state of the corresponding OUT1 or OUT2 current. When configured for Level Control Mode: EN1/2 pins are internally pulled down by a 50kΩ resistor to ground. A high level voltage applied to EN1 or EN2 will enable the corresponding OUT1 or OUT2 current while a ground signal will disable the OUT1 or OUT2 current.
5	PWM	An active signal input to drive both OUT1/2. See Figure 60~66 for the details of its priority with EN1/2.
6,17	GND	Ground pins for the device.
7	FAULTB	Open drain fault reporting pin. Pull low to report LED string short and thermal shutdown fault condition.
8	VIO	Internal 4V LDO output pin for pulling up configuration and FAULTB pins.
9	MODE1	Internally deglitched input pin for PWM mode select. Connecting to VIO for External-PWM-Dimming mode. Grounded for Internal-PWM-Dimming mode.
10	MODE2	Internally deglitched input pin for EN1 and EN2 control mode select. Connect to VIO for Low Pulse Mode; EN1/2 low going pulse will toggle OUT1/2 output current state. Connect to ground for Level Control Mode; Appling a high level voltage (>V_{IH}) to either EN1 or EN2 will turn on the corresponding OUT1 or OUT2 currents. Grounding either EN1 or EN2 will turn off the corresponding OUT1 or OUT2 current.
11	POL	Internally deglitched input pin for PWM polarity selection. Connect to VIO for PWM active high and grounded for PWM active low.
12~14	ISET1~ISET3	Output current setting for OUT1/2/3. Connect a resistor between this pin and GND to set the maximum output current.
15	TSET_UP	Timing control for the Fade ON feature. Connect a resistor between this pin and GND to set the Fade ON time. Connect this pin directly to ground to disable the fade function for instant ON.
16	TSET_DN	Timing control for the Fade OFF feature. Connect a resistor between this pin and GND to set the Fade OFF time. Connect this pin directly to ground to disable the fade function for instant OFF.
18	VCC	Power supply input pin.
19,20	OUT1,OUT2	Max. 150mA output current source channels.
	Thermal Pad	Connect to GND.

ORDERING INFORMATION
Automotive Range: -40°C to +125°C

Order Part No.	Package	QTY/Reel
IS32LT3128A-ZLA3-TR	eTSSOP-20, Lead-free	2500

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ABSOLUTE MAXIMUM RATINGS (NOTE 2)

VCC, OUT1/2/3, PWM, EN1/2/3	-0.3V ~ +45V
VIO, POL, MODE1/2, ISET1/2/3, TSET_UP, TSET_DN, FAULTB	-0.3V ~ +7.0V
Ambient operating temperature, T_A=T_J	-40°C ~ +125°C
Maximum continuous junction temperature, $T_{J(MAX)}$	150°C
Storage temperature range, T_{STG}	-65°C ~ +150°C
Package thermal resistance, junction to ambient (4-layer standard test PCB based on JESD 51-2A), θ_{JA}	34°C/W
Package thermal resistance, junction to thermal PAD (4-layer standard test PCB based on JESD 51-8), θ_{JP}	14.46°C/W
Maximum power dissipation, P_{DMAX}	2.94W
ESD (HBM) ESD (CDM)	±2kV ±750V

Note 2: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

T_J = -40°C ~ +125°C, V_{CC}=12V, refer to each condition description. Typical values are at T_J = 25°C.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{CC}	Supply voltage range		5		42	V
V_{HR}	Minimum headroom voltage	V_{CC} -$V_{OUT1/2}$, $I_{OUT1/2}$= -150mA (Note 3)			900	mV
		V_{CC} -$V_{OUT1/2}$, $I_{OUT1/2}$= -100mA (Note 3)			700	
		V_{CC} -V_{OUT3}, I_{OUT3}= -30mA (Note 3)			900	
I_{CC}	Quiescent supply current	OUT1/2/3 output current are all disabled	0.1	0.31	1	mA
		R_{ISET1}= R_{ISET2} =R_{ISET3}=15kΩ, OUT1/2/3 output current are all enabled by ENx, but OUT1/2/3 are all floating		5.5		mA
		V_{CC}=4.2V, OUT1/2 output current are all are enabled by EN1/2 (only for EN Low Pulse Mode), EN3 floating		0.25		mA
t_{ON}	Startup time	V_{CC}> 6V to I_{OUT}<-5mA (Note 4)			400	μs
I_{OUT_LIM}	OUT1/2 limit current (Note 5)	V_{HR}=2V, OUT1/2 sourcing current, $V_{ISET1/2}$= GND	-240	-205	-160	mA
	OUT3 limit current (Note 5)	V_{HR}=2V, OUT3 sourcing current, V_{ISET3}= GND	-48	-40	-32	
I_{OUT}	OUT1/2 output current (Note 5)	$R_{ISET1/2}$= 15kΩ, V_{HR}= 1V, -40°C<T_J<+125°C	-105	-100	-95	mA
	OUT3 output current (Note 5)	R_{ISET3}= 15kΩ, V_{HR} =1V, -40°C<T_J<+125°C	-22	-20	-18	
E_{OUT}	OUT1/2 absolute current accuracy (Note 5)	-50mA≤$I_{OUT1/2}$≤-20mA, V_{HR}=1V, -40°C< T_J <+125°C	-8		8	%
		-150mA≤$I_{OUT1/2}$<-50mA, V_{HR}=1V, -40°C< T_J <125°C	-6		6	%
E_{IOUTM}	OUT1/2 current matching in case of the same $R_{ISET1/2}$ value (Note 5,6)	$I_{OUT1/2}$ = -100mA, V_{HR}=1V, T_J = 25°C			4	%
		$I_{OUT1/2}$ = -100mA, V_{HR}=1V, -40°C < T_J < +125°C			6	%
t_{SL}	Current slew time	Current rise/fall between 0%~100%, V_{TSET}= GND	45	70	100	μs

ELECTRICAL CHARACTERISTICS (CONTINUE)

T_J = -40°C ~ +125°C, V_{CC}=12V, the detail refer to each condition description. Typical values are at T_J = 25°C.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
f_{INTPWM}	Internal PWM frequency			220		Hz
t_{SW}	Input pin debounce time (EN1/2 pins and PWM pin in internal PWM mode)		25	37	50	ms
t_{TD_ON}	PWM current latency	Delay time between PWM rising edge to 10% of I_{OUT}		10		μs
UVLO	Release from under voltage lock out V_{CC} voltage	V_{CC} rising release from UVLO	4.4	4.6	4.8	V
	Into under voltage lock out V_{CC} voltage	V_{CC} falling into UVLO	4.2	4.5	4.7	V
TSET_UP, TSET_DN and VIO						
V_{TSET}	Voltage reference of TSET_UP and TSET_DN			1		V
T_{ACC}	Fade timing accuracy	*Neglecting the R_{TSET} Tolerance* R_{TSET_UP}=100kΩ, T_J = 25°C	-5		5	%
V_{IO}	VIO pin output voltage			4.3		V
Logic Input PWM, EN1/2/3, MODE1/2, POL						
V_{IL}	Input low voltage				0.8	V
V_{IH}	Input high voltage		2			V
V_{IN_HY}	Input hysteresis	(Note 4)	150	350		mV
I_{PWMPU}	PWM pin Internal pull-up current	V_{PWM}=GND and POL pin grounded	20	38	58	μA
I_{PWMPD}	PWM pin Internal pull-down current	V_{PWM}=12V and POL pin connected to VIO	15	28	46	μA
I_{ENPU}	EN1/2 Internal pull-up current	MODE2 pin connected to VIO, $V_{EN1/2}$=GND		67		μA
I_{ENPD}	EN1/2 Internal pull-down current	MODE2 pin grounded, $V_{EN1/2}$=12V		50		μA
	EN3 Internal pull-down current	V_{EN3}=12V		28		uA
Protection						
V_{SCD}	OUTx pins short detect voltage	Measured at OUTx, voltage falling	1.2		1.8	V
V_{SC_HY}	OUTx pins short detect voltage hysteresis	(Note 4)		220		mV
t_{FD}	Fault detect persistence time	(Note 4)		5		ms
V_{FAULTB}	FAULTB pin voltage	Sink current = 5mA		15	80	mV
T_{RO}	Thermal roll off threshold	(Note 4)		145		°C
T_{SD}	Thermal shutdown threshold	Temperature increasing (Note 4)		175		°C
T_{HY}	Over temperature hysteresis	Recovery = T_{SD} – T_{HY} (Note 4)		30		°C

Note 3: I_{OUT} output current in case of V_{CC}-V_{OUT}=V_{HR} called I_{OUT_VHR}. I_{OUT} output current in case of V_{CC}-V_{OUT}=2V called I_{OUT_VHR2V}, V_{HR} accuracy is computed as $|I_{OUT_VHR}-I_{OUT_VHR2V}|/I_{OUT_VHR2V}$<5%.

Note 4: Guaranteed by design.

Note 5: Output current accuracy is not intended to be guaranteed at output voltages less than 1.8V.

Note 6: OUT1/2 current matching is computed as $100\times[1 - 2\times I_{OUTx}/(I_{OUT1}+I_{OUT2})]$. Output current channel to channel match is computed as 100 × [Max. ($|I_{OUTx}- I_{OUT(AV)}|$) / $I_{OUT(AV)}$] , where $I_{OUT(AV)}$ is the average current of all active outputs.

TYPICAL PERFORMANCE CHARACTERISTICS

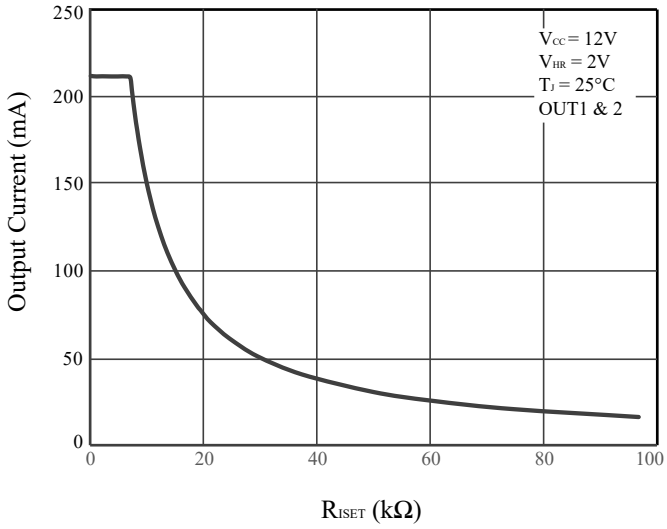


Figure 3 Output Current 1&2 vs. $R_{ISET1/2}$

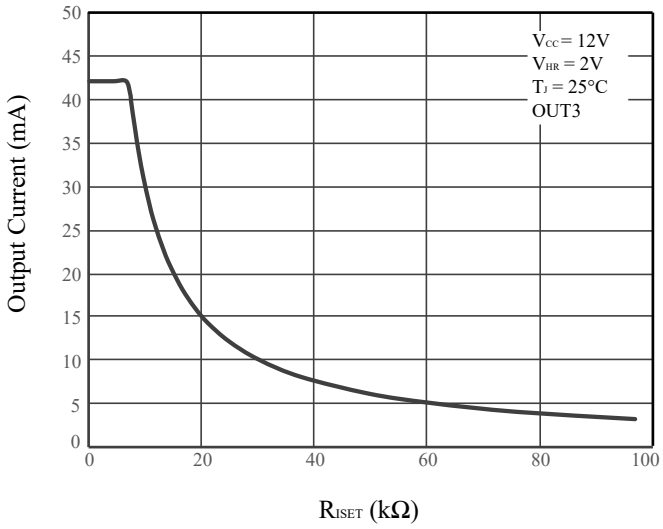


Figure 4 Output Current 3 vs. R_{ISET3}

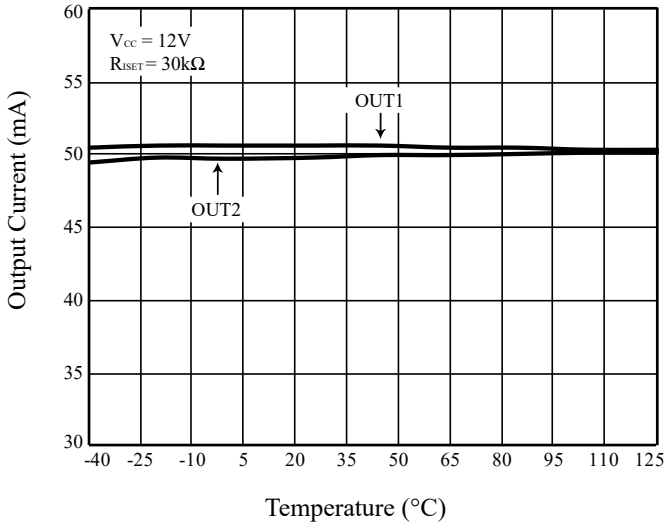


Figure 5 Output Current vs. Temperature

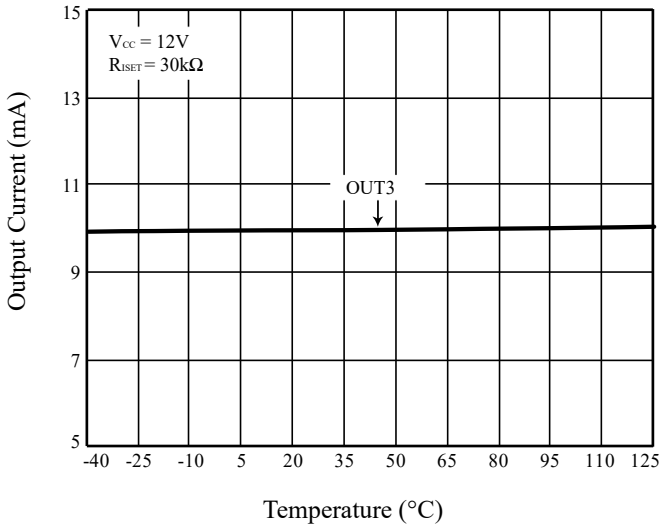


Figure 6 Output Current vs. Temperature

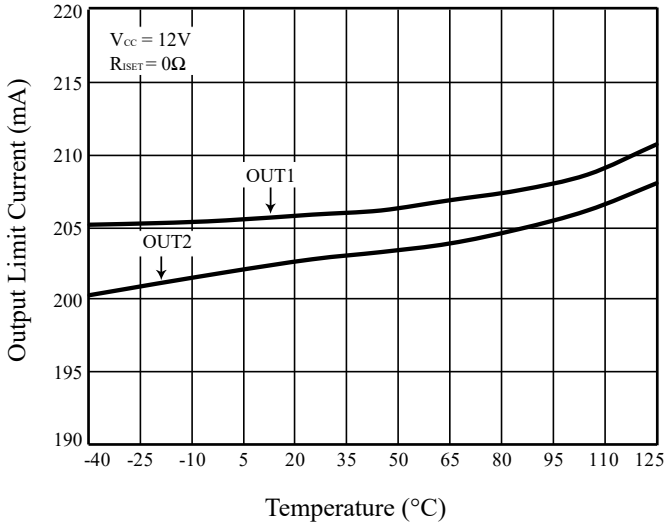


Figure 7 Output 1&2 Limit Current vs. Temperature

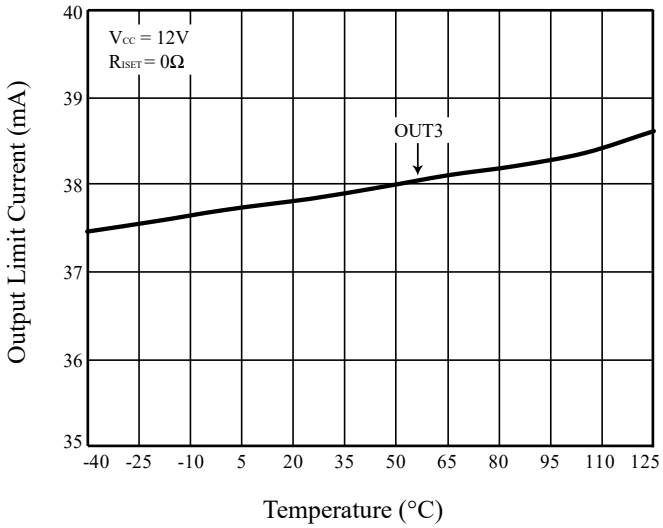


Figure 8 Output 3 Limit Current vs. Temperature

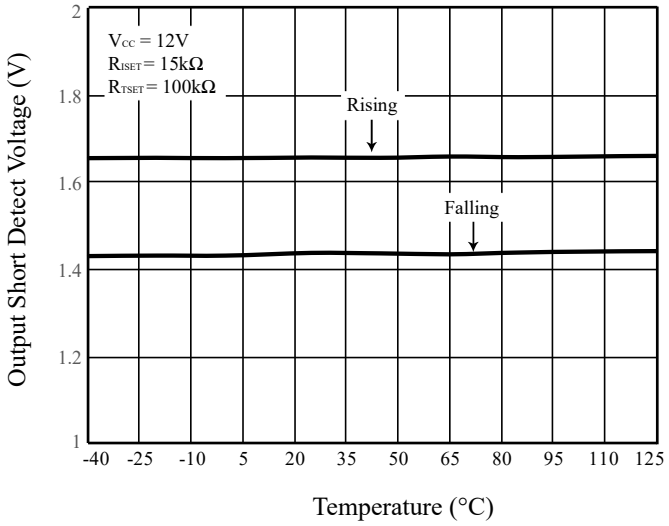


Figure 9 Output Short Detect Voltage vs. Temperature

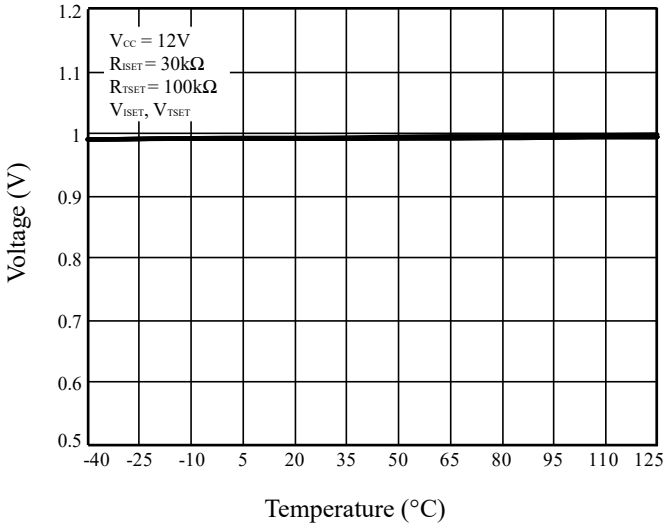


Figure 10 V_{ISET} & V_{TSET} vs. Temperature

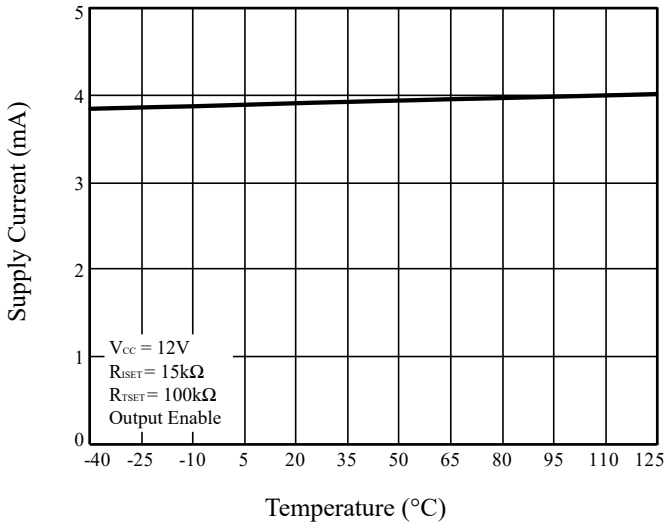


Figure 11 Supply Current vs. Temperature

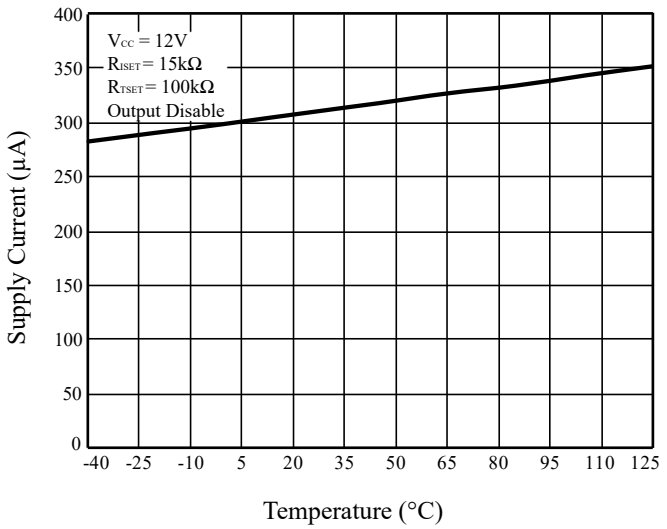


Figure 12 Supply Current vs. Temperature

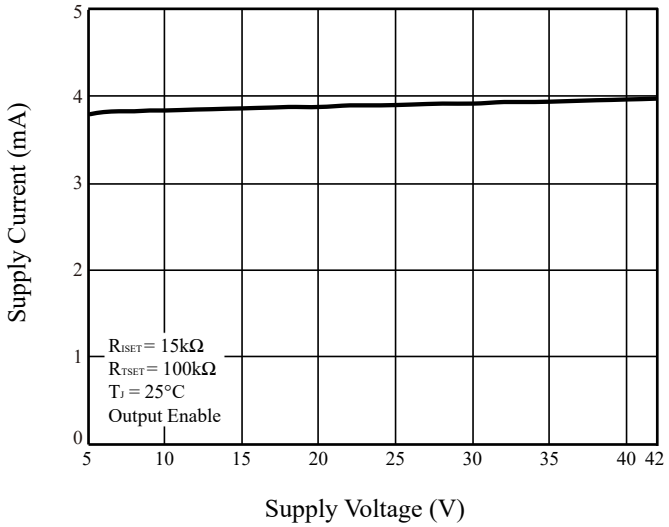


Figure 13 Supply Current vs. Supply Voltage

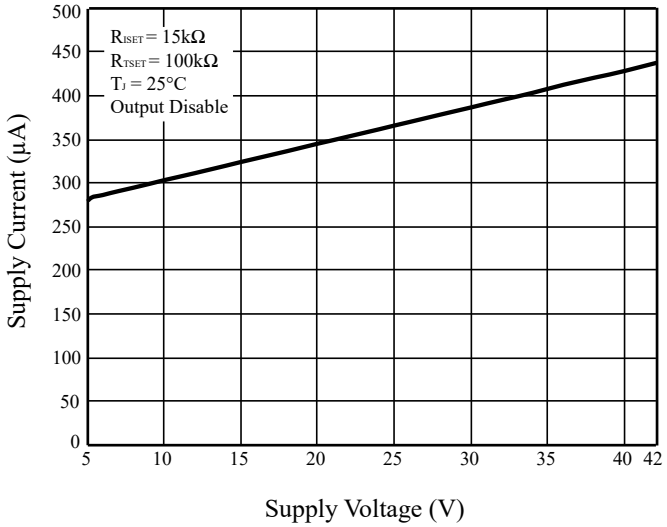


Figure 14 Supply Current vs. Supply Voltage

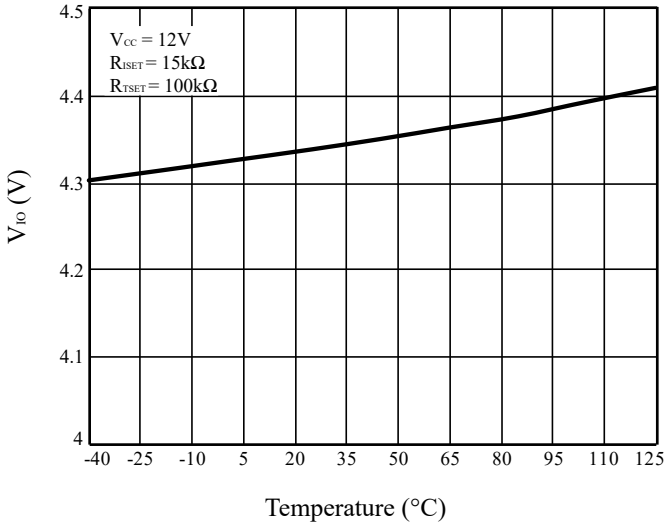


Figure 15 V_{IO} vs. Temperature

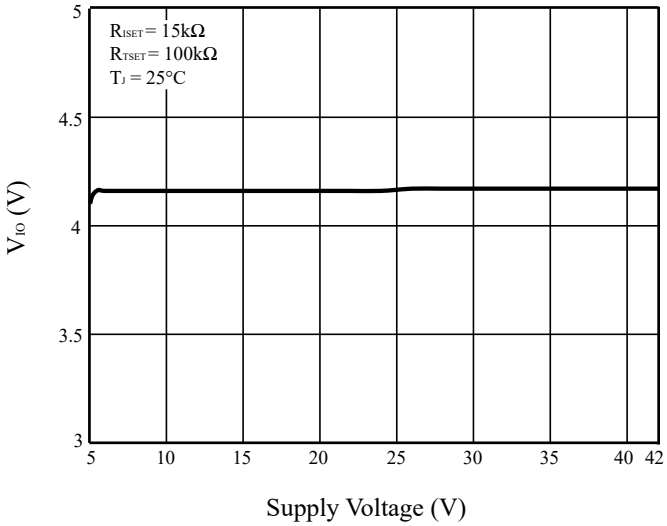


Figure 16 V_{IO} vs. Supply Voltage

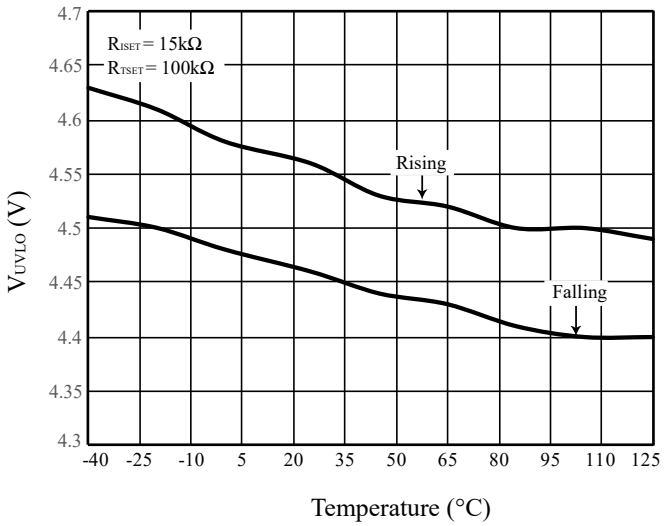


Figure 17 V_{UVLO} vs. Temperature

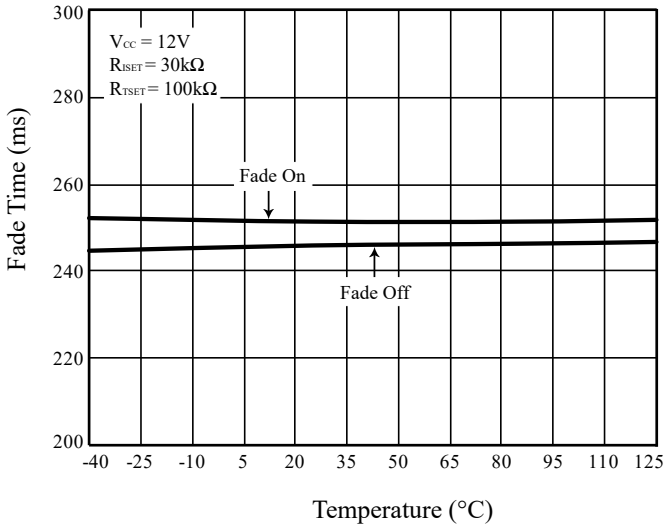


Figure 18 Fade Time vs. Temperature

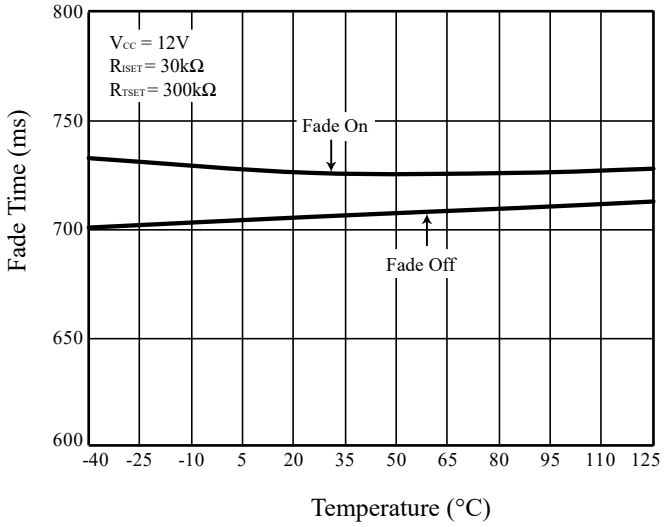


Figure 19 Fade Time vs. Temperature

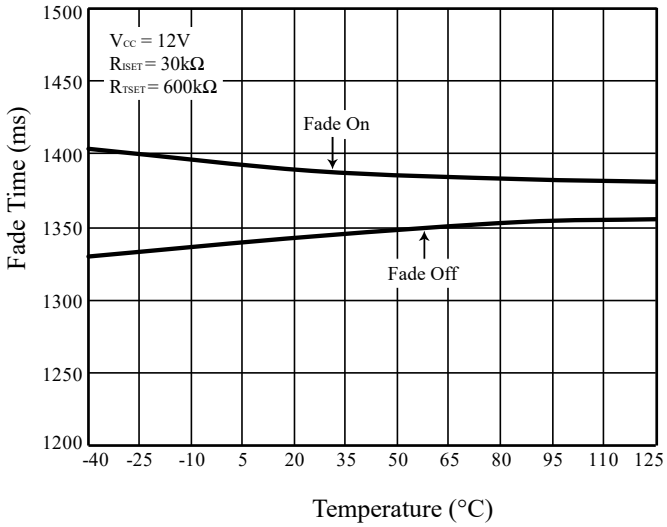


Figure 20 Fade Time vs. Temperature

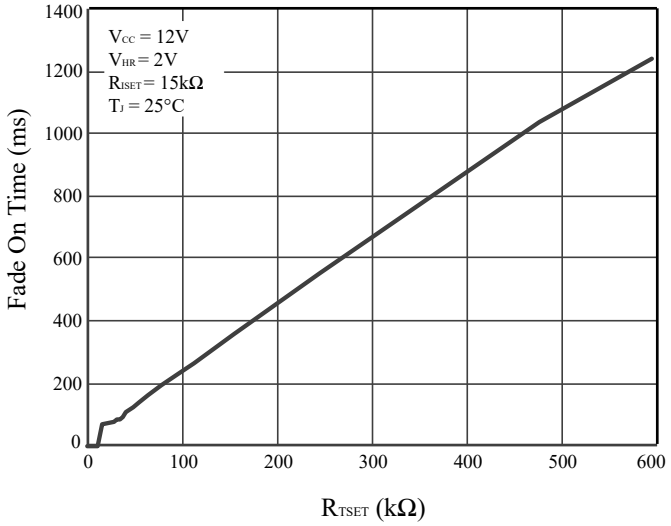


Figure 21 Fade On Time vs. R_{TSET}

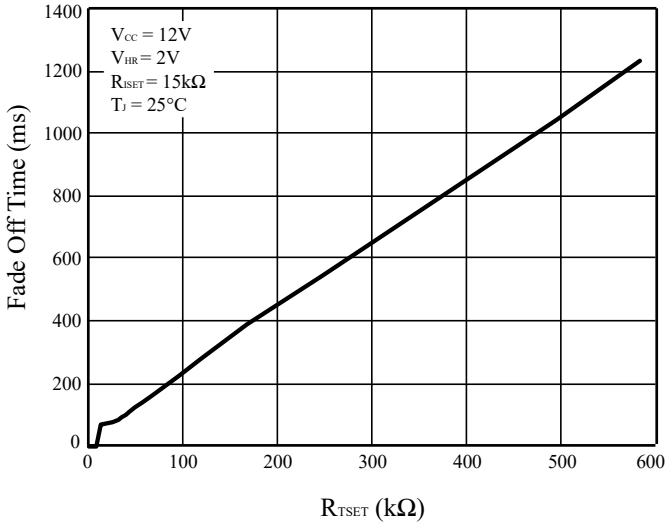


Figure 22 Fade Off Time vs. R_{TSET}

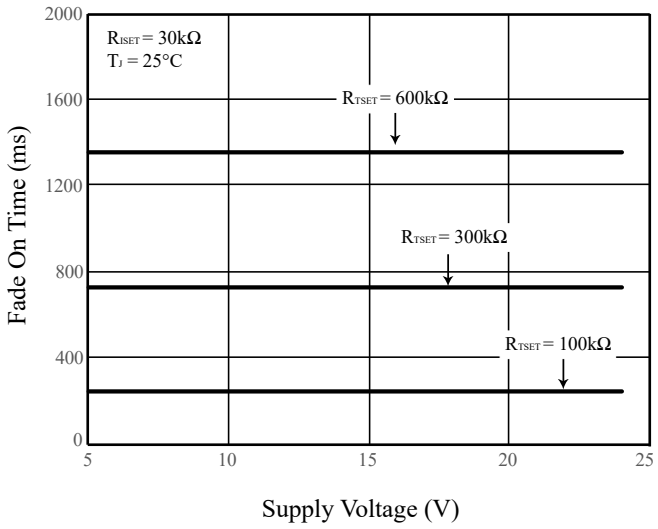


Figure 23 Fade On Time vs. Supply Voltage

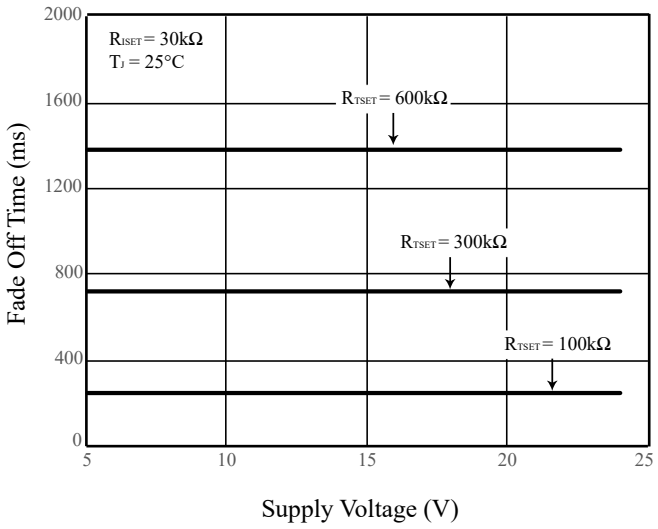


Figure 24 Fade Off Time vs. Supply Voltage

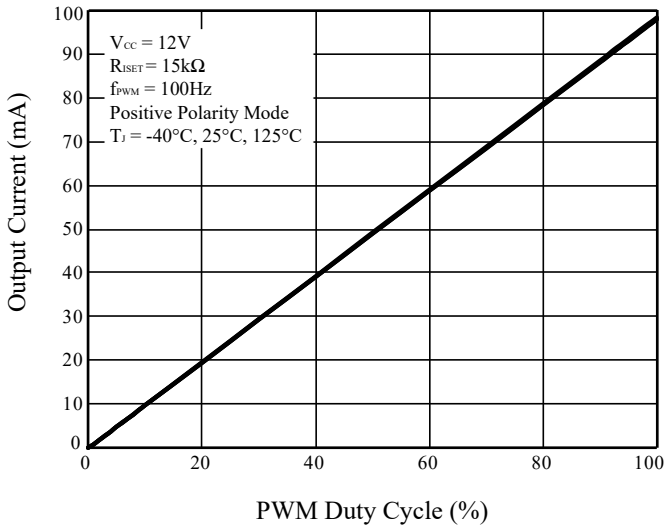


Figure 25 Output Current vs. PWM Duty Cycle

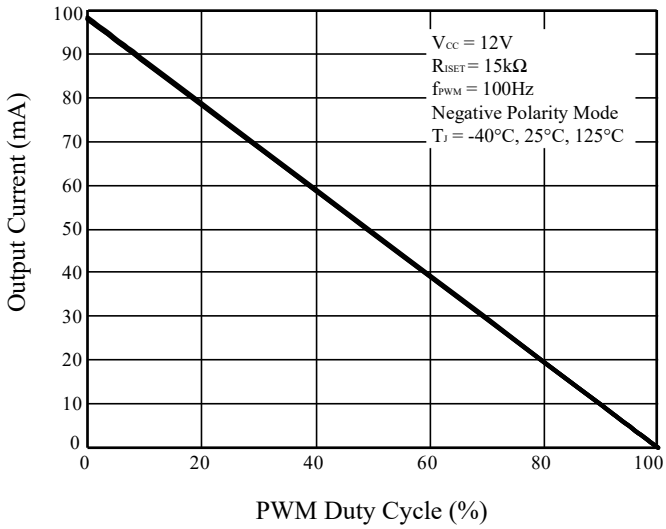


Figure 26 Output Current vs. PWM Duty Cycle

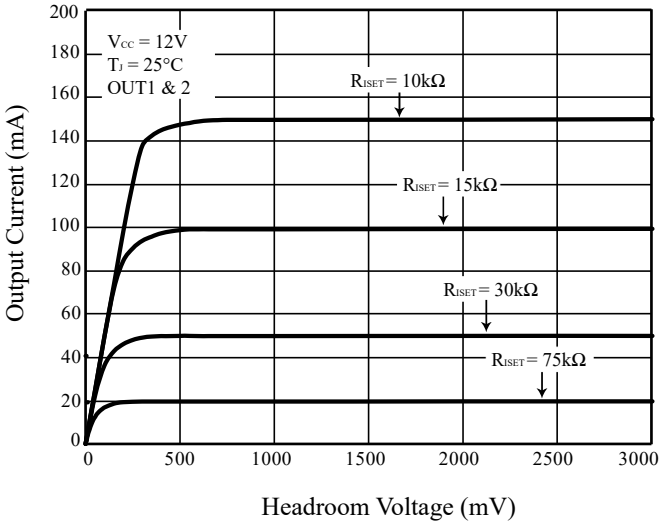


Figure 27 Output Current 1&2 vs. Headroom Voltage

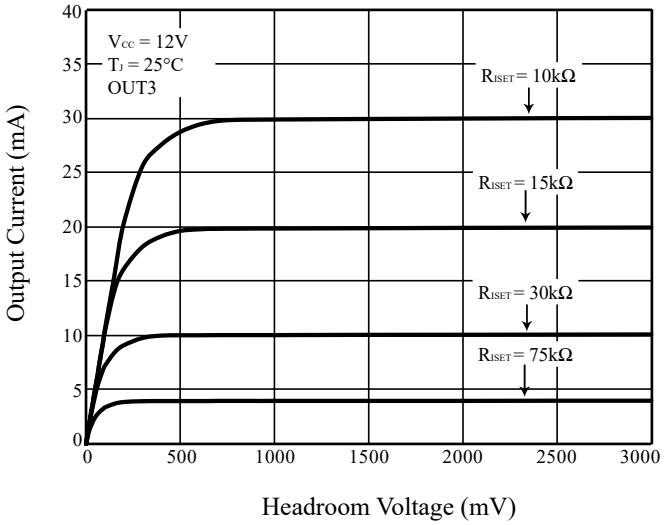


Figure 28 Output Current 3 vs. Headroom Voltage

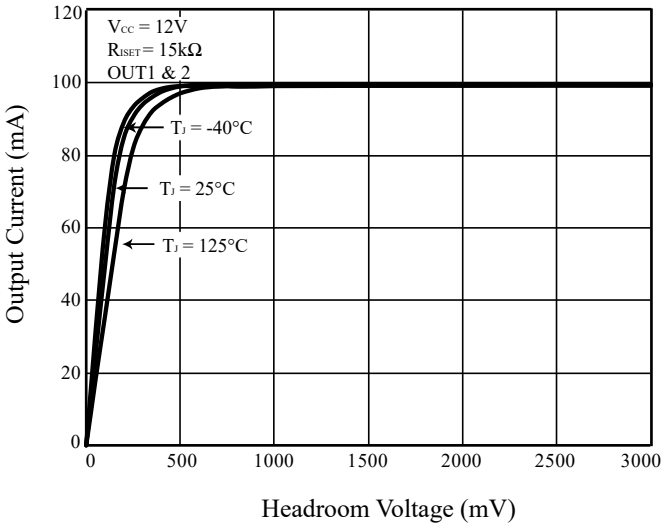


Figure 29 Output Current 1&2 vs. Headroom Voltage

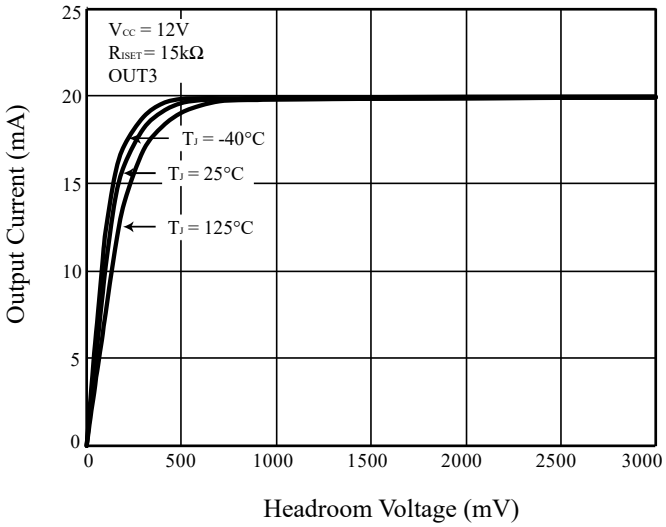


Figure 30 Output Current 1&2 vs. Headroom Voltage

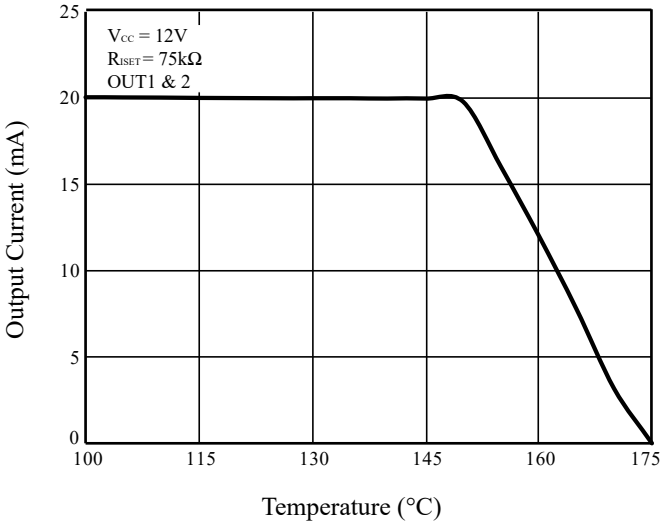


Figure 31 Thermal Roll Off

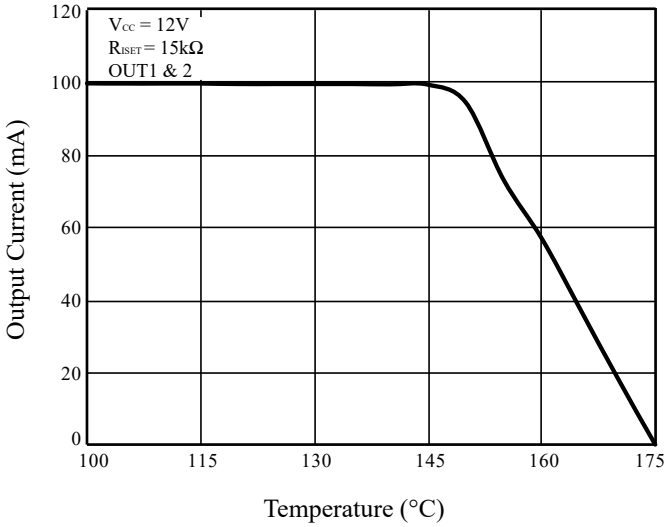


Figure 32 Thermal Roll Off

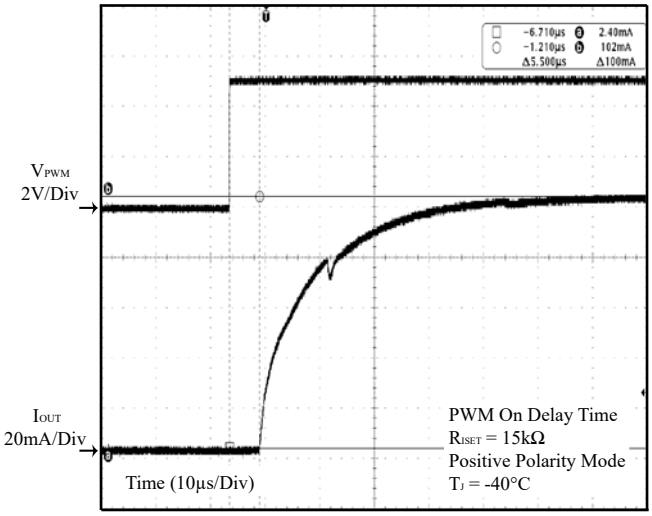


Figure 33 PWM On Delay Time

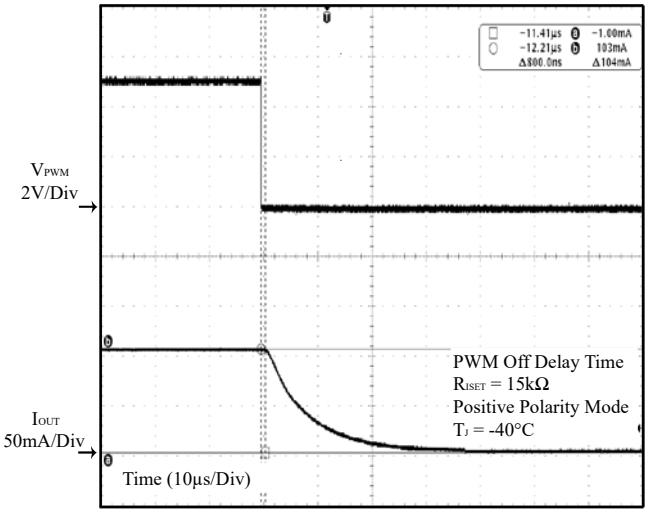


Figure 34 PWM Off Delay Time

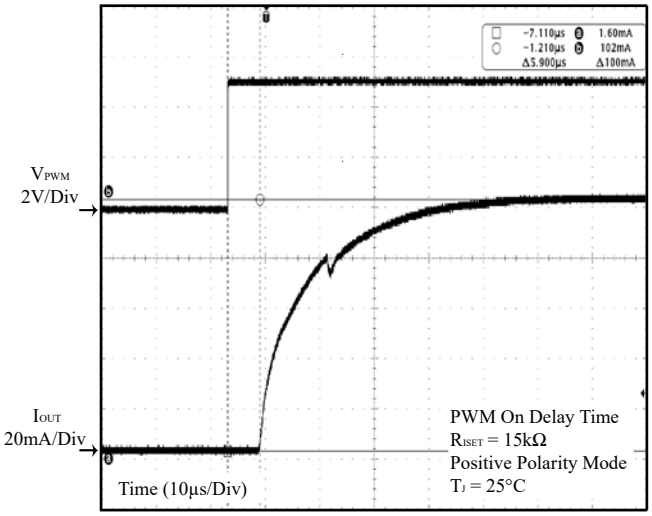


Figure 35 PWM On Delay Time

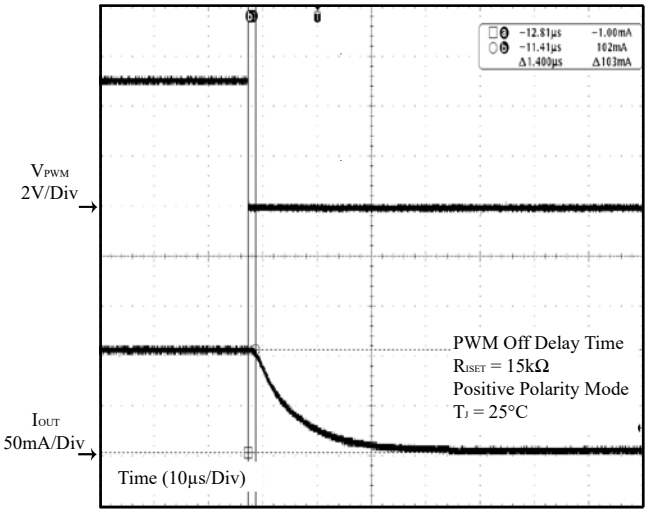


Figure 36 PWM Off Delay Time

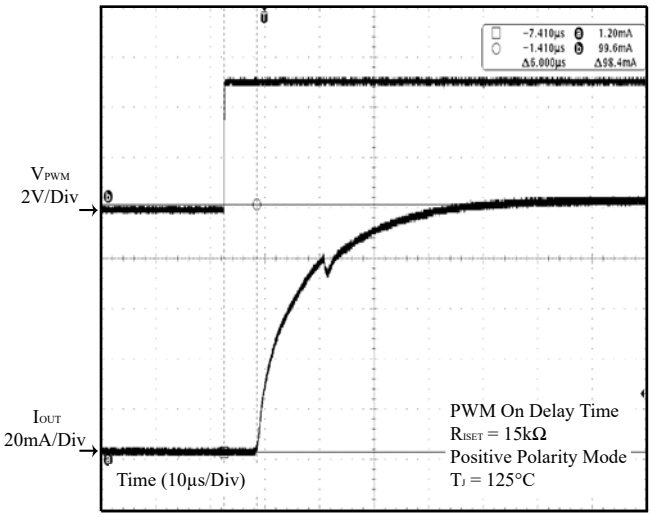


Figure 37 PWM On Delay Time

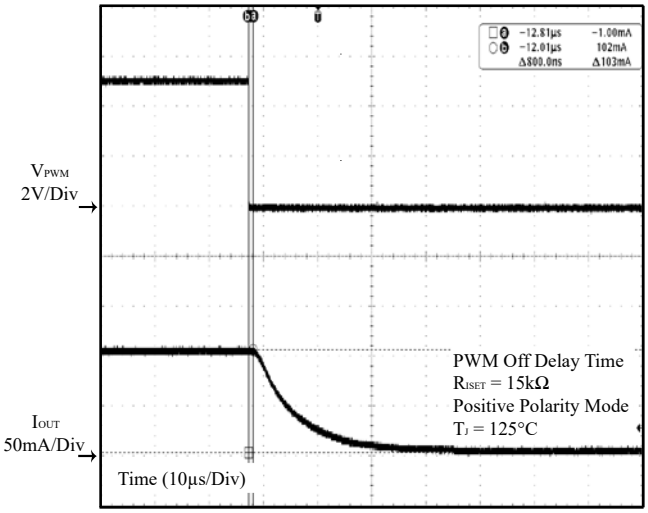


Figure 38 PWM Off Delay Time

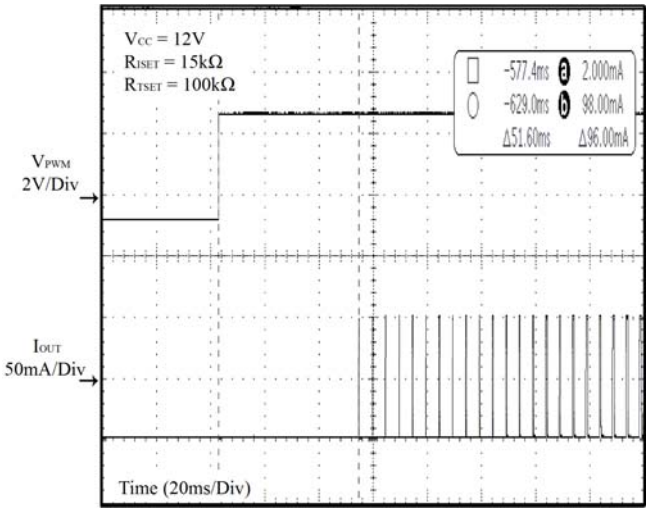


Figure 39 Internal-PWM-Dimming On

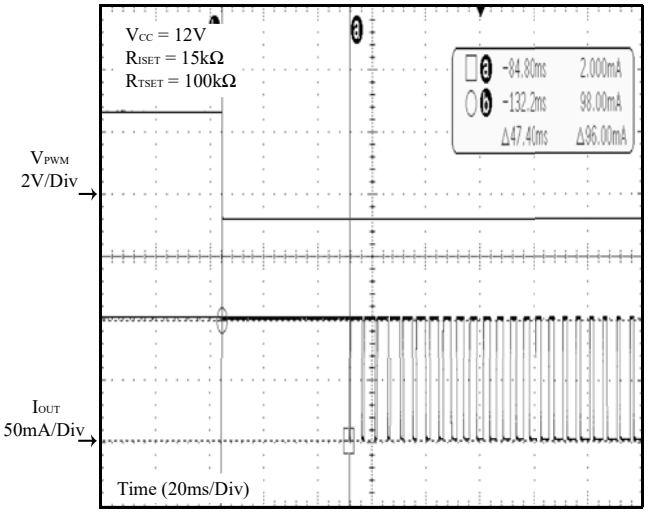


Figure 40 Internal-PWM-Dimming Off

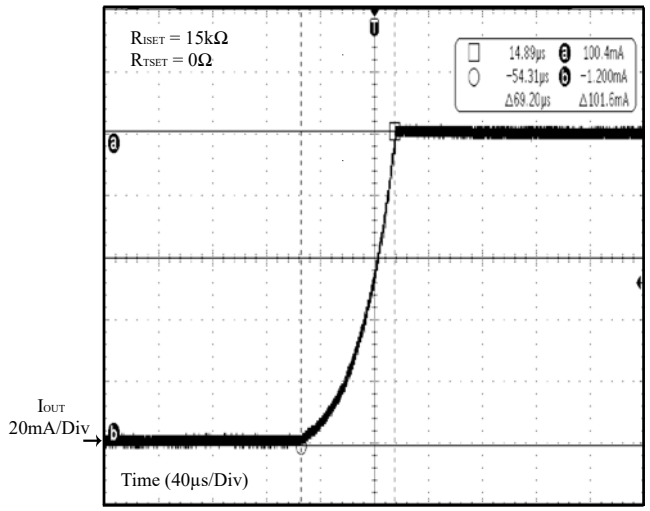


Figure 41 Instant On

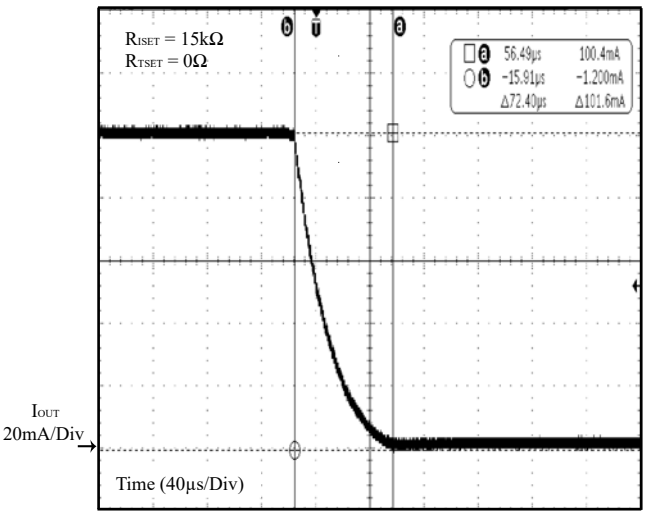


Figure 42 Instant Off

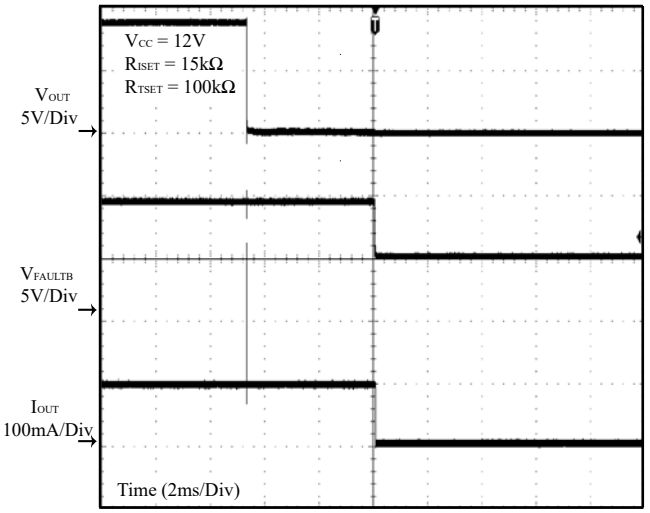


Figure 43 Output Short Detection

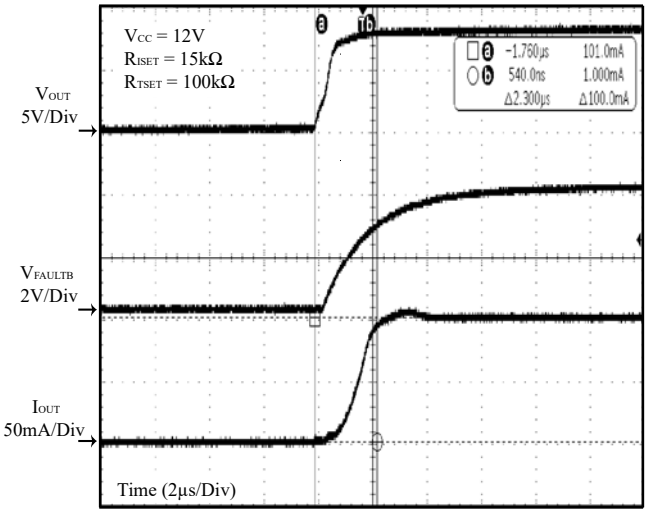


Figure 44 Output Short Recovery

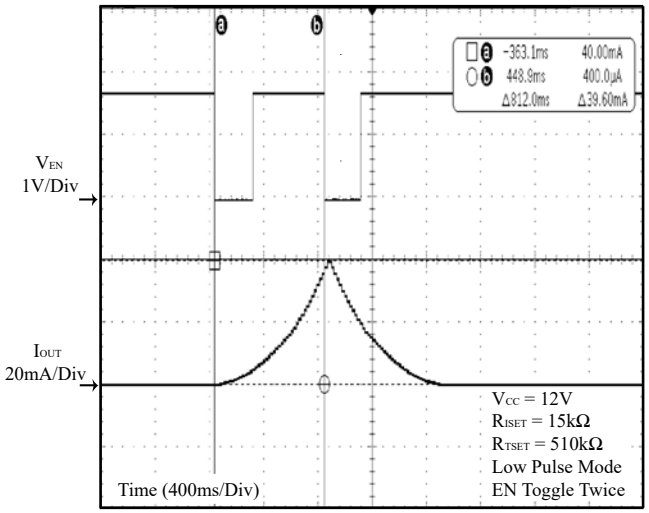


Figure 45 V_{EN} vs. I_{OUT}

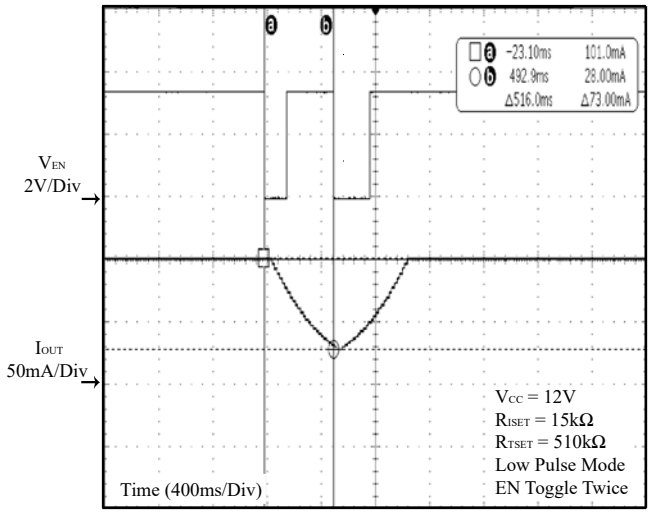


Figure 46 V_{EN} vs. I_{OUT}

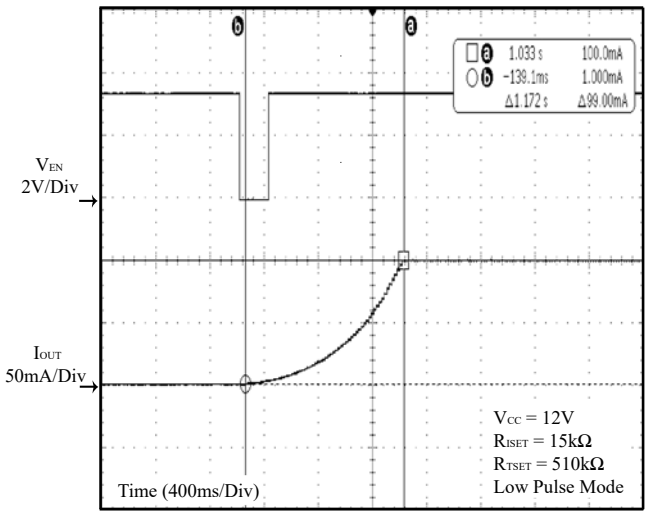


Figure 47 V_{EN} vs. I_{OUT}

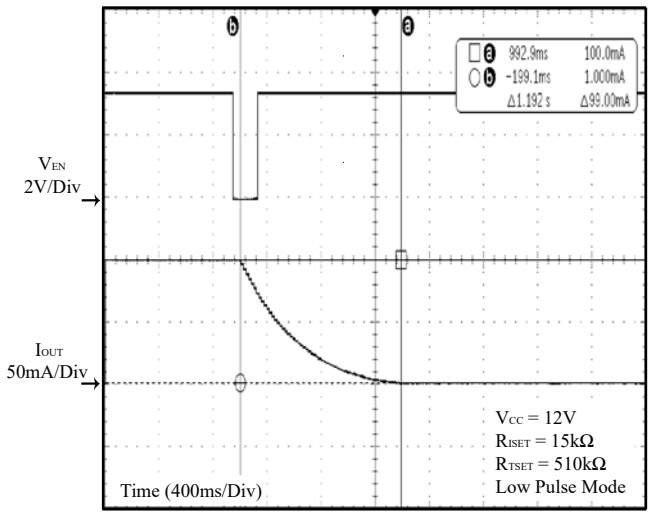


Figure 48 V_{EN} vs. I_{OUT}

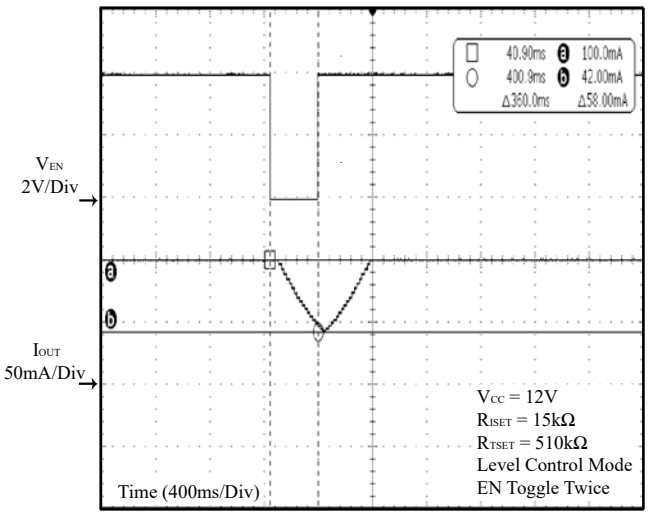


Figure 49 V_{EN} vs. I_{OUT}

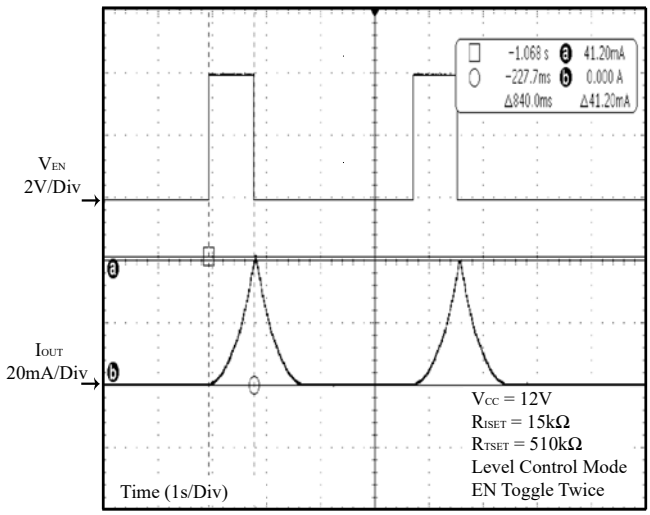


Figure 50 V_{EN} vs. I_{OUT}

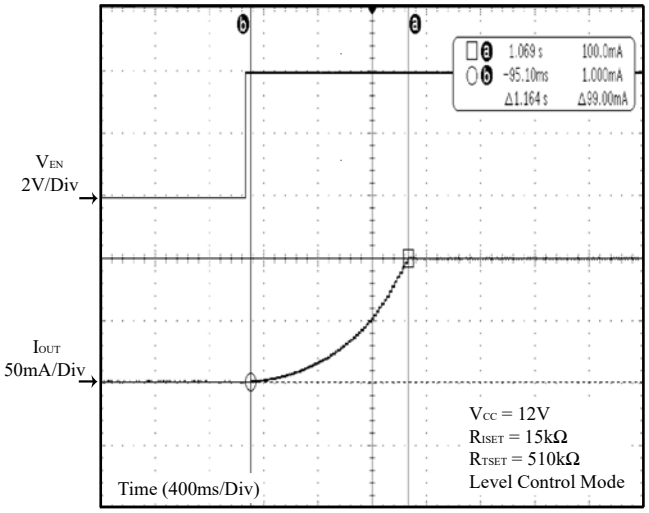


Figure 51 V_{EN} vs. I_{OUT}

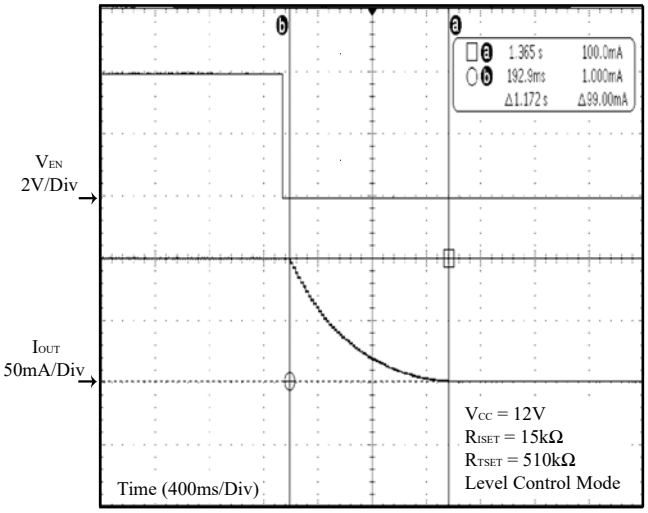
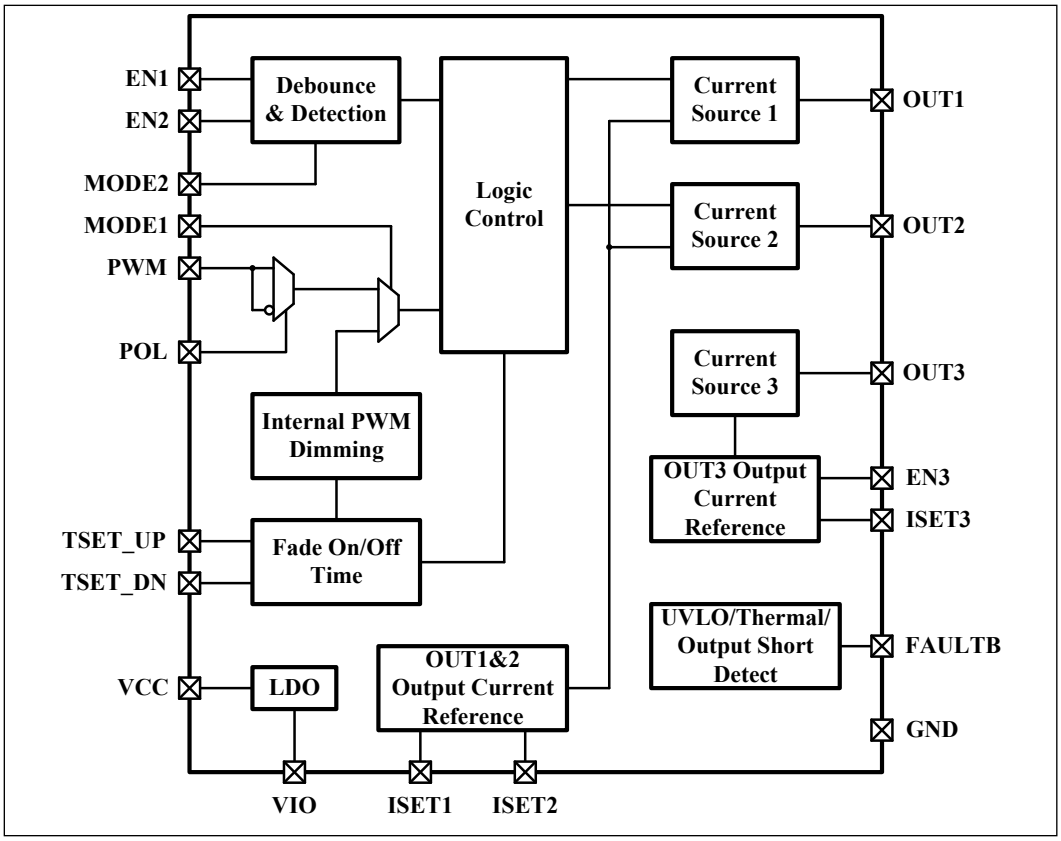


Figure 52 V_{EN} vs. I_{OUT}

FUNCTIONAL BLOCK DIAGRAM



APPLICATION INFORMATION

The IS32LT3128A is triple channel linear current driver optimized to drive an automotive interior LED map light, or other interior lamp which is frequently toggled between the ON and OFF condition. The device integrates a debounce input circuit to enable use of a low cost momentary contact switch or latched switch for controlling ON/OFF of an external LED. In addition, a programmable fade ramp timing function provides flexibility in setting different Fade ON and Fade OFF ramp duration periods. The fade ramp cycle can be interrupted mid-cycle before the ramp has completed, Figure 53.

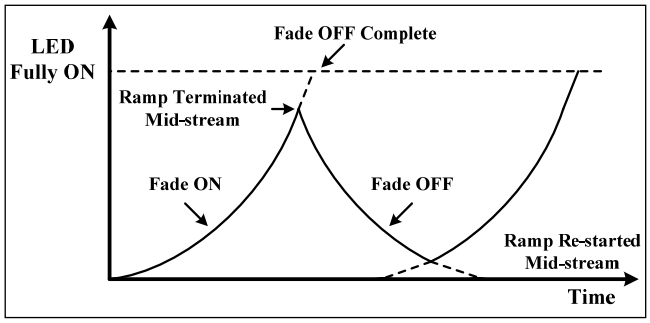


Figure 53 Fade Ramp Interrupted Mid-Cycle

The regulated OUT1/2 LED current (up to 150mA) and OUT3 backlight LED current (up to 30mA) are independently set by their corresponding reference resistor $R_{ISET1/2}$ and R_{ISET3}.

OUTPUT CURRENT SETTING

An individual programming resistor (R_{ISETx}) is connected to the ISETx pin to set the maximum output current for each output channel.

The programming resistor of OUT1/2 can be computed using the following Equation (1):

$$R_{ISET1/2} = \frac{1500}{I_{OUT1/2}} \qquad (1)$$

($10k\Omega \le R_{ISET1/2} \le 75k\Omega$)

Where $I_{OUT1/2}$ is the desired output current value in Amps.

The programming resistor of OUT3 can be computed using the following Equation (2):

$$R_{ISET3} = \frac{300}{I_{OUT3}} \qquad (2)$$

($10k\Omega \le R_{ISET3} \le 75k\Omega$)

Where I_{OUT3} is the desired output current value in Amps.

It is highly recommend to use 1% accuracy R_{ISETx} resistors with good temperature characteristics to ensure accurate and stable output currents.

The device is protected from an output overcurrent condition caused by an accidental short circuit of the ISETx pin, by internally limiting the maximum current in the event of an ISETx short circuit to 205mA (Typ.) for OUT1/2 and 40mA (Typ.) for OUT3.

EN1/2 PIN OPERATION

The EN1/2 pins can individually control the state of the OUT1/2 channels. When driven, the output current will ramp up (or down) in 63 PWM steps, with integrated gamma correction for an extremely visual linear lumen output of the LED. The ramp time can be interrupted mid-cycle each time the EN1/2 pins are toggled.

There are two kinds of operating modes: Low Pulse Mode and Level Control Mode. These modes are selected by the MODE2 pin. Connect it to VIO for Low Pulse Mode and ground it for Level Control Mode as shown in Table 1.

Table 1 EN1 And EN2 Mode

MODE2 Pin	EN1/2 Pin	Output Current
Connected to VIO (Low Pulse Mode)	Low going pulse	If LED off, fade on (ramp up) If LED on, fade off (ramp down)
Grounded (Level Control Mode)	Low to high	If LED off, fade on (ramp up) If LED on, keep on
	High to low	If LED on, fade off (ramp down) If LED off, keep off

Low Pulse Mode (MODE2 pin connected to VIO):

In this mode, the ENx pin is internally pulled-up by a 50kΩ resistor to 4V LDO so that no external components are required to provide the input high level to the pin.

The output channels power up in the “OFF” condition. Toggling the ENx pin from high to low for a period of time that exceeds the debounce time (Typ. 37ms) will cause the corresponding output to be toggled and latched from the OFF condition to the current source condition. When this happens, the corresponding output current gradually ramps up from zero mA to the programmed value (set by $R_{ISET1/2}$) over the time set by the resistor (R_{TSET_UP}) attached to the TSET_UP pin. Conversely, if it is already in the source condition, and the ENx pin is toggled low, then the corresponding output current will begin to ramp down towards zero mA in the time period as programmed by the resistor (R_{TSET_DN}) attached to the TSET_DN pin. So a low cost momentary contact switch can be used in this mode.

Level Control Mode (MODE2 pin grounded):

In this mode, the ENx pin is internally pull-down by 50kΩ resistor to ground so that no external

components are required to provide the input low level to the pin.

Externally pull ENx pin to high level (>V_{IH}) and keep it at high level, after a period of time that exceeds the debounce time (Typ. 37ms) that will cause the corresponding output to be toggled from the OFF condition to the current source condition. When this happens, the corresponding output current gradually ramps up from zero mA to the programmed value (set by $R_{ISET1/2}$) over the time set by the resistor (R_{TSET_UP}) attached to the TSET_UP pin. Conversely, if ENx is already kept in high level and the output is in the source condition, the ENx pin is pulled to low level, then the corresponding output current will begin to ramp down towards zero mA in the time period as programmed by the resistor (R_{TSET_DN}) attached to the TSET_DN pin. So a regular latched switch can be used in this mode.

Debounce – Output control is provided by a debounced switch input, providing an ON/OFF toggle action for various switch or button characteristics. An internal debounce circuit will condition the EN input signal so a single press of the mechanical switch doesn't appear like multiple presses. The EN input is debounced by typically 37ms.

Note: The debounce time applies to both falling and rising edges of the EN signal.

EN3 PIN OPERATION

The EN3 is the enable control of OUT3. There is no fade ON/OFF function as with the EN1/2 pins. EN3 pin is internally pulled down by a 100kΩ resistor to ground. The latency time from EN3 pin pull high over V_{IH} to OUT3 output current rise to 10% is 6μs (Typ.). Float or pull down EN3 to ground to disable OUT3. An external PWM signal driving EN3 pin can implement OUT3 dimming by modulating PWM duty cycle.

The recommended PWM signal frequency range is 50Hz-300Hz. The duty cycle can be 0-100%. The output current of the PWM dimming is given by Equation (3):

$$I_{OUT3_PWM} = \frac{300}{R_{ISET3}} \times D_{PWM} \qquad (3)$$

Where, D_{PWM} is the duty cycle of the PWM.

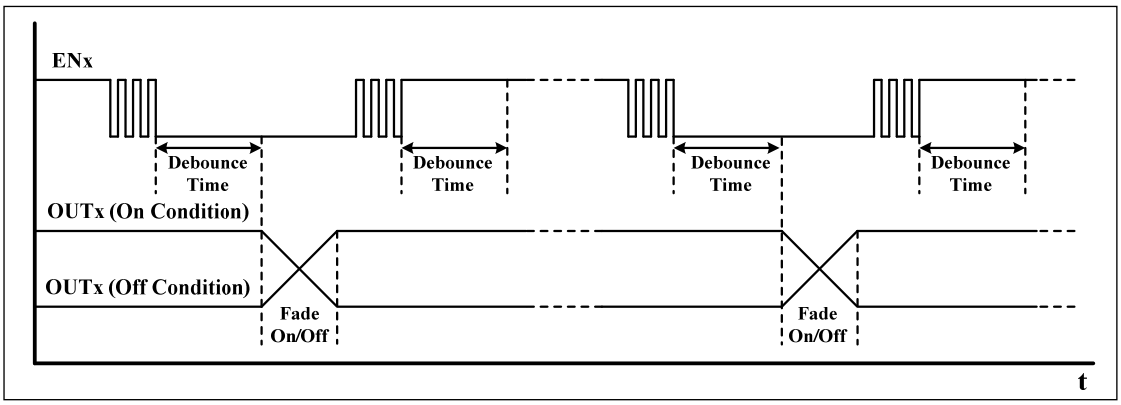


Figure 54 EN1/2 in Low Pulse Mode (Momentory Contact Switch)

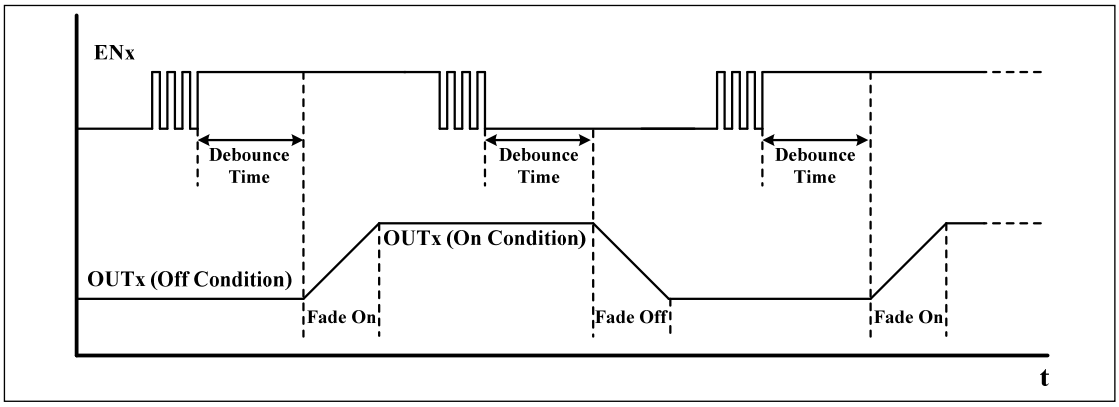


Figure 55 EN1/2 in Level Control Mode (Latched Switch)

FADE ON AND FADE OFF DIMMING

The OUT1/2 LED fade function can be accomplished in one of two methods; 1) by applying a PWM control signal or voltage level to the PWM pin, or 2) when the EN pin is toggled.

PWM PIN Dimming

The PWM pin will simultaneously control both OUT1/2 channels. There are two kinds of dimming via PWM pin: External-PWM-dimming and Internal-PWM-Dimming. The dimming modes are selected by the MODE1 pin. Connect it to VIO for External-PWM-Dimming mode and ground it for Internal-PWM-Dimming mode.

The POL pin will select either positive or negative PWM polarity operation. When this pin is connected to VIO, the PWM pin is in positive polarity and internally pulled down by a 100kΩ to ground. An external PWM high signal will enable both output channels. When the POL pin is grounded, the PWM pin is in negative polarity and internally pulled up by a 100kΩ to 4V LDO. An external PWM low signal will enable both output channels. The Figures 56 and 57 show the different PWM polarity.

External-PWM-Dimming (MODE1 pin connected to VIO):

In this mode, the PWM pin can be driven by an external positive or negative polarity PWM signal source to dim both channels simultaneously. The integrated gamma correction and fade ON/OFF ramp functions are disabled when actively driving the PWM pin.

To get better dimming ratio, the recommended PWM signal frequency range is 50Hz~300Hz. The duty cycle can be 0~100%. The average output current of the PWM dimming is given by Equation (4) and (5):

For PWM positive polarity,

$$I_{OUT1/2_PWM} = \frac{1500}{R_{ISET1/2}} \times D_{PWM} \qquad (4)$$

For PWM Negative polarity,

$$I_{OUT1/2_PWM} = \frac{1500}{R_{ISET1/2}} \times (1 - D_{PWM}) \qquad (5)$$

Where, D_{PWM} is the duty cycle of the PWM. Please refer to Figure 33~38 for the delay time of PWM edge to current change edge.

Internal-PWM-Dimming (MODE1 pin grounded):

In this mode, the integrated PWM source is operational. The PWM pin can trigger this PWM source as shown in table 2. The POL pin decides the PWM pin polarity active mode. When PWM pin is changed the voltage level state and after a period of time that exceeds the debounce time (Typ. 37ms), the both output current will either gradually ramp up from zero mA to the programmed value (set by $R_{ISET1/2}$) over the time set by the resistor (R_{TSET_UP}) attached to the TSET_UP pin or gradually ramp down from programmed value to zero mA over the time set by the resistor (R_{TSET_DN}) attached to the TSET_DN pin. The ramping up (or down) is accomplished by the internal 220Hz PWM source digitally modulating the both output current simultaneously with 63 steps gamma correction, that will perform an extremely visual linear light to human eye.

Table 2 PWM Mode

POL Pin	MODE1 Pin	PWM Pin	Output Current
Connected to VIO (Positive polarity)	Connected to VIO (External-PWM-Dimming)	Low to high	If LED is off, instant on. If LED is on, keep on.
		High to low	If LED is on (due to PWM high), instant off. If LED is off, keep off.
	Grounded (Internal-PWM-Dimming)	Low to high	If LED off, fade on (ramp up) by internal PWM signal. If LED on, keep on.
		High to low	If LED on (due to PWM high), fade off (ramp down) by internal PWM signal. If LED off, keep off.
Grounded (Negative polarity)	Connected to VIO (External-PWM-Dimming)	Low to high	If LED is on (due to PWM low), instant off. If LED is off, keep off.
		High to low	If LED is off, instant on. If LED is on, keep on.
	Grounded (Internal-PWM-Dimming)	Low to high	If LED on (due to PWM low), fade off (ramp down) by internal PWM signal. If LED off, keep off.
		High to low	If LED off, fade on (ramp up) by internal PWM signal. If LED on, keep on.

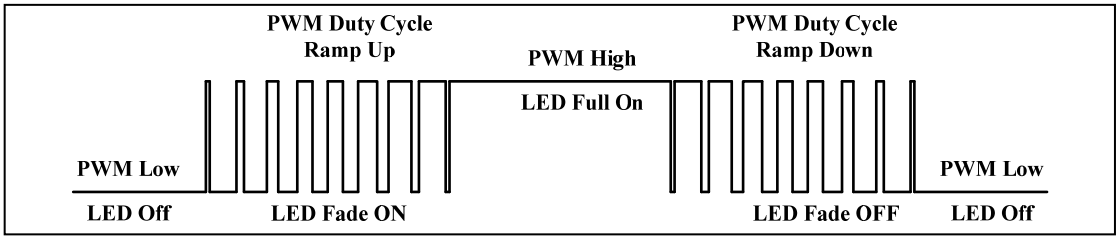


Figure 56 External-PWM-Dimming Input for OUT1/2 (Positive Polarity)

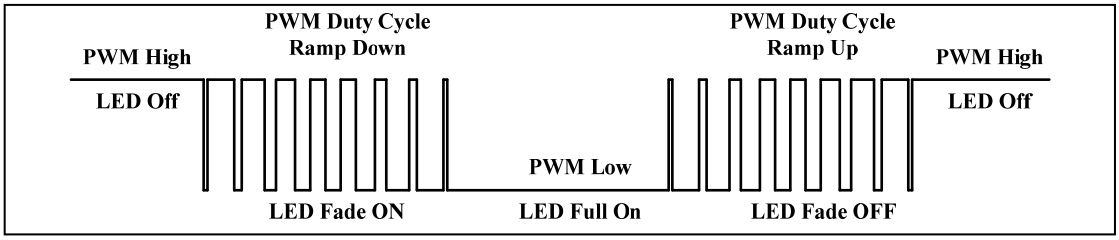


Figure 57 External-PWM-Dimming Input for OUT1/2 (Negative Polarity)

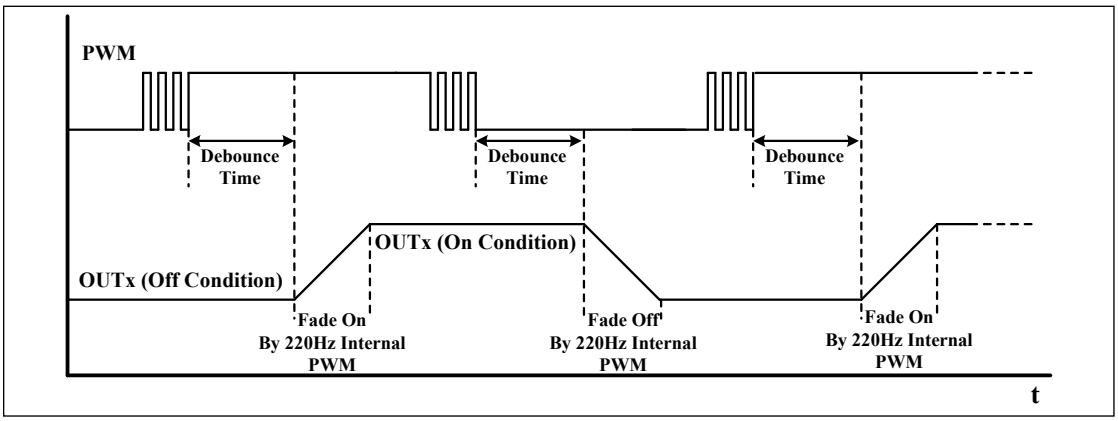


Figure 58 Ineternal-PWM-Dimming for OUT1/2 (Positive Polarity)

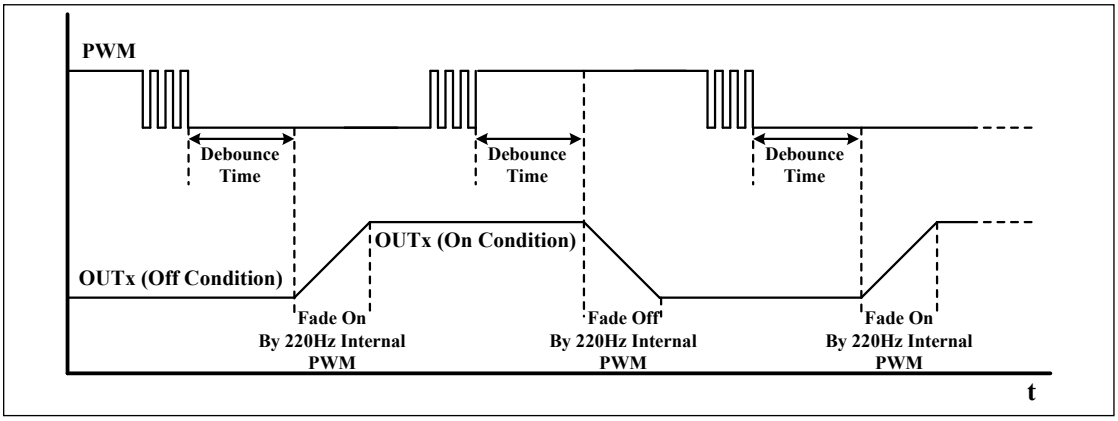


Figure 59 Ineternal-PWM-Dimming for OUT1/2 (Negative Polarity)

THE PRIORITY OF EN1/2 AND PWM DIMMING

EN1/2 pins can individually control the OUT1/2 while PWM pin can simultaneously control the both outputs. The Figure 60~66 lists some critical priority logic of them:

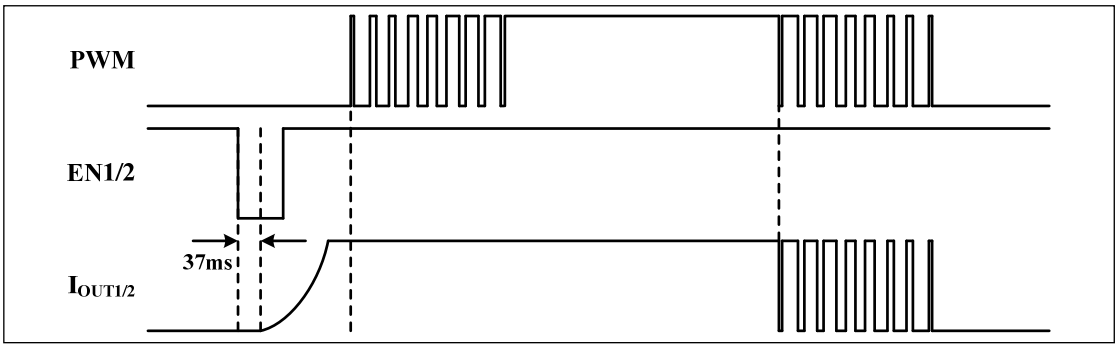


Figure 60 Priority Logic 1 of EN1/2 in Low Pulse Mode

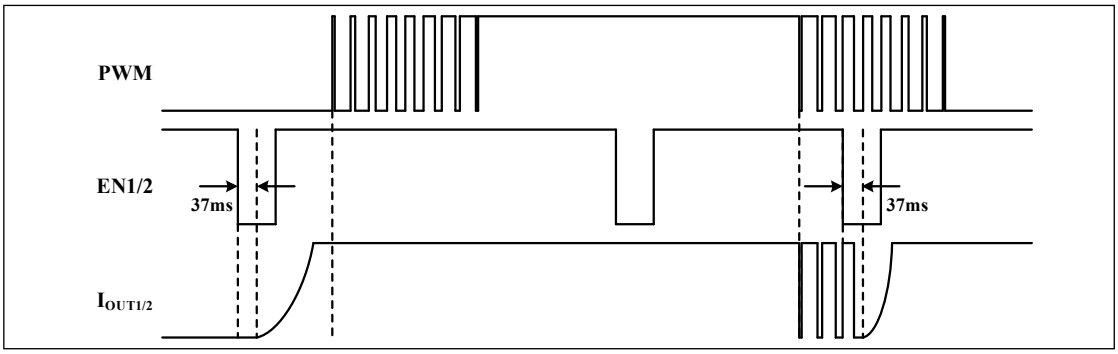


Figure 61 Priority Logic 2 of EN1/2 in Low Pulse Mode

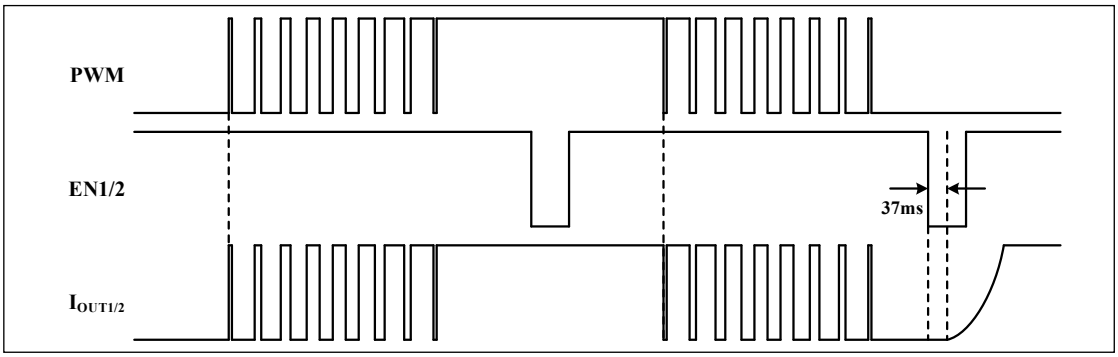


Figure 62 Priority Logic 3 of EN1/2 in Low Pulse Mode

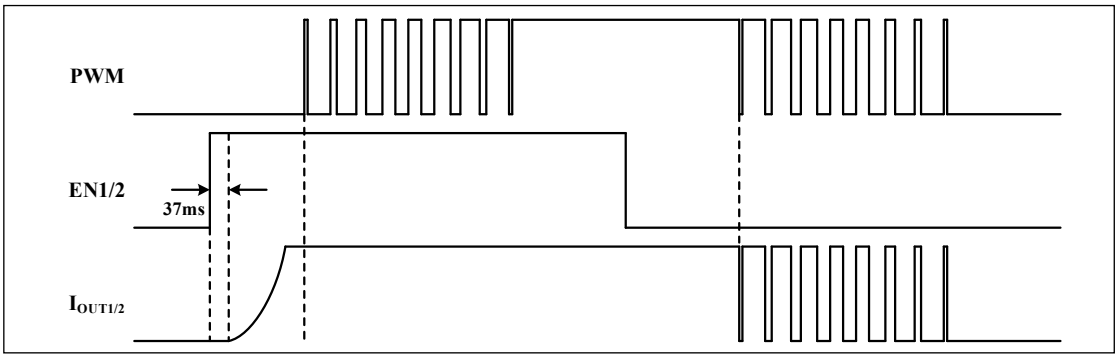


Figure 63 Priority Logic 1 of EN1/2 in Level Contro Mode

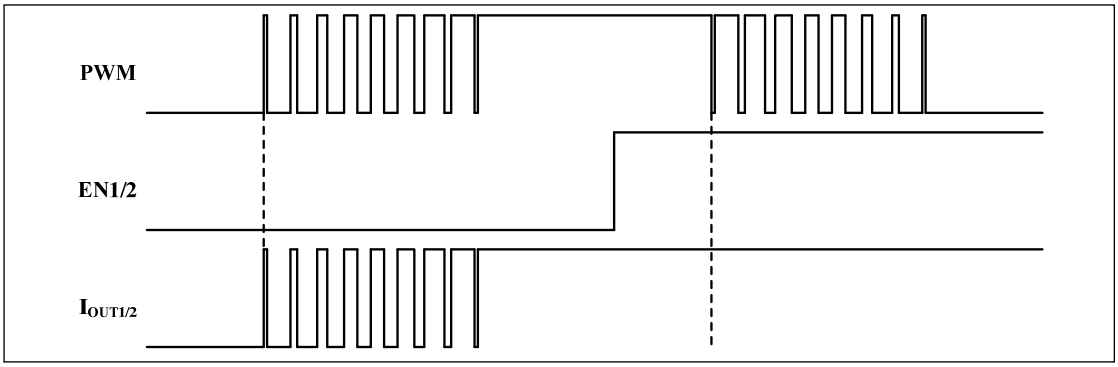


Figure 64 Priority Logic 2 of EN1/2 in Level Control Mode

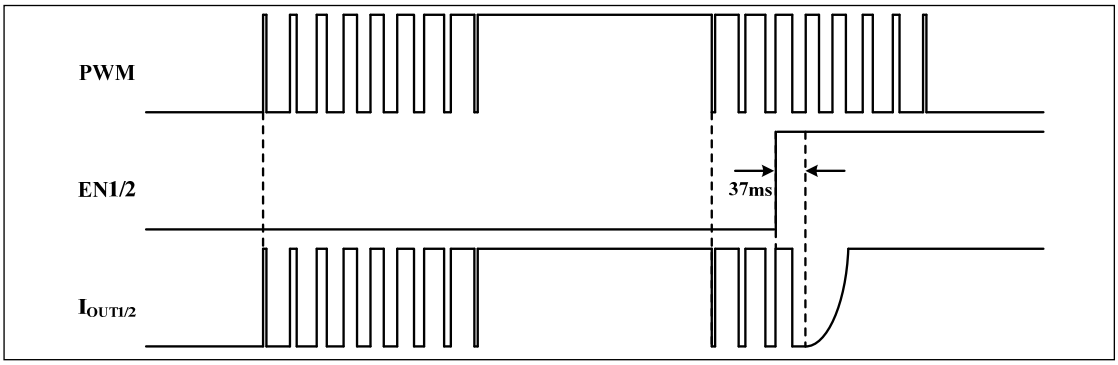


Figure 65 Priority Logic 3 of EN1/2 in Level Control Mode

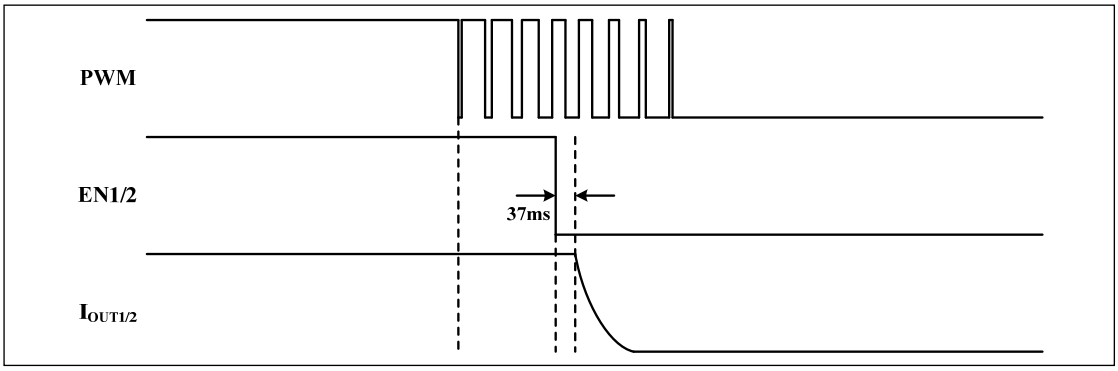


Figure 66 Priority Logic 4 of EN1/2 in Level Control Mode

UNDERVOLTAGE LOCKOUT

IS32LT3128A integrates an undervoltage lockout function to prevent mis-operation of the device during low input voltage conditions.

Should the VCC pin voltage fall below 4.5V (Typ.), the device will turn OFF the current source and maintain the EN latch status as long as the VCC pin voltage remains above 4.0V (Typ.). An external capacitor (Figure 67) is necessary to help maintain the VCC pin voltage > 4.0V (Typ.) and to supply current to the device status latch circuitry. However, should the voltage drop below 4.0V (Typ.), the internal latch will be reset to the power on default status (LED initial off state).

The current source will be turned ON when the input voltage is re-applied and the VCC pin rises above 4.6V (Typ.).

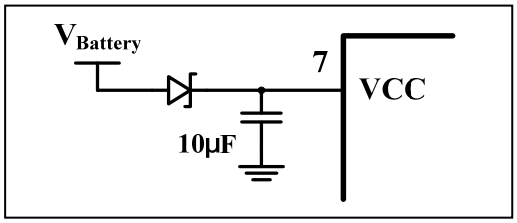


Figure 67 Capacitor For Latch Status

SETTING THE FADE TIME

The fade time is set by two external programming resistors; R_{TSET_UP} and R_{TSET_DN}. The R_{TSET_UP} connected to the TSET_UP pin configures the fade ramp ON time while the R_{TSET_DN} connected to the

TSET_DN pin configures the fade ramp OUT time. The fade time (ON or OFF) is programmable by Equation (6):

$$t \approx R_{TSET} \times 2.5\mu s \qquad (6)$$

For example, R_{TSET}=100kΩ, Fade ON/OFF time is about 0.25s.

Note: In order to get the optimized effect, the recommended fading time is between 1.5s (R_{TSET}= 600kΩ) and 0.25s (R_{TSET}= 100kΩ).

If either the TSET_UP or TSET_DN pin is tied directly to GND, the corresponding fade function is canceled and the ramp time is about 70μs, or 'instant on'. However, the debounce feature of the EN pin is not disabled.

GAMMA CORRECTION

In order to perform a better visual LED breathing effect we recommend using a gamma corrected value to set the LED intensity. This results in a reduced number of steps for the LED intensity setting, but causes the change in intensity to appear more linear to the human eye.

Gamma correction, also known as gamma compression or encoding, is used to encode linear luminance to match the non-linear characteristics of display. Gamma correction will vary the step size of the current such that the fading of the light appears linear to the human eye. Even though there may be 1000 linear steps for the fading algorithm, when gamma corrected, the actual number of steps could be as low as 63.

Table 2 63 Gamma Steps Correction

C(0)	C(1)	C(2)	C(3)	C(4)	C(5)	C(6)	C(7)
0	2	4	6	8	10	12	16
C(8)	C(9)	C(10)	C(11)	C(12)	C(13)	C(14)	C(15)
20	24	28	32	36	42	48	54
C(16)	C(17)	C(18)	C(19)	C(20)	C(21)	C(22)	C(23)
60	66	72	80	88	96	104	112
C(24)	C(25)	C(26)	C(27)	C(28)	C(29)	C(30)	C(31)
120	130	140	150	160	170	180	194
C(32)	C(33)	C(34)	C(35)	C(36)	C(37)	C(38)	C(39)
208	222	236	250	264	282	300	318
C(40)	C(41)	C(42)	C(43)	C(44)	C(45)	C(46)	C(47)
336	354	372	394	416	438	460	482
C(48)	C(49)	C(50)	C(51)	C(52)	C(53)	C(54)	C(55)
504	534	564	594	624	654	684	722
C(56)	C(57)	C(58)	C(59)	C(60)	C(61)	C(62)	
760	798	836	874	914	956	1000	

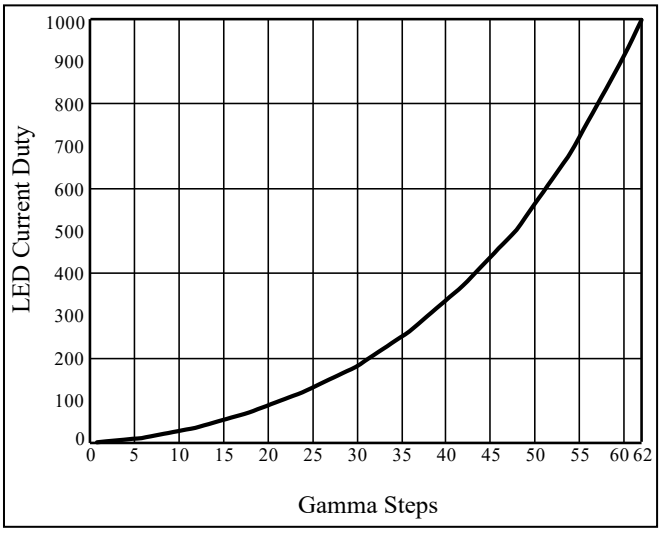


Figure 68 Gamma Correction (63 Steps)

FAULT DETECTION

An output shorted to GND fault is detected if the output voltage on a channel drops below the low voltage threshold V_{SCD} (Typical 1.8V) and remains below the threshold for t_{FD} (Typical 5ms). The channel (OUT1/2/3) with the short condition will reduce its output current to 4mA and FAULTB pin will pull low to report the fault condition. When the short condition is removed, the output current will recover to original value and FAULTB pin will recover to high impedance.

The FAULTB pin is an open drain structure. When a fault is asserted, the pin will change from high impedance to pull low state. If it is externally connected to a pull-up resistor, it will be at the pull-up voltage after fault is released.

When the ISET pin is shorted to GND and output current is larger than limit value, about 205mA for OUT1/2 and 40mA for OUT3, the output current will be clamped. Once the short fault condition is removed, the output current will recover to its original value.

OVER TEMPERATURE PROTECTION

The device features an integrated thermal rollback feature which will reduce the output current in a linear fashion if the silicon temperature exceeds 145°C (typical). In the event that the die temperature continues to increase, the device will enter thermal shutdown if the temperature exceeds 175°C.

THERMAL ROLLOFF

The output current will be equal to the set value as long as the die temperature of the IC remains below 145°C (Typical). If the die temperature exceeds this threshold, the output current of the device will begin to reduce at a rate of 3.8%/°C until 5% of I_{OUT} and turn off after this current level.

THERMAL SHUTDOWN

In the event that the die temperature exceeds 175°C, the output channel will go to the 'OFF' state and

FAULTB pin will pull low to report the fault condition. At this point, the IC presumably begins to cool off. Any attempt to toggle the channel back to the source condition before the IC cooled to < 145°C will be blocked and the IC will not be allowed to restart, and FAULTB pin will recover to high impedance.

THERMAL CONSIDERATIONS

The package thermal resistance, θ_{JA}, determines the amount of heat that can pass from the silicon die to the surrounding ambient environment. The θ_{JA} is a measure of the temperature rise created by power dissipation and is usually measured in degree Celsius per watt (°C/W). The junction temperature, T_J, can be calculated by the rise of the silicon temperature, ΔT, the power dissipation, P_D, and the package thermal resistance, θ_{JA}, as in Equation (7) and (8):

$$P_D = V_{CC} \times I_{CC} + \sum_{x=1}^{3} (V_{CC} - V_{LEDx}) \times I_{OUTx} \quad (7)$$

and,

$$T_J = T_A + \Delta T = T_A + P_D \times \theta_{JA} \quad (8)$$

Where I_{CC} is the IC quiescent current, V_{CC} is the supply voltage, V_{LEDx} is the voltage across VCC to OUTx, I_{OUTx} is the output current of OUTx pin and T_A is the ambient temperature.

When operating the chip at high ambient temperatures, or when driving maximum load current, care must be taken to avoid exceeding the package power dissipation limits. The maximum power dissipation can be calculated using the following Equation (9):

$$P_D < P_{D(MAX)} = \frac{125°C - 25°C}{\theta_{JA}} \quad (9)$$

So,

$$P_D < \frac{125°C - 25°C}{34°C/W} \approx 2.94W$$

The ensured operation temperature range is -40˚C to 125˚C. Please make sure that the junction temperature of the normal operation doesn't exceed 125˚C. Figure 69, shows the power derating of the IS32LT3128A on a JEDEC board (in accordance with JESD 51-5 and JESD 51-7) standing in still air. The power dissipation below solid line is safe area.

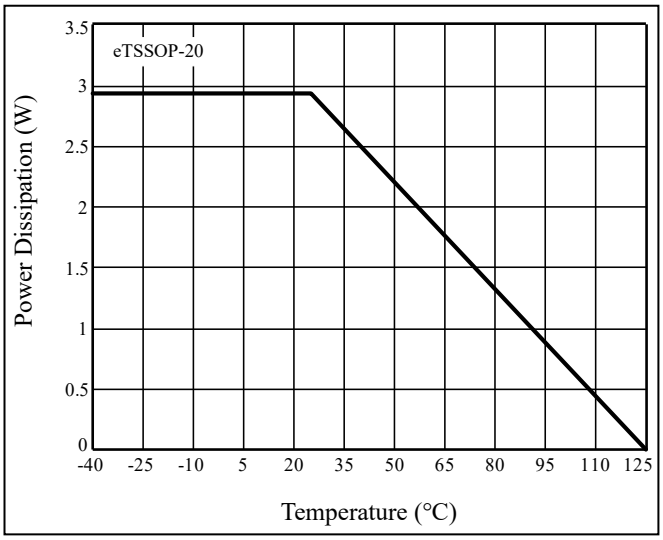


Figure 69 Dissipation Curve

The thermal resistance is achieved by mounting the IS32LT3128A on a standard FR4 double-sided printed circuit board (PCB) with a copper area of a few square inches on each side of the board under the IS32LT3128A. Multiple thermal vias, as shown in Figure 70, help to conduct the heat from the exposed pad of the IS32LT3128A to the copper on each side of the board. The thermal resistance can be reduced by using a metal substrate or by adding a heatsink or thicker copper plane.

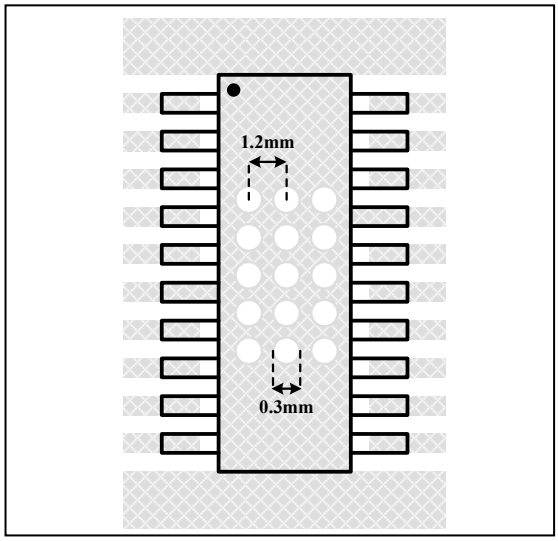


Figure 70 Board Via Layout For Thermal Dissipation

EMI AT THE CABLE AND INTERCONNECT LEVEL

Vehicle electronics can be affected by electromagnetic interference (EMI) caused by "stray" magnetic and electric fields from automotive inductive load switching. Running throughout the vehicle are wiring harnesses which behave as "hidden antennas" and pickup these harmonic frequencies.

Because the IS32LT3128A is usually connected with a long wire to the vehicle's central computer, it could be susceptible to EMI transients. For example, a coupled EMI transient on the wiring harness connected to the

IS32LT3128A's PWM pin can be passed through and cause a slight LED flicker.

To avoid this, an RC low-pass filter can be implemented to attenuate high frequency signals at the PWM pin. The low-pass filter will allow only low frequency signals from 0Hz to its cut-off frequency (fc) to pass while attenuating frequencies above this cut-off frequency.

The formula to calculate the cut-off frequency of an RC filter is:

$$f_C = \frac{1}{2\pi \times R_{PWM} \times C_{PWM}} \qquad (10)$$

As shown in Figure 71, typical values for R_{PWM}=10kΩ and C_{PWM}=3.3nF. For the IS32LT3128A the value of R_{PWM} is fixed at 10kΩ (must always be installed) while C_{PWM} is optional and its value can vary depending on the vehicle's EMI environment.

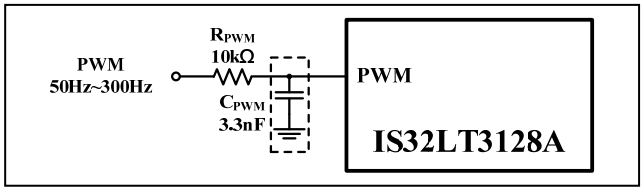


Figure 71 RC filter for PWM EMI

$$f_C = \frac{1}{2\pi \times 10k\Omega \times 3.3nF} \approx 4.7kHz$$

Frequencies above 4.7kHz will be attenuated while frequencies below 4.7kHz will pass through without attenuation.

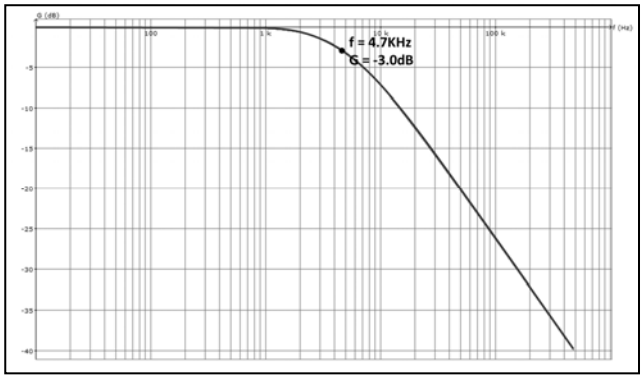


Figure 72 Low-Pass Filter Gain-Magnitude Frequency Response

CLASSIFICATION REFLOW PROFILES

Profile Feature	Pb-Free Assembly
Preheat & Soak Temperature min (Tsmin) Temperature max (Tsmax) Time (Tsmin to Tsmax) (ts)	150°C 200°C 60-120 seconds
Average ramp-up rate (Tsmax to Tp)	3°C/second max.
Liquidous temperature (TL) Time at liquidous (tL)	217°C 60-150 seconds
Peak package body temperature (Tp)*	Max 260°C
Time (tp)** within 5°C of the specified classification temperature (Tc)	Max 30 seconds
Average ramp-down rate (Tp to Tsmax)	6°C/second max.
Time 25°C to peak temperature	8 minutes max.

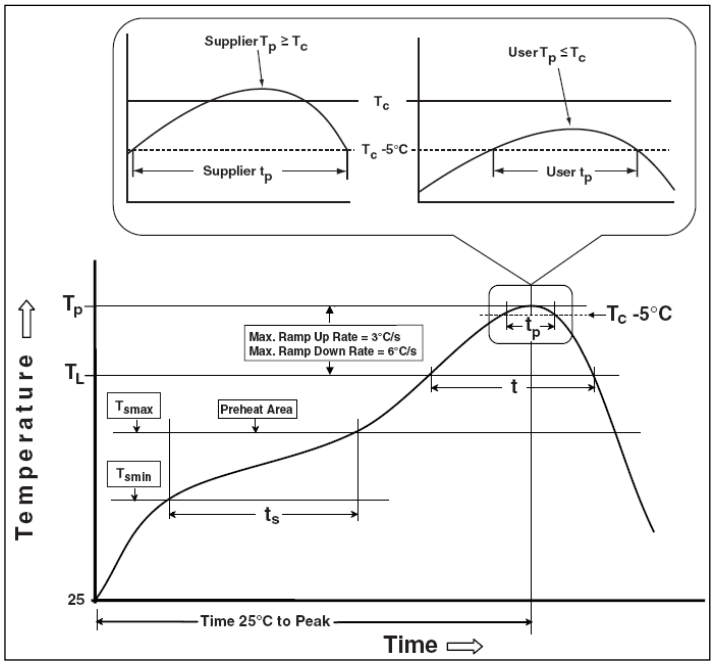
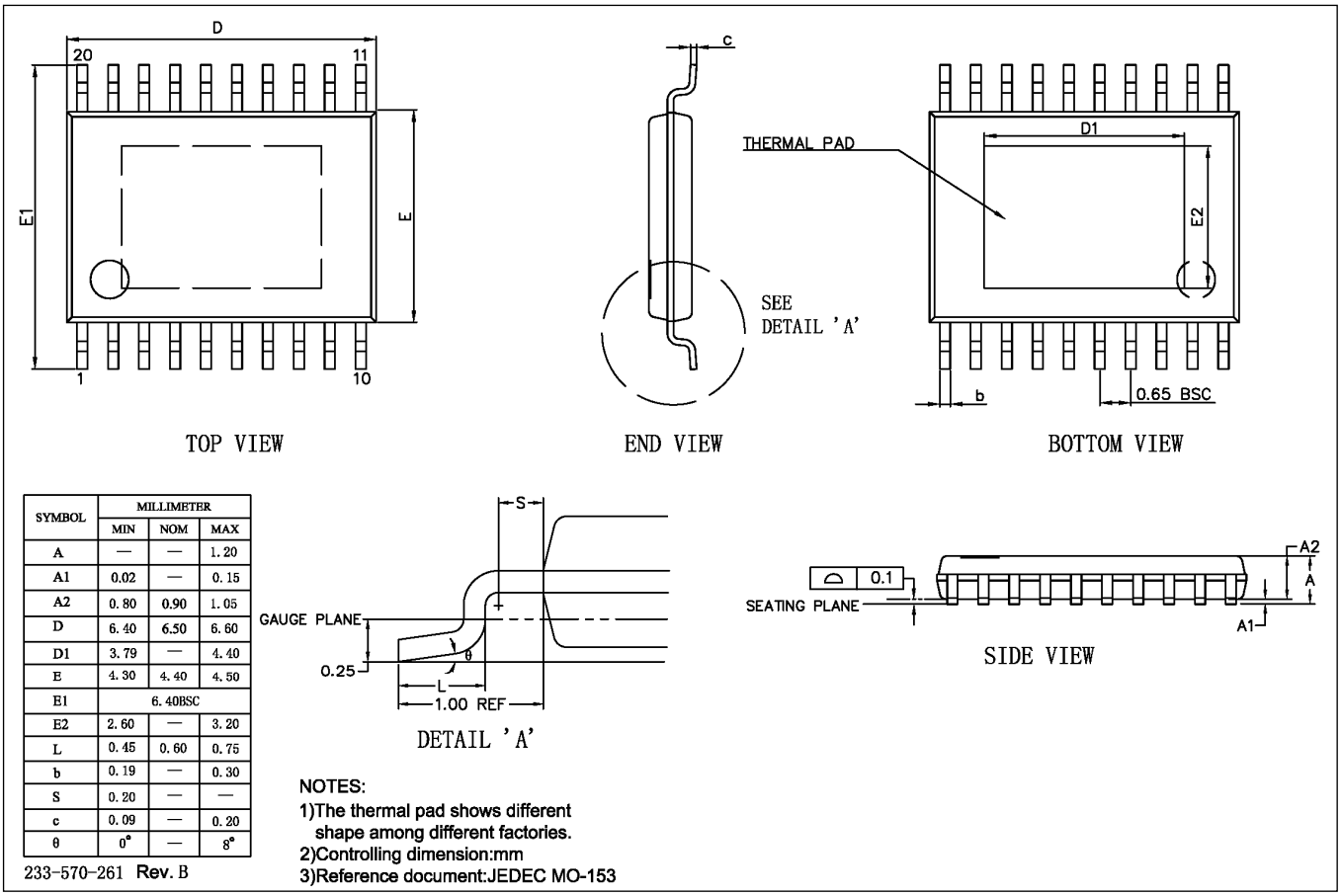


Figure 73 Classification Profile

PACKAGE INFORMATION

eTSSOP-20

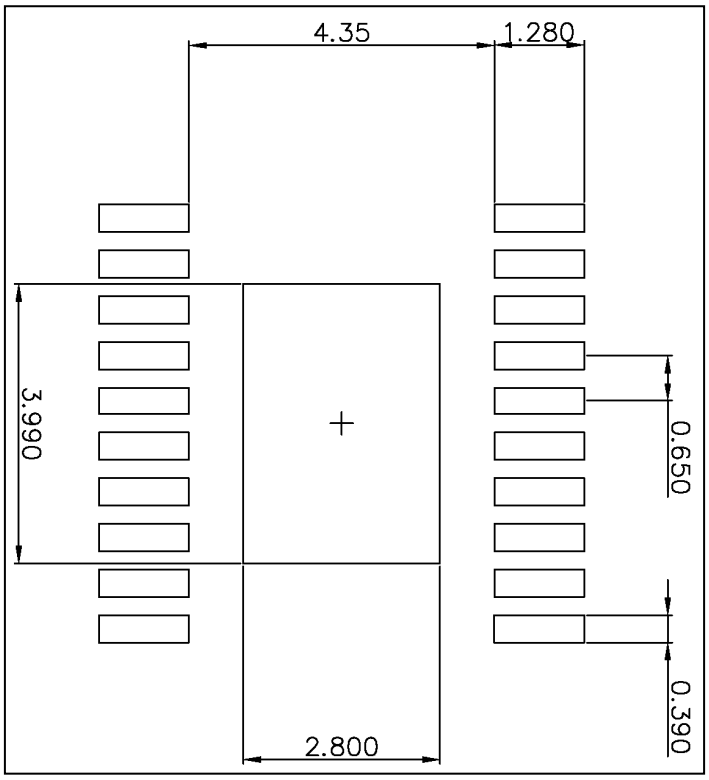


SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.20
A1	0.02	—	0.15
A2	0.80	0.90	1.05
D	6.40	6.50	6.60
D1	3.79	—	4.40
E	4.30	4.40	4.50
E1	6.40BSC		
E2	2.60	—	3.20
L	0.45	0.60	0.75
b	0.19	—	0.30
S	0.20	—	—
c	0.09	—	0.20
θ	0°	—	8°

233-570-261 Rev. B

NOTES:
1)The thermal pad shows different shape among different factories.
2)Controlling dimension:mm
3)Reference document:JEDEC MO-153

RECOMMENDED LAND PATTERN



Note:

1. Land pattern complies to IPC-7351.
2. All dimensions in MM.
3. This document (including dimensions, notes & specs) is a recommendation based on typical circuit board manufacturing parameters. Since land pattern design depends on many factors unknown (eg. User's board manufacturing specs), user must determine suitability for use.

REVISION HISTORY

Revision	Detail Information	Date
0A	Initial release.	2018.08.22
A	1. Update EC and curves 2. Update P_{DMAX} value and figure 69, 70.	2019.05.06
B	Correct mistake in Figure 60~63 and update POD	2021.12.08