IS32LT3134

12-CHANNEL LED ANIMATION CONTROLLER

July 2022

GENERAL DESCRIPTION

IS32LT3134 is a 12-channel LED driver with an embedded animation controller. Multiple IS32LT3134 devices can be cascaded in the same board design. Four animation patterns and pin-select information can be stored in the embedded Flash of each device. The patterns are played by a host which controls the input pins of the devices. For each pattern, two modes can be pre-defined: cascade mode(one device after another) and synchronous mode(all devices simultaneously).

IS32LT3134 can support a GUI on Windows PC for the design and playback of the animation patterns when connected to the Lumissil evaluation board or the customer's design board with IS32LT3134. An In-System-Programming ("ISP") mode is supported for programming patterns into the individual device when the ISP pin is asserted. GUI also provides a tool to automatically detect the device's related position of connection and assign the device's address when more than one IS32LT3134 device is on the same board.

A watchdog timer is used to check if the animation reaches the end of the pattern in the anticipated time when there is no fault generated. In addition, a short circuit condition of the LED output might be detected. If any of the above fails occurs, the Fault pin will be asserted. There are two options under the fault condition: " One fails All Stop." or " One Fails Others Continue". The former would stop animation on all devices while the latter stops only the animation of the defective IS32LT3431.

IS32LT3134 is available in WQFN-24 package. It operates from 3.0V to 5.5V over the temperature range of -40°C to +125°C.

FEATURES

- Supply voltage range: 3.0V to 5.5V
- UART interface operates at 19.2K baud rate and supports dynamic addressing mode
- 12-channel push-pull output driver for the common anode, common cathode, or multiplexed LED drive modes
- Duration of animation is from 0.1s to 15s
- User programmable internal clock pre-scalar
- Four pattern banks with 12KB Flash each
- Watchdog timer monitors valid clock signals and end of animation pattern. A fault is asserted when errors are detected by the WDT
- Animation-end pin signals the end of a synchronous pattern for all devices, a start of animation of the next cascading device, or the end of cascading pattern if it's asserted by the last device in the row.
- Support programmable duty cycle for dimming
- Programmable clock frequency by deriving from 16MHz internal oscillator
- Clock input for external clock option
- Wettable flank QFN-24 (WQFN-24) package with RoHS compliant
- AEC-Q100 qualification

APPLICATIONS

- Tail light animation module with digital interface
- Interior light animation module with digital interface

TYPICAL APPLICATION CIRCUIT

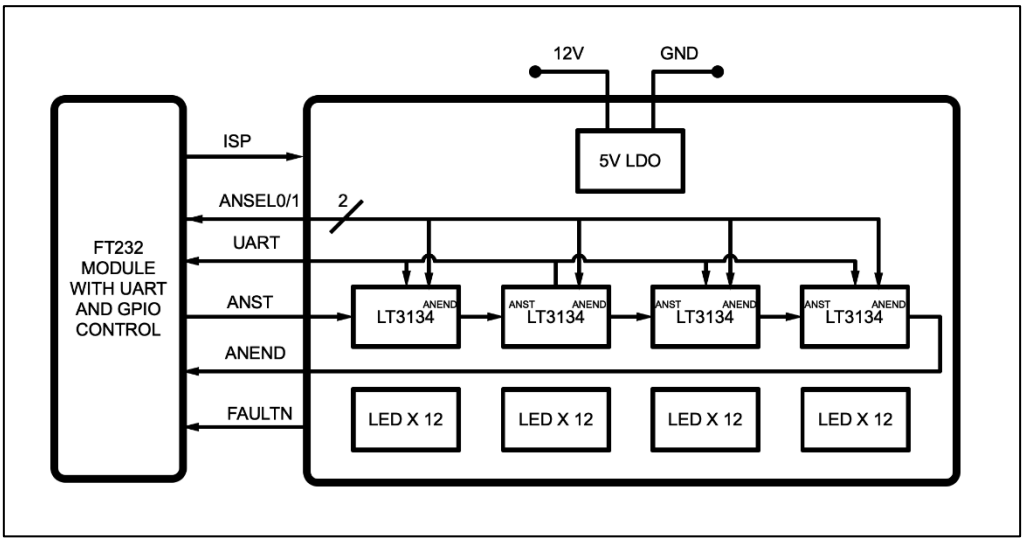
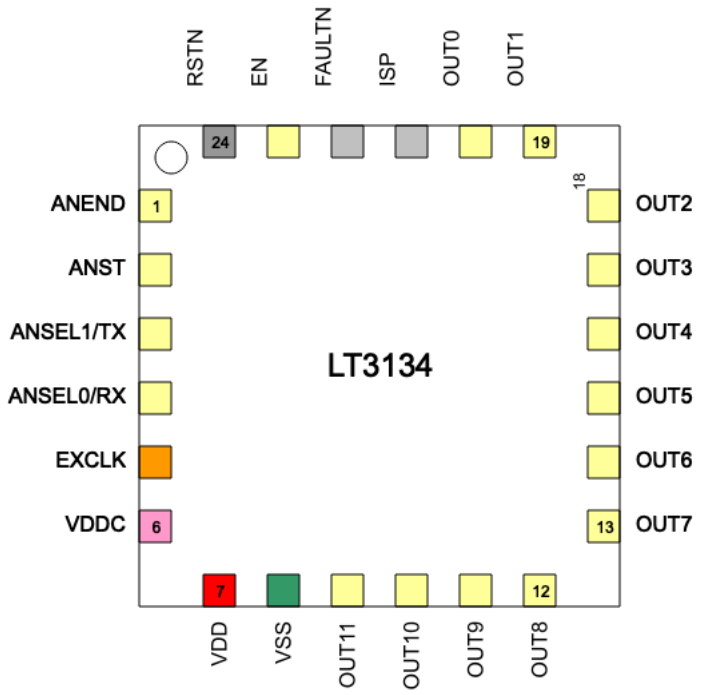


Figure 1. Typical Application Circuit: four LT3134 cascaded for control of 48 LEDs

Note 1: IC should be placed far away from the antenna in order to prevent the EMI.

PINOUT

	Pin Configuration (Top View)
WQFN-24	

PIN DESCRIPTION

No.	Pin	Description
1	ANEND	ANEND = 1, when animation reaches the end
2	ANST	ANST = 1, start animation with the selected pattern
3	ANSEL1/TX	Pattern selection pin; also serve as ISP UART TX.
4	ANSEL 0/RX	Pattern selection pin; also serve as ISP UART RX.
5	EXCLK	External input of pattern clock: 100 Hz – 400 Hz
6	VDDC	1.5V internal regulator output; 0.1uF and 1uF capacitors connected to VSS are required
7	VDD	Input voltage: 3.0V – 5.5V
8	VSS	Ground
9-20	OUT0 – OUT11	Push-pull outputs for driving LEDs
21	ISP	ISP = 1, enter ISP mode with ANSEL0=RX, ANSEL1=TX
22	FAULTN	Open drain I/O; asserted when errors are detected
23	EN	EN = 0, enters low power mode
24	RSTN	Reset with an on-chip pull-up resistor

ORDERING INFORMATION

Industrial Range: -40°C to +125°C

Order Part No.	Package	QTY/Reel
IS32LT3134-QWLA3-TR	Wettable Flank QFN-24, Lead-free	2500

Copyright © 2022 Lumissil Microsystems. All rights reserved. Lumissil Microsystems reserves the right to make changes to this specification and its products at any time without notice. Lumissil Microsystems assumes no liability arising out of the application or use of any information, products or services described herein. Customers are advised to obtain the latest version of this device specification before relying on any published information and before placing orders for products.

Lumissil Microsystems does not recommend the use of any of its products in life support applications where the failure or malfunction of the product can reasonably be expected to cause failure of the life support system or to significantly affect its safety or effectiveness. Products are not authorized for use in such applications unless Lumissil Microsystems receives written assurance to its satisfaction, that:

a.) the risk of injury or damage has been minimized;

b.) the user assumes all such risks; and

c.) potential liability of Lumissil Microsystems is adequately protected under the circumstances.

ABSOLUTE MAXIMUM RATINGS

Supply voltage, V_{DD}	-0.3V ~+6.0V
Voltage at any input pin	-0.3V ~ V_{DD}+0.3V
Maximum junction temperature, T_{JMAX}	+150°C
Storage temperature range, T_{STG}	-65°C ~+150°C
Operating temperature range, T_A=T_J	-40°C ~ +125°C
Package thermal resistance, junction to ambient (4 layer standard test PCB based on JESD 51-2A), θ_{JA}	29°C/W
ESD (HBM) ESD (CDM)	±2kV ±750V

Note 2:

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

The following specifications apply for VDD= 5V, TA= 25°C, unless otherwise noted.

Output Logic Electrical Characteristics (ANEND, FAULTN)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Supply voltage		3.0		5.5	V
I_{SD}	Shutdown current			1		uA
I_{OL}	Logic “0” sink current	(Note 3)		10		mA
I_{OH}	Logic “1” source current	(Note 3)		4		mA
V_{OL}	OUT0-OUT11	(Note 4)		0.5		V
V_{OH}	OUT0-OUT11	(Note 4)		V_{DD}-0.5		V
Input Logic Electrical Characteristics (ANST, ANSEL0/1)						
V_{IL}	Logic “0” input voltage		GND		0.2V_{DD}	V
V_{IH}	Logic “1” input voltage		0.75V_{DD}		V_{DD}	V
V_{HYS}	Input Schmitt trigger hysteresis			0.1		V
I_{IL}	Logic “0” input current	(Note 4)		5		nA
I_{IH}	Logic “1” input current	(Note 4)		5		nA

Note 3: Guaranteed by design.

Total I/O sink and source currents are within ±100mA.

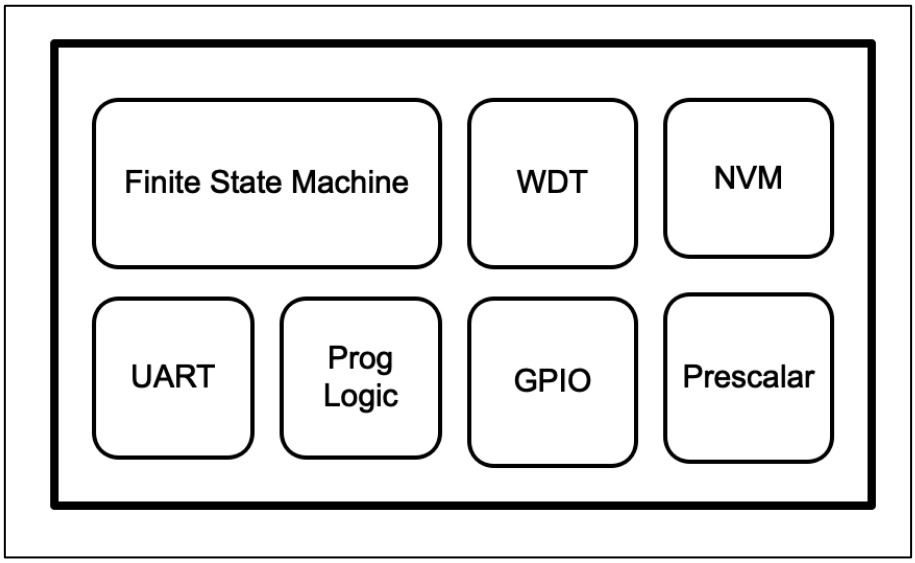
Note 4: Guaranteed by design.

DIGITAL INPUT UART SWITCHING CHARACTERISTICS

Symbol	Parameter	Fast Mode			Units
		Min.	Typ.	Max.	
f_{SCL}	Serial-clock frequency	-		19.2	kHz
t_R	Rise time of signals (Note 5)	-	10		us
t_F	Fall time of signals (Note 5)	-	10		us

Note 5: Guaranteed by design

FUNCTIONAL BLOCK DIAGRAM



DETAILED DESCRIPTION

UART INTERFACE

IS32LT3134 uses a UART-based serial bus. Each frame contains a start byte, a synchronous byte, a command byte, an address byte, data bytes, and a checksum byte. Each byte has one start bit, eight data bits, and one stop bit without parity. The LSB follows the start bit as follows:

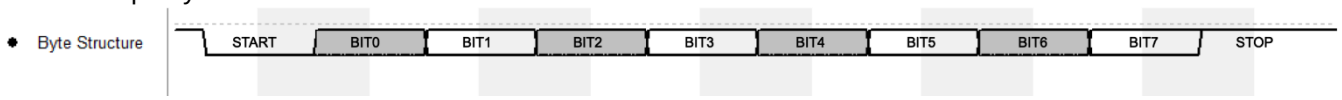


Figure 2. Byte structure

Slave address position detection (SAPD) can be achieved by the bus command cascading method (BCCM).

Once a slave device receives a communication frame, it first verifies the checksum. If the checksum is correct, the slave replies with an acknowledgment. If the communication frame is longer than the timeout timer (1.5 times of a frame period), the slave will reset and wait for the next synchronization on a new frame. If the communication fails, the master cannot receive feedback from the slave. The master should wait for a timeout timer before retransmission and the slave should clear its receiving buffer.

Both write or readback supports burst mode. Figure 3 and Figure 4 show Frame Structure.

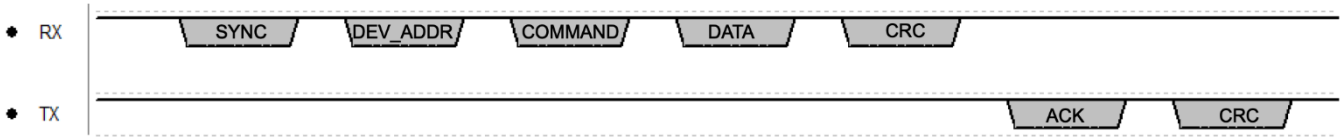


Figure 3. Write command with ACK feedback

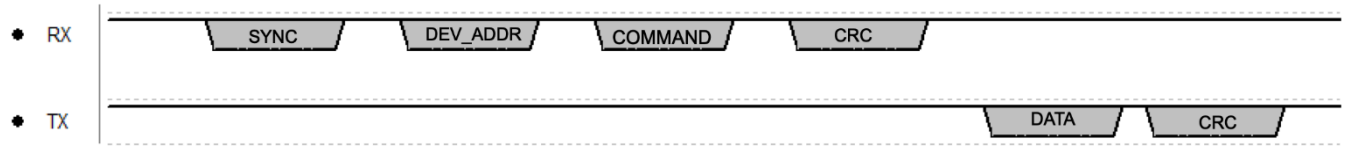


Figure 4. Read command with ACK feedback

Table 1. Frame Structure:

Byte Name	Length	Description
SYNC	1	Synchronization byte sent from Master
DEV_ADDR	1	Device address, Read/Write Command, Burst mode
COMMAND	1	Device configuration, Pattern configuration
DATA	0, 2, 8, 256	Data byte
ACK	1	Acknowledge, reply ID number
CRC	1	CRC for Dev_Add and all Data

SYNC

SYNC byte value is 0x55. The first byte is a frame header. It can be a synchronization signal that comes from the master. Based on the signal, slaves can adjust internal UART clock automatically.

Table 2. Description of DEV_ADD byte

Bit.	Field	Description
3-0	Device address	LT3134 protocol can define maximum of 16 slave devices
5-4	Data Length	00: single byte command with 0 bytes of data 01: single byte command with 2 bytes of data 10: burst mode with 8 bytes of data 11: burst mode with 256 bytes of data
6	Broadcast	Single device = 0; Broadcast = 1
7	Read/Write	Read = 0; Write = 1

Table 3. UART Commands

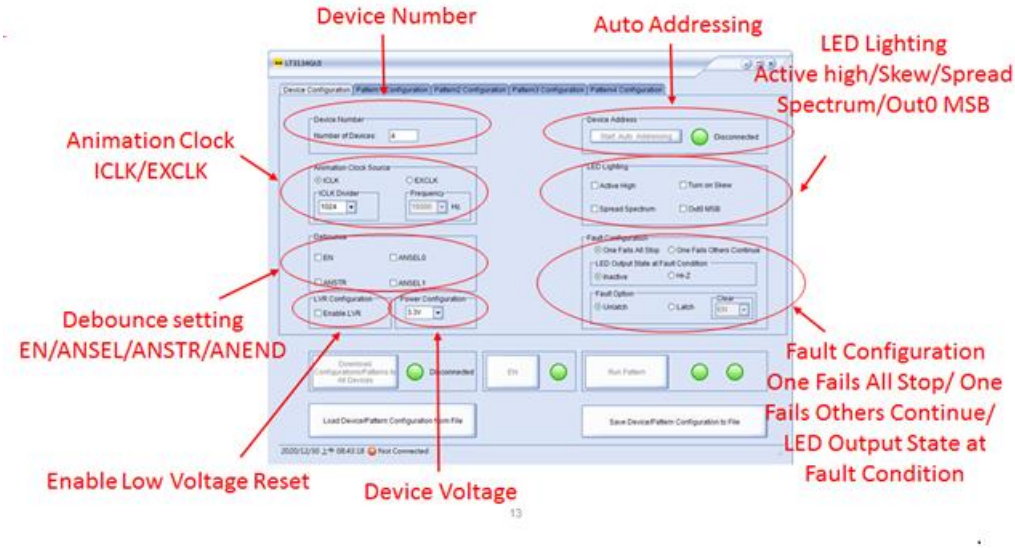
Command No.	Bit 3	Bit 2	Bit 1	Bit 0	Description
	CMD[3]	CMD[2]	CMD[1]	CMD[0]	
0	0	0	0	0	SAPD-RESET
1	0	0	0	1	SAPD
2	0	0	1	0	SAPD-END
3	0	0	1	1	ISP IFB FF
4	0	1	0	0	ISP IFB CF
5	0	1	0	1	ISP FF
6	0	1	1	0	ISP CF
7	0	1	1	1	MCU Part Number
8	1	0	0	0	Firmware version

Bits 7 – 4 of UART command are all 0.

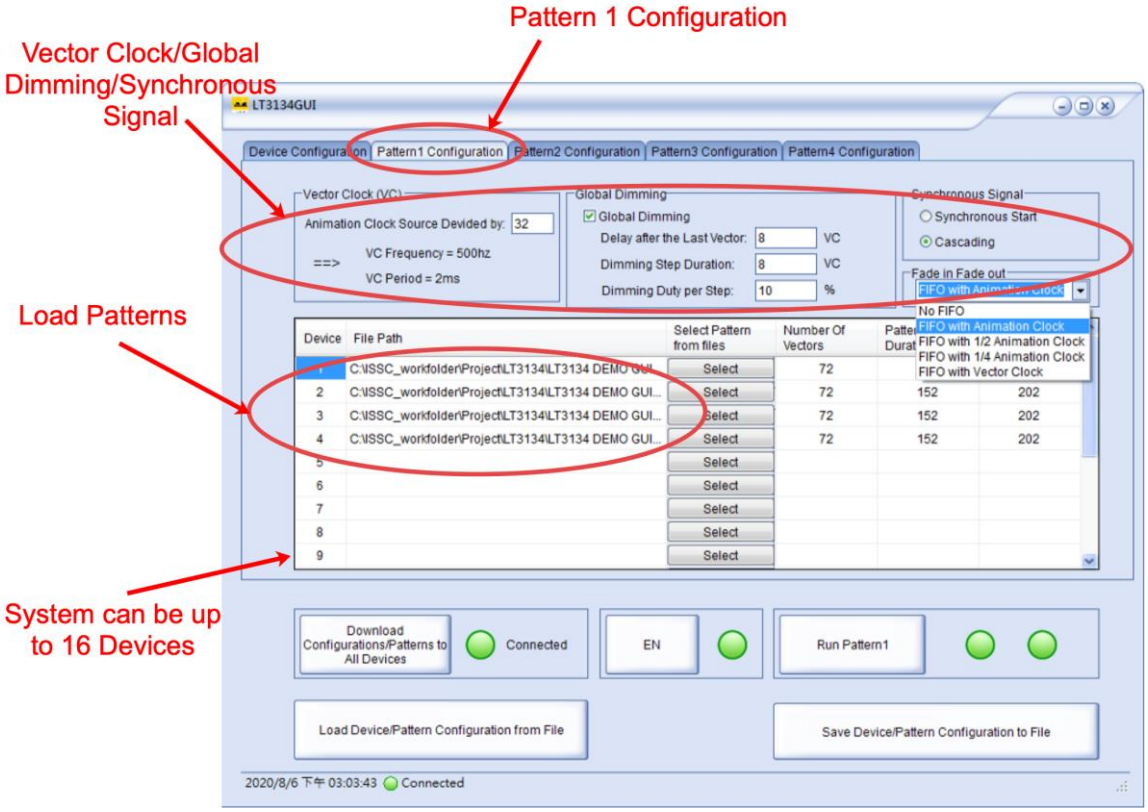
GUI Features

- Animation Clock Source
  - ICLK(16000khz)
  - EXCLK(1khz)
- Debounce setting for EN/ANSEL/ANST/ANEND
  - Debounce time 530usec
- LED Lighting
  - Active High: When on/off bit of Pattern bit[11-0] is 1, push-pull is driven to the high level, and vice versa.
  - Turn on Skew:
  - Spread Spectrum Enable: Spread spectrum frequency range.
  - Out0 MSB: Push-Pull output port 0 to port 11 starting with Pattern bit[11-0] MSB.
- Fault Configuration
  - One fails All Stop/One Fails Others Continue
  - LED status at Fault condition
  - Inactive/Hi-Z
- Vector Clock
  - Programmable clock divider
- Global dimming at end of animation
  - Delay after the last Vector
  - Dimming step Duration
  - Dimming Duty per step
- Synchronous Signal
  - Synchronous
  - Cascading

GUI Device Configuration



GUI Patterns Configuration



CLASSIFICATION REFLOW PROFILES

Profile Feature	Pb-Free Assembly
Preheat & Soak Temperature min (Tsmin) Temperature max (Tsmax) Time (Tsmin to Tsmax) (ts)	150°C 200°C 60-120 seconds
Average ramp-up rate (Tsmax to Tp)	3°C/second max.
Liquidous temperature (TL) Time at liquidous (tL)	217°C 60-150 seconds
Peak package body temperature (Tp)*	Max 260°C
Time (tp)** within 5°C of the specified classification temperature (Tc)	Max 30 seconds
Average ramp-down rate (Tp to Tsmax)	6°C/second max.
Time 25°C to peak temperature	8 minutes max.

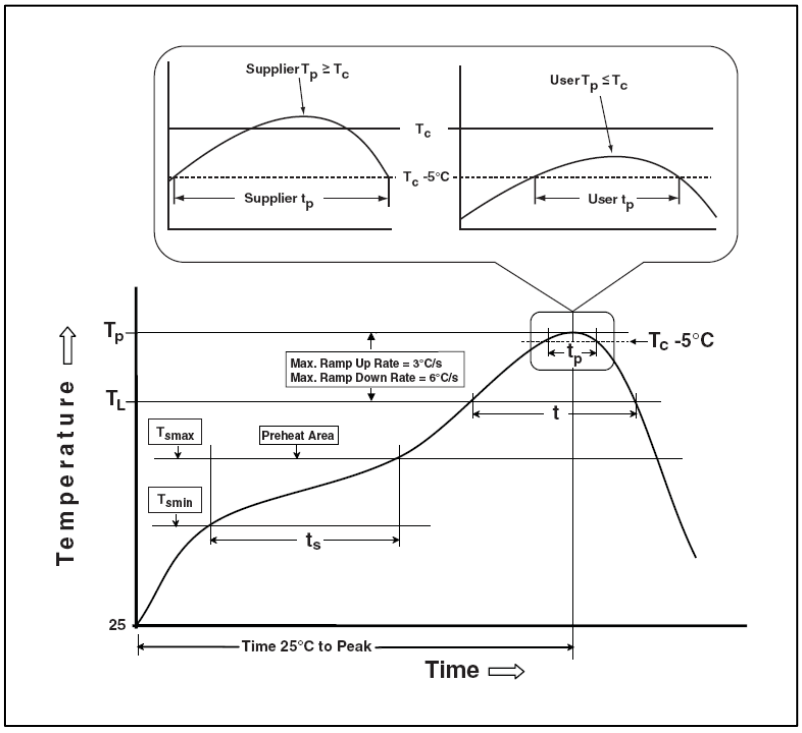
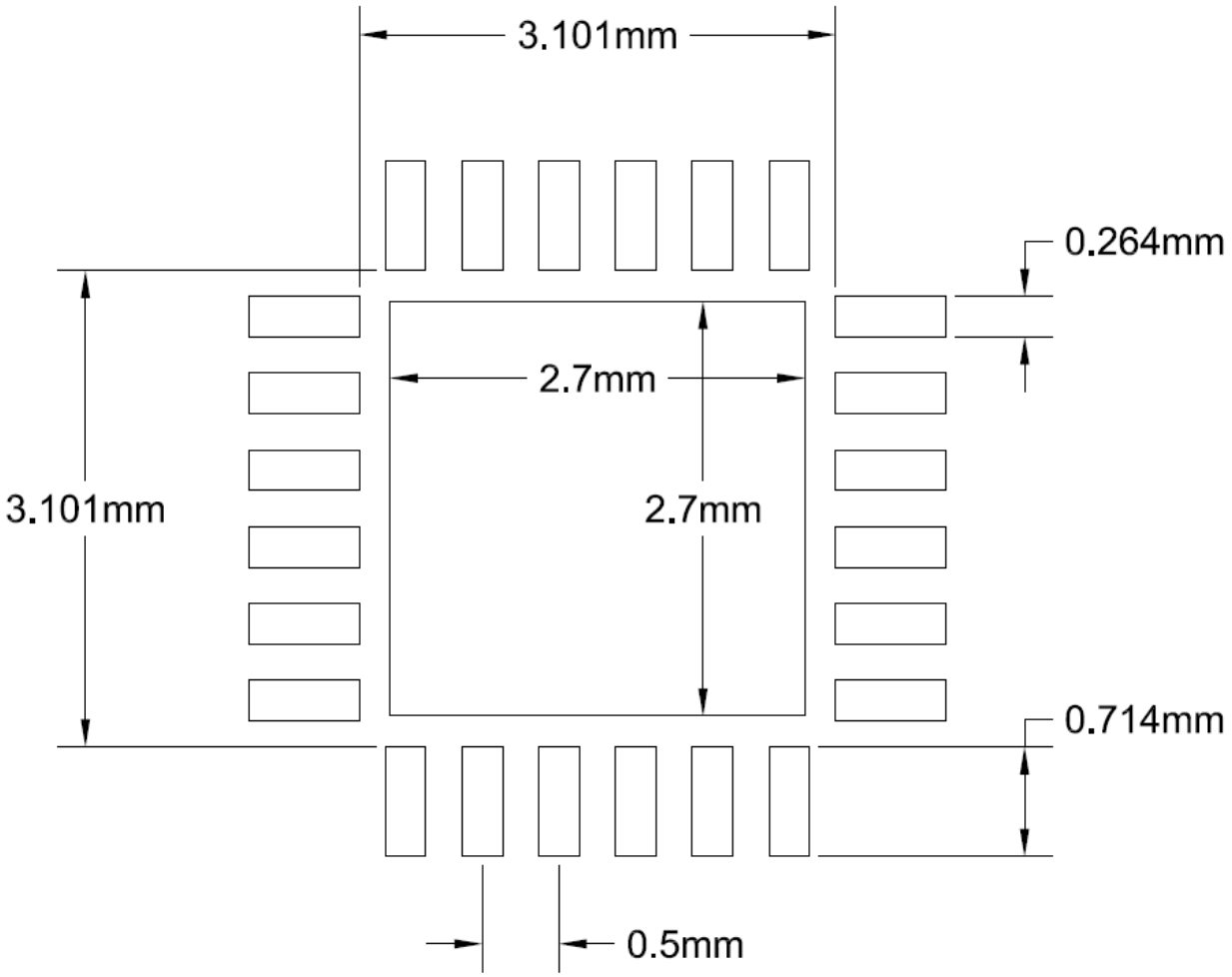


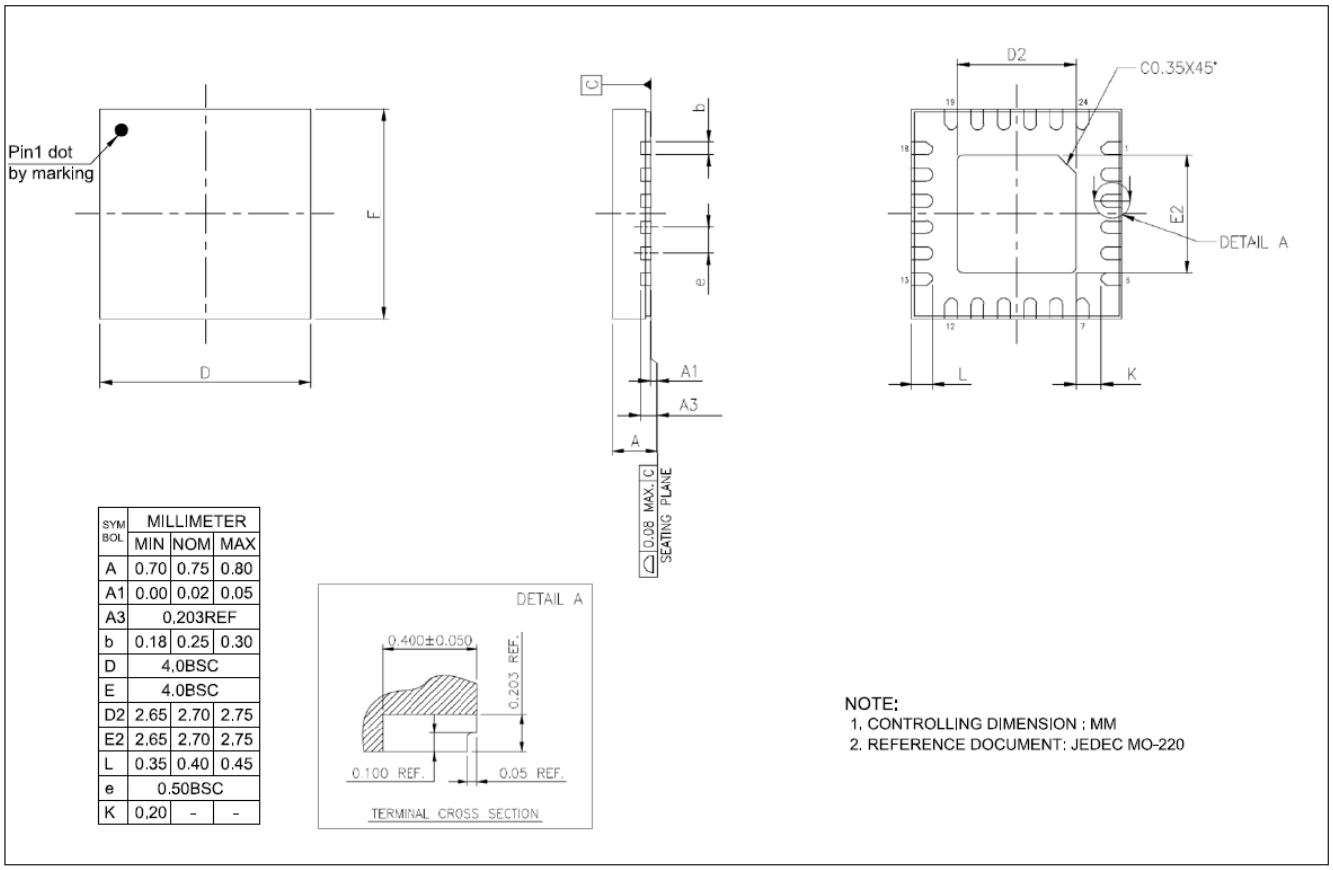
Figure 5. Classification Profile

PACKAGE INFORMATION

Wettable Flank QFN-24
RECOMMENDED LAND PATTERN



POD



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3	0,203REF		
b	0.18	0.25	0.30
D	4,0BSC		
E	4.0BSC		
D2	2.65	2.70	2.75
E2	2.65	2.70	2.75
L	0.35	0.40	0.45
e	0.50BSC		
K	0.20	-	-

NOTE:
1. CONTROLLING DIMENSION : MM
2. REFERENCE DOCUMENT: JEDEC MO-220

REVISION HISTORY

Revision	Detailed Information	Date
0A	Initial Version	2021.02.01
A	First Formal Release	2021.06.08
B	1. Add AEC-Q100 support 2. Rename IS32LT31314 package name from WFQFN-24 to WQFN-24 3. Update WQFN-24 land pattern and POD information 4. Update Input/Output Logic Electrical Characteristics The above description is from ELECTRICAL CHARACTERISTICS 5. Update timing for UART switching characteristics The above description is from DIGITAL INPUT UART SWITCHING CHARACTERISTICS	2022.07.06