# IS32LT3140B

## SINGLE CHANNEL 450mA LED DRIVER WITH THERMAL SHUNT RESISTOR

**August 2021**

### GENERAL DESCRIPTION

The IS32LT3140B is an automotive-grade high-side programmable current regulator consisting of a single output channel capable of 450mA. An external resistor sets the current level for the single-channel current source. An optional thermal shunt resistor can be used to significantly optimize IC power dissipation. It features an EN pin to enable or shutdown the device. It supports either PWM dimming via a PWM pin or power supply modulation (PSM). A resistor divider circuit can be used on the UV pin to set an external VCC under-voltage lockout threshold for LED string open fault detection. In addition, the IS32LT3140B integrates fault protection for LED string open/short, output overcurrent (not reported), and over-temperature condition for robust operation. Detection of these failures is reported by the FAULTB pin. When a fault is detected the device will disable itself and output an active low open drain signal. Multiple devices can have their FAULTB pins connected to create a “one-fail-all-fail” condition.

The IS32LT3140B is targeted at the automotive market with end applications to include interior and exterior lighting. For 12V automotive applications, the low dropout driver can support one to several LEDs on the output channel. The device is offered in a small thermally enhanced SOP-8-EP package.

### FEATURES

- Wide input voltage range, 4.5V to 40V
- Single-channel sources up to 450mA
- High-side external resister sets source current
- ±8% current accuracy over -40°C ~ +150°C
- Low headroom voltage, max 700mV at 150mA
- Low operating current of 350μA and 5μA in shutdown
- Optional thermal shunt resistor to optimize IC power dissipation
- Support for both PWM or PSM dimming
- Programmable VIN under-voltage lockout at PWM pin
- Fault protection with open-drain flag output:
  - LED string open/short
  - Output overcurrent (not reported)
  - Thermal shutdown
- Shared fault flag for multiple device operation to comply with “one-fail-all-fail” function
- AEC-Q100 Qualified
- Operating temperature range from -40°C ~ +150°C

### APPLICATIONS

- Automotive interior/exterior lighting:
  - Turn signal light
  - Rear lamp
  - Dome light

### TYPICAL APPLICATION CIRCUIT

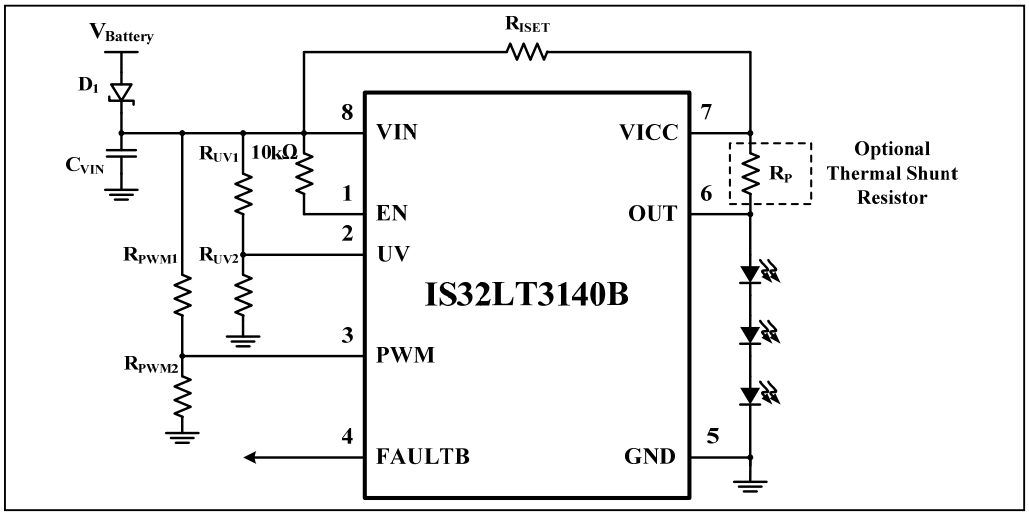



**Figure 1** Typical Application Circuit (PSM Dimming Or Non-Dimming Applications)

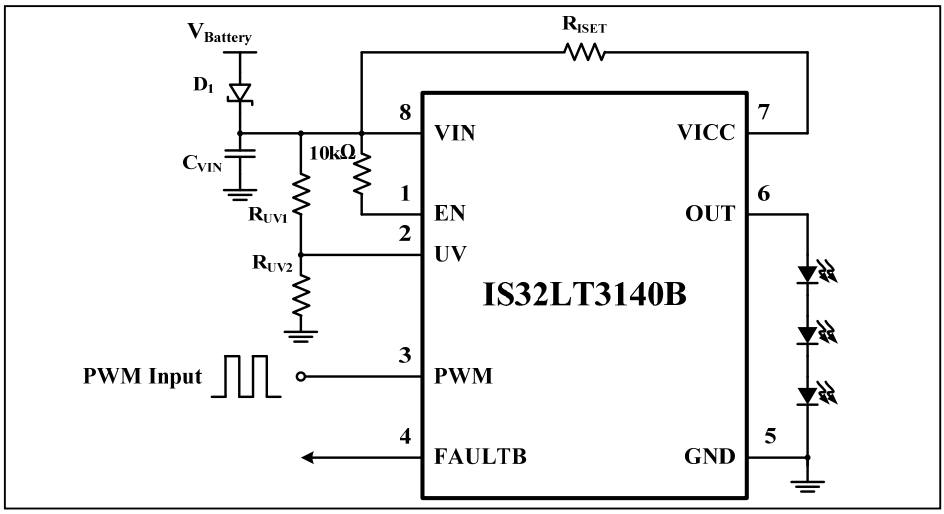


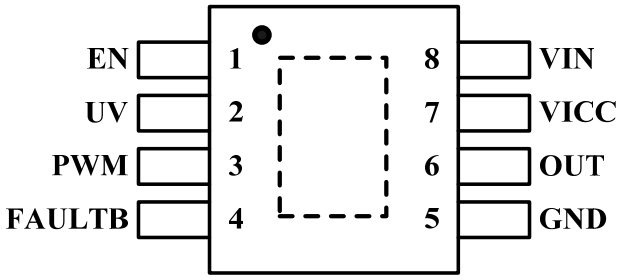

**Figure 2** Typical Application Circuit with PWM Dimming

**Note 1:** For PSM dimming application, a high $C_{VIN}$ capacitor value will affect the dimming accuracy. To get better dimming performance, recommend a value of 0.1μF. If no PSM dimming requirement, $C_{VIN}$ can be a larger value.

**Note 2:** The thermal shunt resistor $R_P$ is only available for applications without EN shutdown, PWM dimming or “one fail all fail” mode fault protection.

**Note 3:** The current sense resistor $R_{ISET}$ must be placed as close as possible to VIN and VICC pins on the PCB layout to avoid noise interference.

## PIN CONFIGURATION

| Package | Pin Configuration (Top View) |
|---|---|
| SOP-8-EP |  |



## PIN DESCRIPTION

| No. | Pin | Description |
|---|---|---|
| 1 | EN | Device enable pin. Internally pulled down to GND by a 4MΩ (Typ.) resistor. Pull low to shutdown the device. If unused, it must be connected to VIN pin via 10kΩ resistor. |
| 2 | UV | External under voltage lockout threshold setting for LED string open fault detection. Pull low will disable the LED open fault detection. If unused, it must be connected to VIN pin via 10kΩ resistor. |
| 3 | PWM | PWM dimming input. It also can be used for external VIN under voltage lockout threshold setting. If unused, it must be connected to VIN pin via 10kΩ resistor. |
| 4 | FAULTB | Open drain I/O diagnostic pin. Active low output driven by the device when it detects a fault condition. As an input, this pin will accept an externally generated FAULTB signal to disable the device output to satisfy the “one fail all fail” function. This pin is internally pulled up to internal 4.5V (Typ.) LDO by a 50kΩ (Typ.) resistor. |
| 5 | GND | Ground. |
| 6 | OUT | Output current source channel. |
| 7 | VICC | Current input and current sense pin. |
| 8 | VIN | Power supply input and current sense pin. |
| | Thermal Pad | MUST be electrically connected to large GND plane for better thermal dissipation. |

## ORDERING INFORMATION

**Automotive Range: -40°C to +125°C**

| Order Part No. | Package | QTY/Reel |
|---|---|---|
| IS32LT3140B-GRLA3-TR | SOP-8-EP, Lead-free | 2500 |

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a.) the risk of injury or damage has been minimized;

b.) the user assume all such risks; and

c.) potential liability of Lumissil Microsystems is adequately protected under the circumstances

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| All pins voltage | -0.3V ~ +45V |
| VIN pin to VICC pin voltage, $V_{IN}$ - $V_{VICC}$ | -0.3V ~ +1V |
| Operating temperature, $T_A$=$T_J$ | -40°C ~ +150°C |
| Maximum continuous junction temperature, $T_{J(MAX)}$ | +150°C |
| Storage temperature range, $T_{STG}$ | -65°C ~ +150°C |
| Package thermal resistance, junction to ambient (4 layer standard test PCB based on JEDEC standard), $\theta_{JA}$ | 43.6°C/W |
| Package thermal resistance, junction to thermal PAD (4 layer standard test PCB based on JEDEC standard), $\theta_{JP}$ | 1.39°C/W |
| Maximum power dissipation, $P_{DMAX}$ | 2.87W |
| ESD (HBM)<br>ESD (CDM) | ±2kV<br>±750V |

**Note 4:** Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## ELECTRICAL CHARACTERISTICS

$T_J$= $T_A$= -40°C ~ +150°C, $V_{IN}$= 12V, the detail refer to each condition description, unless otherwise noted. Typical values are at $T_J$= $T_A$= 25°C (Note 5).

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **Power Up Parameter** | | | | | | |
| $V_{IN}$ | Supply voltage range | | 4.5 | | 40 | V |
| $V_{UVLO_R}$ | VIN under voltage lockout rising threshold | | | 3.2 | 4.0 | V |
| $V_{UVLO_F}$ | VIN under voltage lockout falling threshold | | 2.2 | 3.0 | | V |
| $I_{IN}$ | VIN quiescent current | $V_{PWM}$= high, $V_{EN}$= high, no fault conditions | 0.2 | 0.35 | 0.6 | mA |
| $I_{SD}$ | Shutdown current | $V_{EN}$= low | | 5 | 10 | μA |
| $I_{IN_FLT}$ | VIN supply current in fault condition | $V_{PWM}$= high, $V_{EN}$= high, $V_{UV}$= high, FAULTB externally pulled low | 0.3 | 0.4 | 0.6 | mA |
| $t_{ON}$ | EN high time for IC power up | $I_{OUT}$= -150mA, $V_{IN}$= 12V, $V_{EN}$= high | 20 | 40 | 60 | μs |
| **Channel Parameter** | | | | | | |
| $I_{OUT_R}$ | Channel output current range | 100% duty cycle | -450 | | -4 | mA |
| $V_{SENSE}$ | Current sense voltage ($V_{IN}$-$V_{VICC}$) | $V_{IN}$= 4.5V to 18V, $T_J$= $T_A$ =25°C | 95 | 100 | 105 | mV |
| | | $V_{IN}$= 4.5V to 18V, $T_J$= $T_A$ =-40°C~150°C | 92 | 100 | 108 | |
| $V_{HR_MIN}$ | Minimum headroom voltage, from VIN to OUT ($V_{SENSE}$ included) | $I_{OUT}$= -10mA | | 120 | 150 | mV |
| | | $I_{OUT}$= -70mA | | 250 | 400 | |
| | | $I_{OUT}$= -150mA | | 430 | 700 | |
| | | $I_{OUT}$= -300mA | | 800 | 1300 | |
| $I_{OUT_L}$ | Output limit current | VIN shorted to VICC, $V_{HR}$= 3V | | -600 | | mA |
| $I_{LEAK}$ | Channel leakage current | $V_{EN}$= Low, $V_{OUT}$= 0V | | | 1 | μA |
| | | $V_{PWM}$= Low, $V_{EN}$=high, $V_{OUT}$= 0V | | | 1 | |

**ELECTRICAL CHARACTERISTICS (CONTINUE)**

$T_J$= $T_A$= -40°C ~ +150°C, $V_{IN}$= 12V, the detail refer to each condition description, unless otherwise noted. Typical values are at $T_J$= $T_A$= 25°C (Note 5).

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $t_{SL}$ | Current rising/falling slew time | Enabled/disabled by PWM pin, current rise/fall between 10%~90%, $I_{OUT}$= -300mA | 8 | 16 | 24 | μs |
| **Fault Protect Parameter** | | | | | | |
| $t_{FD_DT}$ | Fault detect deglitch time | *Fault must be present at least this long to trigger the fault detect | 70 | 130 | 190 | μs |
| $t_{FD_RL}$ | Fault release deglitch time | | 30 | 60 | 90 | μs |
| $V_{FAULTB_PU}$ | FAULTB pin internally pull-up voltage | | 4 | | 5.5 | V |
| $R_{FAULTB}$ | FAULTB pin pull-up resistor | | | 50 | | kΩ |
| $V_{FAULTB_PD}$ | FAULTB pin externally pull-down voltage | Sink current= 5mA | | 0.2 | 0.4 | V |
| $V_{FAULTB_IH}$ | FAULTB pin input high enable threshold | | 2 | | | V |
| $V_{FAULTB_IL}$ | FAULTB pin input low disable threshold | | | | 0.7 | V |
| $V_{SCD_R}$ | OUT pin short to GND rising threshold | Measured at OUT pin | 1.1 | 1.2 | 1.3 | V |
| $V_{SCD_F}$ | OUT pin short to GND falling threshold | Measured at OUT pin | 0.82 | 0.865 | 0.91 | V |
| $V_{OD_R}$ | OUT pin open rising threshold | Measured at ($V_{VICC}$-$V_{OUT}$) | 70 | 120 | 160 | mV |
| $V_{OD_F}$ | OUT pin open falling threshold | Measured at ($V_{VICC}$-$V_{OUT}$) | 250 | 320 | 400 | mV |
| $I_{RTR}$ | Output retry current in fault modes | $V_{OUT}$= 0V | -1.6 | -1 | -0.6 | mA |
| $T_{SD}$ | Thermal shutdown threshold | (Note 6) | | 175 | | °C |
| $T_{HY}$ | Over-temperature hysteresis | (Note 6) | | 25 | | °C |
| **Logic Input** | | | | | | |
| $V_{IH}$ | EN pin input logic high voltage | | 2.0 | | | V |
| $V_{IL}$ | EN pin input logic low voltage | | | | 0.7 | V |
| $V_{UV_IH}$ | UV input rising threshold | | 1.14 | 1.20 | 1.3 | V |
| $V_{UV_IL}$ | UV input falling threshold | | 1.045 | 1.1 | 1.155 | V |
| $V_{PWM_IH}$ | PWM input rising threshold | | 1.14 | 1.20 | 1.3 | V |
| $V_{PWM_IL}$ | PWM input falling threshold | | 1.045 | 1.1 | 1.155 | V |
| $f_{PWM}$ | PWM frequency to PWM pin | | | | 1 | kHz |

**ELECTRICAL CHARACTERISTICS (CONTINUE)**

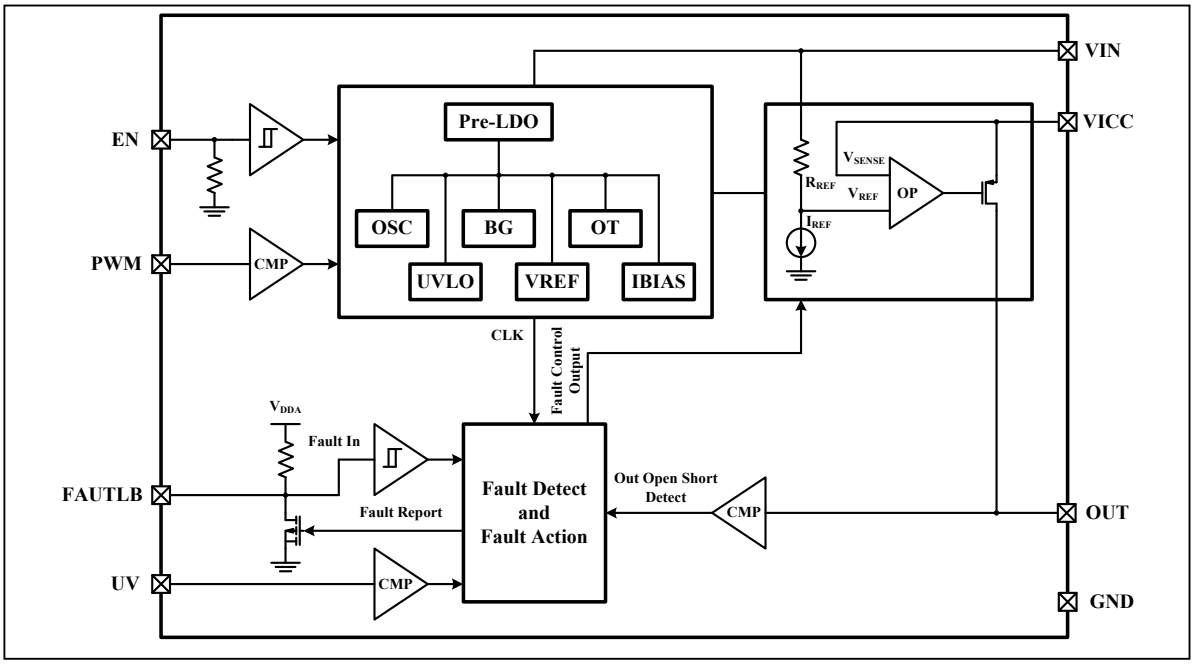
$T_J$= $T_A$= -40°C ~ +150°C, $V_{IN}$= 12V, the detail refer to each condition description, unless otherwise noted. Typical values are at $T_J$= $T_A$= 25°C (Note 5).

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $t_{PWM_R}$ | Delay time of PWM rising edge to 10% output current | $I_{OUT}$= -100mA | 10 | 17 | 25 | μs |
| $t_{PWM_F}$ | Delay time of PWM falling edge to 90% output current | $I_{OUT}$= -100mA | 15 | 21 | 30 | μs |
| $R_{PD_EN}$ | EN pin internal pull-down resistor | | | 4 | | MΩ |

**Note 5:** Limits are 100% production tested at 25ºC. Limits over the operating temperature range verified through either bench and/or tester testing and correlation using Statistical methods.

**Note 6:** Guaranteed by design.

## FUNCTIONAL BLOCK DIAGRAM



## TYPICAL PERFORMANCE CHARACTERISTICS

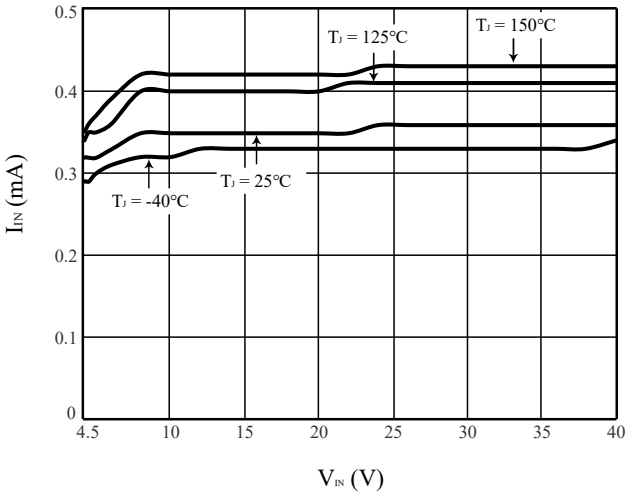



**Figure 3** $I_{IN}$ vs. $V_{IN}$

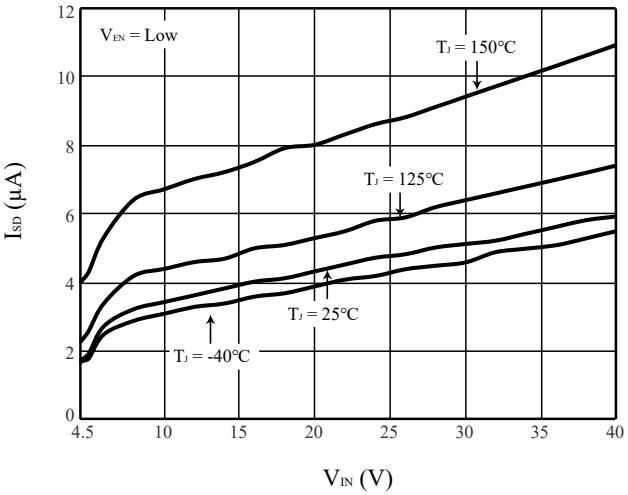



**Figure 4** $I_{SD}$ vs. $V_{IN}$

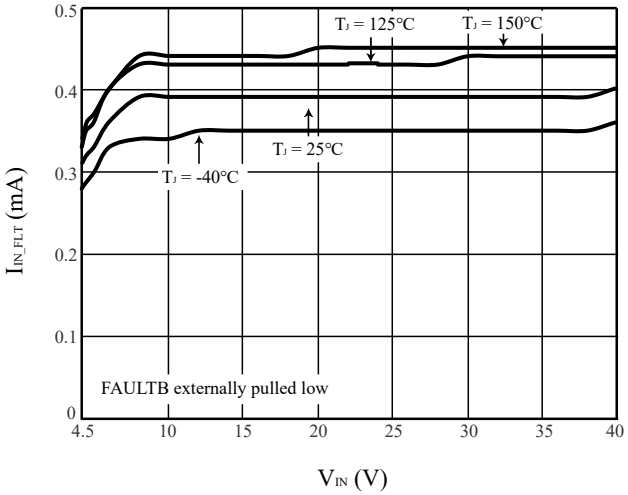



**Figure 5** $I_{IN_FLT}$ vs. $V_{IN}$

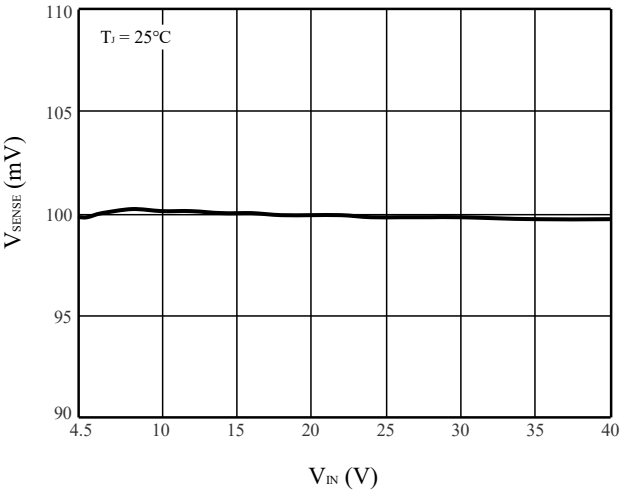



**Figure 6** $V_{SENSE}$ vs. $V_{IN}$

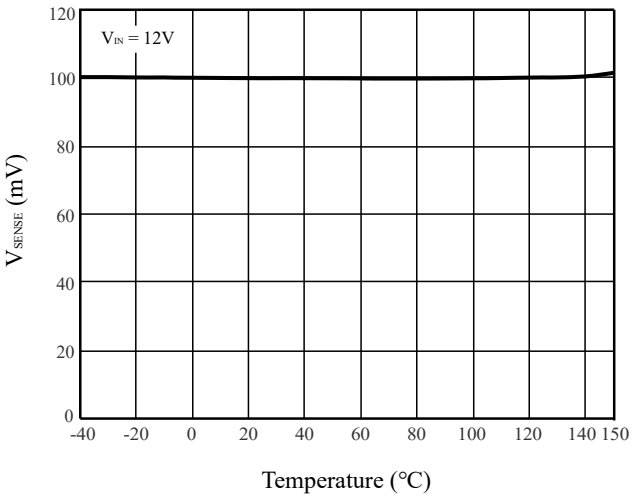



**Figure 7** $V_{SENSE}$ vs. $T_J$

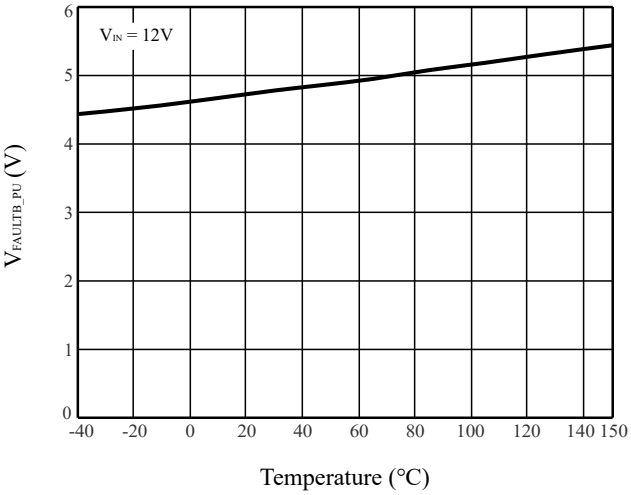



**Figure 8** $V_{FAULTB_PU}$ vs. $T_J$

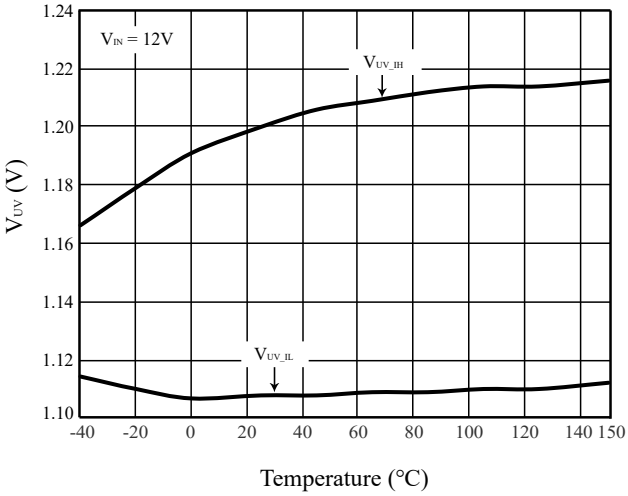



**Figure 9** $V_{UV}$ vs. $T_J$

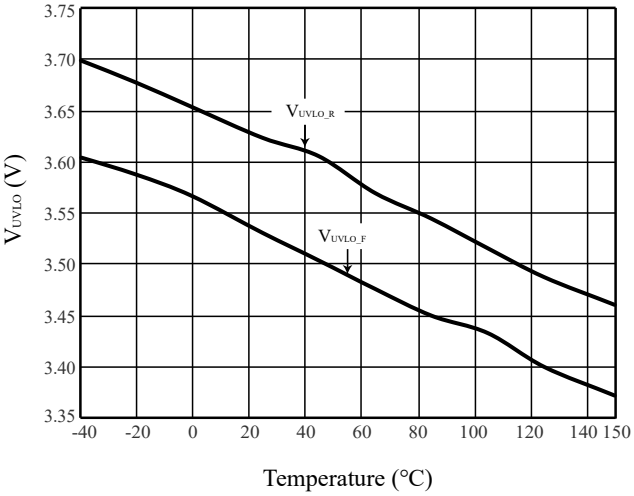



**Figure 10** $V_{UVLO}$ vs. $T_J$

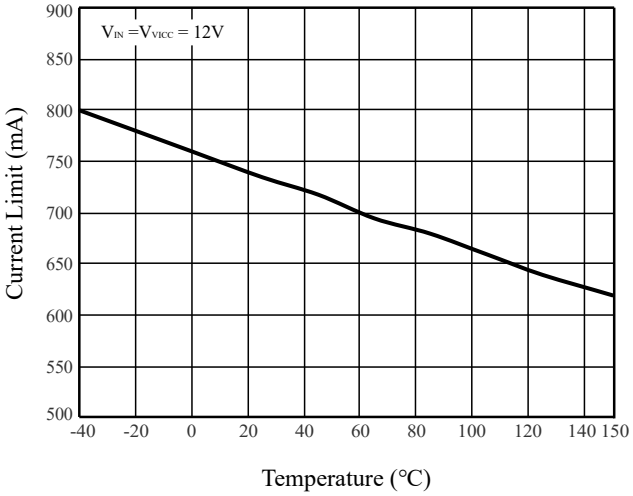



**Figure 11** $I_{OUT_L}$ vs. $T_J$

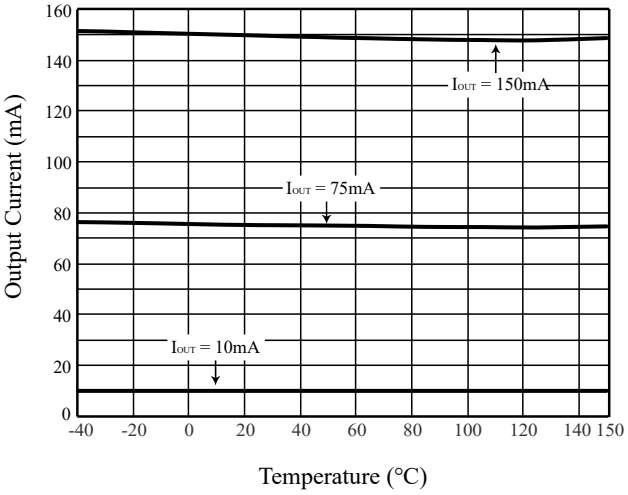



**Figure 12** $I_{OUT}$ vs. $T_J$

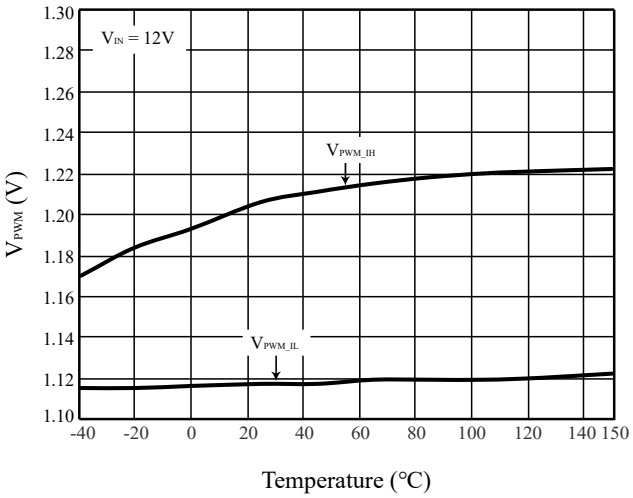



**Figure 13** PWM Threshold vs. $T_J$

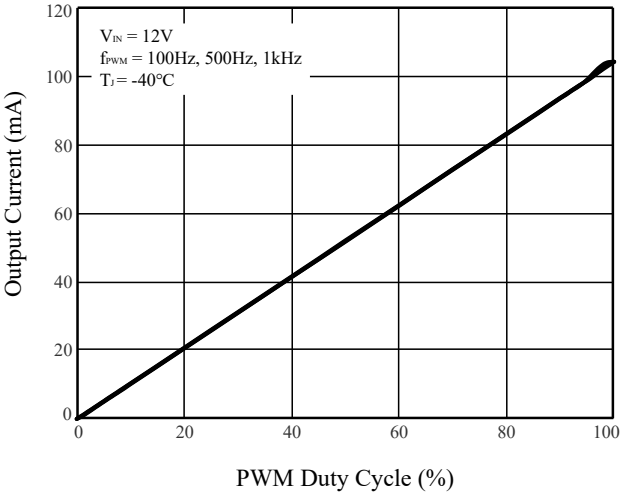



**Figure 14** Output Current vs. PWM Duty Cycle

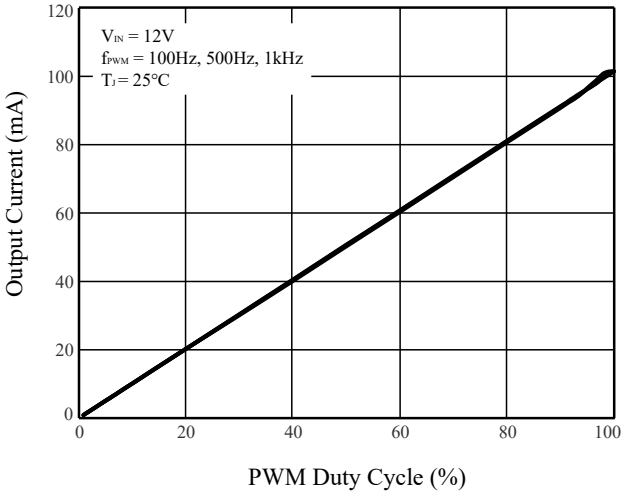



**Figure 15** Output Current vs. PWM Duty Cycle

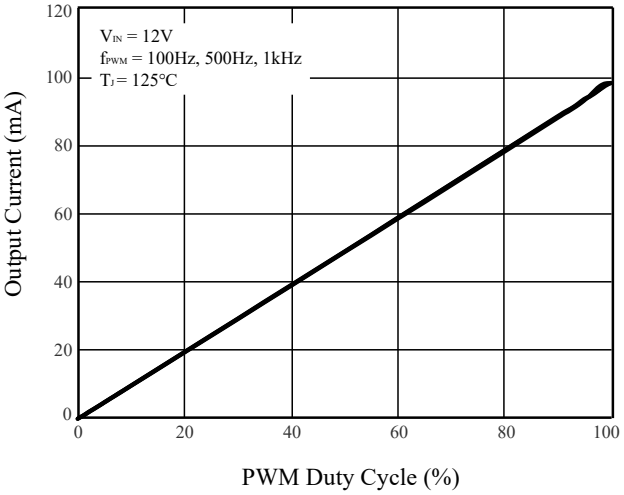



**Figure 16** Output Current vs. PWM Duty Cycle

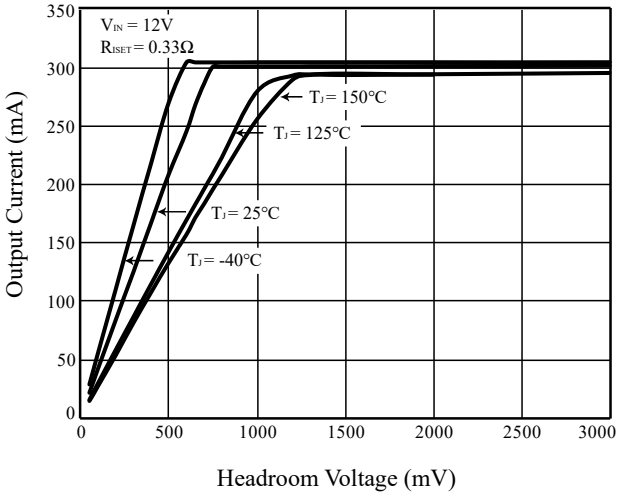



**Figure 17** Output Current vs. Headroom Voltage

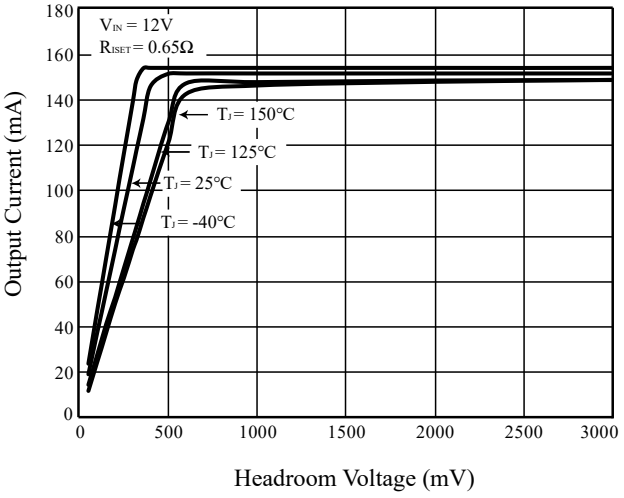



**Figure 18** Output Current vs. Headroom Voltage

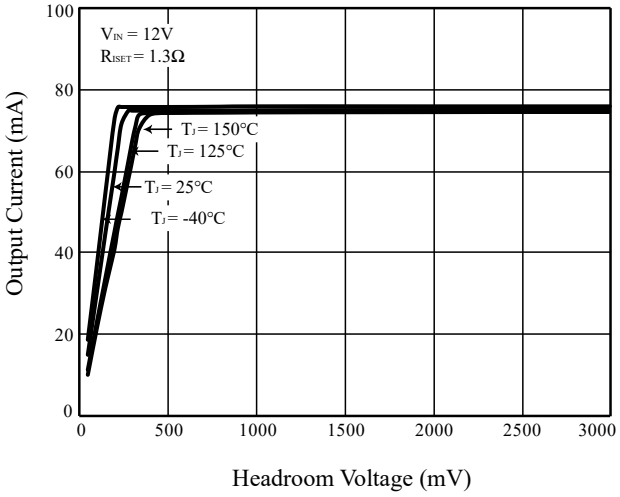



**Figure 19** Output Current vs. Headroom Voltage

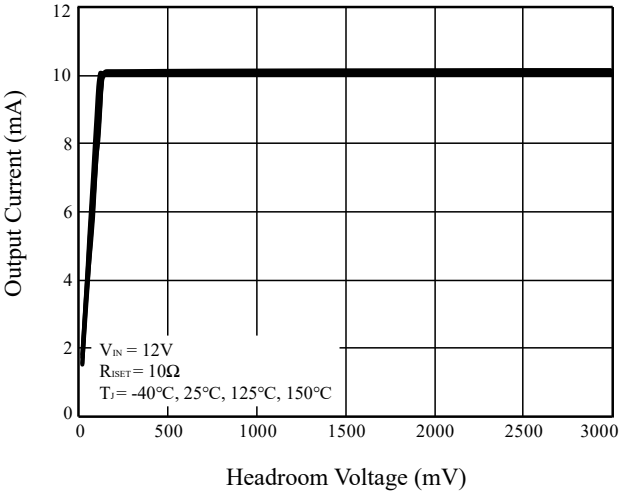



**Figure 20** Output Current vs. Headroom Voltage

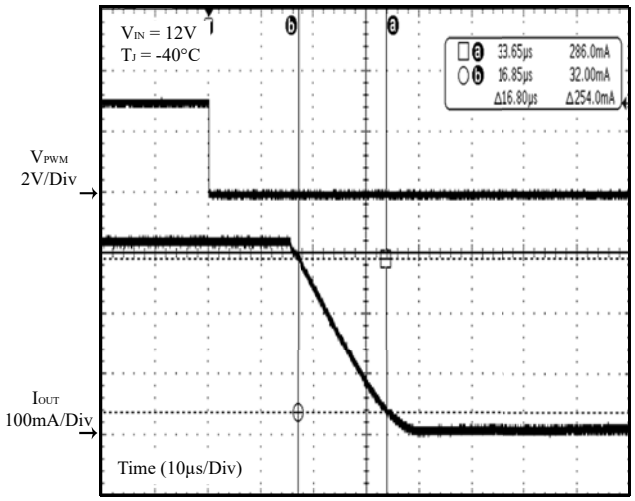



**Figure 21** PWM Off

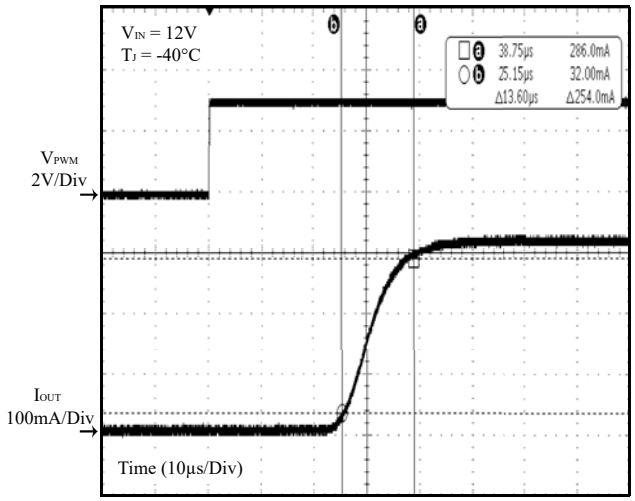



**Figure 22** PWM On

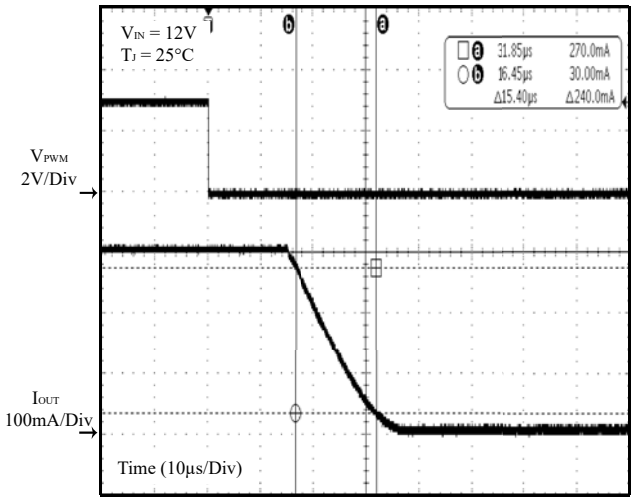



**Figure 23** PWM Off

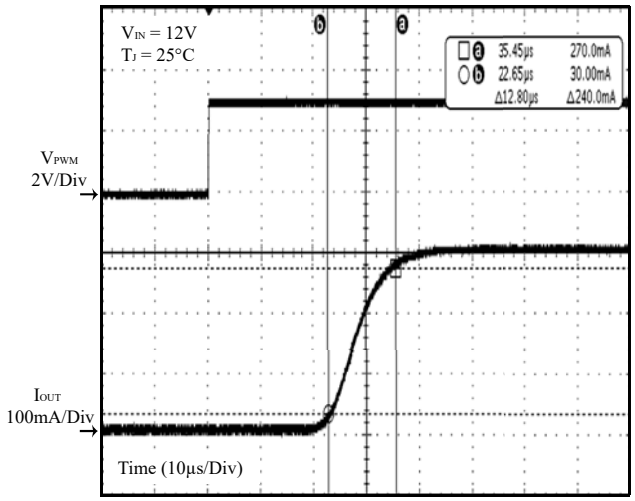



**Figure 24** PWM On

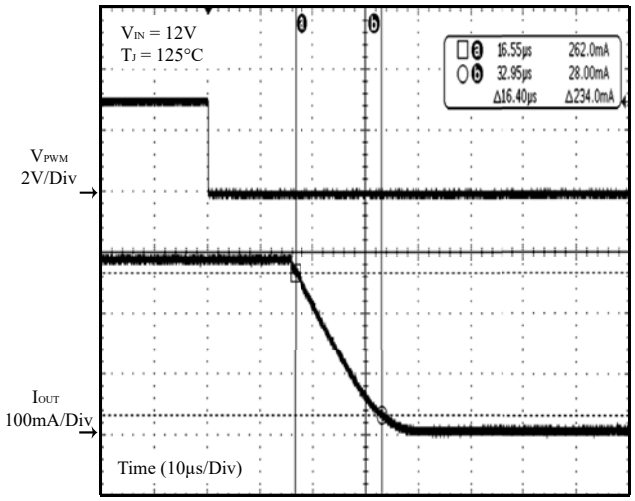



**Figure 25** PWM Off

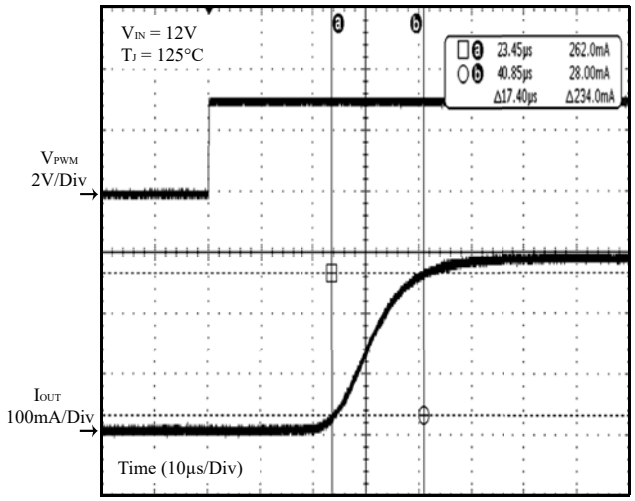



**Figure 26** PWM On

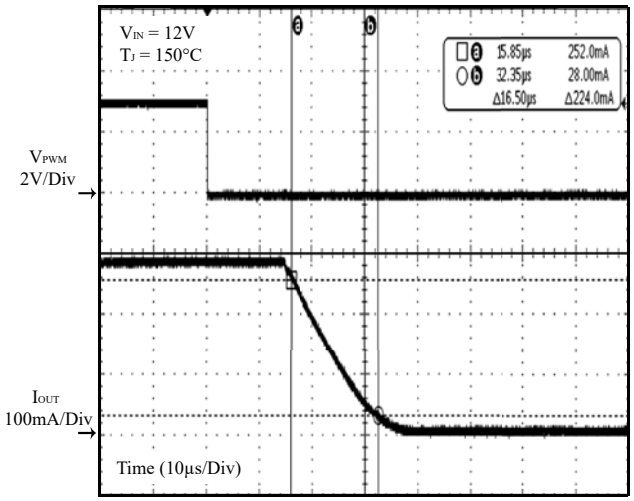



**Figure 27** PWM Off

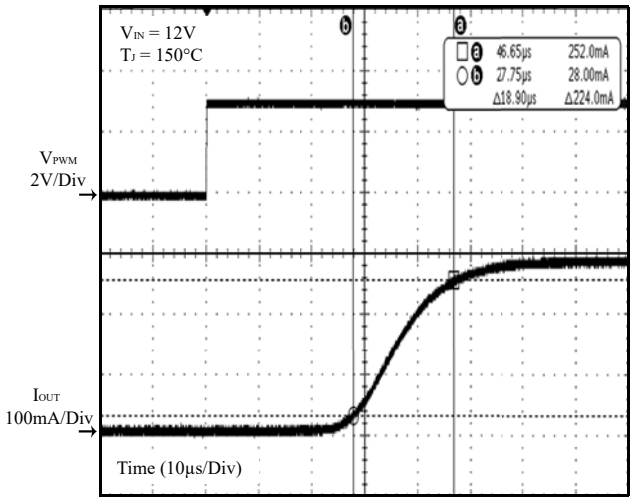



**Figure 28** PWM On

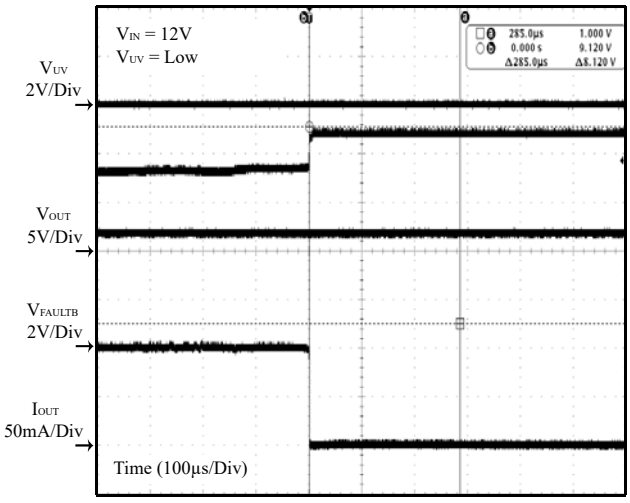



**Figure 29** Output Open

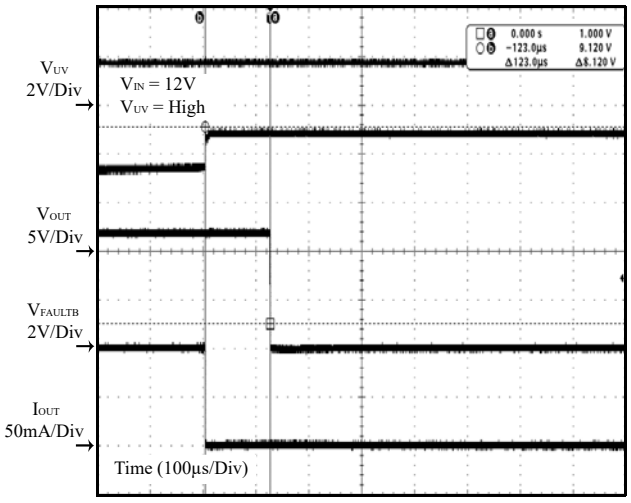



**Figure 30** Output Open

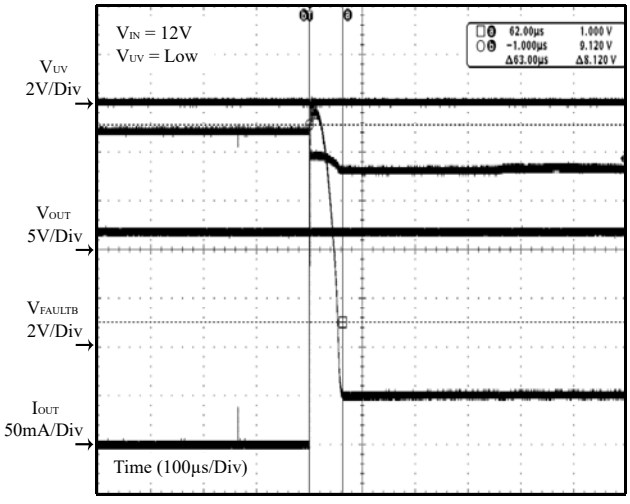



**Figure 31** Output Open Fault Remove

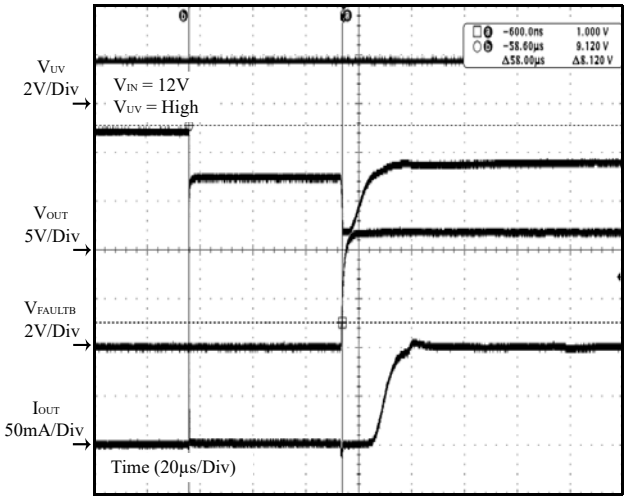



**Figure 32** Output Open Fault Remove

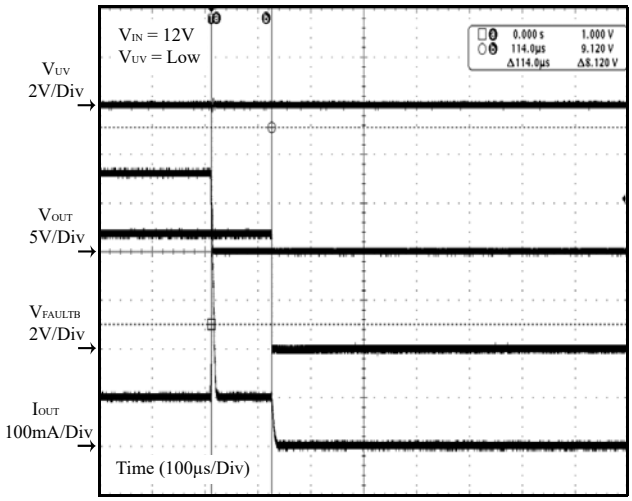



**Figure 33** Output Short

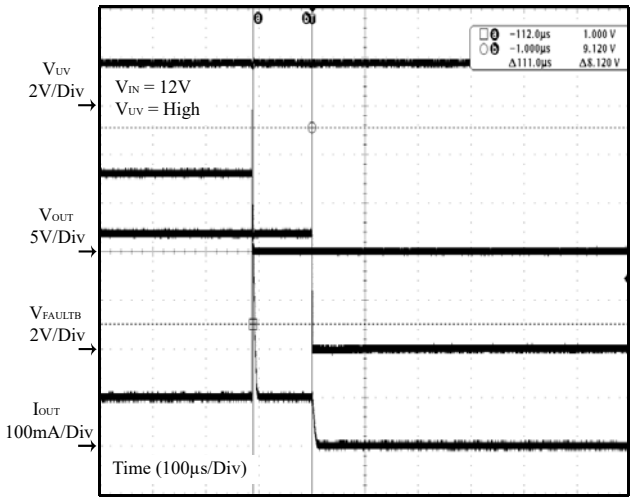



**Figure 34** Output Short

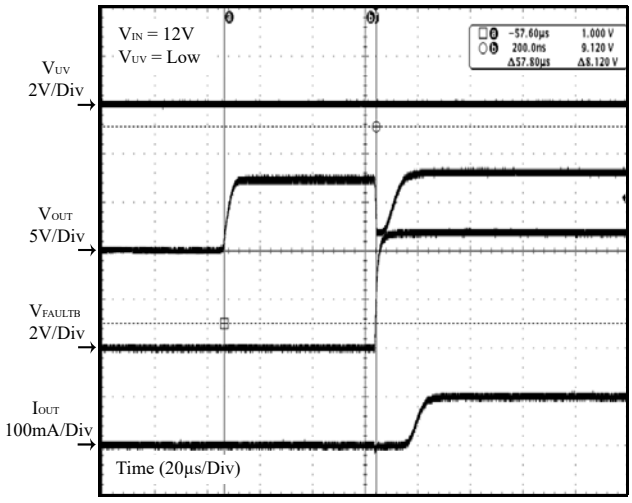



**Figure 35** Output Short Fault Remove

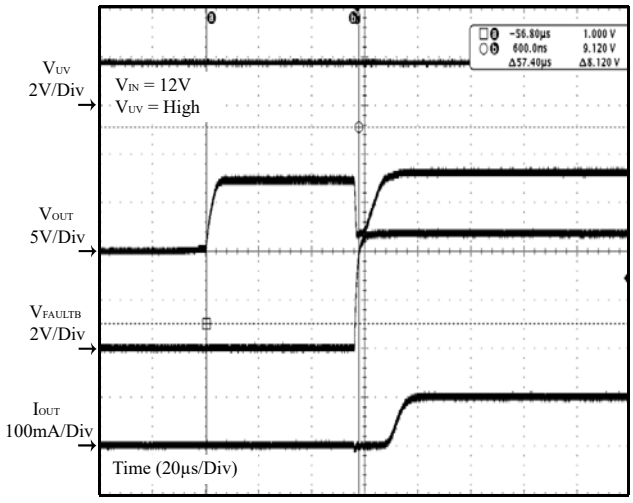



**Figure 36** Output Short Fault Remove

## APPLICATION INFORMATION

The IS32LT3140B is a programmable linear current source capable of regulating a constant current up to 450mA. A single resistor $R_{ISET}$ is connected across the VIN and VICC pins to set the output current value. The current flows from the power supply through the $R_{ISET}$ resistor into the VICC pin and internal current source and out from OUT pin to LED string. The device senses the voltage drop on the $R_{ISET}$ resistor and an internal regulation loop drives the output current source to regulate the voltage drop on the $R_{ISET}$ resistor at $V_{SENSE}$.

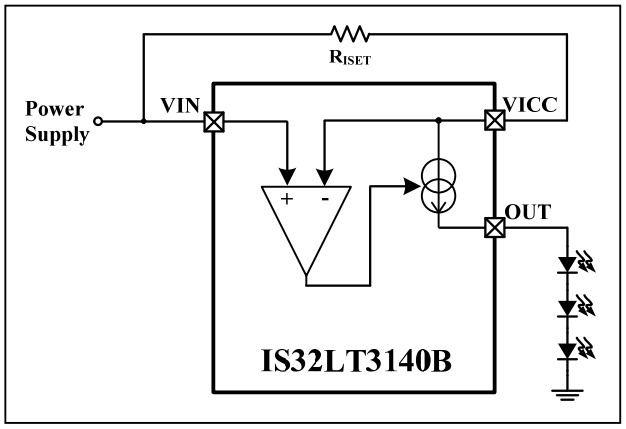



**Figure 37** Constant Current Regulation

## OUTPUT CURRENT SETTING

The regulated maximum LED current is set by the current sense resistor $R_{ISET}$. The $R_{ISET}$ resistor value can be calculated using the following Equation (1):

$$R_{ISET} = \frac{V_{SENSE}}{I_{LED}} \qquad (1)$$

Where $I_{LED}$ is the desired LED current in Amp and $R_{ISET}$ is in Ω. $V_{SENSE}$ is current sense voltage, 0.1V typical.

It is recommend that $R_{ISET}$ be a 1% accuracy resistor with good temperature characteristic to ensure stable and precise output current. On the PCB layout, this resistor must be placed as close to VIN pin and VICC pin as possible to avoid noise interference.

When the desired current is high, the power rating also should be considered. The maximum power dissipation on the $R_{ISET}$ resistor is calculated by:

$$P_{RISET} = V_{SENSE} \times I_{LED} \qquad (2)$$

A single high wattage resistor or several small wattage resistors in parallel can be used to sustain the power dissipation.

The device is protected from an output overcurrent condition caused by $R_{ISET}$ resistor. The output current is limited to an $I_{OUT_L}$ value of 600mA for if a low value resistor is connected to VIN and VICC pins.

## DEVICE ENABLE AND SHUTDOWN

The EN pin is an enable input for the device, pull it higher than $V_{IH}$ to enable the device; pull it lower than $V_{IL}$ to force the device into shutdown mode with an ultralow quiescent current. If the shutdown mode is unused, connect the EN pin to the VIN pin via a 10kΩ resistor.

## PWM DIMMING

PWM pin controls the current source output source. The PWM pin voltage should be higher than $V_{PWM_IH}$ to enable the output source and lower than $V_{PWM_IL}$ to disable it. Note that the output fault detection is also disabled when the PWM pin is low.

An external PWM signal on the PWM pin can be used to modulate the output current to dim the LED light output.. The PWM dimming LED current is based on the PWM signal's duty cycle and can be calculated by the following Equation (3):

$$I_{LED_PWM} = I_{LED} \times D_{PWM} \qquad (3)$$

Where $D_{PWM}$ is the duty cycle of PWM signal.

The recommended frequency range of the external PWM signal is 100Hz~1kHz and the duty cycle can be from 0 to 100%. Due to the output's current slew rate control for EMI consideration plus the propagation time from PWM rising edge to the output activity, a lower frequency PWM will provide a better dimming contrast ratio.

## UNDER VOLTAGE LOCKOUT (UVLO)

IS32LT3140B features an under voltage lockout (UVLO) function on the VIN pin to prevent misoperation at low input voltages. The UVLO threshold is an internally fixed value and cannot be adjusted. The device is enabled when the $V_{IN}$ voltage exceeds $V_{UVLO_R}$ (Typ. 3.2V), and disabled when the $V_{IN}$ voltage falls below $V_{UVLO_F}$ (Typ. 3.0V).

Besides this internal, fixed UVLO, it may be desireable to externally set a higher UVLO threshold for some applications. A precise UVLO threshold voltage can be set by using a resistor voltage divider between VIN and Gnd with the center connected to the PWM pin.

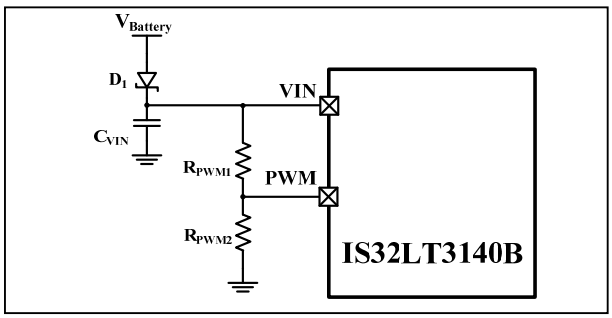



**Figure 38** External UVLO for VIN

The external UVLO threshold voltage can be computed by the following Equations (4) and (5):

$$V_{UVLO_EXTF} = V_{PWM_IL} \times \frac{R_{PWM1} + R_{PWM2}}{R_{PWM2}} \quad (4)$$

$$V_{UVLO_EXTR} = V_{PWM_IH} \times \frac{R_{PWM1} + R_{PWM2}}{R_{PWM2}} \quad (5)$$

The output source is enabled when the $V_{IN}$ voltage exceeds $V_{UVLO_EXTR}$, and disabled when the $V_{IN}$ voltage falls below $V_{UVLO_EXTF}$.

It is recommended that $R_{PWM1}$ and $R_{PWM2}$ be 1% accuracy resistors with good temperature characteristics to ensure a precise detection. On the PCB layout, this resistor divider must be placed as close as possible to the PWM pin to avoid noise coupling into the UVLO detection.

The PWM pin is a high impedance input. If the PWM pin is unused, connect it to the VIN pin using a 10kΩ resistor.

## POWER SUPPLY MODULATION (PSM) DIMMING

The IS32LT3140B can support Power Supply Modulation (PSM), which implements LED dimming by pulse width modulation of the power supply rail. The IS32LT3140B's closed loop stability is not affected by PSM operation. To get better dimming linearity, the recommended PSM frequency should be in the range of 100Hz to 300Hz (200Hz Typ.) and the input capacitor, $C_{VIN}$, should be of a low value (0.1uF Typ.) to ensure rapid discharge during PSM low periods. In PSM dimming applications, the external UVLO should be used to improve the dimming accuracy. It is recommended for the $V_{UVLO_EXTR}$ threshold voltage to be about 0.5V higher than the LED string voltage.

## THERMAL SHUNT MECHANISM

IS32LT3140B is a linear constant current regulator subject thermal dissipation. The device begins current regulation when the voltage drop on the output source, called headroom voltage $V_{HR}$, exceeds the min headroom voltage $V_{HR_MIN}$,. The power dissipation on the device will be proportional to the headroom voltage and LED current $I_{LED}$.

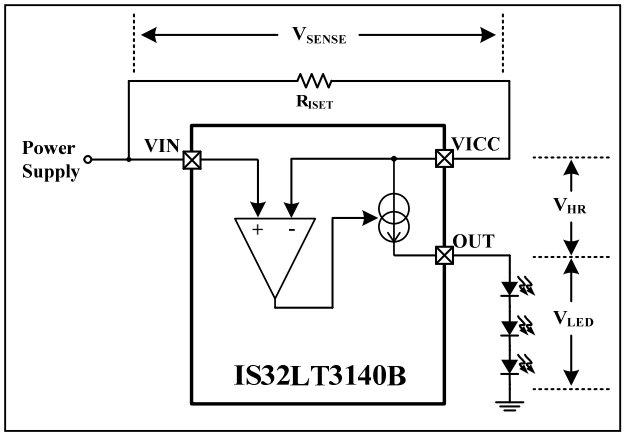



**Figure 39** Voltage Drop

$$P_{3140B} = (V_{IN} - V_{SENSE} - V_{LED}) \times I_{OUT} = V_{HR} \times I_{OUT} \quad (6)$$

Note that the VIN quiescent current consumption is negligible and ignored in this calculation.

With a given LED string voltage ($V_{LED}$) and output current ($I_{LED}$), the higher the input voltage the larger the power dissipation on the IS32LT3140B. In automotive applications, the nominal battery voltage range is about 9V to 16V. However, electrical and radio-frequency disturbance frequently occurs in the vehicle environment that results in the supply voltage jumping over 16V. In a load dump condition the supply voltage could rise well above 40V. So the thermal management on device should be carefully considered when the output current is high, such as $I_{LED}$ ≥ 200mA.

To optimize the thermal resistance on the IS32LT3140B, an external power resistor ($R_P$) can be connected in parallel with the output current source to shunt some thermal energy away from the device..

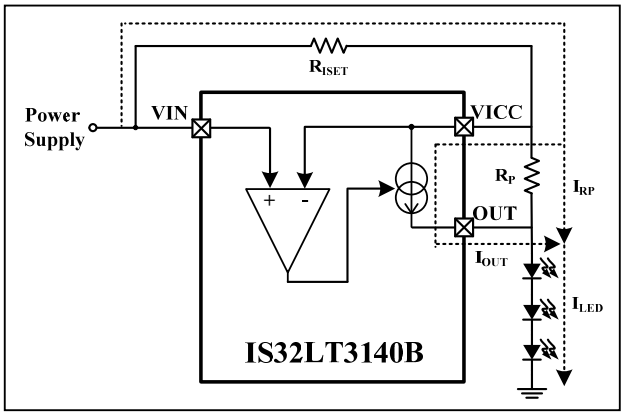



**Figure 40** Thermal Shunt Resistor

When using an $R_P$ power resistor, the internal regulation loop of IS32LT3140B still will drive the current source to regulate the voltage drop on the $R_{ISET}$ resistor to $V_{SENSE}$. As shown in Figure 41, the IS32LT3140B has different operating areas when using a power resistor. When the $V_{IN}$ is low, the

headroom voltage $V_{HR}$ is insufficient for constant LED current regulation. If the $V_{IN}$ rises above ($V_{LED}$+$V_{HR_MIN}$), the transition voltage $V_{IN_OUTOFF}$ splits the operation into two areas: Constant Current area and Current Increasing area.

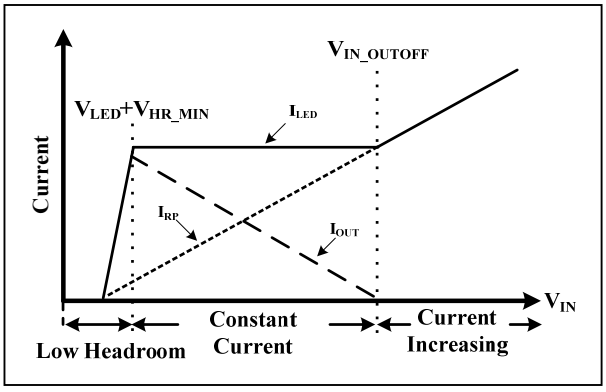



**Figure 41** Current Distribution vs. Power Supply Voltage

**Constant Current Area:**

With a given $R_{ISET}$ value and a proper $R_P$ shunt resistor, the LED current $I_{LED}$ in this area is regulated by IS32LT3140B to be constant and can be calculated by the following Equation (7):

$$I_{LED} = I_{RP} + I_{OUT} = \frac{V_{SENSE}}{R_{ISET}} \qquad (7)$$

Where, $I_{RP}$ is the current through the $R_P$ shunt resistor and $I_{OUT}$ is the output current of the current source.

The $I_{OUT}$ linearly decreases following $V_{IN}$ rising while the $I_{RP}$ linearly increases due to the increase in $V_{HR}$. The $I_{RP}$ is proportional to the headroom voltage $V_{HR}$ and can be calculated by the following Equations:

$$I_{RP} = \frac{V_{HR}}{R_P} = \frac{V_{IN} - V_{SENSE} - V_{LED}}{R_P} \qquad (8)$$

The power consumption on the $R_P$ shunt resistor is:

$$P_{RP} = I_{RP}^{\ 2} \times R_P = \frac{(V_{IN} - V_{SENSE} - V_{LED})^2}{R_P} \qquad (9)$$

The output current of the current source is:

$$I_{OUT} = I_{LED} - I_{RP} = I_{LED} - \frac{(V_{IN} - V_{SENSE} - V_{LED})}{R_P} \qquad (10)$$

The power consumption on IS32LT3140B is:

$$P_{3140B} = I_{OUT} \times V_{HR} = (I_{LED} - I_{RP}) \times (V_{IN} - V_{SENSE} - V_{LED}) \qquad (11)$$

Note that the VIN quiescent current consumption is negligible and ignored in this calculation.

The power consumption distribution of the IS32LT3140B and the $R_P$ shunt resistor are shown in Figure 42.

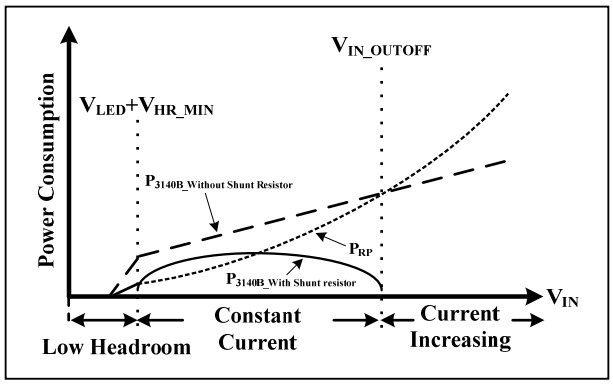



**Figure 42** Power Distribution vs. Power Supply Voltage

The normal operating area is the Constant Current area, where the $R_P$ power resistor shunts much of the thermal energy away from IS32LT3140B, especially at high $V_{IN}$. The thermal shunt mechanism significantly optimizes the device's thermal performance.

It is recommended to select a properly sized wattage resistor for $R_P$. A single high wattage resistor or several small wattage resistors in parallel can be used to sustain the power consumption at high $V_{IN}$ voltage supply levels.

**Constant Increasing Area:**

If the $V_{IN}$ is high enough to meet $I_{RP}$=$I_{LED}$, the $I_{OUT}$ will be regulated to zero mA, which means all LED current flows through the $R_P$ resistor and the current source is completely off.

$$V_{IN_OUTOFF} = I_{LED} \times R_P + V_{SENSE} + V_{LED} \qquad (12)$$

Where, $V_{IN_OUTOFF}$ is the $V_{IN}$ resulting in $I_{OUT}$= 0A. The power consumption on IS32LT3140B will also decrease to zero.

If the $V_{IN}$ continues to rise over $V_{IN_OUTOFF}$, the current source of IS32LT3140B will remain in the off state and the LED current will no longer be constant but will linearly increase following the $V_{IN}$ increase, which will be decided by:

$$I_{LED_INC} = \frac{V_{IN} - V_{LED}}{R_{ISET} + R_P} \qquad (13)$$

Where $V_{IN}$>$V_{IN_OUTOFF}$ and $I_{LED_INC}$ is the LED current in Current Increasing area.

To achieve a constant current over the power supply voltage range, choose an $R_P$ shunt resistor value so that $V_{IN_OUTOFF}$ is never less than the maximum power supply voltage. So the $R_P$ shunt resistor value should be calculated using the maximum power supply voltage $V_{IN_MAX}$:

$$R_P = \frac{V_{IN_MAX} - V_{LED} - V_{SENSE}}{I_{LED}} \qquad (14)$$

The $V_{IN_MAX}$ means the maximum voltage which is possible to apply on the VIN pin. For a 12V automotive system, the $V_{IN}$ voltage can range between 9V to 16V. However, a higher $V_{IN}$ value can be used for passing extreme condition tests, such as a one minute burn-in test at 24V or 28V power supply. In this case, the $V_{IN_MAX}$ should be 24V or 28V. The load dump test is another extreme condition, which could raise the supply voltage up to 40V. If calculating the $R_P$ value according to the load dump voltage, the $R_P$ value will be too large which will significantly degrade the thermal shunt effect in the normal operation voltage range of 9V to 16V. So a lower voltage rating TVS diode should be considered to be used upstream to clamp the maximum voltage appearing on the VIN pin.

Note the current through the $R_P$ shunt resistor is always present and CANNOT be shut off by the IS32LT3140B. Therefore, the $R_P$ shunt resistor should not be implemented if EN shutdown mode, PWM dimming and "one fail all fail" mode fault protection are to be used since they require turning off the output current. Only dimming method when using $R_P$ shunt resistor is power supply modulation (PSM).

## FAULT PROTECTION AND REPORTING

For robust system reliability, the IS32LT3140B integrates the detection circuitry to protect various fault conditions and report the fault conditions on the FAULTB pin which can be monitored by an external host. The fault protections include LED string open/short, output over-current (not reported) and thermal shutdown. The FAULTB pin is an open drain structure with an internal 50kΩ (Typ.) resistor pulled up to an internal 4.5V (Typ.) LDO so it is allowed to float. The FAULTB pin will go low when the device enables fault detection and detects a fault condition. Refer to Table 1.

The FAULTB pin supports both input and output functions. Externally pulling FAULTB pin low will disable the output. For lighting systems with multiple IS32LT3140B drivers which require the complete lighting system be shut down when a fault is detected, the FAULTB pin can be used in a parallel connection. A fault output by one device will pull low the FAULTB pins of the other parallel connected devices and simultaneously turn them off. This satisfies the "one fail all fail" operating requirement.

## LED STRING OPEN PROTECTION

The LED string open detection is enabled if the UV pin voltage is above its rising voltage threshold, $V_{UV_IH}$, and disabled if below its falling voltage threshold, $V_{UV_IL}$. A proper resistor divider ($R_{UV1}$ and $R_{UV2}$) connected from VIN pin to UV pin can set a UVLO function for LED string open protection, which is to prevent insufficient $V_{IN}$ falsely triggering LED string open detection. The UVLO voltage threshold is programmed by the resistor divider.

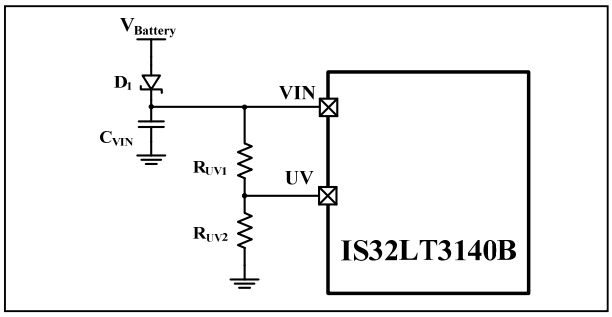



**Figure 43** UVLO for LED String Open Detection

$$V_{UVLO_FLTF} = V_{UV_IL} \times \frac{R_{UV1} + R_{UV2}}{R_{UV2}} \quad (15)$$

$$V_{UVLO_FLTR} = V_{UV_IH} \times \frac{R_{UV1} + R_{UV2}}{R_{UV2}} \quad (16)$$

It is recommend to set $V_{UVLO_FLTF}$ at least 0.5V higher than the LED string voltage. Choose $R_{UV1}$ and $R_{UV2}$ to be 1% accuracy resistors with good temperature characteristic to ensure a stable and precise detection. On the PCB layout, this resistor divider must be placed as close to UV pin as possible to avoid noise interference. If the UV pin is unused, connect it to VIN pin via a 10kΩ resistor.

If the LED string is open, the OUT pin will be pulled up close to VICC pin voltage by the current source. If $V_{IN}$>$V_{UVLO_FLTR}$ and the VICC pin to OUT pin voltage drop, ($V_{VICC}$-$V_{OUT}$), falls below the open LED detect voltage threshold, $V_{OD_R}$, and persists for longer than the deglitch time $t_{FD_DT}$, the LED string open protection will be triggered and FAULTB pin will go low to report the fault condition. The output source will reserve a small current $I_{RTR}$ for recovery detection, ignoring the PWM input.

The device will recover to normal operation and FAULTB pin will go back to high once the open condition is removed, ($V_{VICC}$-$V_{OUT}$) rising above the open LED detect voltage threshold, $V_{OD_F}$.

## LED STRING SHORT PROTECTION

The LED string short condition is detected if the OUT pin voltage is lower than the short detect voltage threshold, $V_{SCD_F}$. Once short condition occurs and persists for longer than the deglitch time $t_{FD_DT}$, the LED string short protection will be triggered the FAULTB pin will go low to report the fault condition. The output source will reserve a small current $I_{RTR}$ for recovery detection, ignoring the PWM input.

The device will recover to normal operation and FAULTB pin will go back to high once the short condition is removed, OUT pin voltage rising above the short detect voltage threshold, $V_{SCD_R}$.

## THERMAL SHUTDOWN

In the event that the junction temperature exceeds $T_{SD}$ (Typ. 175˚C), the output source will go to the "OFF" state and FAULTB pin will pull low to report the fault condition. At this point, the IC presumably begins to cool off. Any attempt to toggle the channel back to the source condition before the IC cooled to below ($T_{SD}$-$T_{HY}$) (Typ. 150˚C) will be blocked and the IC will not be allowed to restart. The FAULTB pin will recover to high once the IC has cooled down.

**Table 1 Fault Actions Description of "One Fail All Fail"**

| UV Pin | Fault Type | Fault Condition | Output State | FAULTB Pin (with input function) | Recovery |
|---|---|---|---|---|---|
| <$V_{UV_IL}$ | LED string open or OUT short to VIN | Disabled | | | |
| | LED string short or OUT short to GND | $V_{OUT}$<$V_{SCD_F}$ | Ignores the PWM input, outputs $I_{RTR}$ for recovery detection | Pull low (If the FAULB pins of multiple devices are connected together, all devices will be off) | $V_{OUT}$>$V_{SCD_R}$ |
| | Over temperature | $T_J$>$T_{SD}$ | Off | | $T_J$<($T_{SD}$-$T_{HY}$) |
| >$V_{UV_IH}$ | LED string open or OUT short to VIN | ($V_{VICC}$-$V_{OUT}$)<$V_{OD_R}$ | Ignores the PWM input, outputs $I_{RTR}$ for recovery detection | | ($V_{VICC}$-$V_{OUT}$)>$V_{OD_F}$ |
| | LED string short or OUT short to GND | $V_{OUT}$<$V_{SCD_F}$ | Ignores the PWM input, outputs $I_{RTR}$ for recovery detection | | $V_{OUT}$>$V_{SCD_R}$ |
| | Over temperature | $T_J$>$T_{SD}$ | Off | | $T_J$<($T_{SD}$-$T_{HY}$) |

## THERMAL CONSIDERATIONS

The package thermal resistance, $\theta_{JA}$, determines the amount of heat that can pass from the silicon die to the surrounding ambient environment. The $\theta_{JA}$ is a measure of the temperature rise created by power dissipation and is usually measured in degree Celsius per watt (°C/W). The junction temperature, $T_J$, can be calculated by the rise of the silicon temperature, ΔT, the power dissipation on IS32LT3140B, $P_{3140B}$, and the package thermal resistance, $\theta_{JA}$, as in Equation (17):

$$T_J = T_A + \Delta T = T_A + P_{3140B} \times \theta_{JA} \qquad (17)$$

The $P_{3140B}$ is descripted in the "Thermal Shunt Mechanism" section.

When operating the chip at high ambient temperatures, or when the supply voltage is high, care must be taken to avoid exceeding the package power dissipation limits. The maximum power dissipation at $T_A$=25˚C can be calculated using the following Equation (18):

$$P_{D(MAX)} = \frac{150°C - 25°C}{\theta_{JA}} \qquad (18)$$

So,

$$P_{D(MAX)} = \frac{150°C - 25°C}{43.6°C/W} \approx 2.87W$$

for SOP-8-EP package.

Figure 44, shows the power derating of the IS32LT3140B on a JEDEC board (in accordance with JESD 51-5 and JESD 51-7) standing in still air.

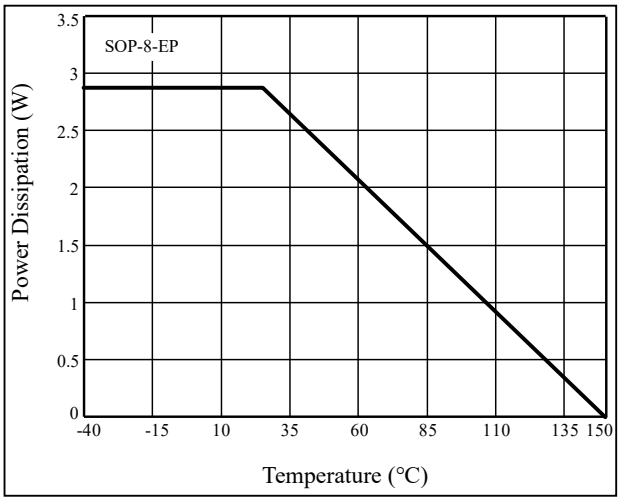



**Figure 44** Dissipation Curve (SOP-8-EP)

In the thermal shunt application, the $R_P$ will share quite a lot power dissipation; therefore its package power rating should be sufficient to prevent heat run away.

When designing the Printed Circuit Board (PCB) layout, double-sided PCB with a large copper area on each side of the board directly under the IS32LT3140B and the thermal shunt resistor. Multiple thermal vias, as shown in Figure 45, will help to conduct heat from the exposed pad of the IS32LT3140B and the thermal shunt resistor to the copper on each side of the board. To avoid the heat buildup, the thermal shunt resistor should be spread out on the PCB board with some distance from IS32LT3140B.

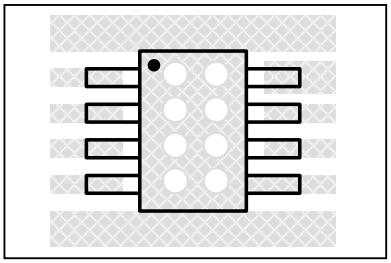


**Figure 45** Board Via Layout For Thermal Dissipation

## CLASSIFICATION REFLOW PROFILES

| Profile Feature | Pb-Free Assembly |
|---|---|
| **Preheat & Soak**<br>Temperature min (Tsmin)<br>Temperature max (Tsmax)<br>Time (Tsmin to Tsmax) (ts) | 150°C<br>200°C<br>60-120 seconds |
| Average ramp-up rate (Tsmax to Tp) | 3°C/second max. |
| Liquidous temperature (TL)<br>Time at liquidous (tL) | 217°C<br>60-150 seconds |
| Peak package body temperature (Tp)* | Max 260°C |
| Time (tp)** within 5°C of the specified classification temperature (Tc) | Max 30 seconds |
| Average ramp-down rate (Tp to Tsmax) | 6°C/second max. |
| Time 25°C to peak temperature | 8 minutes max. |

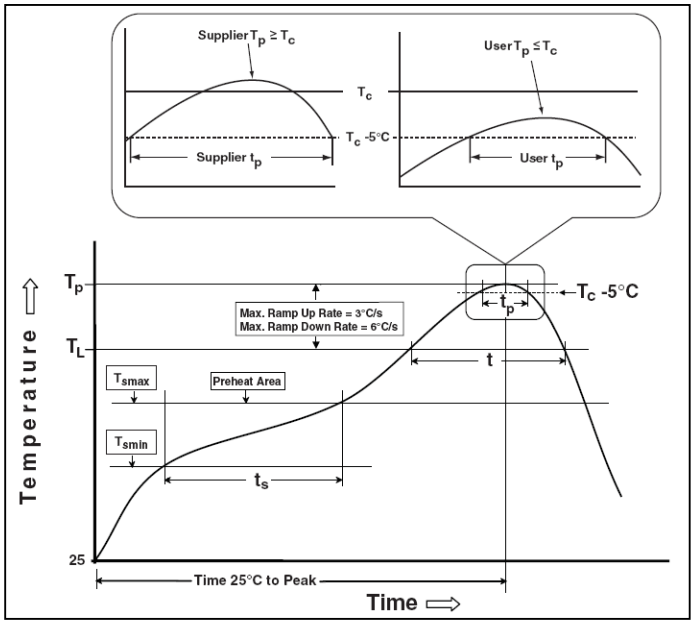
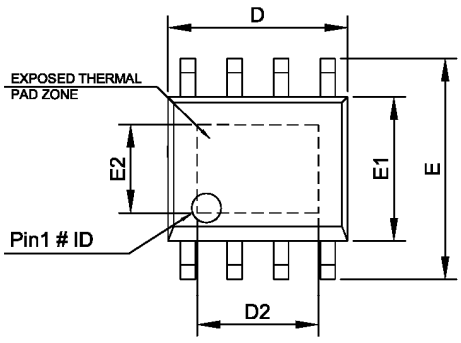
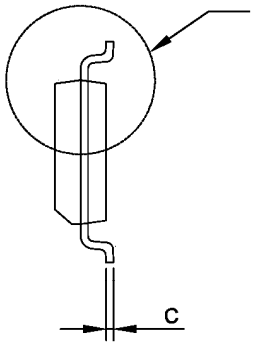


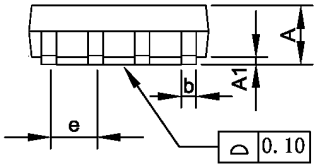

**Figure 46** Classification Profile

## PACKAGE INFORMATION

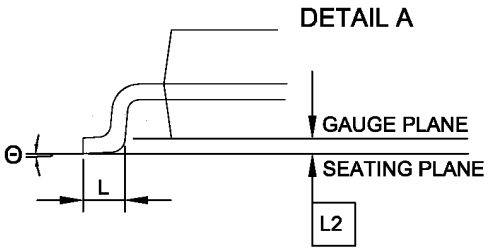
### SOP-8-EP




| SYMBOL | MILLIMETER | | |
|---|---|---|---|
| | MIN | NOM | MAX |
| A | – | – | 1.70 |
| A1 | – | – | 0.15 |
| E1 | 3.70 | 3.90 | 4.10 |
| E | 5.80 | 6.00 | 6.20 |
| D | 4.70 | 4.90 | 5.10 |
| b | 0.31 | – | 0.51 |
| e | 1.27BSC | | |
| L | 0.40 | – | 1.27 |
| L2 | 0.25BSC | | |
| θ | 0° | – | 8° |
| C | 0.10 | – | 0.25 |
| D2 | 3.30 REF. | | |
| E2 | 2.41 REF. | | |

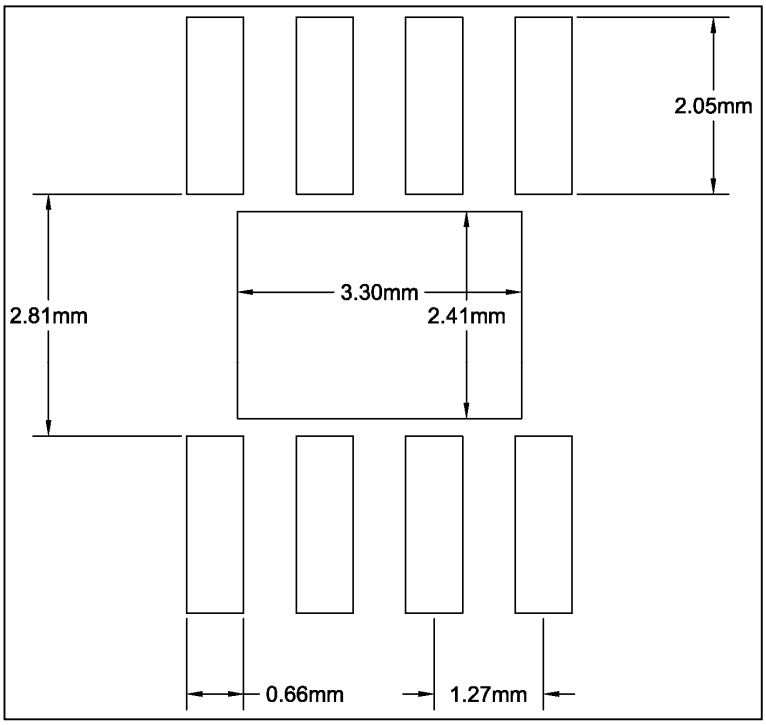



NOTE :

1. CONTROLLING DIMENSION : MM
2. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION.
4. REFERENCE DOCUMENT: JEDEC MS-012
5. THE SHAPE OF BODY AND THERMAL PAD SHOW DIFFERENT SHAPE AMONG DIFFERENT FACTORIES.

## RECOMMENDED LAND PATTERN

### SOP-8-EP




**Note:**

1. Land pattern complies to IPC-7351.
2. All dimensions in MM.
3. This document (including dimensions, notes & specs) is a recommendation based on typical circuit board manufacturing parameters. Since land pattern design depends on many factors unknown (eg. user's board manufacturing specs), user must determine suitability for use.

## REVISION HISTORY

| Revision | Detail Information | Date |
|---|---|---|
| 0A | Initial release | 2020.12.03 |
| A | Update EC table | 2021.07.20 |