SINGLE CHANNEL LINEAR LED DRIVER WITH HALL-EFFECT SWITCH AND FADE IN/OUT FUNCTION

May 2022

GENERAL DESCRIPTION

The IS32LT3168 is a single channel linear programmable current regulator capable of up to 200mA. It operates as a standalone LED driver configurable with external resistors; a single external resistor programs the current level, while another resistor programs the Fade In/Out ramp rate for the channel.

The IS32LT3168 also integrates a low-power and high-sensitivity omnipolar Hall-effect sensor for contactless switching of the LEDs. The Hall-effect switch operates with either a north or a south magnetic pole. For user application flexibility, the switch output polarity can be set by the dedicated POL pin; to assert when a magnet is present or when the magnetic field is removed.

This device features 124 steps Gamma-corrected Fade In and Fade Out algorithm. The output LED current gradually ramps up to the full source value after the ENB pin is asserted (pulled low) or the LED current gradually ramps down to zero when the ENB pin is de-asserted (pulled high). The fade ramp can be interrupted mid-cycle before completion of the ramp cycle. The ENB pin can be connected to either an external logic level for direct control, or the Hall-effect switch output for contactless control.

For 12V automotive applications the low dropout driver can support 1 to 3 LEDs per channel. It is offered in a small thermally enhanced SOP-8-EP package.

FEATURES

- Operating voltage 6.5V to 28V; maximum 36V
  - Withstand 40V load dump
- Super low standby current (50μA) when LED off
- Integrate omnipolar Hall-effect switch
- Hall-effect switch output
  - Drives additional circuits and/or LED drivers
  - Selectable output polarity
- Single channel current source
  - Programmable current via a single external resistor
  - Configurable from 20mA to 200mA
- ENB input pin for LED on/off control with Fade In/Out effect
  - Gamma-corrected Fade In/Out algorithm
  - Pull down resistors set Fade In/Out ramp time
  - PWM dimming control (fade is disabled)
- Fault Protection:
  - OUT pin shorted to GND
  - ISET pin shorted to GND
  - Thermal roll-off
  - Thermal shutdown
- SOP-8-EP package
- AEC-Q100 Qualified
- Operating temperature from -40°C ~ +125°C

APPLICATIONS

- Automotive Interior:
  - Glove box
  - Vanity mirror
  - Trunk light
  - Puddle lamp in doors

TYPICAL APPLICATION CIRCUIT

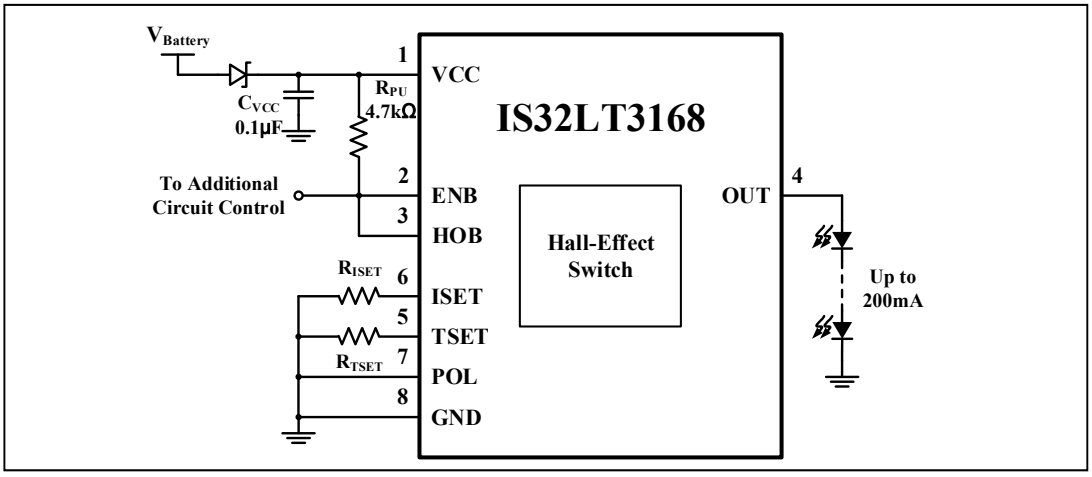
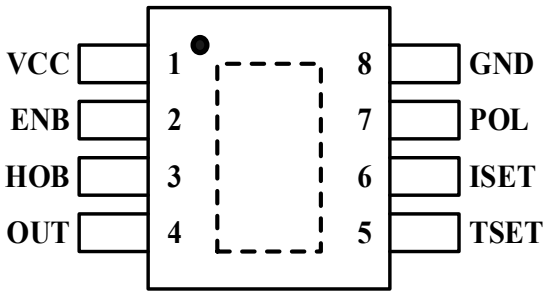


Figure 1 Typical Application Circuit

PIN CONFIGURATION

Package	Pin Configuration (Top view)
SOP-8-EP	

PIN DESCRIPTION

No.	Pin	Description
1	VCC	Power supply input pin. A 0.1μF low ESR X7R type ceramic bypass capacitor should be connected as close as possible between this pin and GND.
2	ENB	Input pin for LED on/off control. Pull it low to enable the output LED. When fade function is disabled by V_{TSET}=GND, this pin can be used for PWM dimming control.
3	HOB	Integrated Hall-effect switch output pin. Active low and open-drain structure.
4	OUT	Output current source channel.
5	TSET	Timing control for the Fade In/Out feature. Connect a resistor between this pin and GND to set the Fade In/Out time. Connect this pin directly to ground to disable the fade function for instant ON/OFF.
6	ISET	Output current setting for channel. Connect a resistor between this pin and GND to set the maximum output current.
7	POL	Polarity setting pin for the Hall-effect switch output HOB. When POL pin is floating, HOB pin will be active-low as the magnetic field is present to Hall-effect switch. When POL pin is pulled low, HOB pin will be active-low as the magnetic field is removed from Hall-effect switch.
8	GND	Ground pin.
	Thermal Pad	Must be connected to GND with sufficient copper plate for heat sink.

ORDERING INFORMATION
Automotive Range: -40°C to +125°C

Order Part No.	Package	QTY/Reel
IS32LT3168-GRLA3-TR	SOP-8-EP, Lead-free	2500

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ABSOLUTE MAXIMUM RATINGS

Voltage at VCC, OUT, ENB, HOB pins	-0.3V ~ +40V
Voltage at ISET, TSET, POL pins	-0.3V ~ +6.0V
Operating temperature, T_A=T_J	-40°C ~ +150°C
Maximum continuous junction temperature, $T_{J(MAX)}$	+150°C
Storage temperature range, T_{STG}	-65°C ~ +150°C
Package thermal resistance, junction to ambient (4-layer standard test PCB based on JEDEC standard), θ_{JA}	42.8°C/W
Package thermal resistance, junction to thermal PAD (4-layer standard test PCB based on JEDEC standard), θ_{JP}	1.41°C/W
Maximum power dissipation, P_{DMAX}	2.92W
ESD (HBM) ESD (CDM)	±2kV ±750V

Note 1: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

T_J = T_A = -40°C ~ +125°C, V_{CC}=6.5V~28V, refers to each condition description. Typical values are at T_J = T_A = 25°C.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{CC}	Supply voltage range		6.5		28	V
t_{PERIOD}	Period time of ultra-low power operation			50		ms
t_{AWAKE}	Awake time of ultra-low power operation			50		μs
I_{CC}	Quiescent supply current	ENB=High, LED off, average current, V_{CC}=12V		50	72	μA
		ENB=High, LED off, current during sleep period, V_{CC}=12V		45	65	μA
		ENB=Low, LED on, V_{CC}=12V, R_{ISET}=1kΩ, R_{TSET}=20kΩ		4	6	mA
t_{ON}	Startup time	V_{CC}> 6.5V to I_{OUT} > 90% of 100mA, POL = GND, ENB and HOB tied together and pulled up to V_{CC} via a resistor, R_{ISET} = 1kΩ, fade disabled (TSET = GND)		50		ms
I_{OUT_LIM}	Output limit current	V_{CC} -V_{OUT} =2V, OUT sourcing current, ISET pin connected to GND. V_{CC}=12V	-330	-255	-220	mA
I_{OUT}	Output current	R_{ISET} = 1kΩ, V_{CC} -V_{OUT} =1V, -40°C<T_J<+125°C	-105	-100	-95	mA
V_{HR_MIN}	Minimum headroom voltage	V_{CC} -V_{OUT}, I_{OUT}= -200mA			1.5	V
		V_{CC} -V_{OUT}, I_{OUT}= -100mA			1.0	V
E_{OUT}	Absolute current accuracy	-200mA≤I_{OUT}<-50mA, V_{CC} -V_{OUT} =2V, V_{CC}=12V	-6		6	%
g_{LINE}	Output current line regulation	I_{OUT} = -50mA, 6.5V<V_{CC}<18V, V_{OUT} = V_{CC}-2V (Note 2)	-0.2		0.2	mA/V
g_{LOAD}	Output current load regulation	2.5V< V_{OUT} <V_{CC}-2V, I_{OUT} = -50mA (Note 2)	-0.2		0.2	mA/V
t_{SL}	Current slew time	Current rise/fall between 10%~90%, TSET pin connected to GND, I_{OUT}= -150mA	3	7	15	μs
t_{TD_ON}	ENB current latency	Delay time between ENB falling edge to 10% of I_{OUT}		26	40	μs

ELECTRICAL CHARACTERISTICS (CONTINUE)

$T_J = T_A$ = -40°C ~ +125°C, V_{CC}=6.5V~28V, refers to each condition description. Typical values are at $T_J = T_A$ = 25°C.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{UVLO}	Undervoltage lock out V_{CC} voltage	V_{CC} rising release from UVLO		5.4	6.3	V
V_{UVLO_HY}	Undervoltage lock out hysteresis			200		mV
Logic Input TSET_UP, TSET_DN						
V_{TSET}	Voltage reference			1		V
T_{ACC}	Fade timing accuracy	*Neglecting the R_{TSET} Tolerance* R_{TSET}=20kΩ, T_J = 25°C	-5		5	%
Logic Input ENB, POL						
V_{IL_ENB}	ENB input logic low voltage				0.8	V
V_{IH_ENB}	ENB input logic high voltage		2			V
V_{PWM}	PWM signal voltage range on ENB		0		5.5	V
f_{PWM}	PWM frequency range on ENB	0V<V_{PWM}<5.5V	0		1	kHz
D_{PWM}	PWM duty cycle range on ENB	0V<V_{PWM}<5.5V	0		100	%
V_{IL_POL}	POL input low voltage				0.8	V
I_{LKPOL}	POL leakage current	POL = GND		80		nA
Hall-effect Switch and Switch Output, HOB						
B_{OPS}	South-polarity operating point	B_{FIELD}>B_{OPS}		40	70	G
B_{OPN}	North-polarity operating point	B_{FIELD}<B_{OPN}	-70	-40		G
B_{RPS}	South-polarity release point	B_{FIELD}<B_{RPS}	5	25		G
B_{RPN}	North-polarity release point	B_{FIELD}>B_{RPN}		-25	-5	G
B_{HYS}	Hysteresis	|B_{OPX}-B_{RPX}|	5	15	25	G
V_{HOB_ON}	HOB pin turn-on voltage	Sink current=20mA, |B_{FIELD}|>|B_{OPX}|, POL pin floating		180	500	mV
I_{HOB_LIM}	HOB pin current limit	T_J<T_J (Max.)	30		60	mA
t_{HOB_R}	HOB pin rising time	R_L=820Ω, C_{HOB}=20pF		200		ns
t_{HOB_F}	HOB pin falling time	R_L=820Ω, C_{HOB}=20pF		100		ns
PS_{HOB}	HOB pin power-on state	POL connected to GND or floating	High Impedance			-
Protection						
V_{SCD}	Short detect voltage	Measured at OUT	1.1		1.4	V
V_{SCD_HY}	Short detect voltage hysteresis	Measured at OUT		350		mV
t_{FD}	Fault detect persistence time	(Note 2)		25		us
T_{RO}	Thermal roll-off threshold	(Note 2)		145		°C
T_{SD}	Thermal shutdown threshold	Temperature increasing (Note 2)		165		°C
T_{HY}	Thermal shutdown hysteresis	(Note 2)		25		°C

Note 2: Guaranteed by design.

TYPICAL PERFORMANCE CHARACTERISTICS

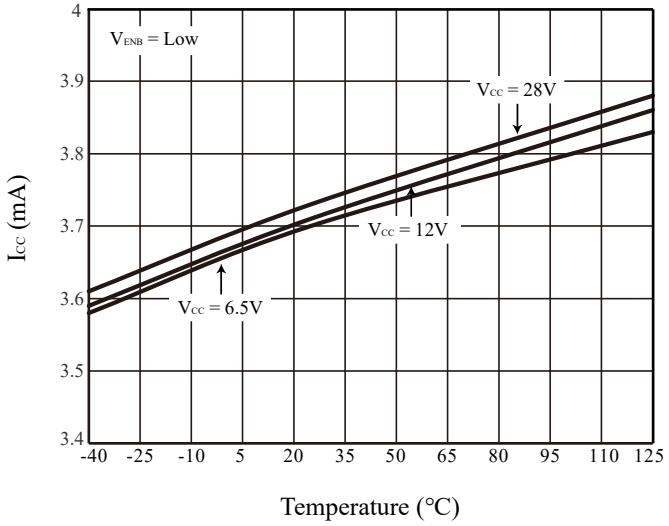


Figure 2 I_{CC} vs. Temperature

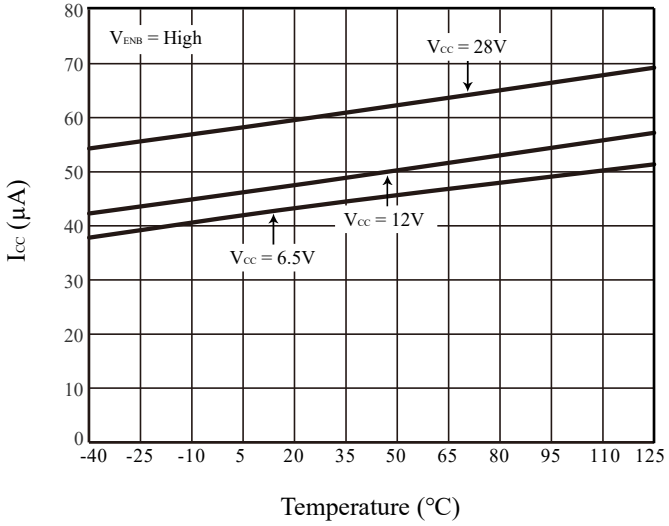


Figure 3 I_{CC} vs. Temperature

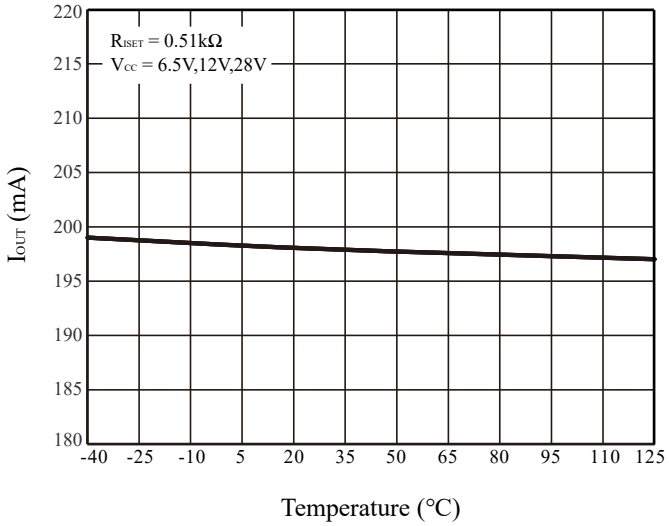


Figure 4 I_{OUT} vs. Temperature

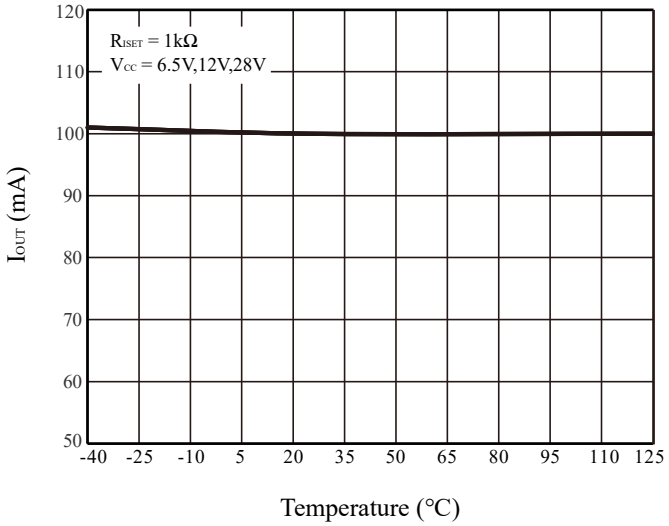


Figure 5 I_{OUT} vs. Temperature

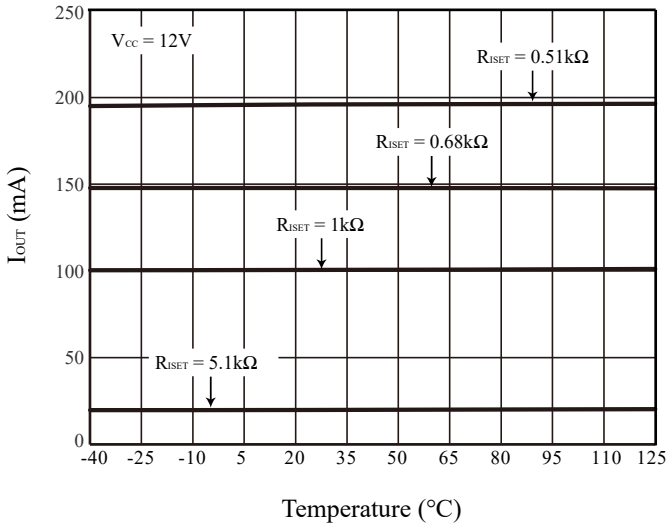


Figure 6 I_{OUT} vs. Temperature

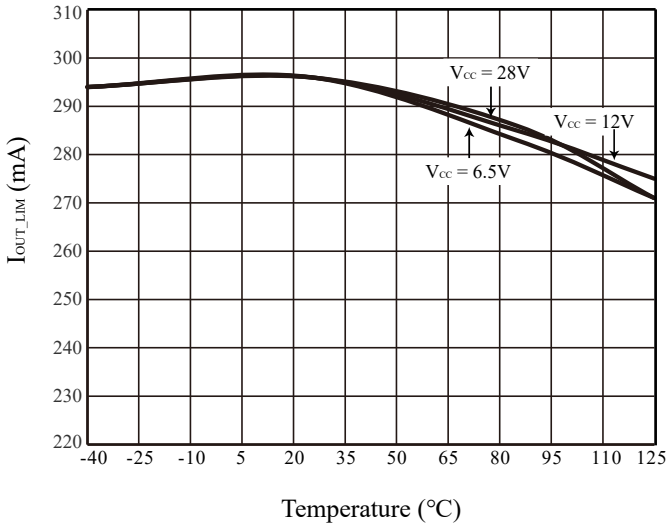


Figure 7 I_{OUT_LIM} vs. Temperature

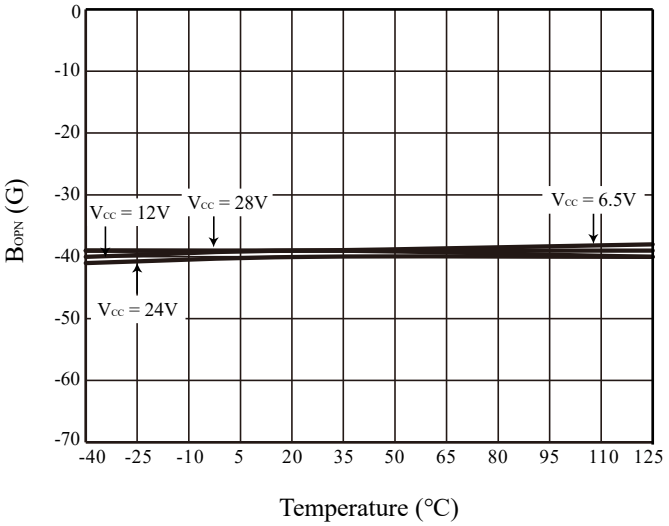


Figure 8 B_{OPN} vs. Temperature

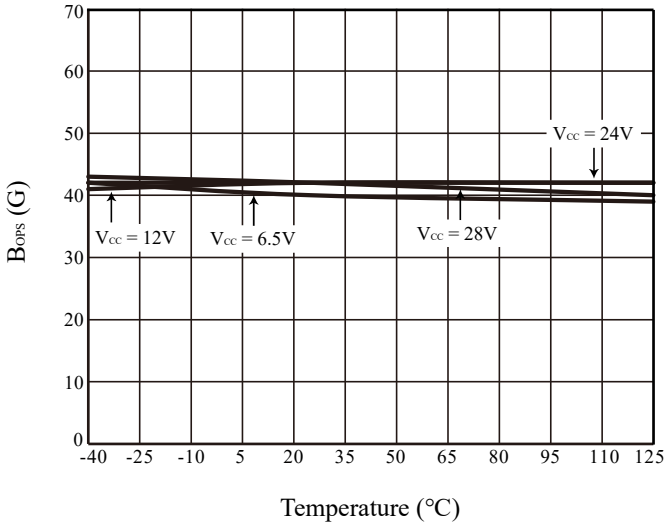


Figure 9 B_{OPS} vs. Temperature

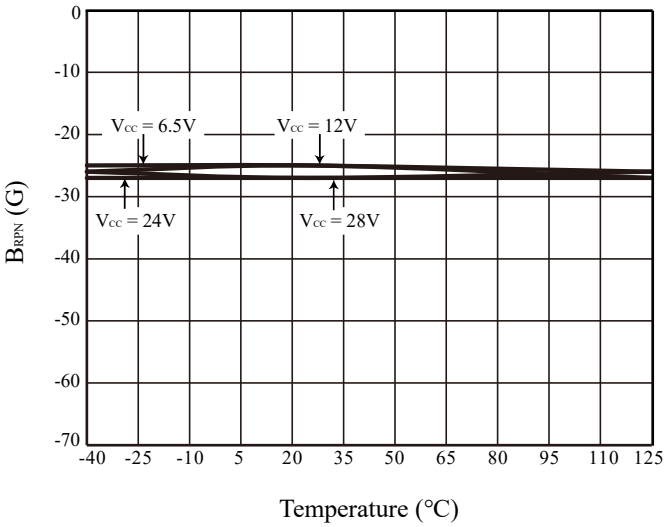


Figure 10 B_{RPN} vs. Temperature

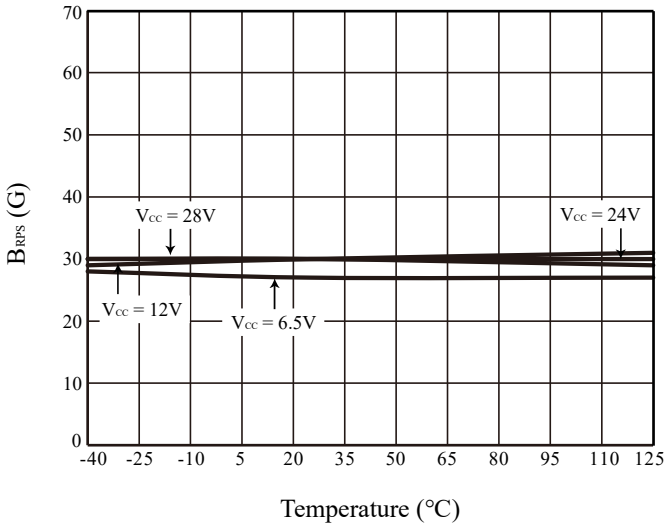


Figure 11 B_{RPS} vs. Temperature

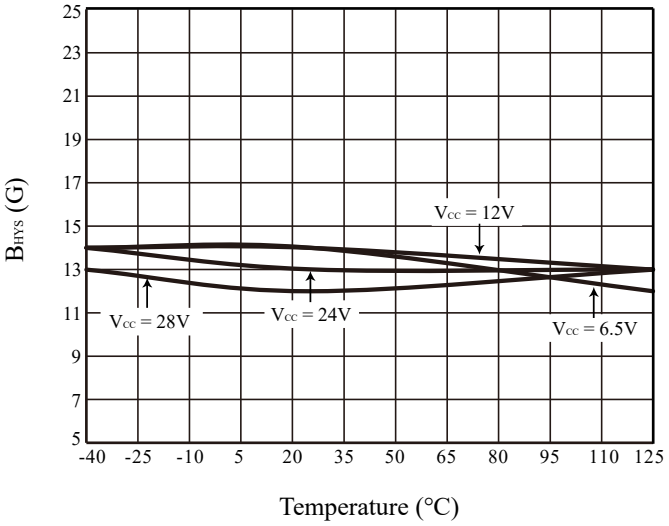


Figure 12 B_{HYS} vs. Temperature (North)

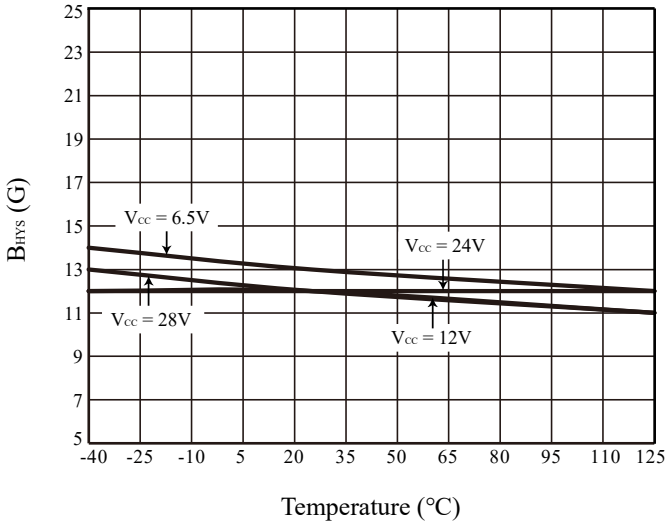


Figure 13 B_{HYS} vs. Temperature (South)

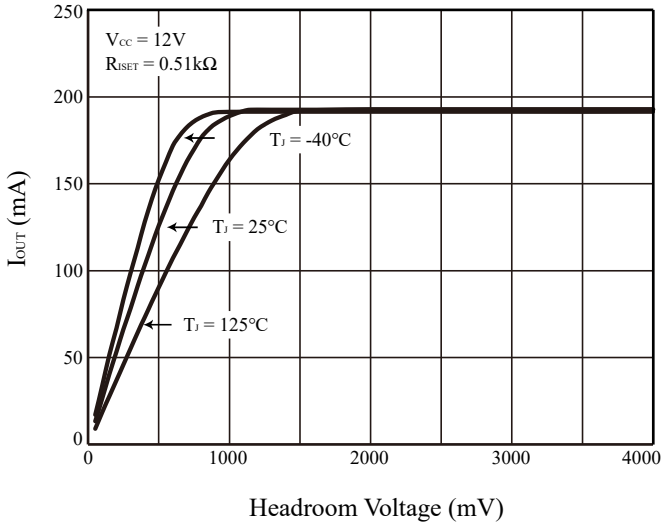


Figure 14 I_{OUT} vs. Headroom Voltage

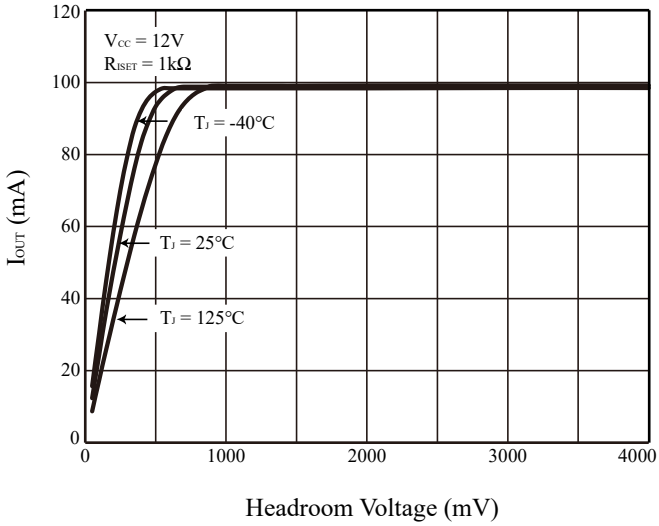


Figure 15 I_{OUT} vs. Headroom Voltage

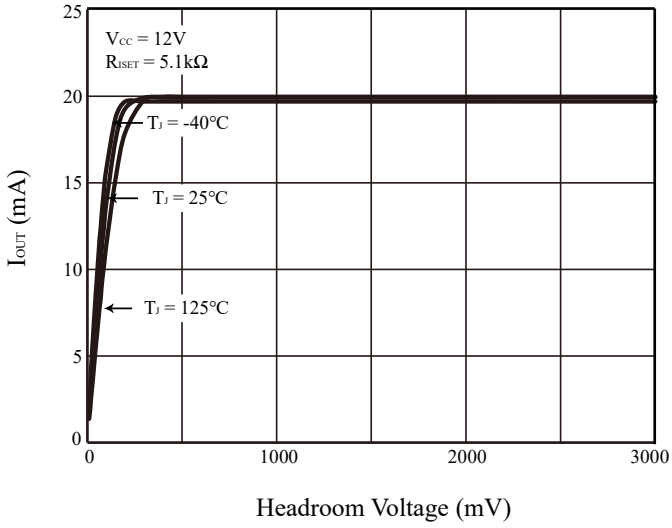


Figure 16 I_{OUT} vs. Headroom Voltage

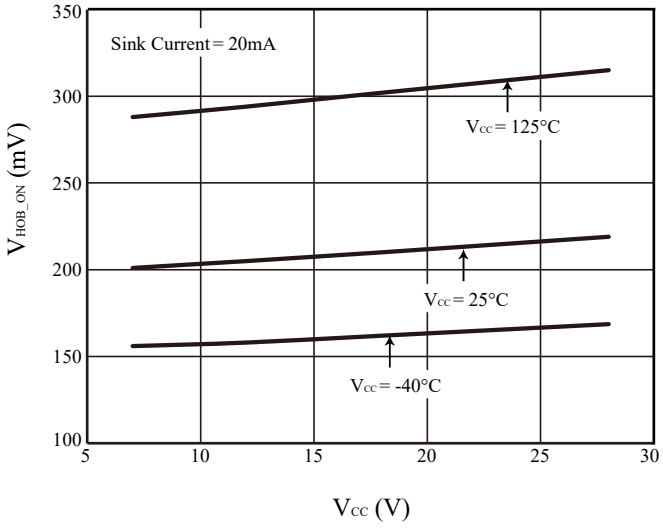


Figure 17 V_{HOB_ON} vs. V_{CC}

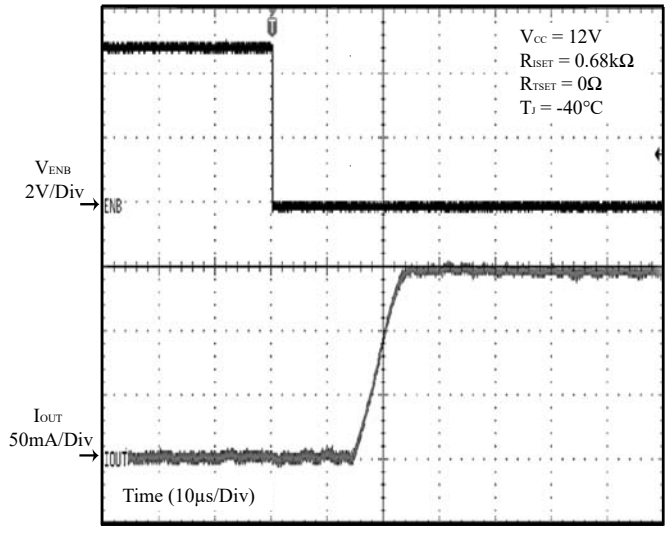


Figure 18 ENB Pulled Low

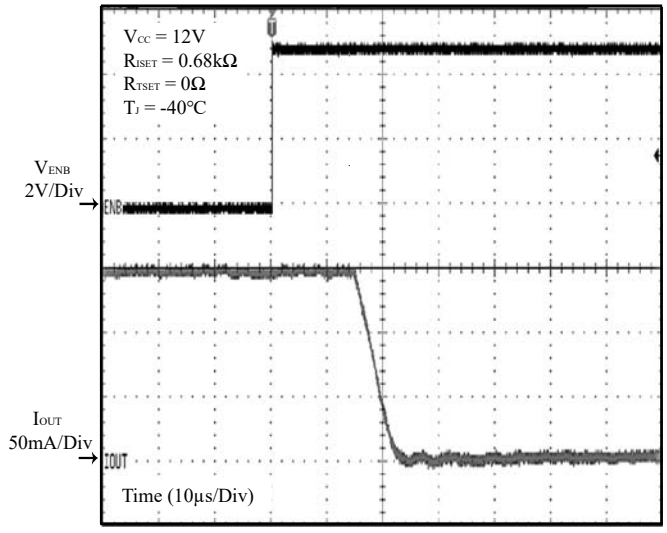


Figure 19 ENB Pulled High

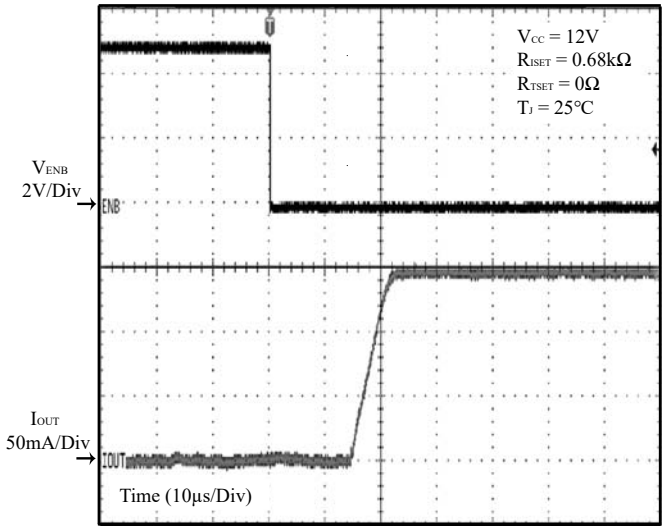


Figure 20 ENB Pulled Low

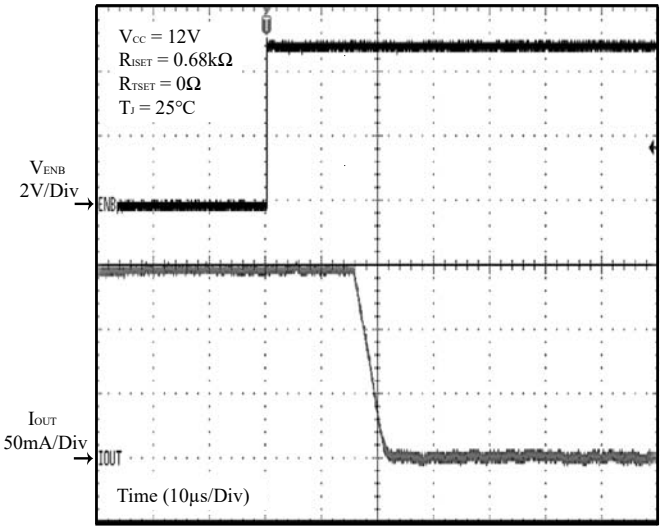


Figure 21 ENB Pulled High

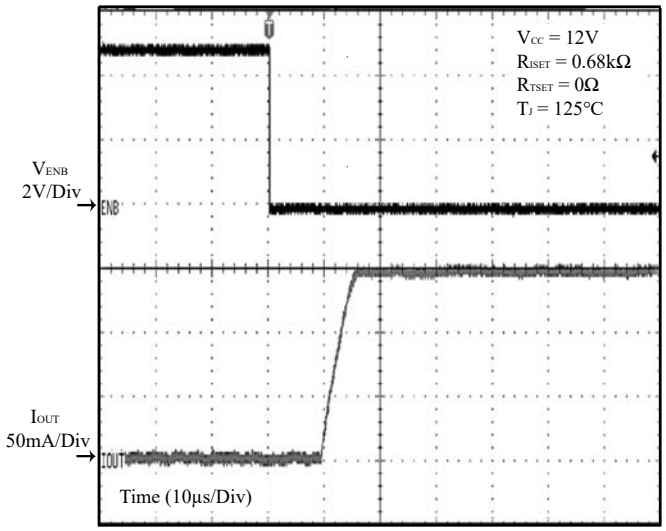


Figure 22 ENB Pulled Low

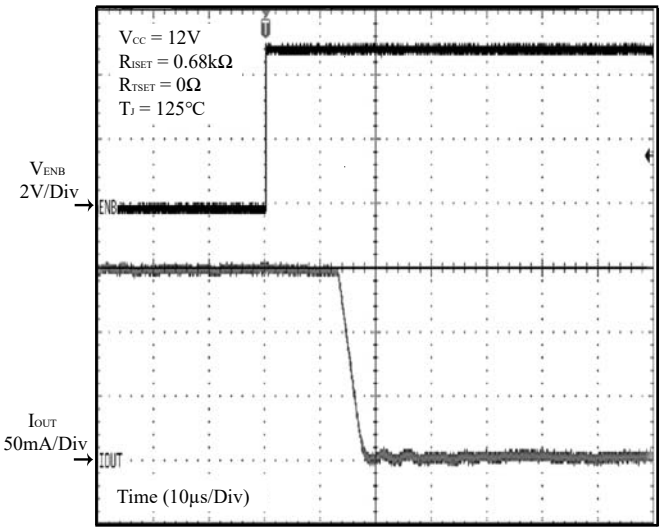
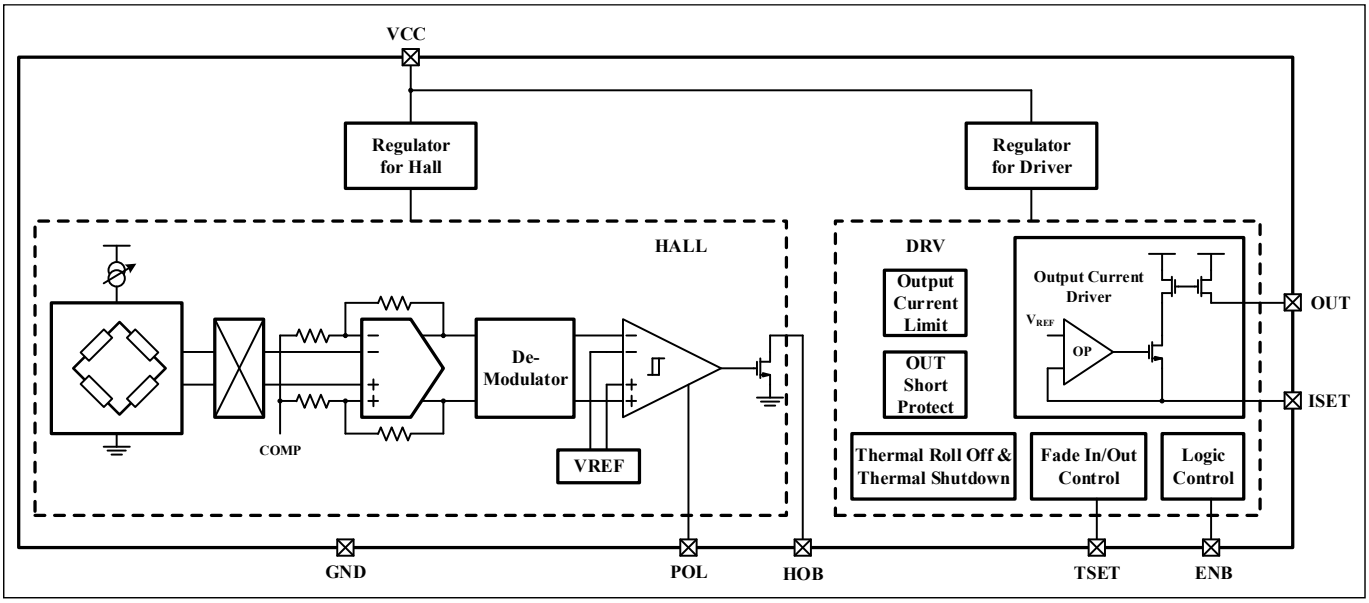


Figure 23 ENB Pulled High

FUNCTIONAL BLOCK DIAGRAM



APPLICATION INFORMATION

The IS32LT3168 is a single channel linear current driver optimized to drive a high current LED string for automotive illumination applications which is frequently toggled between the ON and OFF condition. The LED activity can be controlled by the integrated omnipolar Hall-effect switch, external circuits or by a PWM signal from an MCU. In addition, a programmable fade ramp timing function provides flexibility in setting different Fade In and Fade Out ramp duration periods. The fade ramp cycle can be interrupted mid-cycle before the ramp has completed, Figure 24.

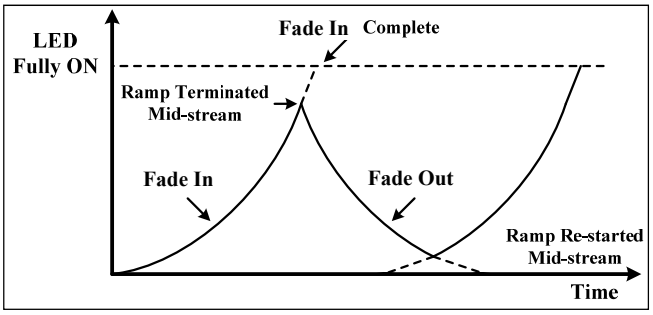


Figure 24 Fade Ramp Interrupted Mid-Cycle

OUTPUT CURRENT SETTING

A single programming resistor (R_{ISET}) controls the maximum output current for the output channel. The programming resistor can be computed using the following Equation (1):

$$R_{ISET} = \frac{100}{I_{OUT}} \qquad (1)$$

($0.5k\Omega \le R_{ISET} \le 5k\Omega$)

Where I_{OUT} is the desired LED current in Amp and R_{ISET} is in Ω.

The device is protected from an output overcurrent condition caused by an accidental short circuit of the ISET pin, by internally limiting the maximum current in the event of an ISET short circuit to 255mA (Typ.).

ENB PIN AND FADE IN/OUT OPERATION

The ENB pin is an active-low logic input for enabling/disabling the LED driver output with Fade In/Out effect. When the ENB pin is pulled low (below V_{IL_ENB}), the LED driver output current will gradually ramp up from zero to the final value as programmed by the R_{ISET} resistor, connected to the ISET pin (Fade In effect). When pulled high (above V_{IH_ENB}), the LED driver output current will gradually ramp down from the final value to zero (Fade Out effect). The time period over which the ramping happens is determined by the resistor (R_{TSET}) connected to the TSET pin. The output current will ramp up (or down) in 124 steps, with integrated gamma correction for a linear visual lumen output of the LED. The ramping can be interrupted mid-cycle by the ENB pin toggling.

Table 1 ENB vs. LED Driver State

ENB State	LED State
Low	LED Driver Enabled; Device is in Active
High	LED Driver Disabled; Device Operates in Ultra-low Power

If the fade function is disabled (the TSET pin grounded to get "instant on", see "FADE TIME SETTING" description), an external PWM signal on the ENB pin can be used to modulate the output current to dim the LED light output. The PWM dimming output current is based on the PWM signal's duty cycle and can be calculated by the following Equation:

$$I_{OUT_PWM} = I_{OUT} \times (1 - D_{PWM}) \qquad (2)$$

Where D_{PWM} is the duty cycle of the PWM signal. Note that, since the ENB pin is active-low, the PWM dimming output current is inversely proportional to the PWM signal's duty cycle.

The recommended frequency range of the external PWM signal is 100Hz~1kHz and the duty cycle range can be from 0 to 100%. Due to the output current slew rate control for EMI consideration plus propagation delay time from PWM falling edge to the output activity, a lower frequency PWM signal will provide a better dimming linearity and contrast ratio.

OMNIPOLAR HALL-EFFECT SWITCH

The integrated Hall-effect switch in the IS32LT3168 is an omnipolar switch. The HOB pin is an open drain output of the Hall-effect switch, so it requires an external pull-up resistor for logic high output. The HOB output transistor is capable of sinking current up to a current limit I_{HOB_LIM}. It switches when a magnetic field B_{FIELD} perpendicular to the Hall-effect switch exceeds the operate point threshold, B_{OPx} ($B_{FIELD} > B_{OPS}$ or $B_{FIELD} < B_{OPN}$). When magnetic field is reduced below the release point, B_{RPx} ($B_{FIELD} < B_{RPS}$ or $B_{FIELD} > B_{RPN}$), the HOB output goes to the opposite state. The difference in the magnetic operate and release points is the hysteresis, B_{HYS}, of the device. This built-in hysteresis allows clean switching of the output even in the presence of external mechanical vibration and electrical noise.

The HOB output state polarity is determined by the POL pin, reference Table 2. The POL pin should only be tied to ground or floated to achieve the desired output polarity. The HOB output can be used to control either the LED driver and/or external circuit.

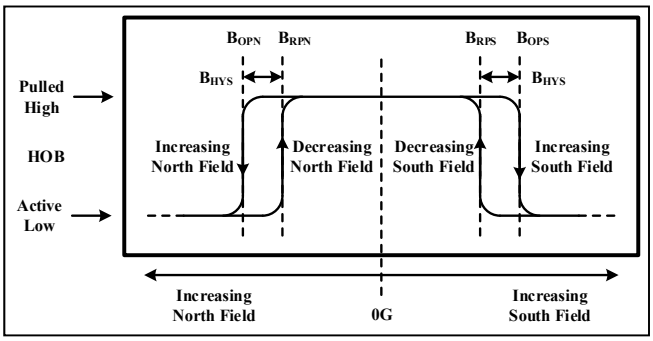


Figure 25 Hall Switch Output (HOB) State versus Magnetic Field (POL = Float)

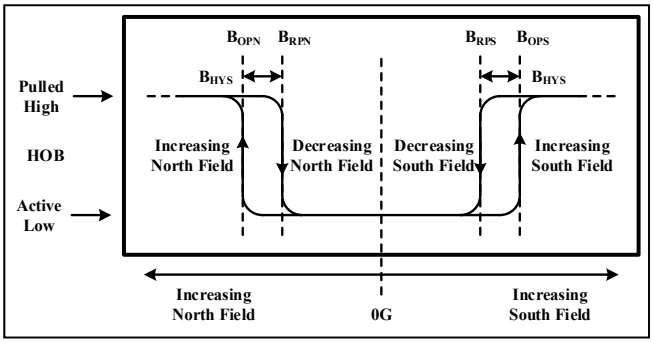


Figure 26 Hall Switch Output (HOB) State versus Magnetic Field (POL = GND)

When the HOB pin is tied to the ENB pin with a pull-up resistor to VCC, the Hall-effect switch can directly control the LED driver output. Since the LED driver output is only enabled when the ENB pin is pulled low, changing the HOB polarity changes the LED behavior between off (POL = GND) and on (POL = Float) with a magnet present.

Table 2 POL vs. HOB and LED State

POL	$\|B_{FIELD}\|$	HOB State	LED State
GND	> $\|B_{OPx}\|$	Pulled High	Off
	< $\|B_{RPx}\|$	Low	On
Float	> $\|B_{OPx}\|$	Low	On
	< $\|B_{RPx}\|$	Pulled High	Off

ULTRA-LOW POWER OPERATION

To achieve ultra-low power operation, the integrated Hall-effect switch operates periodically. It's activated for a short period of time (t_{AWAKE}) and deactivated (sleep) for the remainder of the period time (t_{PERIOD}). The short duration active state allows for Hall-effect switch stabilization prior to sampling of the magnetic field and latching the state on the HOB output. The HOB output state is kept during the sleep period; updates to the HOB output only occur at the end of the active (t_{AWAKE}) pulse. The ultra-low power operation of the Hall-effect switch operates independently of the LED driver state. Therefore, the device's supply current is not significantly affected by the HOB output state when the LED driver is disabled (ENB=High).

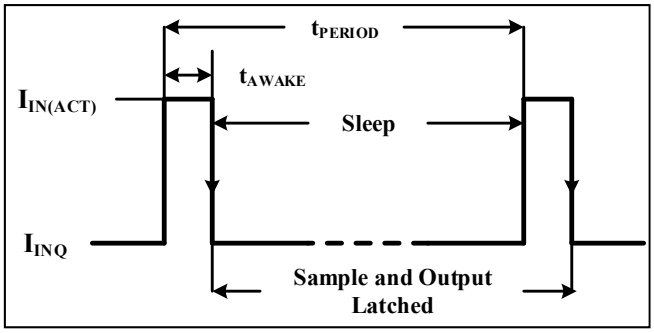


Figure 27 Ultra-low Power Operation Timing

At power-up, device power-on occurs once t_{ON} has elapsed. During the time prior to t_{ON}, and after VCC releasing from UVLO, the HOB output state is high impedance, regardless of the POL configuration. After t_{ON} has elapsed, the Hall-effect switch will sample a t_{AWAKE} cycle before the first t_{SLEEP} cycle and the HOB output will correspond with the applied magnetic field for $|B_{FIELD}| > |B_{OPx}|$ or $|B_{FIELD}| < |B_{RPx}|$.

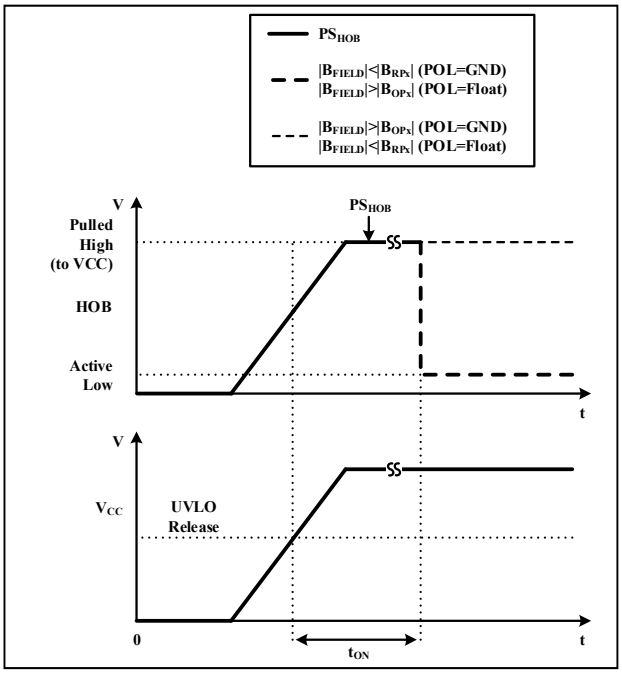


Figure 28 Power-on Timing

FADE TIME SETTING

The fade time (In or Out) is set by an external programming resistor, R_{TSET}, connected between the TSET pin and GND. The fade time (In or Out) in seconds is calculated by Equation (3):

$$t_{FADE} \approx R_{TSET} \times 16 \times 10^{-6} \qquad (3)$$

For example, R_{TSET}=20kΩ, Fade In/Out time is about 0.32s.

Note: In order to get the optimized effect, the recommended fading time is between 3.5s (R_{TSET}= 219kΩ) and 0.25s (R_{TSET}= 15.6kΩ).

If the TSET pin is tied directly to GND, the fade function is disabled and the ramp time is about 7μs (Typ.), or “instant on”.

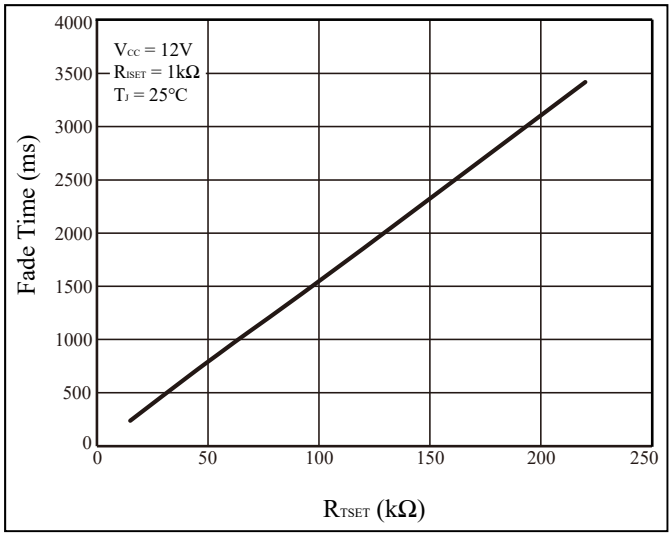


Figure 29 Fade Time vs. R_{TSET}

GAMMA CORRECTION

In order to perform a better visual LED fading effect, we recommend using a Gamma-corrected value to set the LED intensity. This results in a reduced number of steps for the LED intensity setting, but causes the change in intensity to appear more linear to the human eye.

Gamma correction, also known as gamma compression or encoding, is used to encode linear luminance to match the non-linear characteristics of display. Gamma correction will vary the step size of the current such that the fading of the light appears linear to the human eye. Even though there may be 2000 linear steps for the fading algorithm, when gamma corrected, the actual number of steps could be as low as 124.

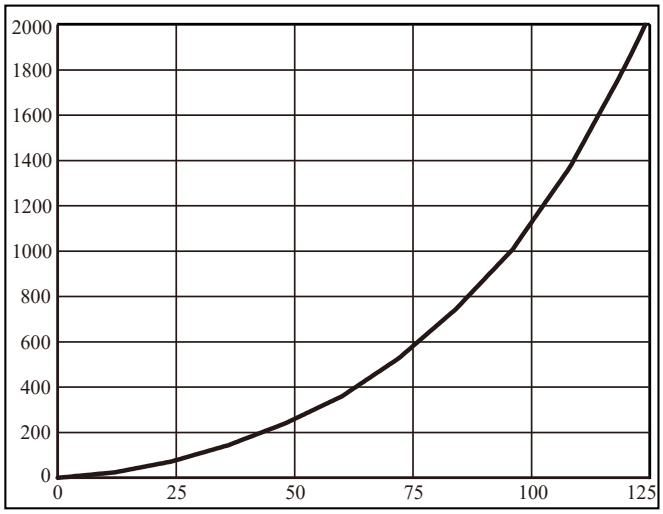


Figure 30 Gamma Correction(124 Steps)

Table 3 124 Gamma Steps Correction

C(0)	C(1)	C(2)	C(3)	C(4)	C(5)	C(6)	C(7)
0	2	4	6	8	10	12	14
C(8)	C(9)	C(10)	C(11)	C(12)	C(13)	C(14)	C(15)
16	18	20	22	24	28	32	36
C(16)	C(17)	C(18)	C(19)	C(20)	C(21)	C(22)	C(23)
40	44	48	52	56	60	64	68
C(24)	C(25)	C(26)	C(27)	C(28)	C(29)	C(30)	C(31)
72	78	84	90	96	102	108	114
C(32)	C(33)	C(34)	C(35)	C(36)	C(37)	C(38)	C(39)
120	126	132	138	144	152	160	168
C(40)	C(41)	C(42)	C(43)	C(44)	C(45)	C(46)	C(47)
176	184	192	200	208	216	224	232
C(48)	C(49)	C(50)	C(51)	C(52)	C(53)	C(54)	C(55)
240	250	260	270	280	290	300	310
C(56)	C(57)	C(58)	C(59)	C(60)	C(61)	C(62)	C(63)
320	330	340	350	360	374	388	402
C(64)	C(65)	C(66)	C(67)	C(68)	C(69)	C(70)	C(71)
416	430	444	458	472	486	500	514
C(72)	C(73)	C(74)	C(75)	C(76)	C(77)	C(78)	C(79)
528	546	564	582	600	618	636	654
C(80)	C(81)	C(82)	C(83)	C(84)	C(85)	C(86)	C(87)
672	690	708	726	744	766	788	810
C(88)	C(89)	C(90)	C(91)	C(92)	C(93)	C(94)	C(95)
832	854	876	898	920	942	964	986
C(96)	C(97)	C(98)	C(99)	C(100)	C(101)	C(102)	C(103)
1008	1038	1068	1098	1128	1158	1188	1218
C(104)	C(105)	C(106)	C(107)	C(108)	C(109)	C(110)	C(111)
1248	1278	1308	1338	1368	1406	1444	1482
C(112)	C(113)	C(114)	C(115)	C(116)	C(117)	C(118)	C(119)
1520	1558	1596	1634	1672	1710	1748	1788
C(120)	C(121)	C(122)	C(123)	C(124)			
1828	1870	1912	1956	2000			

FAULT DETECTION

An output shorted to GND fault is detected if the output voltage on the channel drops below the low voltage threshold V_{SCD} and remains below the threshold for t_{FD} time. The channel (OUT) with the short condition will reduce its output current to 3.6mA (Typ.). When the short condition is removed, the output current will recover to original value.

When the ISET pin is shorted to GND and output current is larger than limit value, about 255mA (typ.), the output current will be clamped. Once the short fault condition is removed, the output current will recover to its original value.

THERMAL ROLL-OFF

The output current will be equal to the set value as long as the die temperature of the IC remains below 145°C (Typ.). If the die temperature exceeds this threshold, the output current of the device will begin to reduce at a rate of 3.25%/°C (Typ.) until thermal shutdown (Typ. 165°C).

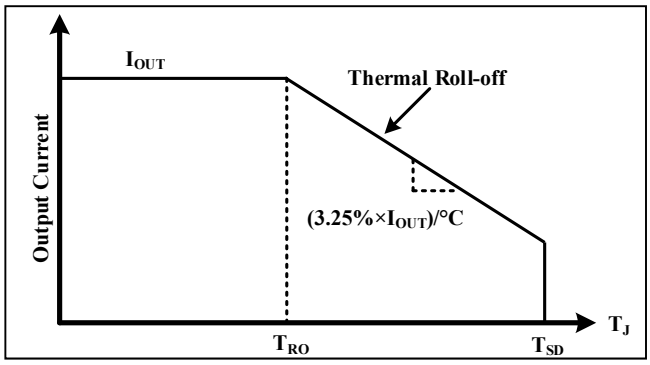


Figure 31 Thermal Roll-off

THERMAL SHUTDOWN

In the event that the die temperature exceeds 165°C, the output current will go to the "OFF" state. At this point, the IC presumably begins to cool off. Restart after IC cooled to <140°C.

THERMAL CONSIDERATIONS

The package thermal resistance, θ_{JA}, determines the amount of heat that can pass from the silicon die to the surrounding ambient environment. The θ_{JA} is a measure of the temperature rise created by power dissipation and is usually measured in degree Celsius per watt (°C/W). The junction temperature, T_J, can be calculated by the rise of the silicon temperature, ΔT, the power dissipation, P_D, and the package thermal resistance, θ_{JA}, as in Equation (4):

$$P_D = V_{CC} \times I_{CC} + (V_{CC} - V_{LED}) \times I_{OUT} \qquad (4)$$

and,

$$T_J = T_A + \Delta T = T_A + P_D \times \theta_{JA} \qquad (5)$$

Where I_{CC} is the IC quiescent current, V_{CC} is the supply voltage, V_{LED} is the voltage from VOUT to GND and T_A is the ambient temperature.

When operating the chip at high ambient temperatures, or when driving maximum load current, care must be taken to avoid exceeding the package power dissipation limits. The maximum power dissipation can be calculated using the following Equation (6):

$$P_{D(MAX)} = \frac{150°C - 25°C}{\theta_{JA}} \qquad (6)$$

So,

$$P_{D(MAX)} = \frac{150°C - 25°C}{42.8°C/W} \approx 2.92W$$

Figure 32, shows the power derating of the IS32LT3168 on a JEDEC board (in accordance with JESD 51-5 and JESD 51-7) standing in still air.

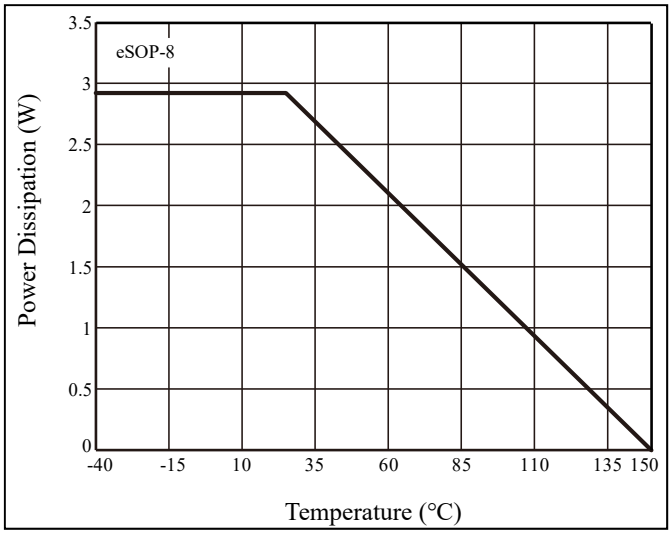


Figure 32 Dissipation Curve

The thermal resistance is achieved by mounting the IS32LT3168 on a standard FR4 double-sided printed circuit board (PCB) with a copper area of a few square inches on each side of the board under the IS32LT3168. Multiple thermal vias, as shown in Figure 33, help to conduct the heat from the exposed pad of the IS32LT3168 to the copper on each side of the board. The thermal resistance can be reduced by using a metal substrate or by adding a heatsink or thicker copper plane.

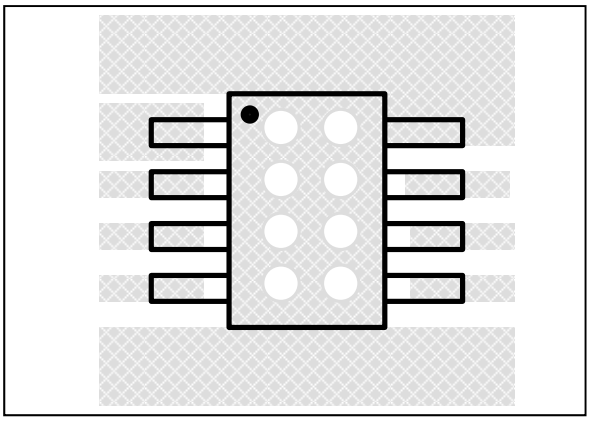


Figure 33 Board Via Layout For Thermal Dissipation

CLASSIFICATION REFLOW PROFILES

Profile Feature	Pb-Free Assembly
Preheat & Soak Temperature min (Tsmin) Temperature max (Tsmax) Time (Tsmin to Tsmax) (ts)	150°C 200°C 60-120 seconds
Average ramp-up rate (Tsmax to Tp)	3°C/second max.
Liquidous temperature (TL) Time at liquidous (tL)	217°C 60-150 seconds
Peak package body temperature (Tp)*	Max 260°C
Time (tp)** within 5°C of the specified classification temperature (Tc)	Max 30 seconds
Average ramp-down rate (Tp to Tsmax)	6°C/second max.
Time 25°C to peak temperature	8 minutes max.

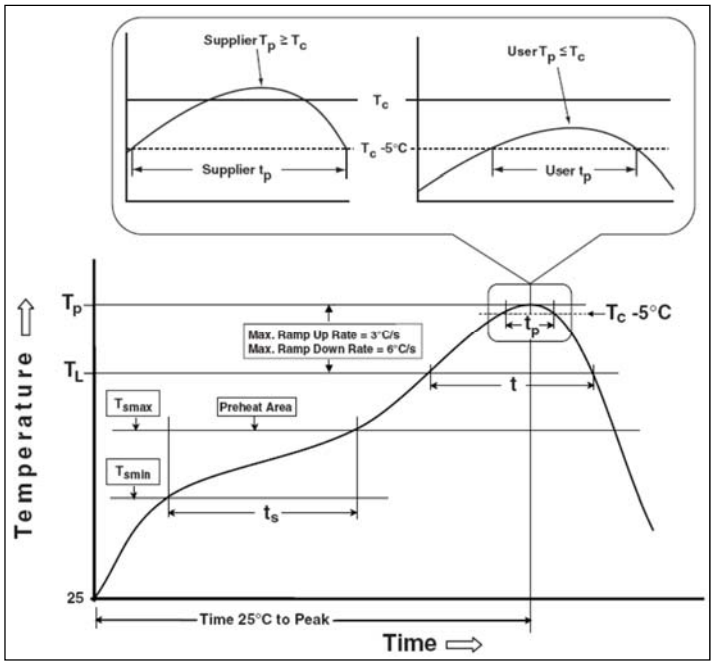
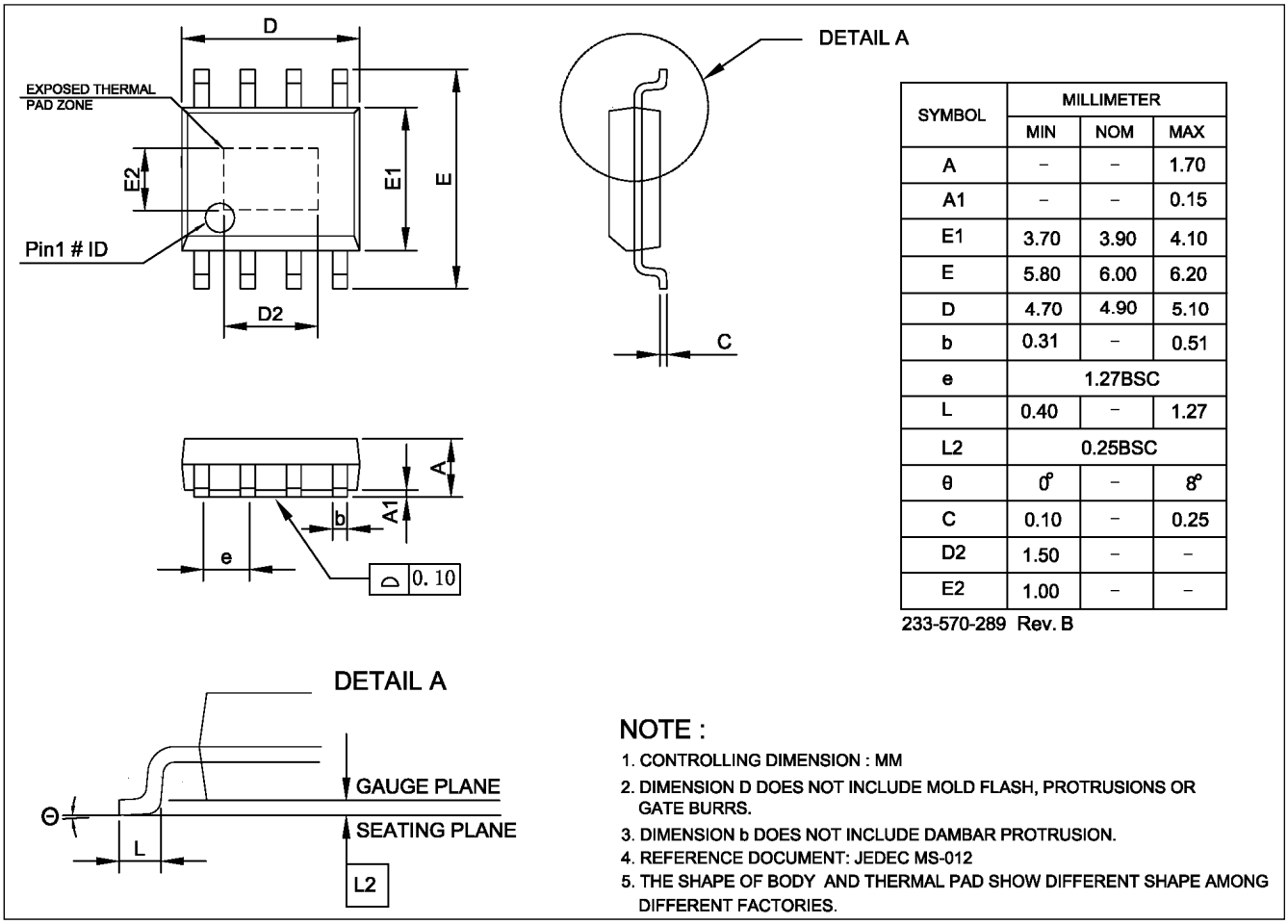


Figure 34 Classification Profile

PACKAGE INFORMATION

SOP-8-EP



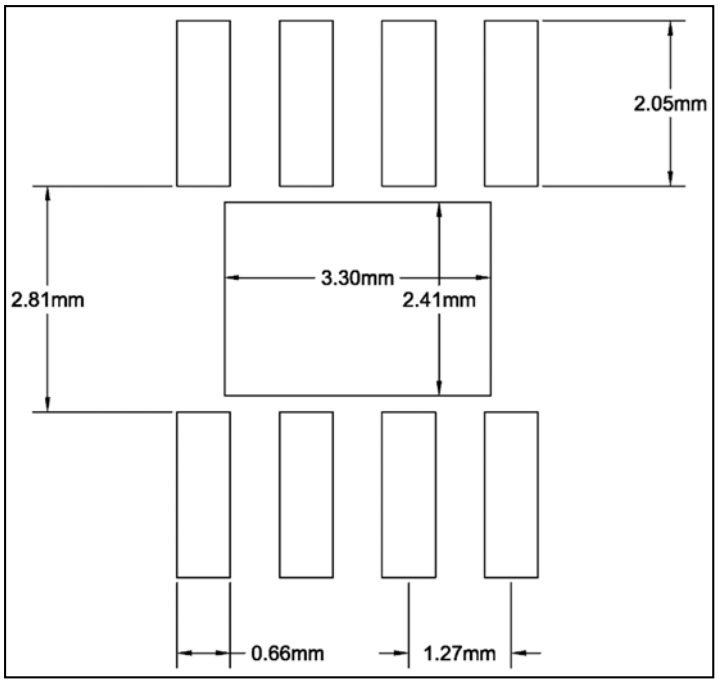
SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	–	–	1.70
A1	–	–	0.15
E1	3.70	3.90	4.10
E	5.80	6.00	6.20
D	4.70	4.90	5.10
b	0.31	–	0.51
e	1.27BSC		
L	0.40	–	1.27
L2	0.25BSC		
θ	0°	–	8°
C	0.10	–	0.25
D2	1.50	–	–
E2	1.00	–	–

233-570-289 Rev. B

NOTE :

1. CONTROLLING DIMENSION : MM
2. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION.
4. REFERENCE DOCUMENT: JEDEC MS-012
5. THE SHAPE OF BODY AND THERMAL PAD SHOW DIFFERENT SHAPE AMONG DIFFERENT FACTORIES.

RECOMMENDED LAND PATTERN



Note:

1. Land pattern complies to IPC-7351.
2. All dimensions in MM.
3. This document (including dimensions, notes & specs) is a recommendation based on typical circuit board manufacturing parameters. Since land pattern design depends on many factors unknown (eg. User's board manufacturing specs), user must determine suitability for use.

REVISION HISTORY

Revision	Detail Information	Date
A	Initial release	2022.05.17