# ISL88031

Quintuple Voltage Monitor

FN8227
Rev 2.00
June 9, 2009

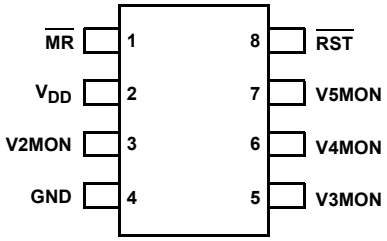
The ISL88031 is a quintuple voltage-monitoring supervisor combining competitive reset threshold accuracy and low power consumption. This device combines popular functions such as Power-On Reset, Undervoltage Supply Supervision, reset signaling and Manual Reset. Monitoring up to five different voltages in a small 8 Ld MSOP package, the ISL88031 devices can help to lower system cost, reduce board space requirements, and increase the reliability of multi-voltage systems.

Low $V_{DD}$ detection circuitry protects the user's system from low voltage conditions, resetting the system when $V_{DD}$ or any of the other monitored power supply voltages fall below their respective minimum voltage thresholds. The reset signal remains asserted until all of these voltages return to proper operating levels and stabilize.

With two of the five voltage monitors being preset for common supplies, users can adjust the threshold voltages of the third, fourth, and fifth voltage monitors in order to meet specific system level requirements.

## Pinout

**ISL88031**
**(8 LD MSOP)**
TOP VIEW




## Features

- Quintuple Voltage Monitoring
- Fixed-Voltage Options Allow Precise Monitoring of +5.0V, +3.3V, +3.0V, +2.5V and +1.8V Power Supplies
- Adjustable Voltage Inputs Monitor Voltages > 0.6V
- 120ms Nominal Reset Pulse Width
- Manual Reset Capability
- Reset Signals Valid Down to $V_{DD}$ = 1V
- Accurate ±1.8% Voltage Threshold
- Immune to Power-Supply Transients
- Low 19µA Maximum Supply Current at 5V
- Pb-Free (RoHS Compliant)

## Applications

- Telecom and Datacom Systems
- Routers and Servers
- Access Concentrators
- Cable/Satellite Applications
- Desktop and Notebook Computer Systems
- Data Storage Equipment
- Set-Top Boxes
- Industrial Equipment
- Multi-Voltage Systems

## Ordering Information

| PART NUMBER (Notes 1, 2) | PART MARKING | $V_{TH1}$ | $V_{TH2}$ | TEMP RANGE (°C) | PACKAGE (Pb-free) | PKG. DWG. # |
|---|---|---|---|---|---|---|
| ISL88031IU8HFZ | AMA | 4.634V | 3.078V | -40 to +85 | 8 Ld MSOP | M8.118 |
| ISL88031IU8HEZ | ANZ | 4.634V | 2.955V | -40 to +85 | 8 Ld MSOP | M8.118 |
| ISL88031IU8HCZ | APR | 4.634V | 2.333V | -40 to +85 | 8 Ld MSOP | M8.118 |
| ISL88031IU8HAZ | APS | 4.634V | 1.683V | -40 to +85 | 8 Ld MSOP | M8.118 |
| ISL88031IU8ECZ | APT | 2.866V | 2.333V | -40 to +85 | 8 Ld MSOP | M8.118 |
| ISL88031IU8EAZ | APZ | 2.866V | 1.683V | -40 to +85 | 8 Ld MSOP | M8.118 |

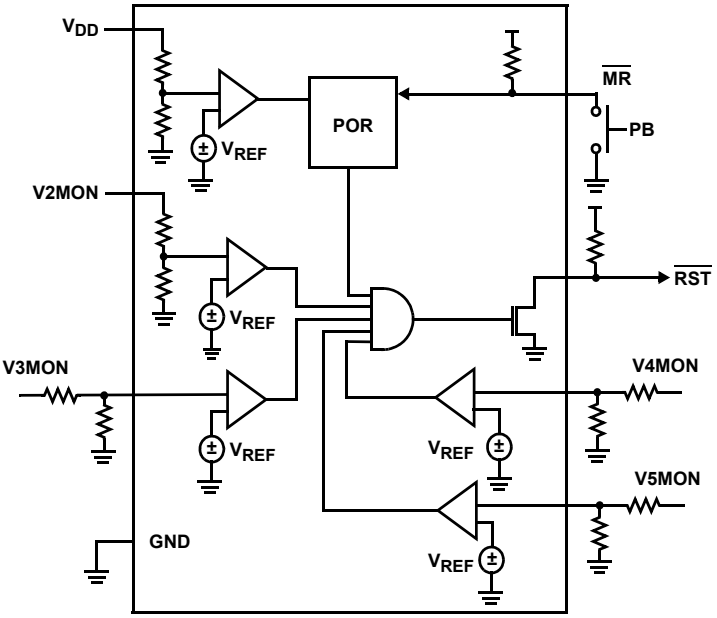
NOTES:

1. Add "-TK" suffix for tape and reel. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

## Pin Descriptions

| PIN NUMBER | PIN NAME | FUNCTION |
|---|---|---|
| 1 | $\overline{MR}$ | Active-Low Open Drain Manual Reset Input with internal pull-up resistor |
| 2 | $V_{DD}$ | Chip Bias Input and integrated preset undervoltage monitor |
| 3 | V2MON | Second Preset Undervoltage Monitor Input |
| 4 | GND | Ground |
| 5 | V3MON | Adjustable Third Undervoltage Monitor Input |
| 6 | V4MON | Adjustable Fourth Undervoltage Monitor Input |
| 7 | V5MON | Adjustable Fifth Undervoltage Monitor Input |
| 8 | $\overline{RST}$ | Active-Low Open Drain Reset Output |

## Functional Block Diagram



## Absolute Maximum Ratings

Temperature Under Bias . . . . . .-40°C to +125°C
Voltage on any Pin With Respect to Gnd. . . . . .-1.0V to +7V
DC Output Current. . . . . 5mA

## Recommended Operating Conditions

Operating Temperature Range (Industrial) . . . . . .-40°C to +85°C
Storage Temperature Range . . . . . .-65°C to +150°C

## Thermal Information

Thermal Resistance (Typical, Note 3) $\theta_{JA}$ (°C/W)
8 Ld MSOP Package . . . . . 175
Pb-free Reflow Profile . . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

*CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.*

NOTE:

3. $\theta_{JA}$ is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.

## Electrical Specifications

Over the recommended operating conditions, unless otherwise specified. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

| SYMBOL | PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| $V_{DD}$ | Supply Voltage Range | | 2.0 | | 5.5 | V |
| $I_{DD1}$ | $V_{DD}$ Supply Current | $V_{DD}$ = 5.0V | | 14 | 19 | µA |
| $I_{DD2}$ | V2MON Input Current | V2MON = 3.3V | | 5.5 | 7 | µA |
| $I_{DDA}$ | V3MON, V4MON, V5MON Input Current | V3MON, V4MON, V5MON = 1.0V | | 19 | 100 | nA |
| **VOLTAGE THRESHOLDS** | | | | | | |
| $V_{TH1}$ | ISL88031IU8HxZ Fixed Voltage Trip Point for $V_{DD}$ | +25°C | 4.550 | 4.634 | 4.717 | V |
| | | 0°C to +70°C | 4.461 | 4.634 | 4.807 | V |
| | | -40°C to +85°C | 4.453 | 4.634 | 4.815 | V |
| | ISL88031IU8ExZ Fixed Voltage Trip Point for $V_{DD}$ | +25°C | 2.814 | 2.866 | 2.917 | V |
| | | 0°C to +70°C | 2.759 | 2.866 | 2.973 | V |
| | | 40°C to +85°C | 2.754 | 2.866 | 2.978 | V |
| $V_{TH1HYST}$ | Hysteresis of $V_{TH1}$ | $V_{TH1}$ = 4.64V | | 46 | | mV |
| | | $V_{TH1}$ = 2.90V | | 29 | | mV |
| $V_{TH2}$ | ISL88031IU8xFZ Fixed Voltage Trip Point for V2MON | +25°C | 3.022 | 3.078 | 3.133 | V |
| | | 0°C to +70°C | 2.963 | 3.078 | 3.193 | V |
| | | -40°C to +85°C | 2.958 | 3.078 | 3.198 | V |
| | ISL88031IU8xEZ Fixed Voltage Trip Point for V2MON | +25°C | 2.901 | 2.955 | 3.008 | V |
| | | 0°C to +70°C | 2.845 | 2.955 | 3.065 | V |
| | | -40°C to +85°C | 2.840 | 2.955 | 3.070 | V |
| | ISL88031IU8xCZ Fixed Voltage Trip Point for V2MON | +25°C | 2.291 | 2.333 | 2.375 | V |
| | | 0°C to +70°C | 2.246 | 2.333 | 2.420 | V |
| | | -40°C to +85°C | 2.242 | 2.333 | 2.424 | V |
| | ISL88031IU8xAZ Fixed Voltage Trip Point for V2MON | +25°C | 1.652 | 1.683 | 1.713 | V |
| | | 0°C to +70°C | 1.620 | 1.683 | 1.746 | V |
| | | -40°C to +85°C | 1.617 | 1.683 | 1.749 | V |

**Electrical Specifications** Over the recommended operating conditions, unless otherwise specified. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested. **(Continued)**

| SYMBOL | PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| $V_{TH2HYST}$ | Hysteresis of $V_{TH2}$ | $V_{TH2}$ = 3.09V | | 37 | | mV |
| | | $V_{TH2}$ = 2.92V | | 29 | | mV |
| | | $V_{TH2}$ = 2.32V | | 23 | | mV |
| | | $V_{TH2}$ = 1.69V | | 17 | | mV |
| $V_{REF}$ | $V_{TH}$ for V3MON, V4MON, V5MON Adj. Reset Threshold Voltage | +25°C | 0.589 | 0.600 | 0.611 | V |
| | | 0°C to +70°C | 0.578 | 0.600 | 0.622 | V |
| | | -40°C to +85°C | 0.577 | 0.600 | 0.623 | V |
| $V_{REFHYST}$ | Hysteresis Voltage | | | 3 | | mV |
| **RESET** | | | | | | |
| $V_{OL}$ | Reset Output Voltage Low | $V_{DD} \geq$ 3.3V, Sinking 2.5mA | | 0.05 | 0.40 | V |
| | | $V_{DD}$ < 3.3V, Sinking 1.5mA | | 0.05 | 0.40 | V |
| $t_{RPD}$ | $V_{TH}$ to Reset Asserted Delay | | | 6 | | µs |
| $t_{POR}$ | POR Timeout Delay | | 80 | 120 | 180 | ms |
| $C_{LOAD}$ | Load Capacitance on Reset Pins | | | 5 | | pF |
| **MANUAL RESET** | | | | | | |
| $V_{MRL}$ | $\overline{MR}$ Input Voltage Low | | | | 0.8 | V |
| $V_{MRH}$ | $\overline{MR}$ Input Voltage High | | $V_{DD}$ - 0.6 | | | V |
| $t_{MR}$ | $\overline{MR}$ Minimum Pulse Width | | 550 | | | ns |
| $R_{PU}$ | Internal Pull-Up Resistor | | | 10 | | kΩ |

## Pin Descriptions

### $\overline{RST}$

The $\overline{RST}$ output is an open drain output, which is asserted low whenever:

1. the device is initially powered up to 1V or,
2. $V_{DD}$, V2MON, V3MON, V4MON, or V5MON fall below their minimum voltage sense level.

### $\overline{MR}$

The $\overline{MR}$ input is an active low debounced input to which a user can connect a push-button to add manual reset capability or use a signal to pull low. $\overline{MR}$ has an internal pull-up resistor.

### $V_{DD}$

The $V_{DD}$ pin is the IC power supply terminal. The voltage at this pin is compared against an internal factory-programmed voltage trip point, $V_{TH1}$. $\overline{RST}$ is first asserted low when the device is initially powered and $V_{DD}$ < 1V and then at any time thereafter when $V_{DD}$ falls below $V_{TH1}$. The device is designed with hysteresis to help prevent chattering due to noise and is immune to brief power-supply transients.

### V2MON

The V2MON input is the second preset monitored voltage that causes the $\overline{RST}$ output to go low when the voltage on V2MON falls below $V_{TH2}$.

### V3MON, V4MON, and V5MON

The VxMON inputs provide monitoring and UV compliance of three additional voltages through resistor dividers. A reset is issued on the ISL88031 if the voltage on any VxMON falls below the internal $V_{REF}$ of 0.6V.

## Principles of Operation

The ISL88031 device provides those functions needed for monitoring critical voltages, such as power-supply and battery functions in microprocessor systems. It provides such features as Power-On Reset control, Supply Voltage Supervision, and Manual Reset Assertion. The integration of all these features along with competitive reset threshold accuracy and low power consumption, makes the ISL88031 device suitable for a wide

variety of applications needing multi-voltage monitoring. See Figure 1 for the typical application diagram..

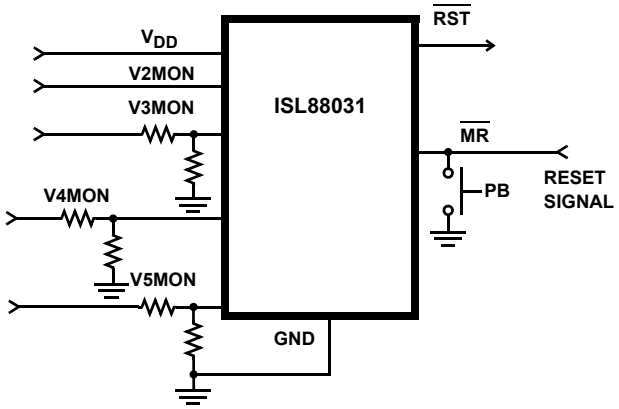



**FIGURE 1. TYPICAL APPLICATION DIAGRAM**

### *Low Voltage Monitoring*

During normal operation, the ISL88031 monitors the voltage levels of $V_{DD}$, V2MON, V3MON, V4MON, and V5MON. If the voltage on any of these five inputs falls below their respective voltage trip points, a reset is asserted ($\overline{RST}$ = low) to prevent the microprocessor from operating during a power failure or brownout condition. This reset signal remains low until the voltages exceeds the voltage threshold settings for the reset time delay period $t_{POR}$.

The ISL88031 allows users to customize the minimum voltage sense level for three of the five monitored voltages. For example, the user can adjust the voltage input trip point ($V_{TRIP}$) for V3MON, V4MON and V5MON inputs. To do this, connect an external resistor divider network to the VxMON pin in order to set the trip point to some other voltage above 600mV according to Equation 1:

$$V_{TRIP} = 0.6V \times R_1 + R_2/R_2 \quad \text{(EQ. 1)}$$

### *Power-On Reset (POR)*

Applying power to the ISL88031 activates a POR circuit, which makes the reset pin(s) active (i.e. RST goes high while $\overline{RST}$ goes low). These signals provide several benefits:

- It prevents the system microprocessor from starting to operate with insufficient voltage.
- It prevents the processor from operating prior to stabilization of the oscillator.
- It ensures that the monitored device is held out of operation until internal registers are properly loaded.
- It allows time for an FPGA to download its configuration prior to initialization of the circuit.

The reset signal remains active until $V_{DD}$ rises above the minimum voltage sense level for time period $t_{POR}$. This ensures that the supply voltage has stabilized to sufficient operating levels.

### *Manual Reset*

The manual-reset input ($\overline{MR}$) allows the user to trigger a reset by using a push-button switch or by signaling the input low. The $\overline{MR}$ input is an active low debounced input. Reset is asserted if the $\overline{MR}$ pin is pulled low to less than 100mV for the minimum $\overline{MR}$ pulse width or longer while the push-button is closed. After $\overline{MR}$ is released, the reset output remains asserted low for $t_{POR}$ (200ms) and then is released.

Figures 2 and 3 illustrate the ISL88031's operation. Figure 4 shows the ISL88031EVAL1, the evaluation platform for this family of voltage monitors. Figures 5 and 6 illustrate the $\overline{RST}$ output response times.

## *The ISL88031EVAL1 and Applications*

The ISL88031EVAL1 supports all variants of the ISL88031 devices, enabling evaluation of basic functional operation and common application implementations. Figure 4 illustrates the ISL88031EVAL1 in schematic and photographic forms. The ISL88031EVAL1 has two isolated circuits; the left circuit is populated with the ISL88031IU8HFZ ($V_{DD}$ $V_{TH1}$ = 4.64V, V2MON $V_{TH2}$ = 3.08V). The right circuit is unpopulated for the user to customize to provide a specific voltage monitoring solution with the accompanying loose packed variants.

With adequate bias on the two preset and the three adjustable monitor inputs, the $\overline{RST}$ output will release to pull high indicating that all supplies are compliant for a minimum of $t_{POR}$. For the ISL88031EVAL1 as shipped, the $V_{DD}$ and V2MON nominal thresholds are as previously noted with the voltage thresholds being monitored by V3MON, V4MON and V5MON being nominally 1.990V, 1.44V and 0.95V respectively.

### *Special Application Considerations*

Using good decoupling practices on bias and other monitoring inputs will prevent transients (i.e. due to switching noises and short duration droops in the supply voltage) from causing unwanted resets.

In unusually noisy environments or situations where unwanted signals may be injected into adjustable VMONx pins, lowering the node impedance and/or positioning a small valued filter capacitor as close to the pin as possible can increase noise immunity.

Although the internal ISL88031 threshold references are guaranteed over the full temp range, accuracy errors due to external component tolerances and distribution losses will occur. High tolerance resistors and layout for extreme accuracy and critical performance must be considered.

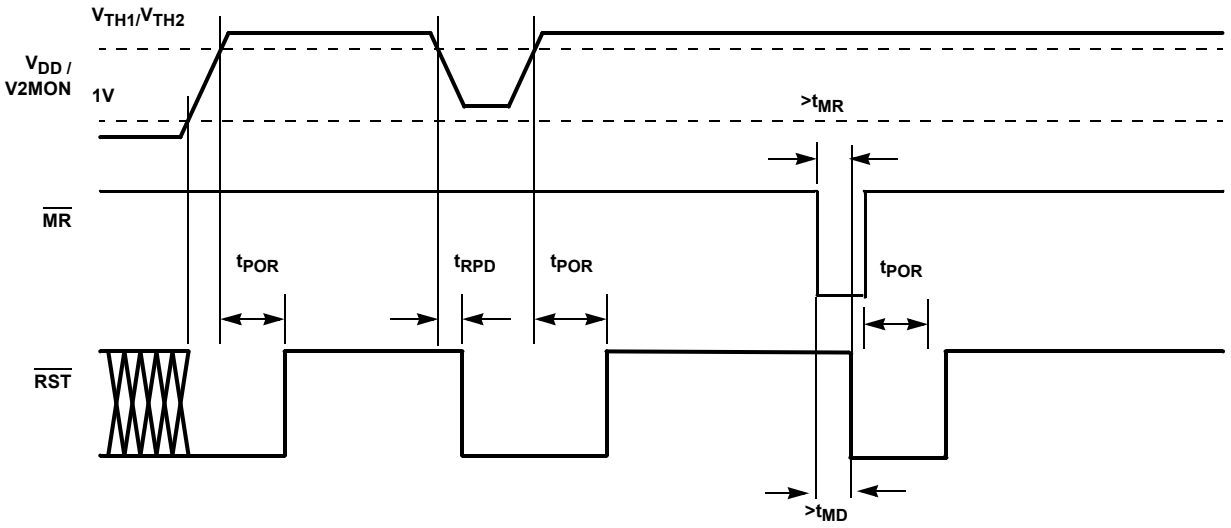



FIGURE 2. POWER SUPPLY MONITORING DIAGRAM

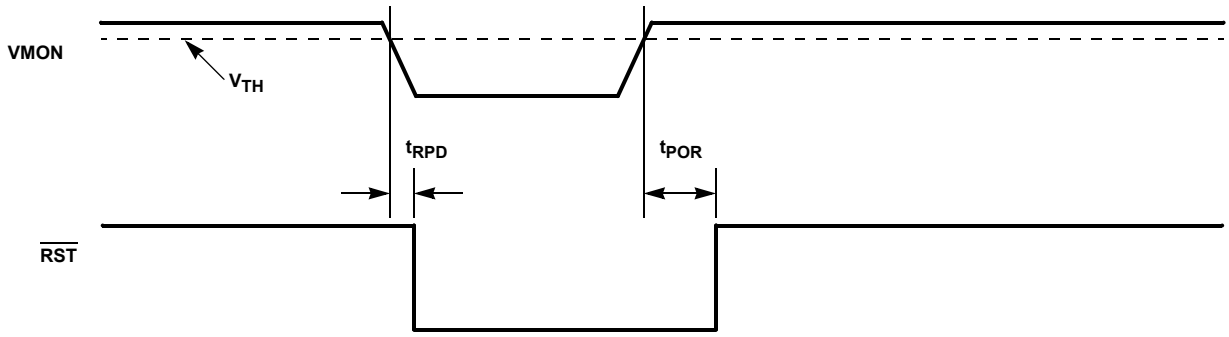
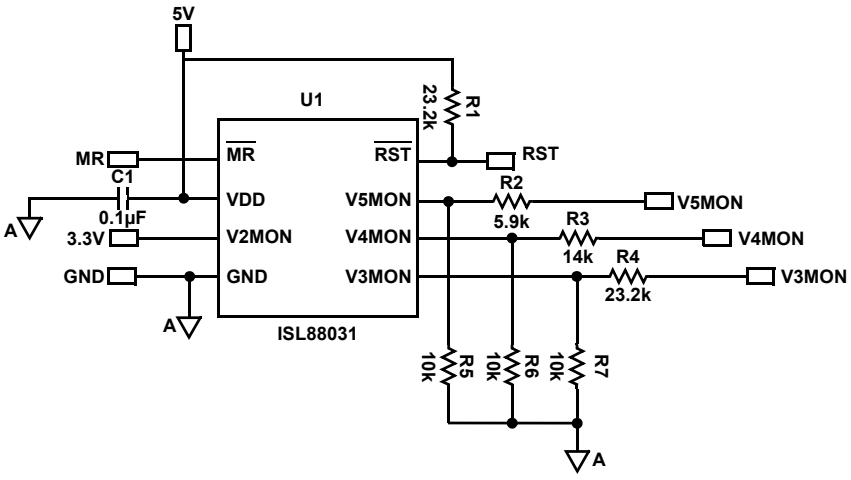



FIGURE 3. VOLTAGE MONITORING DIAGRAM



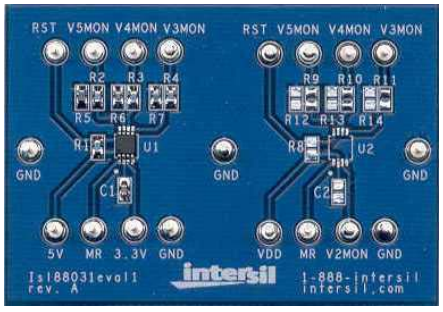




FIGURE 4. ISL88031EVAL1 SCHEMATIC AND PHOTOGRAPH

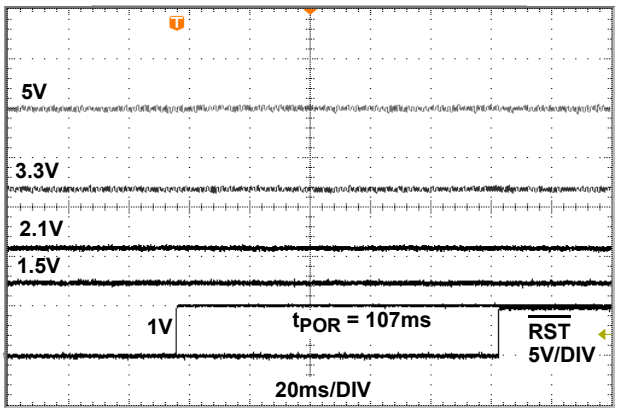



FIGURE 5. ISL88031 $t_{POR}$

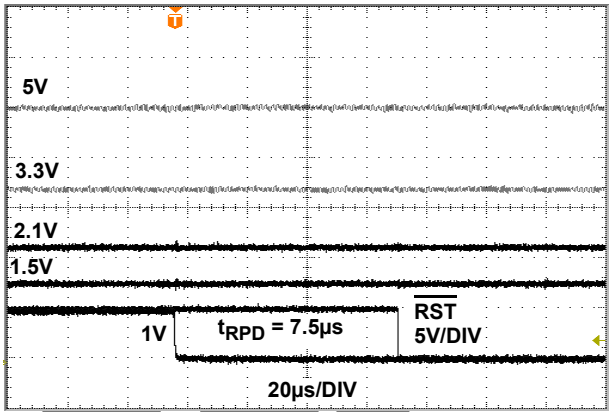



FIGURE 6. ISL88031 $t_{RPD}$

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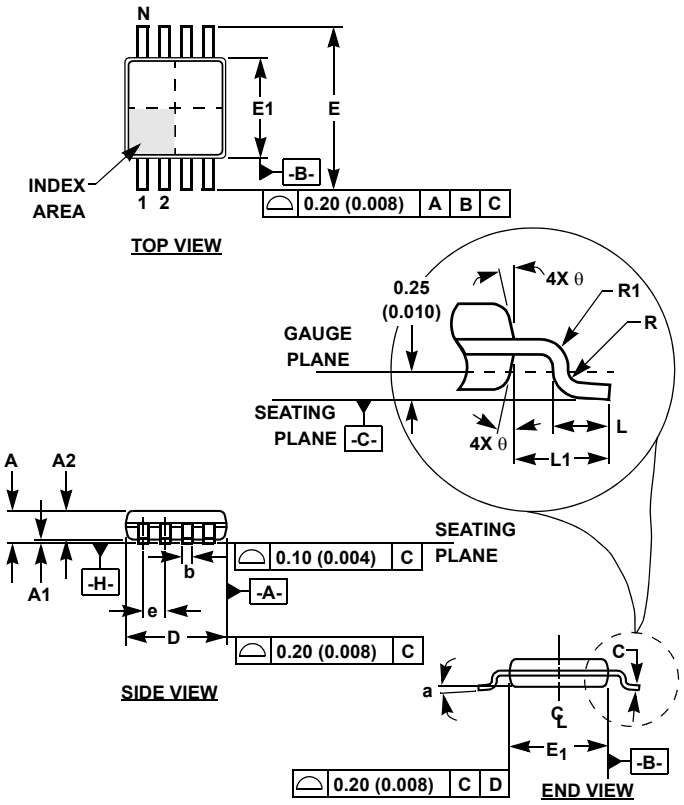
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## *Mini Small Outline Plastic Packages (MSOP)*




### M8.118 (JEDEC MO-187AA)

**8 LEAD MINI SMALL OUTLINE PLASTIC PACKAGE**

| SYMBOL | INCHES | | MILLIMETERS | | NOTES |
|---|---|---|---|---|---|
| | MIN | MAX | MIN | MAX | |
| A | 0.037 | 0.043 | 0.94 | 1.10 | - |
| A1 | 0.002 | 0.006 | 0.05 | 0.15 | - |
| A2 | 0.030 | 0.037 | 0.75 | 0.95 | - |
| b | 0.010 | 0.014 | 0.25 | 0.36 | 9 |
| c | 0.004 | 0.008 | 0.09 | 0.20 | - |
| D | 0.116 | 0.120 | 2.95 | 3.05 | 3 |
| E1 | 0.116 | 0.120 | 2.95 | 3.05 | 4 |
| e | 0.026 BSC | | 0.65 BSC | | - |
| E | 0.187 | 0.199 | 4.75 | 5.05 | - |
| L | 0.016 | 0.028 | 0.40 | 0.70 | 6 |
| L1 | 0.037 REF | | 0.95 REF | | - |
| N | 8 | | 8 | | 7 |
| R | 0.003 | - | 0.07 | - | - |
| R1 | 0.003 | - | 0.07 | - | - |
| 0 | $5^o$ | $15^o$ | $5^o$ | $15^o$ | - |
| $\alpha$ | $0^o$ | $6^o$ | $0^o$ | $6^o$ | - |

Rev. 2 01/03

NOTES:

1. These package dimensions are within allowable dimensions of JEDEC MO-187BA.
2. Dimensioning and tolerancing per ANSI Y14.5M-1994.
3. Dimension “D” does not include mold flash, protrusions or gate burrs and are measured at Datum Plane. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E1” does not include interlead flash or protrusions and are measured at Datum Plane. [- H -] Interlead flash and protrusions shall not exceed 0.15mm (0.006 inch) per side.
5. Formed leads shall be planar with respect to one another within 0.10mm (0.004) at seating Plane.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. Dimension “b” does not include dambar protrusion. Allowable dambar protrusion shall be 0.08mm (0.003 inch) total in excess of “b” dimension at maximum material condition. Minimum space between protrusion and adjacent lead is 0.07mm (0.0027 inch).
10. Datums [-A -] and [- B -] to be determined at Datum plane [- H -].
11. Controlling dimension: MILLIMETER. Converted inch dimensions are for reference only.