Click here to ask an associate for production status of specific part numbers.

MAX16165/MAX16166

Highly Integrated, 4-Channel Sequencer and Supervisor

General Description

The MAX16165/MAX16166 monitor up to five voltages and sequence up to four voltages. These devices provide an adjustable delay as each supply is turned on as well as monitor each power-supply voltage, including the input voltage V_{DD}.

The MAX16165/MAX16166 operate from a supply range of 2.7V to 16V and have an internal regulator output (ABP), power internal circuits, and supply more than 1mA additional current to any external circuitry.

The sequencing is enabled by two inputs, ON and $\overline{OFF}$. A rising edge on the ON input initiates power-on sequencing of the channels whereas a falling edge on $\overline{OFF}$ input initiates power-off sequencing. During the power-on sequencing, when all of the voltages reach their final values, a sequencing done output DONE asserts high followed by a Power-OK (POK) output after the reset delay timer has expired, allowing the microcontroller (µC) to operate. If any voltage falls below its threshold, the reset output asserts and all voltage supplies are turned off. When the sequencer initiates a power-off sequencing, the MAX16165/MAX16166 can reverse sequence the outputs.

Output options available are open-drain (MAX16165) and push-pull (MAX16166). The MAX16165/MAX16166 can be daisy-chained unlimited amount to time to control any number of voltages in a system.

The MAX16165/MAX16166 feature a bidirectional active low $\overline{FAULT}$ input/output, which asserts low during any fault condition. $\overline{FAULT}$ stays low as long as an undervoltage event is present at UVSET Input and it is a one-shot output during all other $\overline{FAULT}$ conditions. An external signal pulling $\overline{FAULT}$ low disables all outputs immediately. The MAX16165/MAX16166 are available in a 1.63mm x 2.03mm, 20-bump Wafer-Level Package (WLP) and a 4mm x 4mm, 20L TQFN package. The device is fully specified over the -40°C to +125°C operating temperature range.

Applications

- Latch-Up Prevention and Inrush Current Protection in Multi-Supply Systems
- FPGA/ASIC Power Supply Sequencing
- Servers and Security Cameras
- Test Equipment
- Networking Equipment
- Industrial Sensors and Motor Controls

Benefits and Features

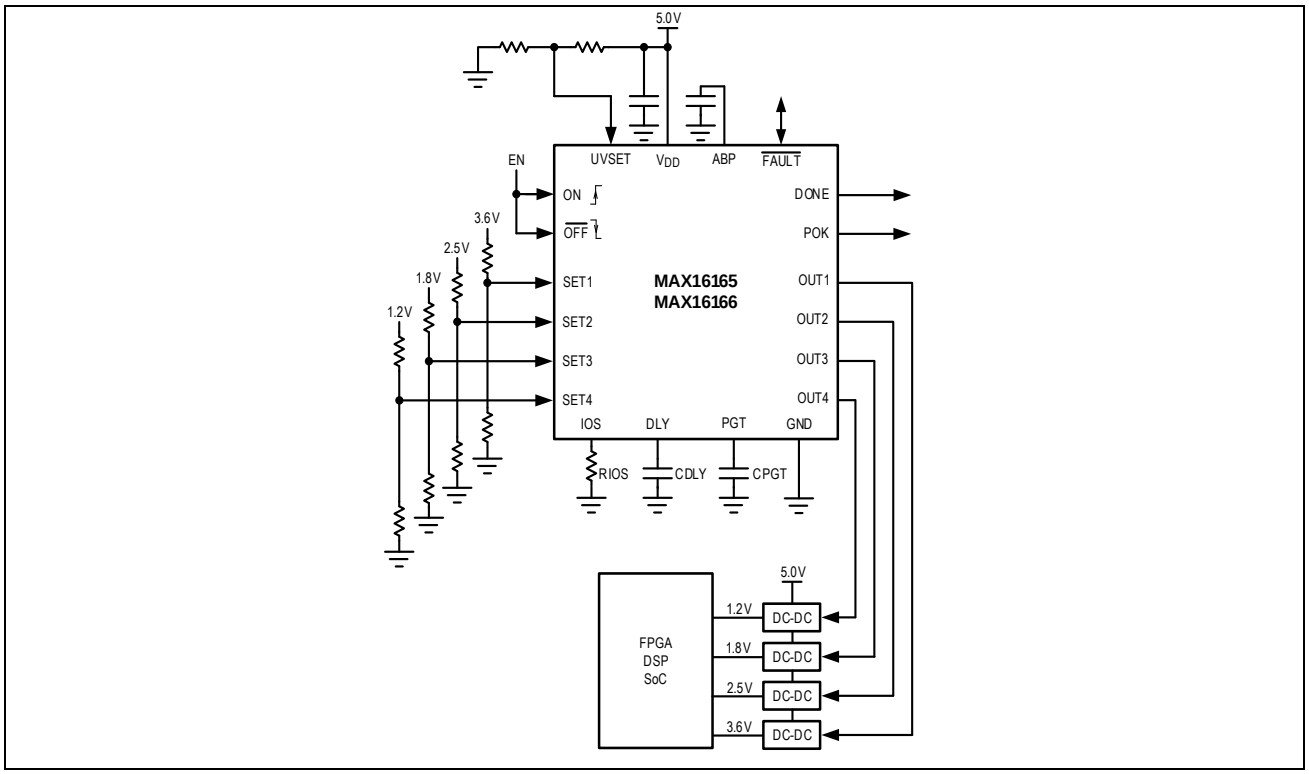
- 2.7V to 16.0V Wide Operating Voltage Range
- Monitor Up to Five Voltages
- Sequence Up to Four Voltages
- Power-Off in Reverse Order or Simultaneously
- Unlimited Daisy-Chain
- Capacitor-Adjustable Sequencing Delay
- Capacitor-Adjustable Power-Good Timeout
- Resistor-Configurable Power-Supply On and Off Thresholds
- Open-Drain (MAX16165)/Push-Pull (MAX16166) Outputs
- POK Output for System Microcontroller Reset
- Bidirectional $\overline{FAULT}$ Input/Output
- 4 x 5-Bump WLP and 20L TQFN Package
- -40°C to +125°C Operating Temperature Range

***Ordering Information* appears at end of data sheet.**

19-101178; Rev 1; 4/22

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Typical Application Circuit



Absolute Maximum Ratings

V_{DD} to GND .....-0.3V to +30V

OUT_ (Open-drain) to GND.....-0.3V to +30V

OUT_ (Push-pull) to GND..... -0.3 to Min.(V_{ABP} + 0.3V, +6V)

DONE, POK (Open-drain) to GND .....-0.3V to +6V

DONE (Push-pull) to GND..... -0.3 to Min.(V_{ABP} + 0.3V, +6V)

POK (Push-pull) to GND..... -0.3 to Min.(V_{ABP} + 0.3V, +6V)

SET_, $\overline{FAULT}$, ON, $\overline{OFF}$ to GND.....-0.3V to +6V

UVSET, ABP, IOS, DLY, PGT to GND .....-0.3V to +6V

Input/Output Current 20mA

Continuous Power Dissipation, WLP, Multilayer Board (T_A = +70°C, derate 18.02mW/°C above +70°C) 1441.7mW

Continuous Power Dissipation, TQFN, Multilayer Board (T_A = +70°C, derate 25.60mW/°C above +70°C) 2051.3mW

Operating Temperature Range ..... -40°C to +125°C

Junction Temperature ..... +150°C

Storage Temperature Range ..... -40°C to +150°C

Soldering Temperature (reflow)..... +260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

WLP

Package Code	W201C2+2
Outline Number	*21-0779*
Land Pattern Number	Refer to *Application Note 1891*
THERMAL RESISTANCE, FOUR-LAYER BOARD	
Junction-to-Ambient (θ_{JA})	55.49°C/W
Junction-to-Case Thermal Resistance (θ_{JC})	N/A

TQFN

Package Code	T2044+3C
Outline Number	*21-0139*
Land Pattern Number	*90-0037*
THERMAL RESISTANCE, FOUR-LAYER BOARD	
Junction-to-Ambient (θ_{JA})	39°C/W
Junction-to-Case Thermal Resistance (θ_{JC})	6°C/W

For the latest package outline information and land patterns (footprints), go to *www.maximintegrated.com/packages*. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to *www.maximintegrated.com/thermal-tutorial*.

Electrical Characteristics

(V_{DD} = 2.7V to 16.0V, V_{EN} = V_{ABP}, T_A = -40ºC to +125ºC, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SUPPLY VOLTAGE						
Operating Voltage Range	V_{DD}		2.7		16	V
Regulated Supply Voltage	V_{ABP}	I_{ABP} = +1mA (external sourcing current from ABP)	2.45		3.20	V
Undervoltage Lockout	V_{UVLO}	Minimum voltage on ABP, ABP rising		1.7	2.35	V
Undervoltage Lockout Hysteresis	V_{UVLO_HYS}	ABP falling		100		mV
Supply Current	I_{DD}	V_{DD} = 5V, all OUT_ = HIGH, No load		105	170	µA
ON, $\overline{OFF}$ INPUTS						
ON Input Threshold	V_{ON_TH}	ON rising	0.496	0.5	0.504	V
$\overline{OFF}$ Input Threshold	V_{OFF_TH}	$\overline{OFF}$ falling	0.496	0.5	0.504	V
ON, $\overline{OFF}$ Threshold Tempco				20		ppm/°C
ON, $\overline{OFF}$ Input Current	I_{ON_OFF}		-100		100	nA
MONITORED ANALOG INPUTS (UVSET, SET_)						
UVSET, SET_ Threshold	V_{TH}	UVSET, SET_ falling	0.496	0.5	0.504	V
UVSET, SET_ Threshold Hysteresis	V_{HYST}	UVSET, SET_ rising		1		%V_{TH}
UVSET, SET_ Threshold Tempco				20		ppm/°C
UVSET, SET_ Input Current		V_{UVSET} = $V_{SET_}$ = 0.5V	-100		+100	nA
OFFSET CURRENT SETTING INPUT (IOS)						
Offset Current Voltage Source			0.4925	0.5	0.5075	V
Offset Current Voltage Source Tempco				30		ppm/°C
Offset Current Range		R_{IOS} = 10kΩ to 1MΩ	0.5		50	µA
Offset Current Error		0.5µA to 5µA	-25		+25	%
		5µA to 50µA	-5		+5	
DELAY TIMER INPUT (DLY) AND POWER-GOOD TIMER INPUT (PGT)						
Source Current		-40°C to +85°C	3.8	4	4.2	µA
		-40°C to +125°C	3.8	4	4.4	
Voltage Threshold				0.5		V
SEQUENCER OUTPUTS (OUT_)						
OUT_ Output Voltage Low	V_{OUTL}	MAX16165, Open-drain Output, I_{SINK} = 3.2mA			0.3	V
		MAX16166, Push-pull Output, I_{SINK} = 3.2mA			0.3	
OUT_ Output Voltage High	V_{OUTH}	MAX16166, Push-pull Output, I_{SOURCE} = 1mA	0.85 x V_{ABP}			V
OUT_ Leakage Current	I_{OUT_LKG}	MAX16165, Open-drain Output, OUT_ = HIGH, $V_{OUT_}$ = 5V			1	µA
$\overline{FAULT}$ INPUT/OUTPUT						

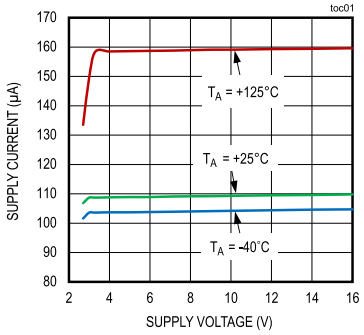
(V_{DD} = 2.7V to 16.0V, V_{EN} = V_{ABP}, T_A = -40ºC to +125ºC, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
$\overline{FAULT}$ Output Voltage Low	V_{FAULTL}	I_{SINK} = 3.2mA			0.3	V
$\overline{FAULT}$ Leakage Current	I_{FAULT_LKG}	$\overline{FAULT}$ = HIGH, V_{FAULT} = 5V			1	µA
$\overline{FAULT}$ Input Threshold	V_{FAULT_TH}	$\overline{FAULT}$ falling		0.5		V
POWER-OK OUTPUT (POK)						
POK Output Voltage Low	V_{POKL}	MAX16165, Open-drain Output, I_{SINK} = 3.2mA			0.3	V
		MAX16166, Push-pull Output, I_{SINK} = 3.2mA			0.3	
POK Output Voltage High	V_{POKH}	MAX16166, Push-pull Output, I_{SOURCE} = 1mA	0.85 x V_{ABP}			V
POK Leakage Current	I_{POK_LKG}	MAX16165, Open-drain Output, POK = HIGH, V_{POK} = 5V			1	µA
DONE OUTPUT (DONE)						
DONE Output Voltage Low	V_{DONEL}	MAX16165, Open-drain Output, I_{SINK} = 3.2mA			0.3	V
		MAX16166, Push-pull Output, I_{SINK} = 3.2mA			0.3	
DONE Output Voltage High	V_{DONEH}	MAX16166, Push-pull Output, I_{SOURCE} = 1mA	0.85 x V_{ABP}			V
DONE Leakage Current	I_{DONE_LKG}	MAX16165, Open-drain Output, DONE = HIGH, V_{DONE} = 5V			1	µA
TIMING						
POK Reset Timeout Accuracy	t_{POK_ACC}		-15		+15	%
ON Input Pulse Width	t_{ON_PW}	ON rising	6			µs
$\overline{OFF}$ Input Pulse Width	t_{OFF_PW}	$\overline{OFF}$ falling	6			µs
External $\overline{FAULT}$ Input Pulse Width	t_{FAULT_PW}	$\overline{FAULT}$ falling	6			µs
ON Input, $\overline{OFF}$ Input, External $\overline{FAULT}$ Input Transient Immunity					1	µs
$\overline{FAULT}$ Output Hold Timeout			68	80	92	µs
SET_ to $\overline{FAULT}$, OUT_ Low Delay Time	t_{SET_FAULT}	SET_ falling below V_{TH}		1		µs
External $\overline{FAULT}$ to OUT_ Low Delay Time	t_{FAULT_OUT}	$\overline{FAULT}$ falling below V_{TH}		3		µs
ON to $\overline{FAULT}$, OUT_ low Delay Time		ON rising above V_{TH}		3		µs
$\overline{OFF}$ to $\overline{FAULT}$, OUT_ Low Delay Time		$\overline{OFF}$ falling below V_{TH}		3		µs

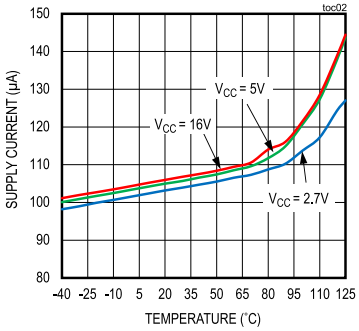
Typical Operating Characteristics

V_{DD} = 5.0V, V_{EN} = V_{ABP}, T_A = 25°C, unless otherwise noted.

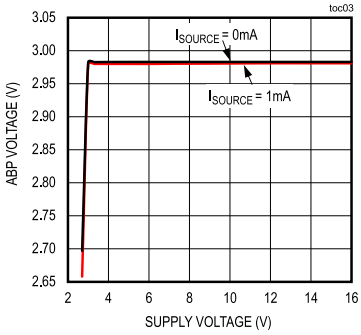
SUPPLY CURRENT vs. SUPPLY VOLTAGE



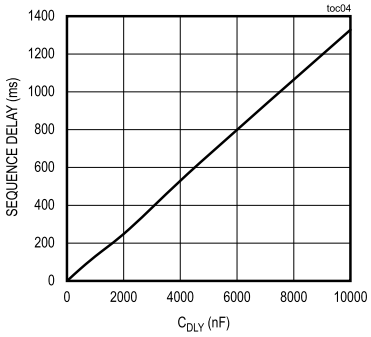
V_{DD} SUPPLY CURRENT vs. TEMPERATURE



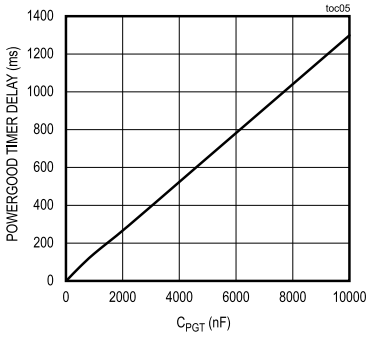
ABP VOLTAGE vs. SUPPLY VOLTAGE



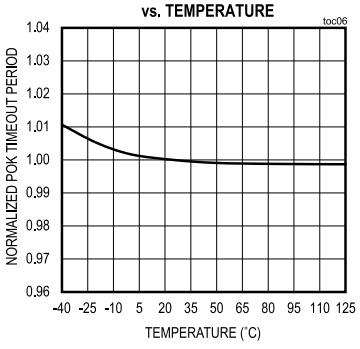
SEQUENCE DELAY vs. C_{DLY}



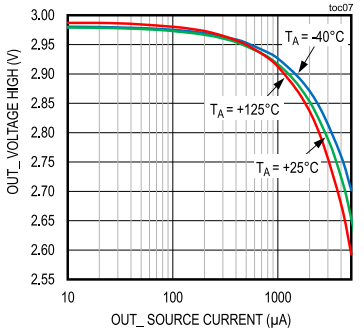
POWERGOOD TIMER DELAY vs. C_{PGT}



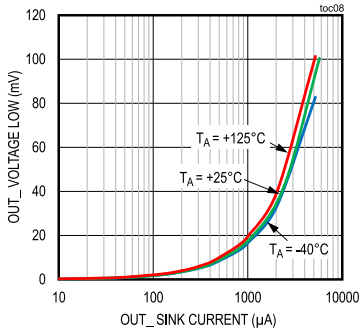
NORMALIZED POK TIMEOUT PERIOD vs. TEMPERATURE



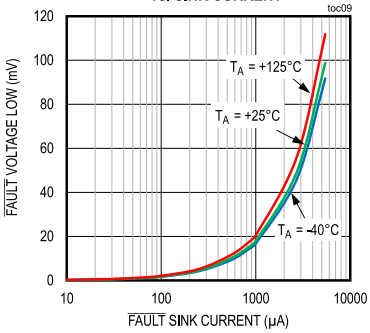
OUT_ VOLTAGE HIGH vs. SOURCE CURRENT



OUT_ VOLTAGE LOW vs. SINK CURRENT

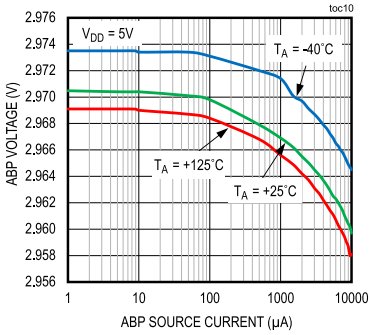


FAULT VOLTAGE LOW vs. SINK CURRENT

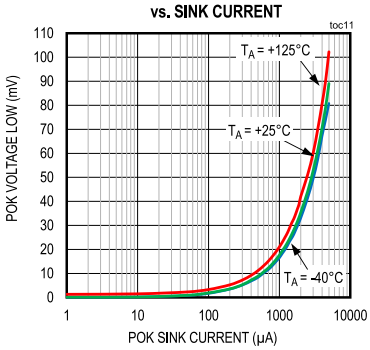


V_{DD} = 5.0V, V_{EN} = V_{ABP}, T_A = 25°C, unless otherwise noted.

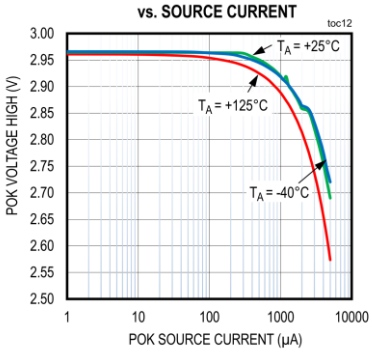
ABP VOLTAGE vs. SOURCE CURRENT



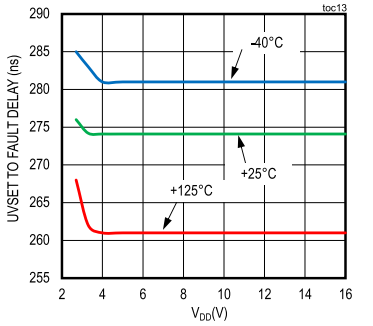
POK VOLTAGE LOW vs. SINK CURRENT



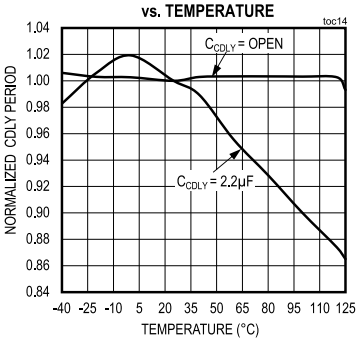
POK VOLTAGE HIGH vs. SOURCE CURRENT



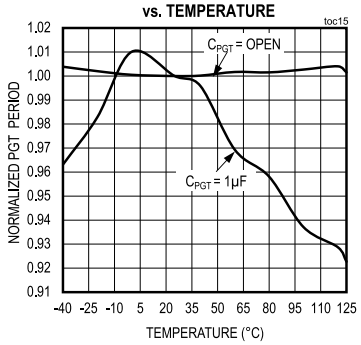
UVSET FALLING TO FAULT ASSERTION DELAY vs. V_{DD}



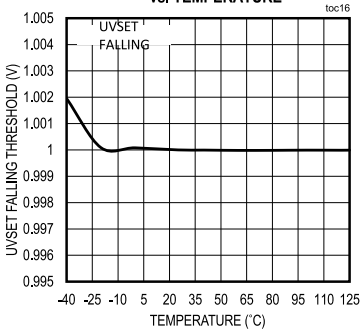
NORMALIZED CDLY PERIOD vs. TEMPERATURE



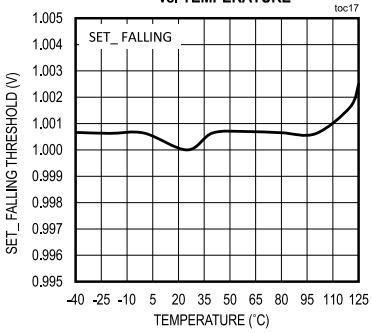
NORMALIZED PGT PERIOD vs. TEMPERATURE



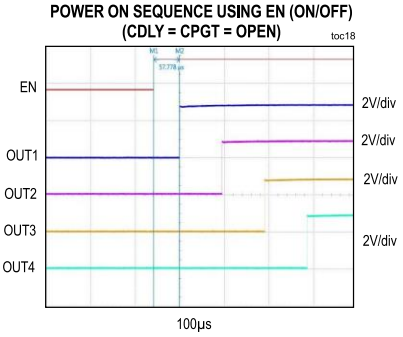
UVSET FALLING THRESHOLD vs. TEMPERATURE



SET_ FALLING THRESHOLD vs. TEMPERATURE

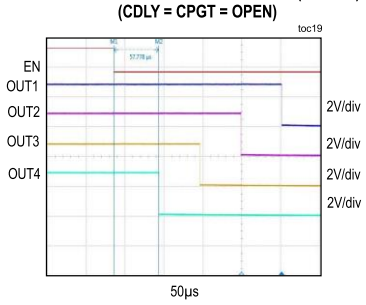


POWER ON SEQUENCE USING EN (ON/OFF) (CDLY = CPGT = OPEN)

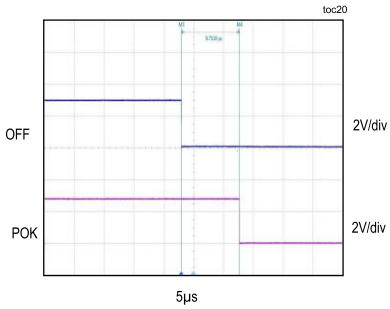


V_{DD} = 5.0V, V_{EN} = V_{ABP}, T_A = 25°C, unless otherwise noted.

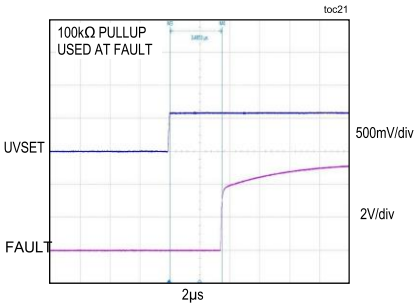
POWER DOWN SEQUENCE USING EN (ON/OFF) (CDLY = CPGT = OPEN)



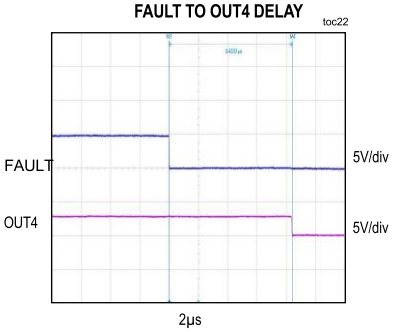
OFF TO POK DELAY



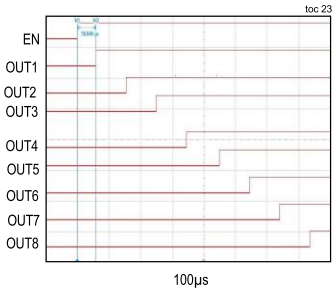
UVSET TO FALUT DELAY



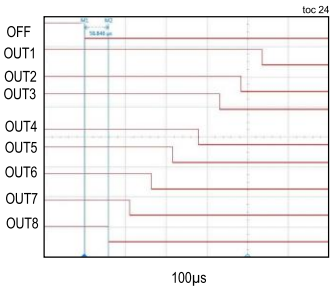
FAULT TO OUT4 DELAY



DAISY-CHAINING TWO DEVICES WITH EN RISING (CDLY = CPGT = OPEN)

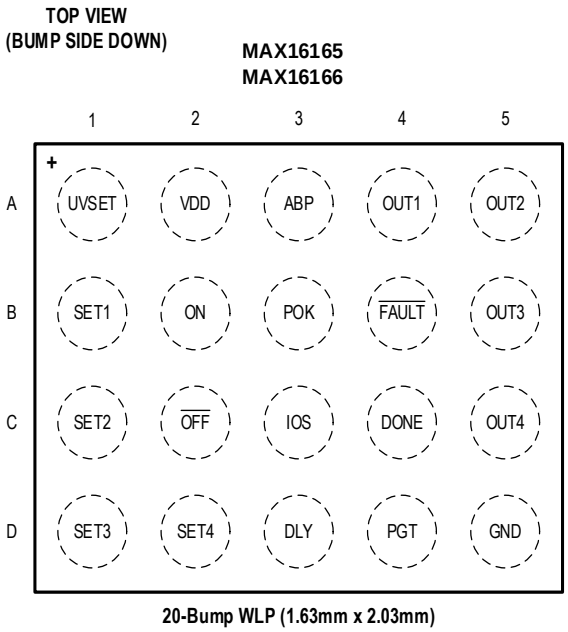


DAISY-CHAINING TWO DEVICES WITH EN RISING (CDLY = CPGT = OPEN)



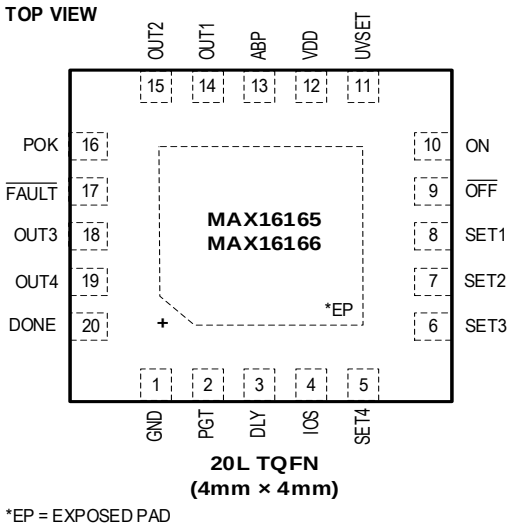
Pin Configurations

WLP



20-Bump WLP (1.63mm x 2.03mm)

TQFN



20L TQFN
(4mm × 4mm)

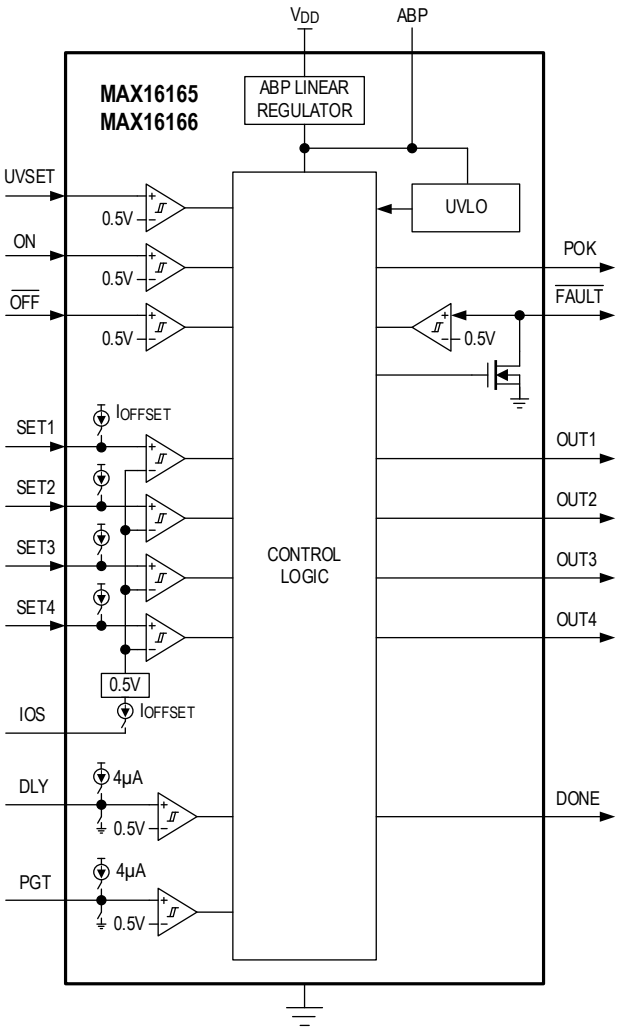
*EP = EXPOSED PAD

Pin Descriptions

PIN		NAME	FUNCTION
20 WLP	TQFN		
A1	11	UVSET	Set Monitored Threshold Input. Monitor a voltage by setting the threshold with an external resistive divider. The threshold is 0.5V.
A2	12	VDD	Device Power-Supply Input. Connect to 2.7V to 16V. Bypass V_{DD} to GND with a 0.1µF capacitor.
A3	13	ABP	Internal Supply Bypass Input. Connect a 1µF capacitor from ABP to GND. ABP is an internally generated voltage that powers internal circuits, and can supply more than 1mA additional current to any external circuitry. Do not leave ABP unconnected or short to GND.
A4	14	OUT1	MAX16165: Open-Drain Output 1. Upon power-on sequencing (ON input rises from low to above 0.5V), OUT1 changes from low to high impedance after sequence delay t_{DLY}. During power-off sequencing, when the voltage at the SET2 pin falls below 0.5V, OUT1 goes from high impedance to low after sequence delay t_{DLY}. OUT1 requires an external pullup resistor. MAX16166: Push-Pull Output 1. Upon power-on sequencing (ON input rises from low to above 0.5V), OUT1 changes from low to high after sequence delay t_{DLY}. During power-off sequencing, when the voltage at the SET2 pin falls below 0.5V, OUT1 goes from high to low after sequence delay t_{DLY}.
A5	15	OUT2	MAX16165: Open-Drain Output 2. During power-on sequencing, when the voltage at SET1 rises above threshold voltage (Rising), OUT2 goes from low to high impedance after sequence delay t_{DLY}. During power-off sequencing, when the voltage at the SET3 pin falls below 0.5V, OUT2 goes from high impedance to low after sequence delay t_{DLY}. OUT2 requires an external pullup resistor. MAX16166: Push-Pull Output 2. During a power-on sequencing, when the voltage at SET1 rises above threshold voltage (Rising), OUT2 goes from low to high after sequence delay t_{DLY}. During a power-off sequencing, when the voltage at SET3 pin falls below 0.5V, OUT2 goes from high to low after sequence delay t_{DLY}.
B1	8	SET1	Set Monitored Threshold 1 Input. Monitor a voltage by setting the threshold with an external resistive divider. The SET1 threshold is 0.5V. To disable Channel 1, connect SET1 to ABP. Do not leave SET1 unconnected or short to GND. Connect OUT1 directly to SET1 for sequencing without monitoring Channel 1.
B2	10	ON	Noninverting Comparator Input. A rising voltage above 0.5V on this pin initiates power-on sequencing.
B3	16	POK	MAX16165: Open-Drain Power-OK Output. During power-on sequencing, when SET4 voltage rises above 0.5V, this output changes from low to high impedance after the reset timeout period. This output is driven low if the voltage on any SET_ or UVSET input drops below 0.5V or when $\overline{FAULT}$ is pulled low by an an external signal. POK requires an external pullup resistor. MAX16166: Push-Pull Power-OK Output. During power-on sequencing, when SET4 voltage rises above 0.5V, this output changes from low to high after the reset timeout period. This output is driven low if the voltage on any SET_ or UVSET input drops below 0.5V or when $\overline{FAULT}$ is pulled low by an external signal.
B4	17	$\overline{FAULT}$	Bidirectional Input and Active Low Open-Drain Output. When an internal fault is detected, this pin is asserted low. An external signal pulling this pin low disables all outputs and sets the MAX16165/66 to initialization state.
B5	18	OUT3	MAX16165: Open-Drain Output 3. During power-on sequencing, when the voltage at SET2 rises above threshold voltage (Rising), OUT3 goes from low to high impedance after sequence delay t_{DLY}. During power-off sequencing, when the voltage at SET4 pin falls below 0.5V, OUT3 goes from high impedance to low after sequence delay t_{DLY}. OUT3 requires an external pullup resistor.

			MAX16166: Push-Pull Output 3. During power-on sequencing, when the voltage at SET2 rises above threshold voltage (Rising), OUT3 goes from low to high after sequence delay t_{DLY}. During power-off sequencing, when the voltage at the SET4 pin falls below 0.5V, OUT3 goes from high to low after sequence delay t_{DLY}.
C1	7	SET2	Set Monitored Threshold 2 Input. Monitor a voltage by setting the threshold with an external resistive divider. The SET2 threshold is 0.5V. To disable Channel 2, connect SET2 to ABP. Do not leave SET2 unconnected or short to GND. Connect OUT2 directly to SET2 for sequencing without monitoring Channel 2.
C2	9	$\overline{OFF}$	Noninverting Comparator Input. A falling voltage below 0.5V on this pin initiates power-off sequencing.
C3	4	IOS	Offset Current Setting Input. Connect a resistor (10kΩ to 1MΩ) to GND to set the offset current during power-off sequencing. Do not leave it unconnected or short to GND.
C4	20	DONE	MAX16165: Open-Drain Sequencing Done Output. When power-on sequencing is complete, DONE changes from low to high impedance. During power-off sequencing, the pin remains high impedance until SET1 voltage drops below its threshold. When a fault occurs, this pin is asserted low. MAX16166: Push-Pull Sequencing Done Output. When power-on sequencing is complete, DONE changes from low to high. During power-off sequencing, the pin remains high until SET1 voltage drops below its threshold. When a fault occurs, this pin is asserted low.
C5	19	OUT4	MAX16165: Open-Drain Output 4. During power-on sequencing, when the voltage at SET3 rises above threshold Voltage (Rising), OUT4 goes from low to high impedance after sequence delay t_{DLY}. During power-off sequencing, when the voltage at the OFF pin falls below 0.5V, OUT4 goes from high impedance to low after sequence delay t_{DLY}. OUT4 requires an external pullup resistor. MAX16166: Push-Pull Output 4. During power-on sequencing, when the voltage at SET3 rises above 0.5V, OUT4 goes from low to high after sequence delay t_{DLY}. During power-off sequencing, when the voltage at the OFF pin falls below 0.5V, OUT4 goes from high to low after sequence delay t_{DLY}.
D1	6	SET3	Set Monitored Threshold 3 Input. Monitor a voltage by setting the threshold with an external resistive divider. The SET3 threshold is 0.5V. To disable Channel 3, connect SET3 to ABP. Do not leave SET3 unconnected or short to GND. Connect OUT3 directly to SET3 for sequencing without monitoring Channel 3.
D2	5	SET4	Set Monitored Threshold 4 Input. Monitor a voltage by setting the threshold with an external resistive divider. The SET4 threshold is 0.5V. To disable channel 4, connect SET4 to ABP. Do not leave SET4 unconnected or short to GND. Connect OUT4 directly to SET4 for sequencing without monitoring the Channel 4.
D3	3	DLY	Adjustable Sequence Delay Timing Input. Connect a capacitor from DLY to GND to set the sequence delay between each OUT_. Leave DLY unconnected for a 40µs (typ) delay.
D4	2	PGT	Monitored Power-Supply Power-Good Timer Setting Input. The capacitor connected to this input to GND sets the time allowed between OUT_ being enabled and SET_ voltage goes above its threshold voltage (Rising). If SET_ does not rises above its threshold voltage (Rising) before the timer expires, the MAX16165/MAX16166 generates a fault condition and enters initialization state. Leave PGT unconnected for a 5µs (typ) delay.
D5	1	GND	Ground.
-	-	EP	Exposed Pad. EP is internally connected to GND. Connect EP to the GND plane for improved heat dissipation. Do not use EP as the only ground connection.

Functional Diagrams



Detailed Description

The MAX16165/MAX16166 enable four power supplies when the sequencer turns on and disable the four power supplies in reverse order when the sequencer turns off. The MAX16165/MAX16166 monitor each power supply once they are turned on. The device also includes an undervoltage (UV) sensing input (UVSET) that monitors VDD or any other power supply.

When the sequencer initiates power-on sequencing, the MAX16165/MAX16166 provide a capacitor-adjustable delay time (t_{DLY}) before the first output is enabled. After the first output is enabled, the MAX16165/MAX16166 monitor the enabled power supply voltage by feeding it back to the voltage sensing input SET1. If the voltage at SET1 reaches its threshold (V_{TH} + V_{HYST}) within a capacitor-adjustable power-good timeout period (t_{PGT}), the sequencer waits for the delay time t_{DLY} and enables the second output. The power-on sequencing repeats until the fourth output is enabled and the voltage at SET4 reaches its threshold. At that time, a sequencing done output DONE asserts high and a POK output asserts high after the reset timeout period (t_{RP}), allowing a system microcontroller (µC) to reset and start to operate. The MAX16165/MAX16166 monitor each sequenced voltage fed back on SET_ after the respective channel is enabled. The MAX16165/MAX16166 also monitor UVSET input for undervoltage condition after power up. If any voltage falls below its threshold, the POK and DONE outputs deassert and all outputs are disabled simultaneously to turn off all sequenced power supplies. During any fault condition except UVSET undervoltage detection, a one-shot pulse of pulse width 80µs (typ) is asserted on the $\overline{FAULT}$ pin. The device enters into the fault condition and initializes the state machine, waiting for a power-on sequencing command again. If an undervoltage condition is present at UVSET, $\overline{FAULT}$ stays low as long as the undervoltage condition persists.

When the sequencer initiates a power-off sequencing, the MAX16165/MAX16166 provide the delay time t_{DLY} before the fourth output is disabled. At the time the fourth output is disabled, the device injects a resistor-programmable offset current (I_{OFFSET}) to SET4 input and monitors the voltage at SET4. When SET4 voltage drops below its threshold, the MAX16165/MAX16166 wait for another delay time t_{DLY}, and then disable the third output. The power-off sequencing repeats until the first output is disabled. When the power-off sequencing is completed, DONE output asserts low. The MAX16165/MAX16166 can be cascaded to control a higher number of power supplies in a system.

$\overline{FAULT}$ Input/Output

$\overline{FAULT}$ is bidirectional. It is an active low input and active low open-drain output. When an internal fault is detected, this pin is asserted low. An external signal pulling this pin low disables all outputs and sets the MAX16165/MAX16166 to a fault condition. See the *State Diagram* for all the conditions that assert a $\overline{FAULT}$. During any fault condition except UVSET undervoltage detection, a one-shot pulse of pulse width 80µs (typ) is asserted. See the *Applications Information* section to understand how the $\overline{FAULT}$ output can be modified to achieve extended assert duration in applications where DC-DC converters having slow powerup are used.

For multichip solutions, all of the $\overline{FAULT}$ input/outputs can be connected together. In case of a fault condition, all outputs on every device are turned off simultaneously.

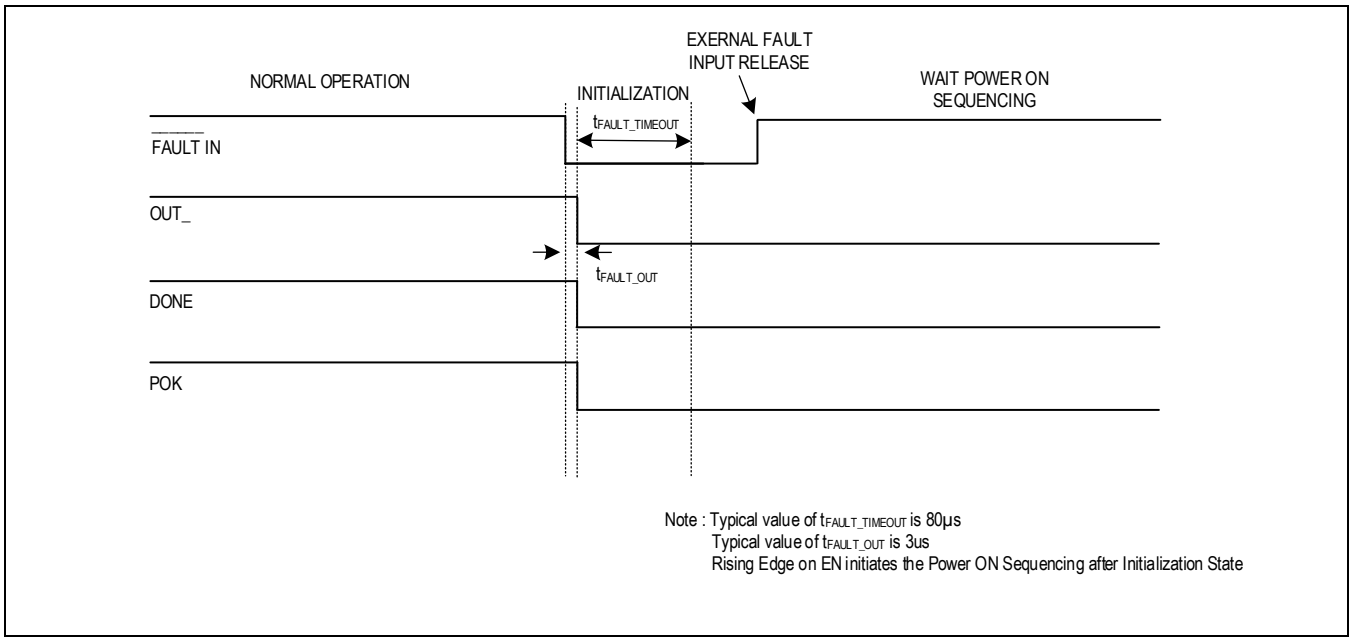


Figure 1. External Fault Response

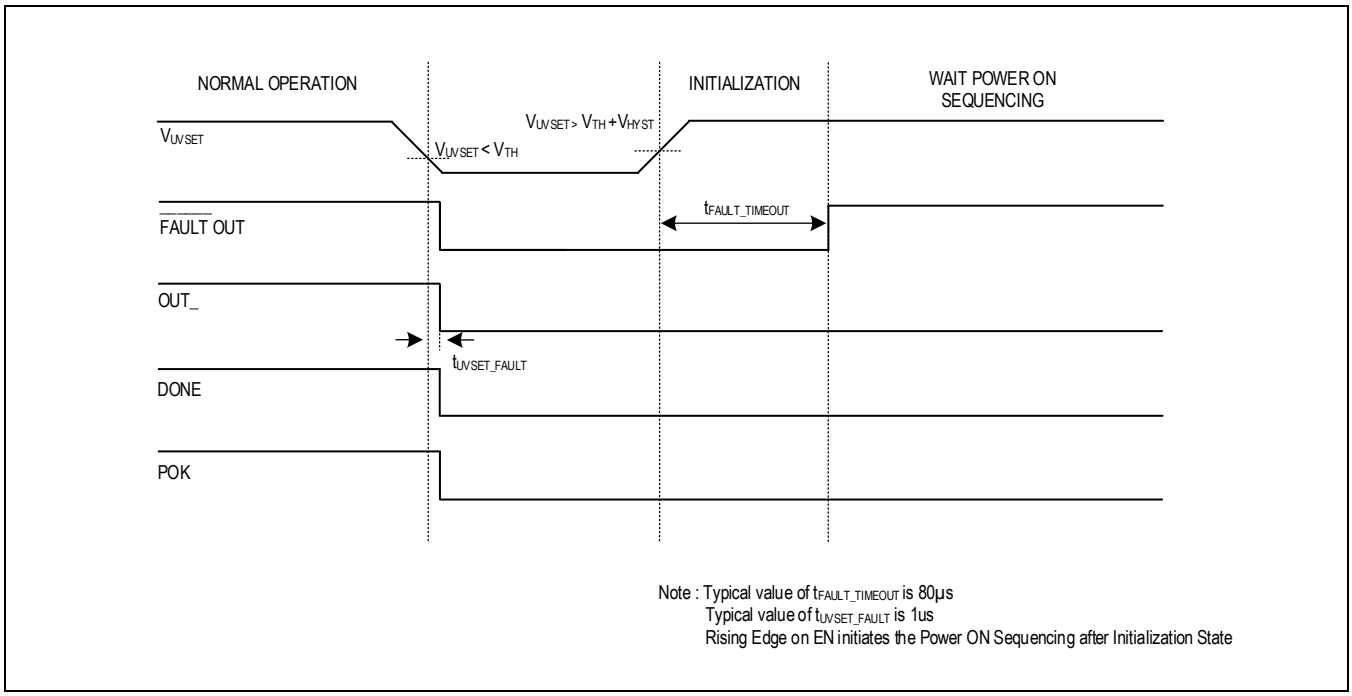


Figure 2. UVSET Fault Response

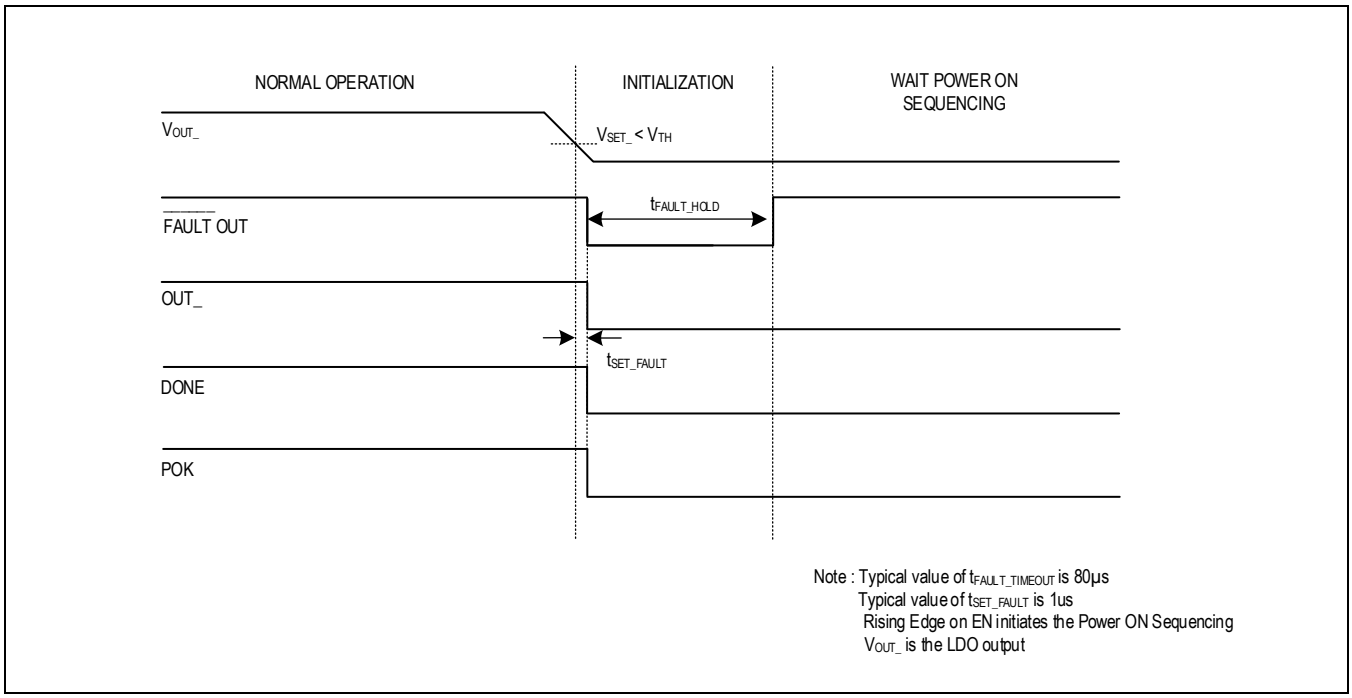


Figure 3. SET Fault Response

Skip or Disable Channels

If fewer than four channels are required, skip a channel by connecting the SET_ pin to ABP pin. The sequencing is similar with four-channel sequencing, just treat the MAX16165/MAX16166 like fewer channels. For example, if SET2 is connected to ABP, all logic for Channel 2 is removed from the state machine so there is not a delay, timer, UV detection, or fault triggered from this channel. If all channels are skipped, the device asserts DONE and POK immediately after initialization.

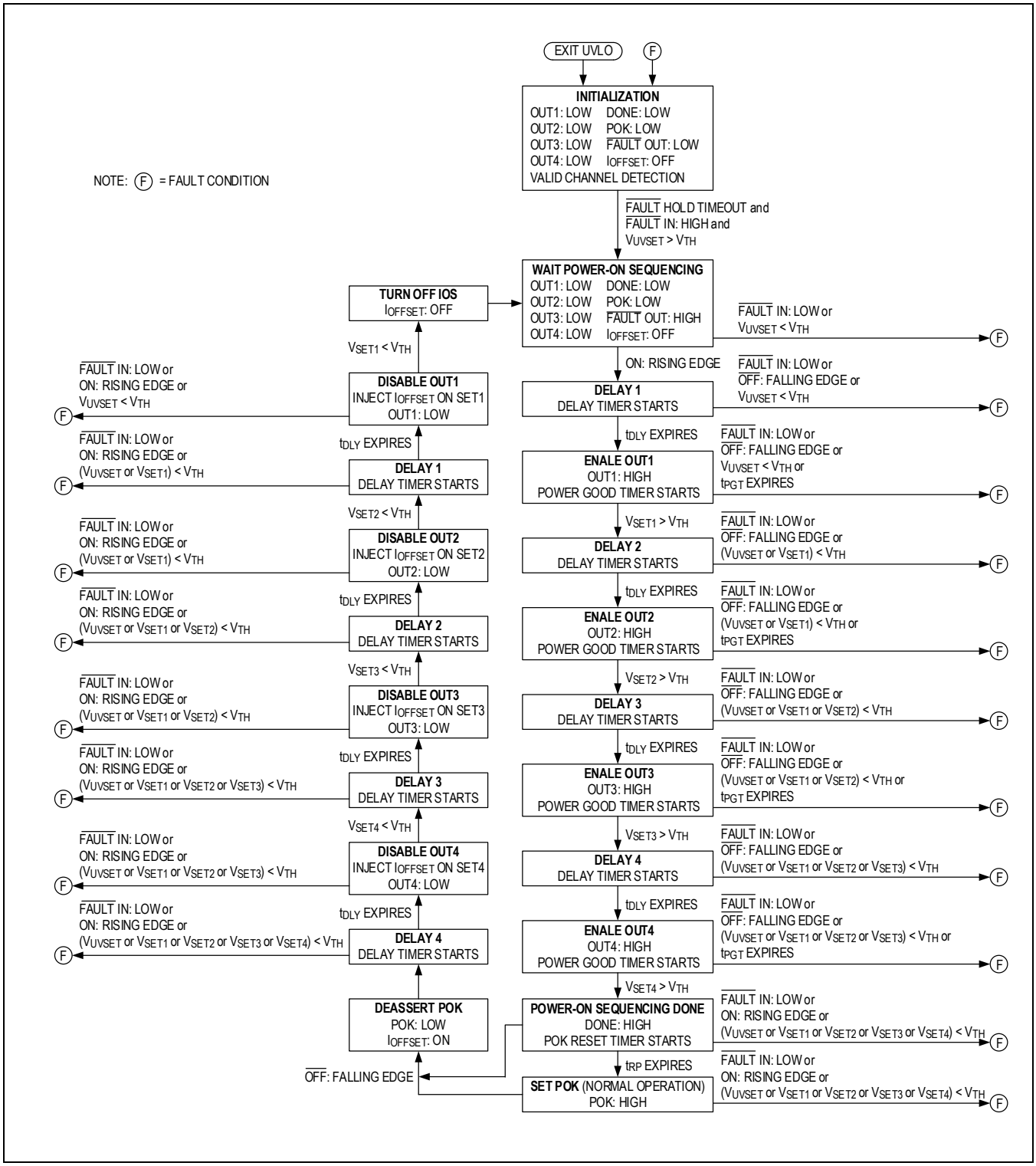
Channel skipping decision is decided during the initialization phase after every fault condition. The MAX16165/MAX16166 checks for the respective SET_ voltage during the initialization phase. If the voltage at SET_ is above 0.5V, the corresponding channel gets skipped. Therefore, it is important to ensure the voltage at SET_ is below 0.5V after each fault condition. If the power supplies are not properly loaded, it can take a long time to discharge the channel SET_ voltage. This situation is more crucial when V_{OFF} voltage levels are low or the load current of the power supply is less. See the *Applications Information* section for more information on how to avoid the false skipping of channels in this situation.

ON and $\overline{\text{OFF}}$ Inputs

The ON and $\overline{\text{OFF}}$ inputs are edge triggered inputs with a threshold of 500mV, which are used to initiate power sequencing. If no FAULT condition persists, a rising edge on the ON input initiates power-on sequencing while a falling edge on $\overline{\text{OFF}}$ initiates a power-down sequencing in the reverse order. A falling edge on ON input and a rising edge on $\overline{\text{OFF}}$ input are ignored. Normally ON and $\overline{\text{OFF}}$ inputs are tied together and used separately in special cases such as daisy-chaining.

It is important to ensure a voltage above 0.5V at ON input until the sequencing gets completed. If the ON input voltage falls below 0.5V or another rising edge happens at ON input, a FAULT is asserted resulting in stopping the sequencing and simultaneous power-off of all the outputs. See the *Daisy-Chaining the MAX16165/MAX16166* and *Typical Application Circuits* sections for more information.

State Diagram



Applications Information

Selecting SET_ Feedback Resistors and Offset Current

For each sequenced power supply, choose a voltage when the power supply is considered to be ON during power-on sequencing (V_{ON}) and a voltage when the power supply is considered to be OFF during power-off sequencing (V_{OFF}). During power-off sequencing, an offset current I_{OFFSET} is injected to the SET_ pin so that V_{OFF} is lower than V_{ON} (see *Figure 4*). Calculate resistor values according to the following equations:

$$R1 = \left(\frac{V_{ON} - V_{OFF}}{I_{OFFSET}}\right)$$

$$R2 = R1 \times \left(\frac{0.5V}{V_{ON}}\right)$$

Use the formula shown below to calculate the RIOS for an offset current I_{OFFSET}:

$$R_{IOS} = \left(\frac{0.5V}{I_{OFFSET}}\right)$$

For example, if power supply V1 nominal voltage is 1.8V, choose V_{ON} = 1.71V and V_{OFF} = 0.8V, offset current I_{OFFSET} = 5µA, R1 = 182kΩ, R2 = 75.21kΩ.

$$R1 = \left(\frac{1.71V - 0.8V}{5\mu A}\right) = 182k\Omega$$

$$R2 = 182k\Omega \times \left(\frac{0.5V}{1.71V - 0.5V}\right) = 75.21k\Omega$$

$$R_{IOS} = \left(\frac{0.5V}{5\mu A}\right) = 10k\Omega$$

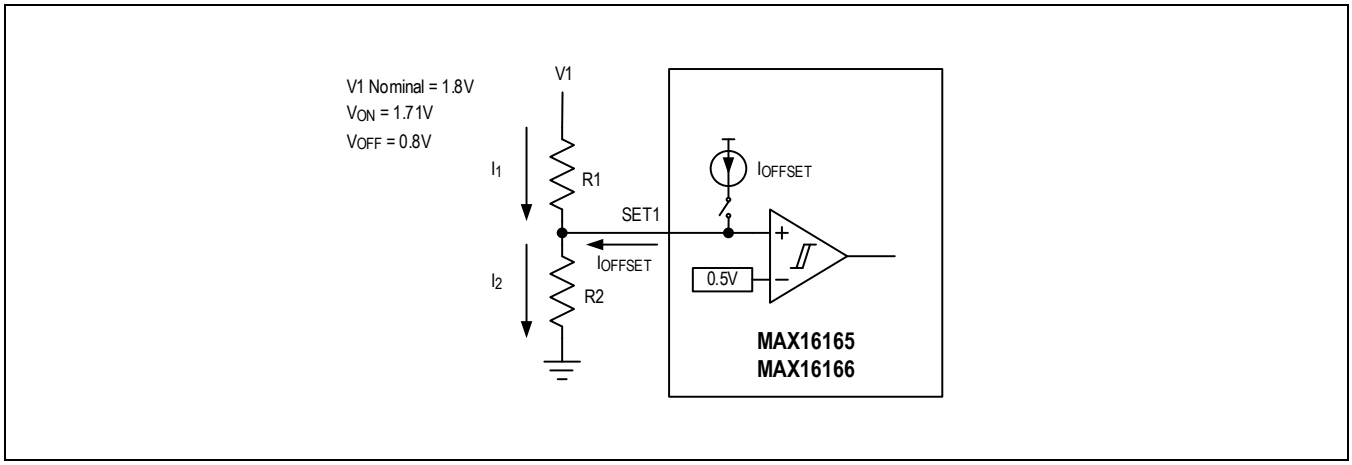


Figure 4. Design of SET_ Feedback Resistors and Offset Current

Connect a resistor with 1% tolerance from 10kΩ to 1MΩ at the IOS pin to achieve an offset current from 0.5µA to 50µA. To ensure correct power-down sequencing, adhere to the calculations provided in this section and calculate the SET_ divider resistors in accordance with the I_{OFFSET} chosen. The resistor connected at IOS decides the I_{OFFSET} of all the channels.

Sequence Delay Time Input

When the power-on sequence starts, the sequence delay time input (DLY) has an internal switch in series with an internal current source of 4µA, which is connected to the C_{DLY} present at the DLY pin. This current charges the C_{DLY} linearly until the voltage reaches the threshold of 0.5V and signal to continue enabling the subsequent channel. Connect a capacitor (C_{DLY}) between DLY and GND to adjust the sequencing delay period (t_{DLY}) that occurs between sequenced channels. Use the following formula to estimate the delay:

$$t_{DLY} = 125K\Omega \; X \; C_{DLY}$$

where t_{DLY} is in seconds and C_{DLY} is in Farads. Leave DLY unconnected for the minimum 40µs (typ) delay. After each t_{DLY} the DLY capacitor discharges (internal 4Ω) with typical 40µs ($t_{DISCHARRGE}$) shown in *Figure 5*. The accuracy of the t_{DLY} is affected by the C_{DLY} capacitor leakage and tolerance. A low leakage ceramic capacitor is recommended.

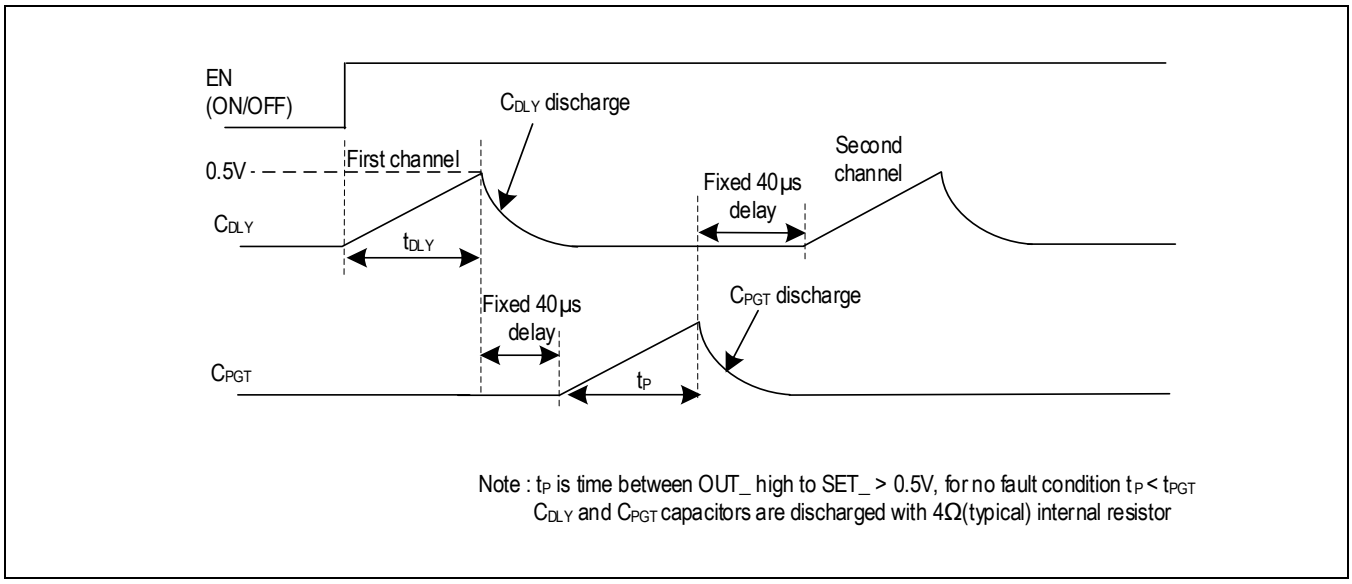


Figure 5. Charging and Discharging of DLY and PGT Capacitor

Power-Good Timer (PGT) and Power-Good Time Input

The Power Good Timer is used to check the capability of a power supply to reach a set voltage within a capacitor adjustable delay (t_{PGT}). The $\overline{FAULT}$ output is asserted when any enabled voltage cannot reach its threshold on the SET_ pin within tPGT. The internal state machine should stop the PGT if SET_ voltage reaches 0.5V before the PGT expires. The MAX16165/MAX16166 do not have to wait for t_{PGT} to expire before moving to the next step. The PGT is only for power-on sequencing and not used during power-off sequencing. Like the DLY timer, the PGT circuit is also enabled by a 4µA current source to charge the C_{PGT} capacitor.

Connect a capacitor (C_{PGT}) between PGT and GND to adjust the sequencing delay period (t_{PGT}). Use the following formula to estimate the delay:

$$t_{DLY} = 5\mu s + 125K\Omega \; X \; C_{DLY}$$

where t_{PGT} is in seconds and C_{PGT} is in Farads. Leave PGT unconnected for a minimum 5µs (typ) delay. The accuracy of the delay is affected by the C_{PGT} capacitor leakage and tolerance. A low-leakage ceramic capacitor is recommended.

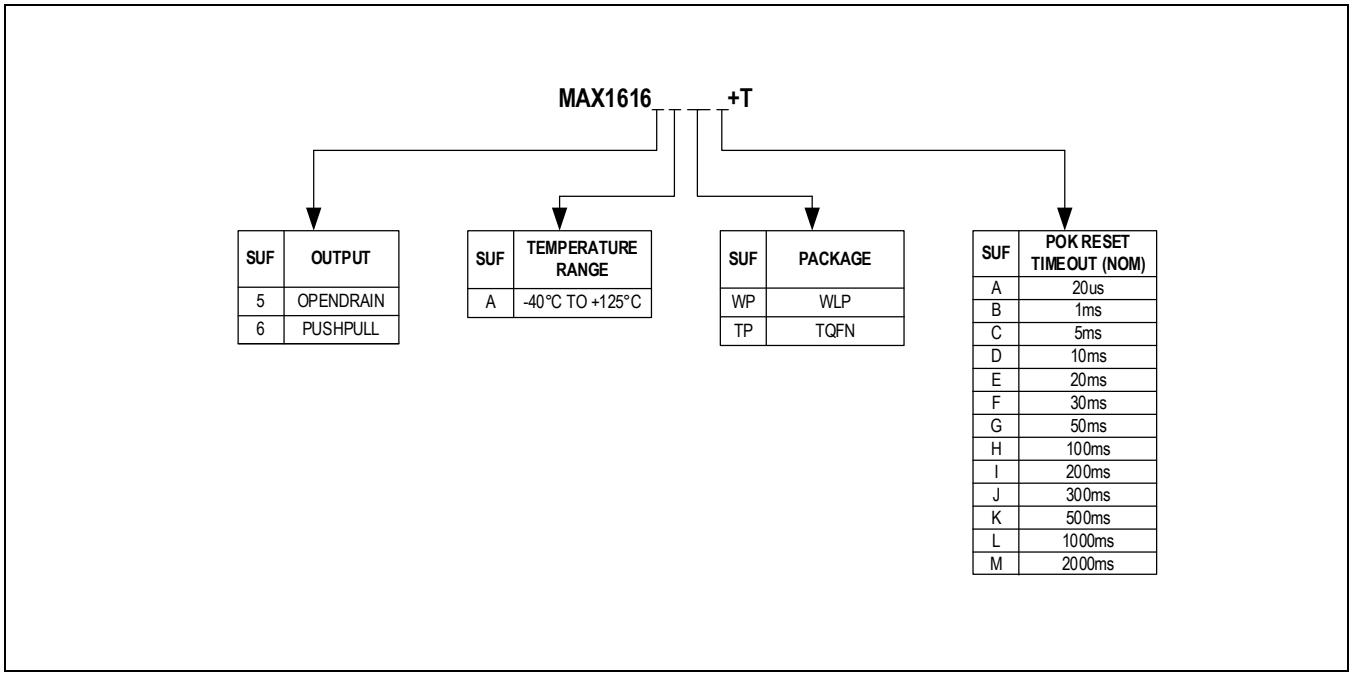
Pullup Resistor Values

The exact value of the pullup resistors for the open-drain outputs is not critical, but some consideration should be made to ensure the proper logic levels when the device is sinking current. For example, if V_{DD} = 3.3V and the pullup voltage is 5V, keep the sink current less than 3.2mA as shown in the *Electrical Characteristics* table. As a result, the pullup resistor should be greater than 1.6kΩ. For a 12V pullup, the resistor should be larger than 3.74kΩ.

Daisy-Chaining the MAX16165/MAX16166

Multiple MAX16165/MAX16166 devices can be daisy-chained to sequence and monitor a large number of voltages. When a fault occurs on any of the monitored inputs, $\overline{FAULT}$ goes low which signals a fast power-down. Connect all $\overline{FAULT}$ pins of the MAX16165/MAX16166 together to ensure that all power supplies are turned off during a fault. *Figure 13* shows an example of two daisy-chained devices.

Selector Guide



SUF	OUTPUT
5	OPENDRAIN
6	PUSHPULL

SUF	TEMPERATURE RANGE
A	-40°C TO +125°C

SUF	PACKAGE
WP	WLP
TP	TQFN

SUF	POK RESET TIMEOUT (NOM)
A	20us
B	1ms
C	5ms
D	10ms
E	20ms
F	30ms
G	50ms
H	100ms
I	200ms
J	300ms
K	500ms
L	1000ms
M	2000ms

Layout and Bypassing

For better noise immunity, bypass VDD to GND with a 0.1µF capacitor installed as close to the device as possible. Bypass ABP to GND with a 1µF capacitor installed as close to the device as possible. Minimize stray capacitance on the SET_ inputs. The layout of the divider resistors should be as close to the MAX16165/MAX16166 as possible. Connect the exposed pad (EP) to the ground plane for improved heat dissipation. Do not use EP as the only ground connection for the device.

Typical Application Circuits

Sequence Four Power Supplies, Monitor V_{DD}, and Power-Good/Power-OK Outputs

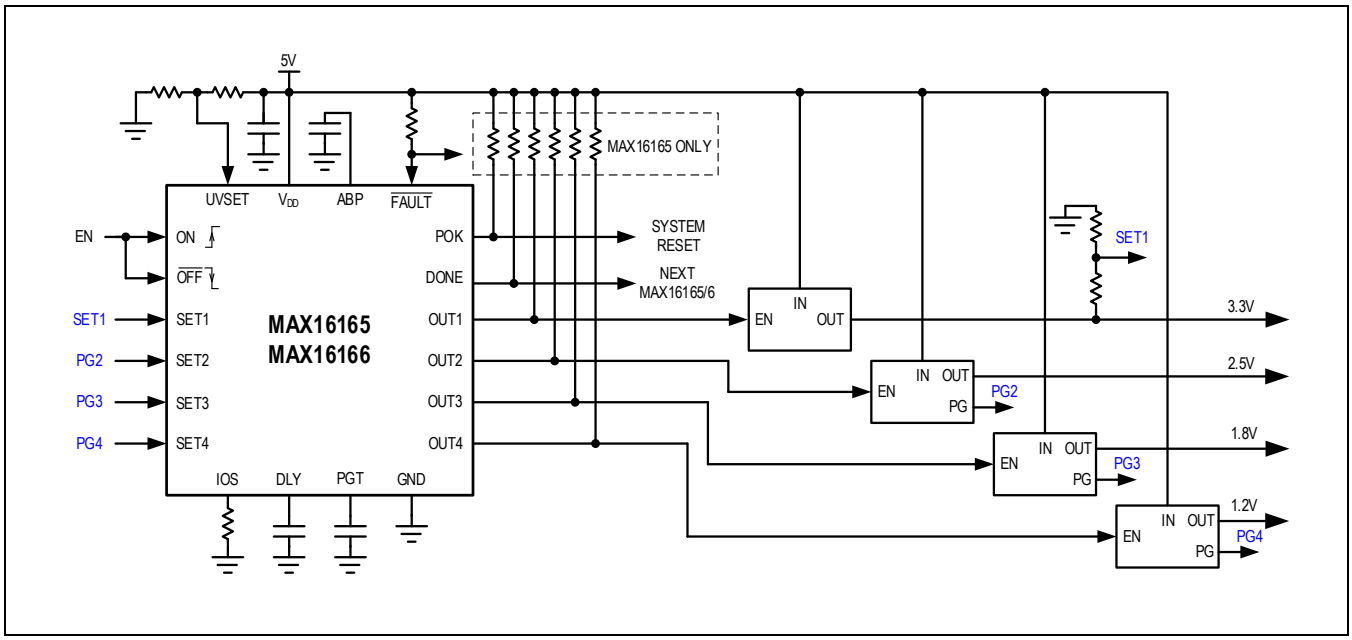


Figure 6. Sequence Four Power Supplies, Monitor V_{DD}, V1 = 3.3V, and Power-Good Signals of the Other Three Power Supplies.

Monitor V_{DD} and Sequence Four Power Supplies, without Monitoring

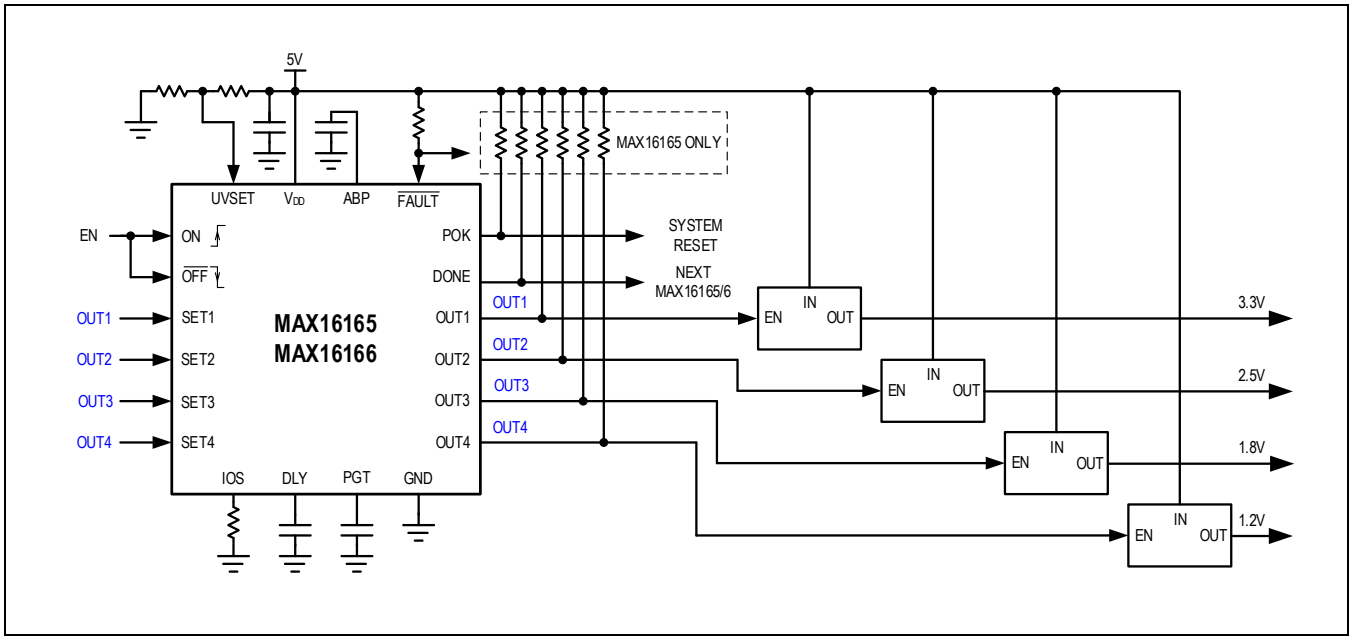


Figure 7. Sequence Four Power Supplies, without Monitoring. Only Monitor V_{DD}.

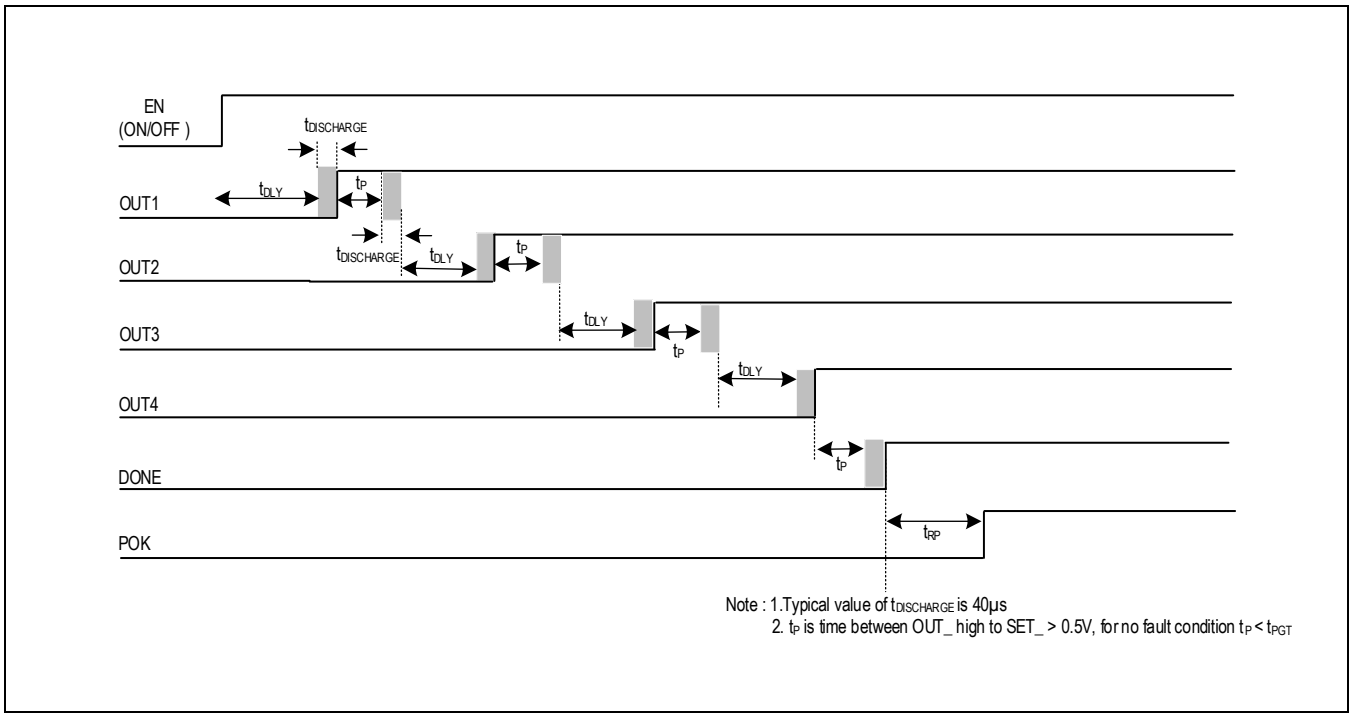


Figure 8. Power-Up Sequencing Timing Diagram. See the Typical Application Circuit (Figure 3).

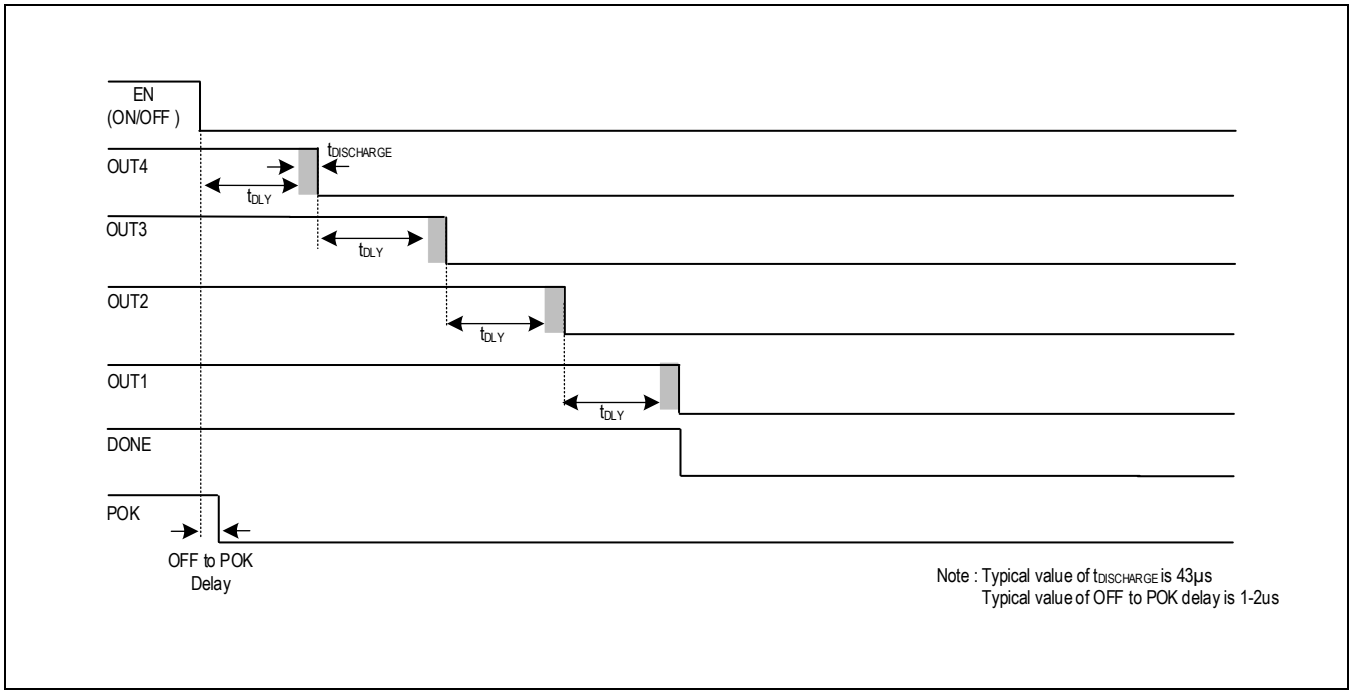


Figure 9. Power-Down Sequencing Timing Diagram. See the Typical Application Circuit (Figure 3).

Sequence and Monitor Four Power Supplies and Monitor V_{DD}

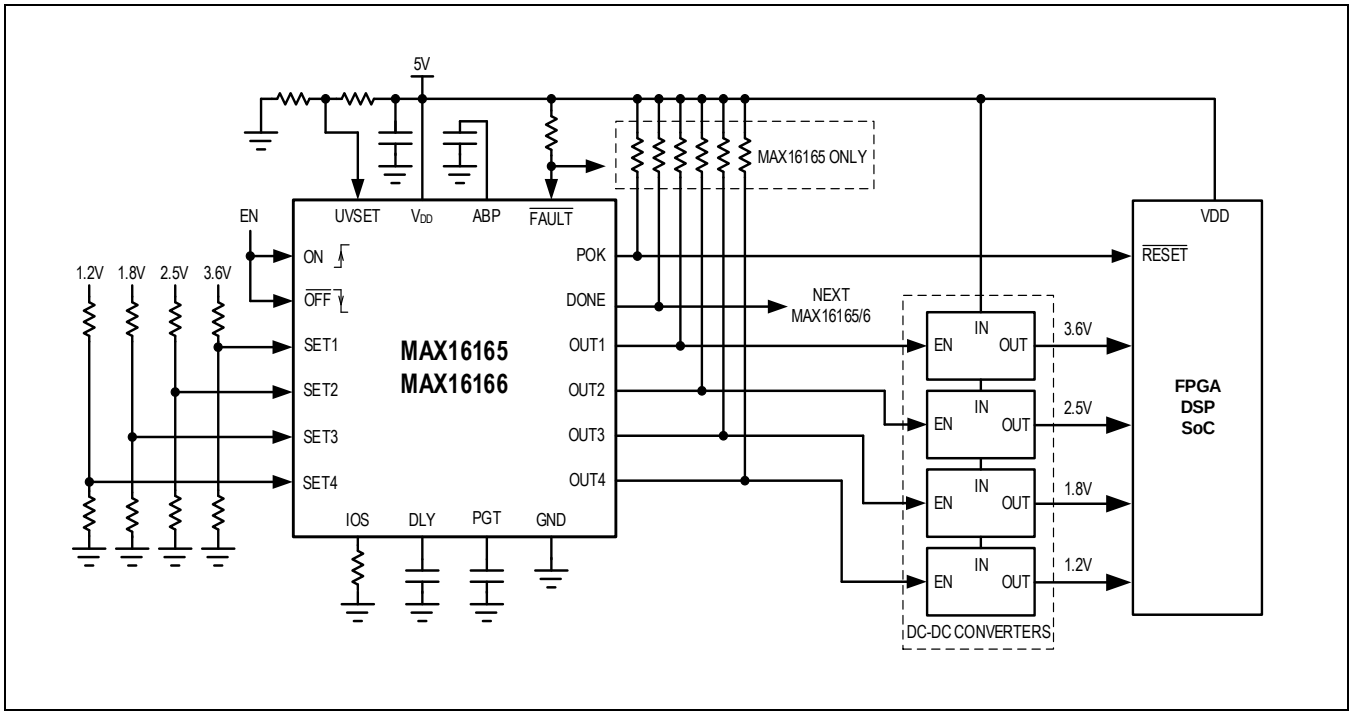


Figure 10. Sequence Four Power Supplies and Monitor V_{DD} and the Four Power Supplies.

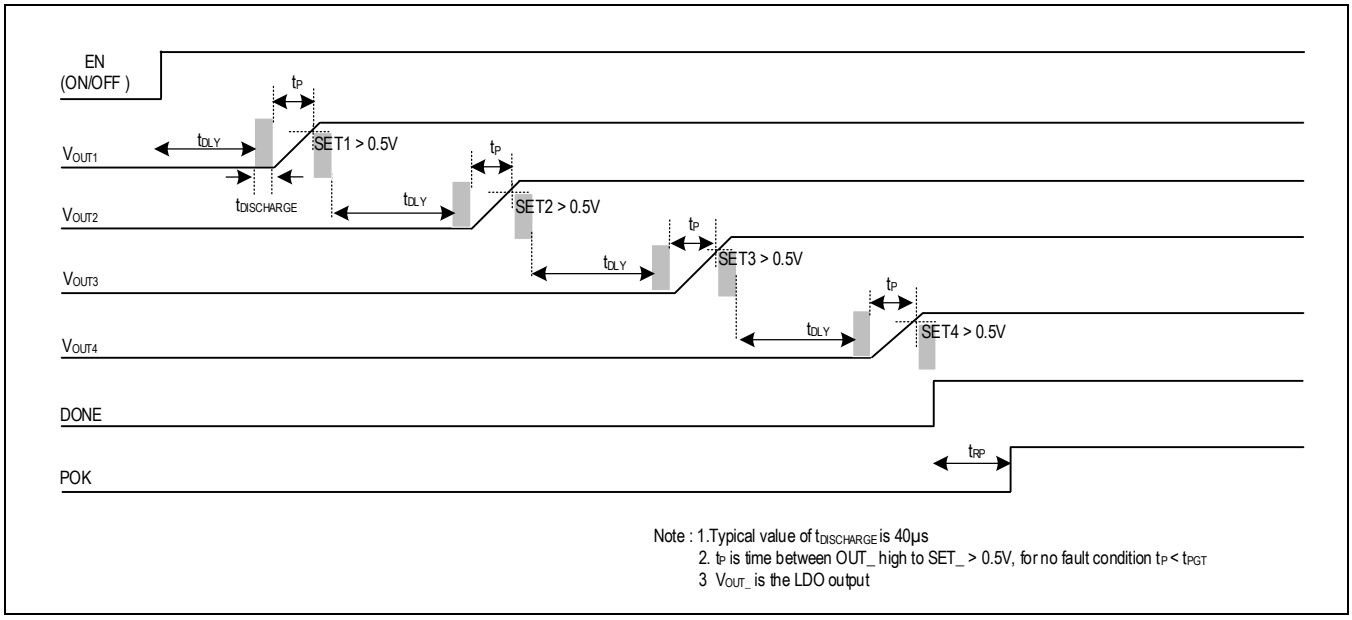


Figure 11. Power-Up Monitoring Timing Diagram. See the Typical Application Circuit (Figure 6).

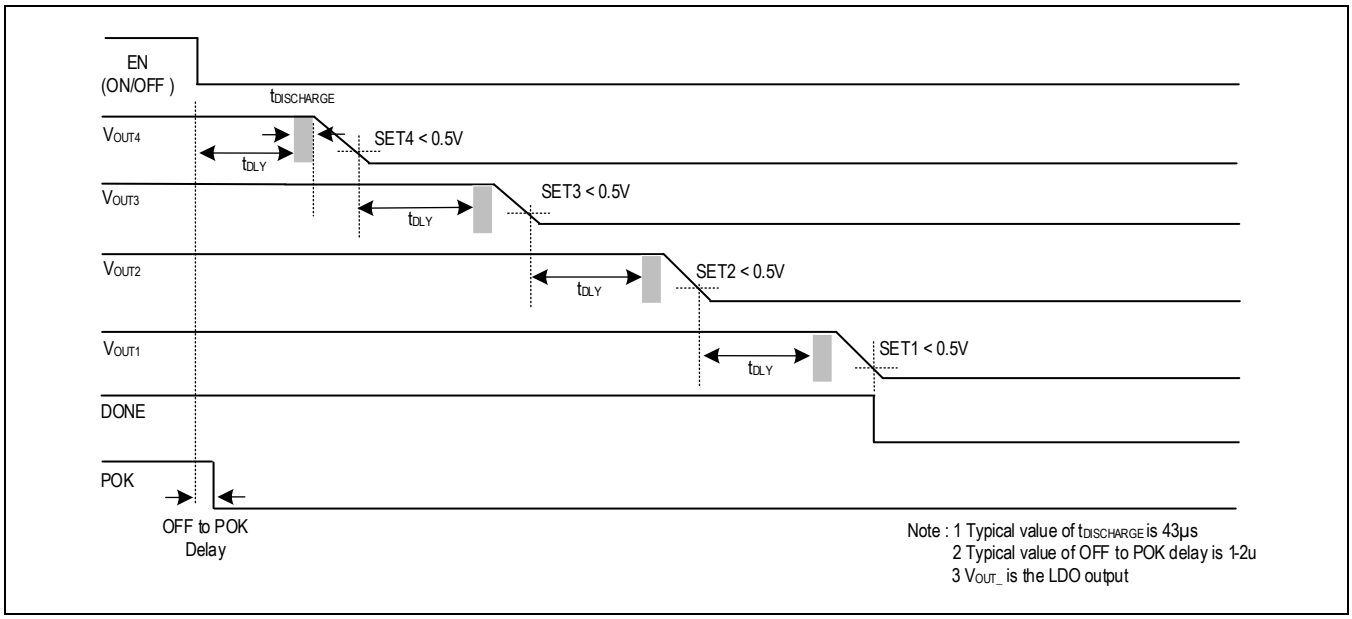


Figure 12. Power-Down Monitoring Timing Diagram. See the Typical Application Circuit (Figure 6).

Daisy-Chaining Using MAX16165/MAX16166

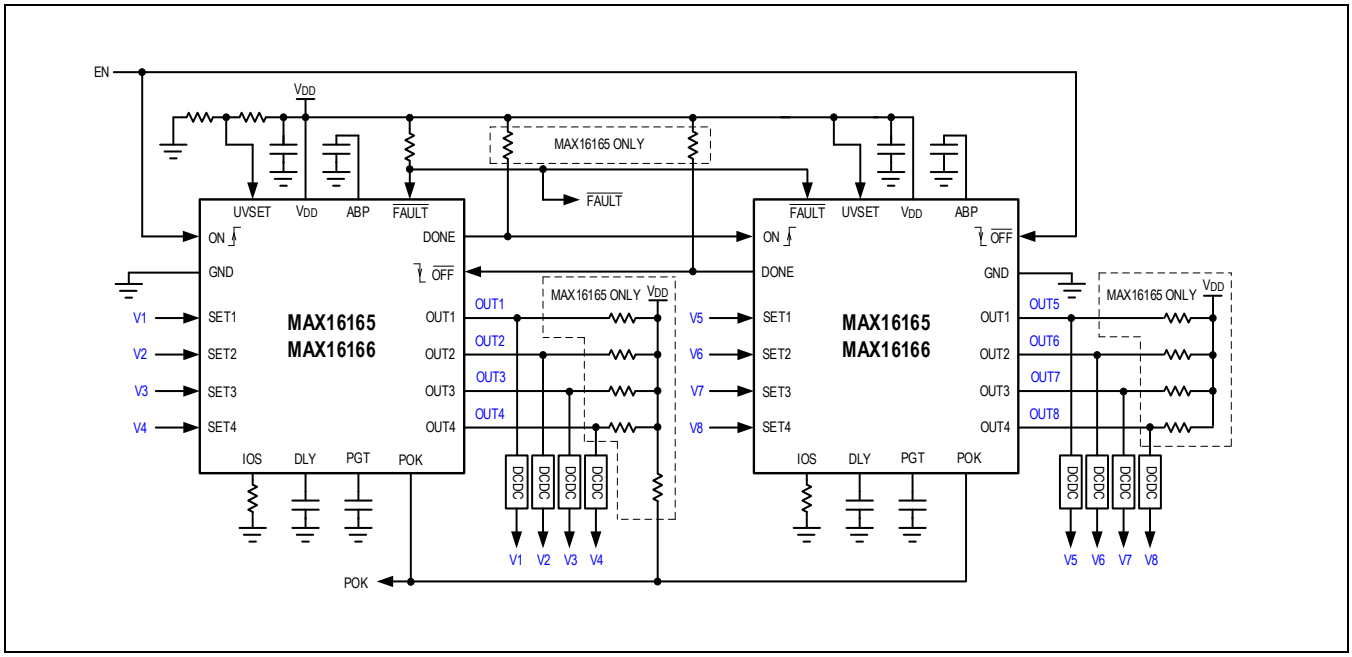


Figure 13. Sequence and Monitor Eight Power Supplies and Monitor V_{DD}.

Ordering Information

PART NUMBER	TEMP. RANGE	PIN-PACKAGE	OUTPUTS	POK RESET TIMEOUT
MAX16166AWPH+T	-40°C to +125°C	20 WLP	Push-pull	100ms
MAX16166A---+T*	-40°C to +125°C	See *Selector Guide* for information	Push-pull	See *Selector Guide* for information
MAX16165ATPH+T	-40°C to +125°C	20 TQFN	Open-drain	100ms
MAX16165A---+T*	-40°C to +125°C	See *Selector Guide* for information	Open-drain	See *Selector Guide* for information

+Denotes a lead(Pb)-free/RoHS-compliant package.

T = Tape and reel.

**Future product—contact factory for availability.*

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	11/21	Release for Market Intro	—
1	4/22	Added MAX16165ATPH+T to the *Ordering Information* table	24

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