AUDIO CLOCK SOURCE

MK2705

Description

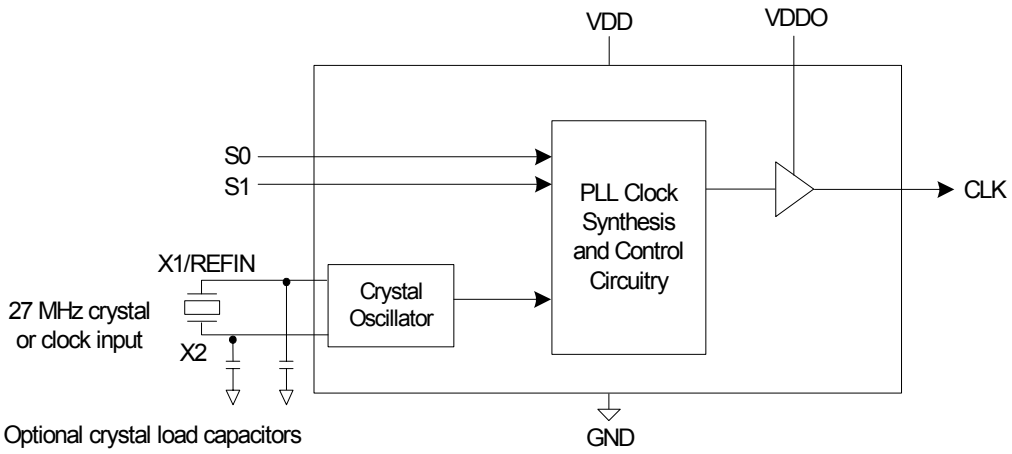
The MK2705 provides synchronous clock generation for audio sampling clock rates derived from an MPEG stream, or can be used as a standalone clock source with a 27 MHz crystal. The device uses the latest PLL technology to provide good phase noise and long term jitter characteristics in a small 8-pin package.

Contact IDT if you have a requirement for an input and output frequency not included in this document.

Features

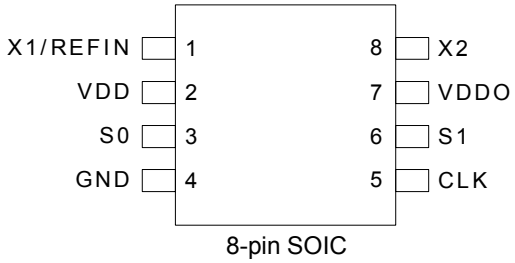
- Packaged in 8-pin (150 mil wide) SOIC
- Clock or crystal input
- Low phase noise
- Low jitter
- Exact (0 ppm) multiplication ratios
- Independent output voltage
- Support for 256 times sampling rate

Block Diagram



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Pin Assignment



8-pin SOIC

Output Clock Selection Table

S1	S0	Input Frequency (MHz)	Output Frequency (MHz)
0	0	27	8.192
0	1	27	11.2896
1	0	27	12.288
1	1	27	24.576

Pin Descriptions

Pin Number	Pin Name	Pin Type	Pin Description
1	X1/REFIN	Input	Connect this pin to a 27 MHz crystal or clock input
2	VDD	Power	Power supply for crystal oscillator and PLL.
3	S0	Input	Output frequency selection. Determines output frequency per table above. On-chip pull-up.
4	GND	Power	Connect to ground.
5	CLK	Output	Clock output.
6	S1	Input	Output frequency selection. Determines output frequency per table above. On-chip pull-up.
7	VDDO	Power	Power supply for output stage.
8	X2	Input	Connect this pin to a 27 MHz crystal. Leave open if using a clock input.

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Application Information

Series Termination Resistor

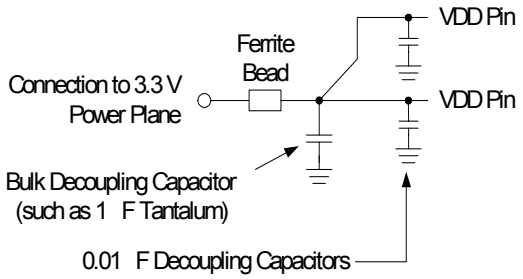
Clock output traces should use series termination. To series terminate a 50Ω trace (a commonly used trace impedance), place a 33Ω resistor in series with the clock line and as close to the clock output pin as possible. The nominal impedance of the clock output is 20Ω

Decoupling Capacitors

As with any high-performance mixed-signal IC, the MK2705 must be isolated from system power supply noise to perform optimally.

Decoupling capacitors of 0.01µF must be connected between each VDD and the PCB ground plane. To further guard against interfering system supply noise, the MK2705 should use one common connection to the PCB power plane as shown in the diagram on the next page. The ferrite bead and bulk capacitor help reduce lower frequency noise in the supply that can lead to output clock phase modulation.

Recommended Power Supply Connection for Optimal Device Performance



Both VDD pins must be connected to the same voltage.

Crystal Load Capacitors

If a crystal is used, the device crystal connections should include pads for capacitors from X1 to ground and from X2 to ground. These capacitors are used to adjust the stray capacitance of the board to match the nominally required crystal load capacitance. To reduce possible noise pickup, use very short PCB traces (and no vias) been the crystal and device.

The value of the load capacitors can be roughly determined by the formula $C = 2(C_L - 6)$ where C is the load capacitor connected to X1 and X2, and C_L is the specified value of the load capacitance for the crystal. A typical crystal C_L is 18 pF, so $C = 2(18 - 6) = 24$ pF. Because these capacitors adjust the stray capacitance of the PCB, check the output frequency using your final layout to see if the value of C should be changed.

PCB Layout Recommendations

Observe the following guidelines for optimum device performance and lowest output phase noise:

1) Each 0.01µF decoupling capacitor should be mounted on the component side of the board as close to the VDD pin as possible. No vias should be used between decoupling capacitor and VDD pin. The PCB trace to VDD pin should be kept as short as possible, as should the PCB trace to the ground via. Distance of the ferrite bead and bulk decoupling from the device is less critical.

2) The external crystal should be mounted next to the device with short traces. The X1 and X2 traces should not be routed next to each other with minimum spaces, instead they should be separated and away from other traces.

3) To minimize EMI and obtain the best signal integrity, the 33Ω series termination resistor should be placed close to the clock output.

4) An optimum layout is one with all components on the same side of the board, minimizing vias through other signal layers (the ferrite bead and bulk decoupling capacitor can be mounted on the back). Other signal traces should be routed away from the MK2705. This includes signal traces just underneath the device, or on layers adjacent to the ground plane layer used by the device.

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Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the MK2705. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Item	Rating
Supply Voltage, VDD	4.5 V
All Inputs and Outputs	-0.5 V to VDD+0.5 V
Ambient Operating Temperature	0 to +70° C
Storage Temperature	-65 to +150° C
Junction Temperature	175° C
Soldering Temperature	260° C

Recommended Operation Conditions

Parameter	Min.	Typ.	Max.	Units
Ambient Operating Temperature	0		+70	° C
Power Supply Voltage (measured in respect to GND)	+3.0		+3.6	V

DC Electrical Characteristics

Unless stated otherwise, **VDD = 3.3 V ±10%**, Ambient Temperature 0 to +70° C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Operating Voltage	VDD		3.0		3.6	V
	VDDO		1.8		VDD	V
Input High Voltage	V_{IH}		2			V
Input Low Voltage	V_{IL}				0.8	V
Output High Voltage	V_{OH}	I_{OH} = -4 mA	VDD-0.4			V
Output High Voltage	V_{OH}	I_{OH} = -20 mA	2.4			V
Output Low Voltage	V_{OL}	I_{OL} = 20 mA			0.4	V
Supply Current	IDD	No Load		24		mA
Short Circuit Current	I_{OS}	Each output		±65		mA
Nominal Output Impedance	Z_{OUT}			20		Ω
Input Capacitance	C_{IN}	Input pins		7		pF
Internal pull-up resistor value	R_{PU}			120		kΩ

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AC Electrical Characteristics

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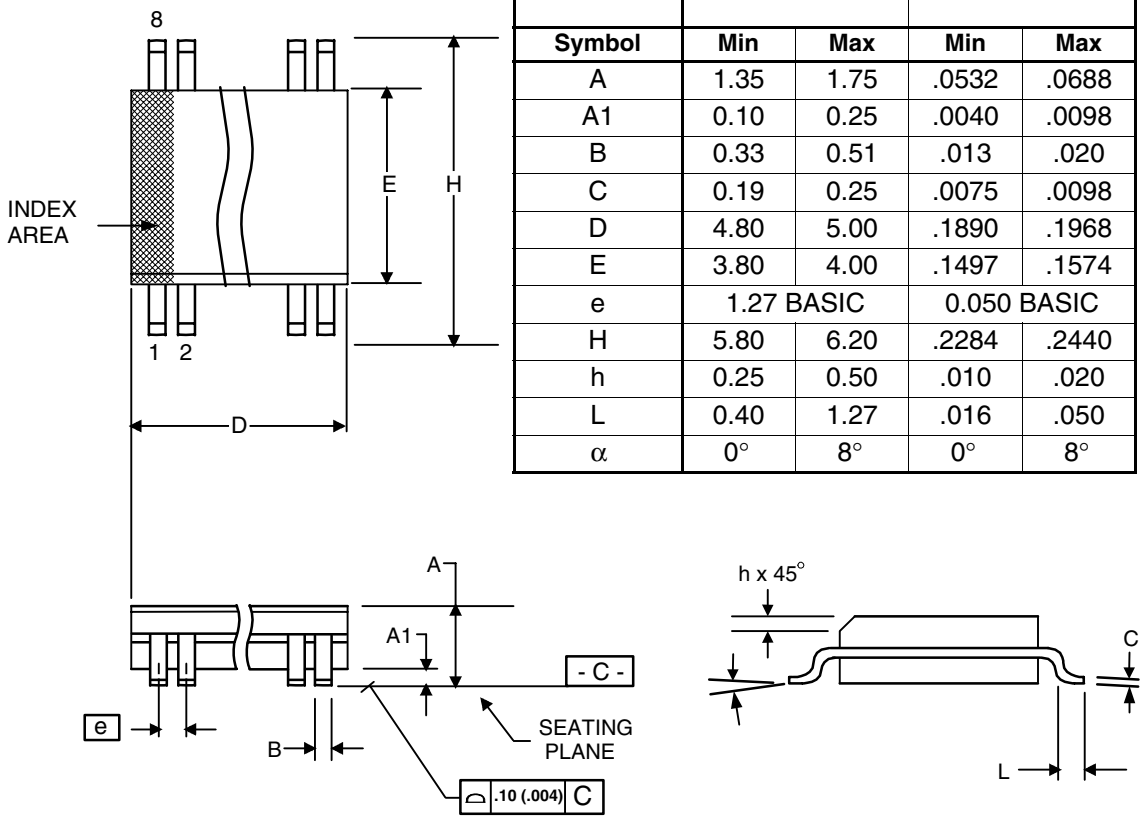
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input frequency				27		MHz
Output duty cycle	t_{OD}	VDD/2, Note 1	45	49 to 51	55	%
Output clock rise time	t_{OR}	20% to 80%, Note 1			1.5	ns
Output clock fall time	t_{OF}	80% to 20%, Note 1			1.5	ns
Jitter, short term		peak to peak, Note 1		175		ps
Jitter, long term		10 us delay peak to peak, Note 1		300		ps
Frequency synthesis error				0		ppm
Single sideband phase noise		10 kHz offset		-110		dBc

Note 1: Measured with 15 pF load

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Package Outline and Package Dimensions (8-pin SOIC, 150 mil Body)

Package dimensions are kept current with JEDEC Publication No. 95



	Millimeters		Inches	
Symbol	**Min**	**Max**	**Min**	**Max**
A	1.35	1.75	.0532	.0688
A1	0.10	0.25	.0040	.0098
B	0.33	0.51	.013	.020
C	0.19	0.25	.0075	.0098
D	4.80	5.00	.1890	.1968
E	3.80	4.00	.1497	.1574
e	1.27 BASIC		0.050 BASIC	
H	5.80	6.20	.2284	.2440
h	0.25	0.50	.010	.020
L	0.40	1.27	.016	.050
α	0°	8°	0°	8°

Ordering Information

Part / Order Number	Marking	Shipping packaging	Package	Temperature
MK2705SLF	MK2705SL	Tubes	8-pin SOIC	0 to +70° C
MK2705SLFTR	MK2705SL	Tape and Reel	8-pin SOIC	0 to +70° C

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