BLU-RAY DISC VCXO

MK3732-22

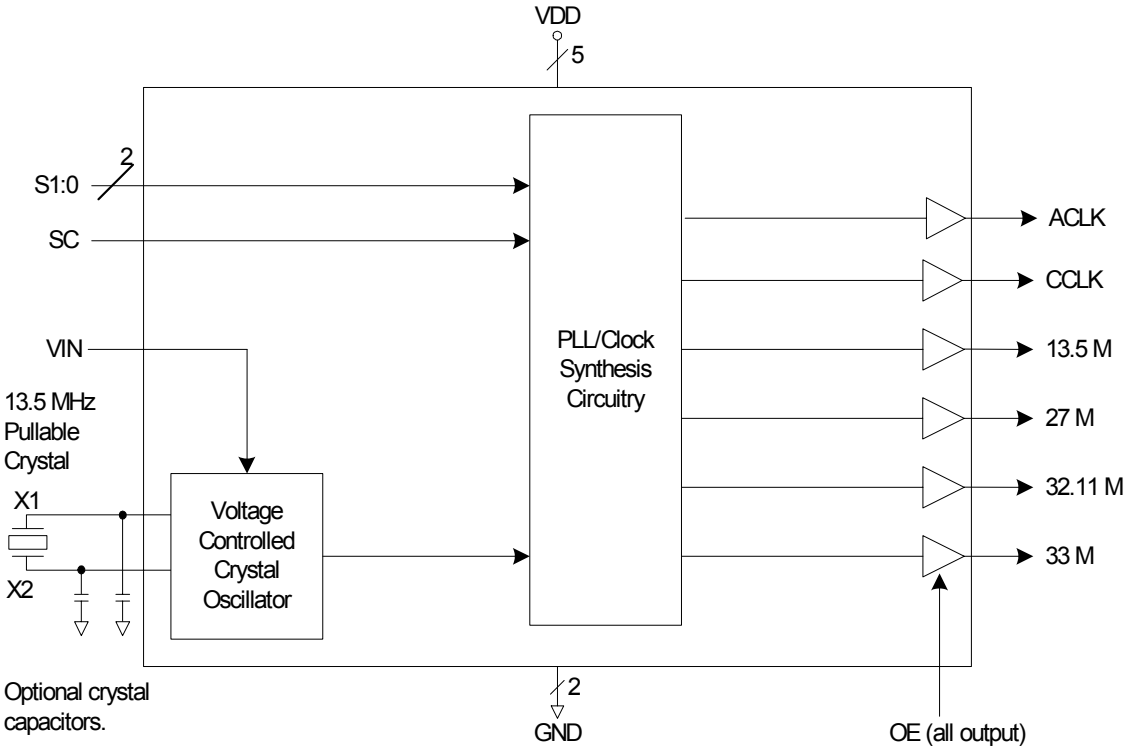
Description

The MK3732-22 is a low-cost, low-jitter, 3.3 Volt VCXO designed to replace expensive VCXOs. Using an advanced clock synthesizer with on-chip Phase-Locked Loops (PLLs), MK3732-22 generates six high-quality clock outputs from a low cost, 13.5 MHz crystal. It can replace multiple voltage controlled crystal oscillators, saving board space and cost. The patented on-chip Voltage Controlled Crystal Oscillator accepts a 0 to 3.3 V input voltage to cause the output clocks to vary by ±100 ppm. The higher intrinsic VCXO gain of the MK3732-22 helps compensate for the reduced pullability of a low quality crystal and is ideal for PWM applications.

Features

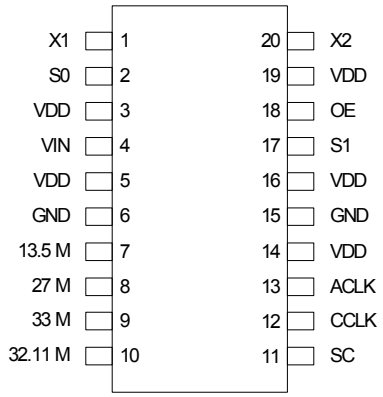
- Packaged in 20-pin SSOP
- Available in Pb (lead) free package
- Input frequency of 13.5 MHz
- Multiple output frequencies
- 200 ohms start-up margin at all levels of VIN
- OE pin tri-states the outputs for board testing
- Operating voltage of 3.3 V
- Advanced, low-power CMOS process

Block Diagram



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Pin Assignment



20 pin (150 mil) SSOP (QSOP)

AUDIO CLK Output Table

S1	S0	ACLK (MHz)
0	0	8.192
0	1	11.2896
1	0	12.288
1	1	18.4323

COMM CLK Output Table

SC	CCLK (MHz)
0	26.8
1	24.576

Note 1: S1, S0, SC have an internal pull-up resistor.

Pin Descriptions

Pin Number	Pin Name	Pin Type	Pin Description
1	X1	Input	Crystal connection. Connect to 13.5 MHz fundamental mode pullable crystal.
2	S0	Input	Select ACLK per table above. Internal pull-up.
3	VDD	Power	Connect to +3.3 V.
4	VIN	Input	VCXO voltage input. Zero to 3.3 V analog voltage for VCXO.
5	VDD	Power	Connect to +3.3 V.
6	GND	Power	Connect to ground.
7	13.5 M	Output	13.5 MHz clock output. Output tri-stated when OE is low.
8	27 M	Output	27 MHz clock output. Output tri-stated when OE is low.
9	33 M	Output	33 MHz reference clock output. Output tri-stated when OE is low.
10	32.11 M	Output	32.11 MHz clock output. Output tri-stated when OE is low.
11	SC	Input	Select CCLK per table above. Internal pull-up.
12	CCLK	Output	Communication clock output. Determined by table above.
13	ACLK	Output	Audio clock output. Determined by table above.
14	VDD	Power	Connect to +3.3 V.
15	GND	Power	Connect to ground.
16	VDD	Power	Connect to +3.3 V.
17	S1	Input	Select ACLK per table above. Internal pull-up.

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Pin Number	Pin Name	Pin Type	Pin Description
18	OE	Input	Output enable. Tri-states all output when low. Internal pull-up
19	VDD	Power	Connect to +3.3 V.
20	X2	Output	Crystal connection. Connect to 13.5 MHz fundamental mode pullable crystal.

External Components

Decoupling Capacitor

As with any high-performance mixed-signal IC, the MK3732-22 must be isolated from system power supply noise to perform optimally.

A decoupling capacitor of 0.01µF must be connected between each VDD and the PCB ground plane.

Series Termination Resistor

Clock output traces over one inch should use series termination. To series terminate a 50Ω trace (a commonly used trace impedance), place a 33Ω resistor in series with the clock line, as close to the clock output pin as possible. The nominal impedance of the clock output is 20Ω.

Quartz Crystal

The MK3732-22 VCXO function consists of the external crystal and the integrated VCXO oscillator circuit. To assure the best system performance (frequency pull range) and reliability, the layout guidelines discussed in the following section must be followed.

The frequency of oscillation of a quartz crystal is determined by its “cut” and by the load capacitors connected to it. The MK3732-22 incorporates on-chip variable load capacitors that “pull” (change) the frequency of the crystal. The crystal specified for use with the MK3732-22 is designed to have zero frequency error when the total of on-chip + stray capacitance is 12 pF.

The external crystal must be connected as close to the chip as possible and should be on the same side of the PCB as the MK3732-22. There should be no vias between the crystal pins and the X1 and X2 device pins. There should be no signal traces underneath or close to the crystal.

Crystal Tuning Load Capacitors

The crystal traces should include pads for small fixed capacitors, one between X1 and ground, and another between X2 and ground. Stuffing of these capacitors on the PCB is optional. The need for these capacitors is determined at system prototype evaluation, and is influenced by the particular crystal used (manufacture and frequency) and by PCB layout. The typical required capacitor value is 1 to 4 pF.

To determine the need for and value of the crystal adjustment capacitors, you will need a PC board of your final layout, a frequency counter capable of about 1 ppm resolution and accuracy, two power supplies, and some samples of the crystals which you plan to use in production, along with measured initial accuracy for each crystal at the specified crystal load capacitance, CL.

To determine the value of the crystal capacitors:

1. Connect VDD of the MK3732-22 to 3.3 V. Connect pin 4 of the MK3732-22 to the second power supply. Adjust the voltage on pin 4 to 0V. Measure and record the frequency of the 13.5 M output.

2. Adjust the voltage on pin 4 to 3.3 V. Measure and record the frequency of the same output.

To calculate the centering error:

$$Error = 10^6 x\left[\frac{(f_{3.3V} - f_{target}) + (f_{0V} - f_{target})}{f_{target}}\right] - error_{xtal}$$

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Where:

f_{target} = nominal crystal frequency

$error_{xtal}$ =actual initial accuracy (in ppm) of the crystal being measured

If the centering error is less than ±25 ppm, no adjustment is needed. If the centering error is more than 25 ppm negative, the PC board has excessive stray capacitance and a new PCB layout should be considered to reduce stray capacitance. (Alternately, the crystal may be re-specified to a higher load capacitance. Contact ICS for details.) If the centering error is more than 25 ppm positive, add identical fixed centering capacitors from each crystal pin to ground.

The value for each of these caps (in pF) is given by:

External Capacitor =

2 x (centering error)/(trim sensitivity)

Trim sensitivity is a parameter which can be supplied by your crystal vendor. If you do not know the value, assume it is 30 ppm/pF. After any changes, repeat the measurement to verify that the remaining error is acceptably low (typically less than ±25 ppm).

PCB Layout Recommendations

For optimum device performance and lowest output phase noise, the following guidelines should be observed.

1) The 0.01µF decoupling capacitors should be mounted on the component side of the board as close to the VDD pins as possible. No vias should be used between the decoupling capacitors and VDD pins. The PCB trace to VDD pin should be kept as short as possible, as should the PCB trace to the ground via.

2) The external crystal should be mounted just next to the device with short traces. The X1 and X2 traces should not be routed next to each other with minimum spaces, instead they should be separated and away from other traces.

3) To minimize EMI, the 33Ω series termination resistor (if needed) should be placed close to the clock output.

4) An optimum layout is one with all components on the same side of the board, minimizing vias through other signal layers. Other signal traces should be routed away from the MK3732-22. This includes signal traces just underneath the device, or on layers adjacent to the ground plane layer used by the device.

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the MK3732-22. These ratings, which are standard values for ICS commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Parameter	Condition	Min.	Typ.	Max.	Units
Supply Voltage, VDD	Referenced to GND			7	V
Inputs	Referenced to GND	-0.5		VDD+ 0.5	V
Clock Outputs	Referenced to GND	-0.5		VDD+ 0.5	V
Storage Temperature		-65		150	°C
Soldering Temperature	Max 10 seconds			260	°C
Junction Temperature				125	°C

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Recommended Operation Conditions

Parameter	Min.	Typ.	Max.	Units
Ambient Operating Temperature	0		+70	°C
Power Supply Voltage (measured in respect to GND)	+3.15	+3.3	+3.45	V
Power Supply Ramp Time			4	ms

DC Electrical Characteristics

Unless stated otherwise, **VDD = 3.3V ±5%**, Ambient Temperature 0 to +70°C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Operating Voltage	VDD		3.135	3.3	3.465	V
Supply Current	IDD	No load, OE = 1		48		mA
	IDDPD	No load, OE = 0		38		mA
Input High Voltage	V_{IH}	SEL	2			V
Input Low Voltage	V_{IL}	SEL			0.8	V
Output High Voltage	V_{OH}	I_{OH} = -4 mA	VDD-0.4			V
Output High Voltage	V_{OH}	I_{OH} = -12 mA	2.4			V
Output Low Voltage	V_{OL}	I_{OL} = 12 mA			0.4	V
Short Circuit Current	I_{OS}	Clock outputs		±70		mA
Input Capacitance	C_{IN}	Input selects		5		pF
Nominal Output Impedance	Z_{OUT}			20		Ω
Internal Pull-up Resistor	R_{PU}	Input selects		360		kΩ

AC Electrical Characteristics

Unless stated otherwise, **VDD = 3.3V ±5%**, Ambient Temperature 0 to +70° C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input Frequency, crystal input	f_{IN}	Note 1		13.5		MHz
Output Rise Time	t_{OR}	20% to 80%, Note 2		1.2		ns
Output Fall Time	t_{OF}	80% to 20%, Note 2		1.0		ns
Crystal Pullability	f_p	0V≤ VIN ≤ 3.3 V, Note 1		±100		ppm
VCXO Gain	k_O	VIN=VDD/2 ±1 V, Note1		120		ppm/V
Cycle Jitter (short term)		peak-to-peak, Note 2		±250		ps
Duty Cycle		Note 2	40	50	60	%
Output Frequency Synthesis Error		All outputs except 32.11 MHz, and 18.4323 MHz clocks		0		ppm

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Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Output Frequency Synthesis Error		32.11 MHz clocks		6		ppm
Output Frequency Synthesis Error		18.4323 MHz clock		-3		ppm
Power-up Time	t_{PU}	from VDD minimum to output clock stable to ±1%		3		ms

Note 1: With an ICS approved crystal.

Note 2: Measured with 15 pF load.

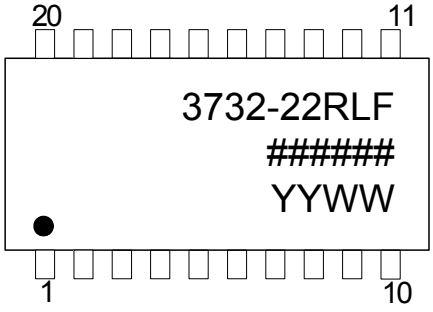
Thermal Characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Thermal Resistance Junction to Ambient	θ_{JA}	Still air		78		°C/W
	θ_{JA}	1 m/s air flow		70		°C/W
	θ_{JA}	3 m/s air flow		68		°C/W
Thermal Resistance Junction to Case	θ_{JC}			37		°C/W

Marking Diagram



Marking Diagram (Pb free)



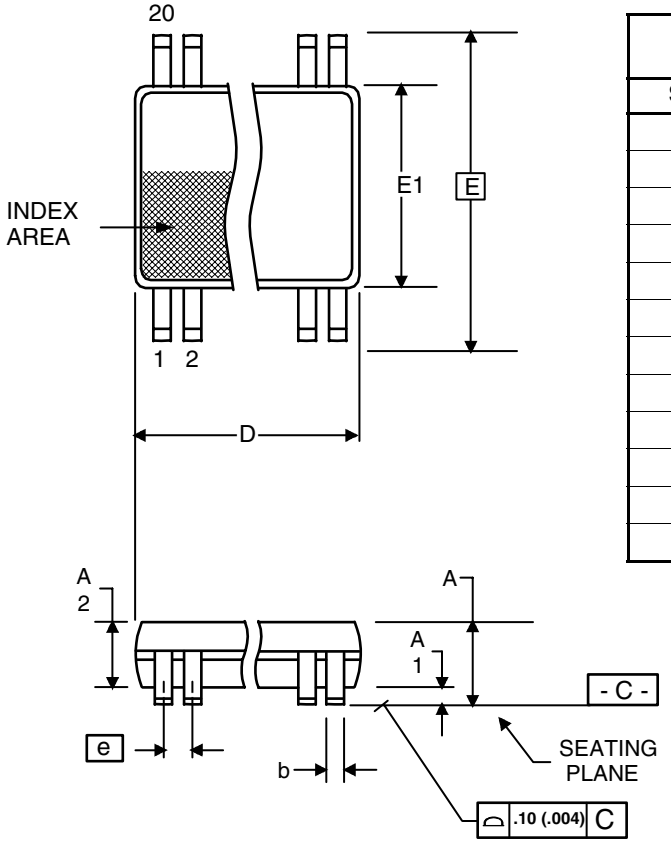
Notes:

1. ###### is the lot code.
2. YYWW is the last two digits of the year, and the week number that the part was assembled.
3. “LF” designates Pb (lead) free package.

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Package Outline and Package Dimensions (20-pin SSOP, 10 Mil. Wide Body)

Package dimensions are kept current with JEDEC Publication No. 95



	Millimeters		Inches	
Symbol	**Min**	**Max**	**Min**	**Max**
A	1.35	1.75	0.053	0.069
A1	0.10	0.25	0.004	0.010
A2	--	1.50	--	0.059
b	0.20	0.30	0.008	0.012
c	0.18	0.25	0.007	0.010
D	8.55	8.75	0.337	0.344
E	5.80	6.20	0.228	0.244
E1	3.80	4.00	0.150	0.157
e	.635 Basic		.025 Basic	
L	0.40	1.27	0.016	0.050
α	0°	8°	0°	8°
aaa	--	0.10	--	0.004

Ordering Information

Part / Order Number	Marking	Shipping Packaging	Package	Temperature
MK3732-22R	See page 6	Tubes	20-pin SSOP	0 to +70° C
MK3732-22RTR		Tape and Reel	20-pin SSOP	0 to +70° C
MK3732-22RLF	See page 6	Tubes	20-pin SSOP	0 to +70° C
MK3732-22RLFTR		Tape and Reel	20-pin SSOP	0 to +70° C

Parts that are ordered with a "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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