DUAL 1 TO 8 BUFFALO™ CLOCK DRIVER MK74CB218

Description

The MK74CB218 Buffalo™ is a monolithic CMOS high speed clock driver. It consists of two identical single input to eight low-skew output, non-inverting clock drivers. This eliminates concerns of part to part matching in many systems. The MK74CB218 is packaged in the tiny 28-pin SSOP, which uses the same board space as the narrow 16-pin SOIC. The inputs can be connected together for a 1 to 16 fanout buffer.

A quad 1 to 4, and PECL versions, are also available. Consult IDT for more details.

The MK74CB218 can also act as a voltage translator, since it is possible to run the inputs at 3.3 V and the outputs at 2.5 V.

Features

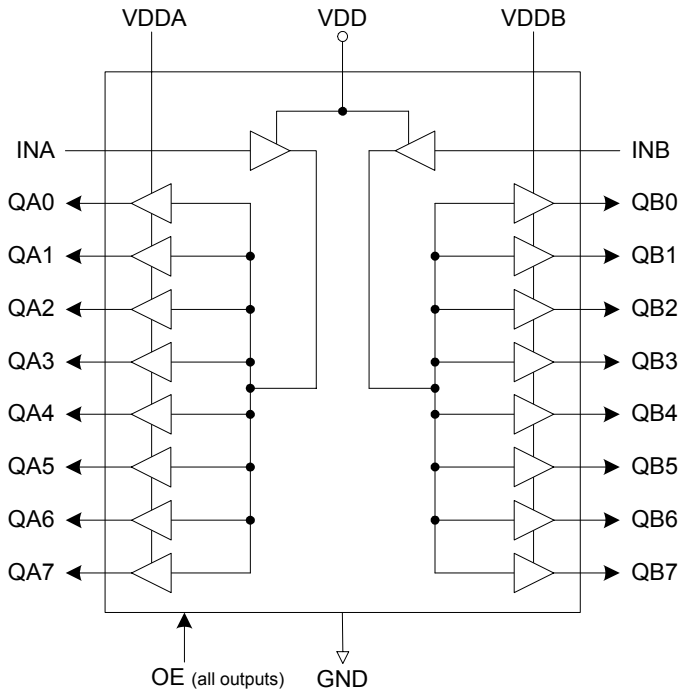
- Packaged as 28-pin SSOP (150 mil body)
- Pb (lead) free package, RoHS compliant
- Dual one input to eight output clock drivers
- Outputs are skew matched to within 250 ps
- A outputs and B outputs matched to 250 ps
- 2.5 V or 3.3 V output voltages
- Output Enable tri-states each bank of eight
- Clock speeds up to 200 MHz

Family of IDT Parts

The MK74CB218 Buffalo™ is designed to be used with IDT's clock synthesizer devices. The inputs of the Buffalo are matched to the outputs of IDT clock synthesizers. Consult IDT for applications support.

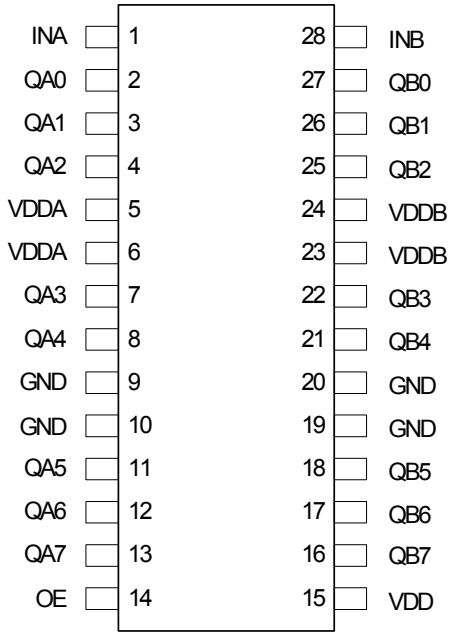
Not recommended for new designs. See the MK74CB218B for new designs.

Block Diagram

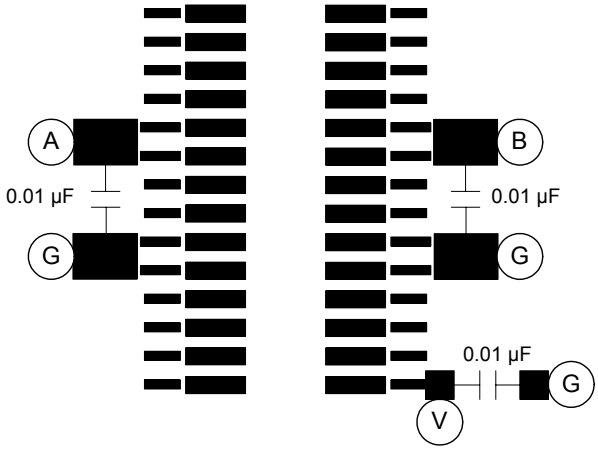


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Pin Assignment



Suggested Layout



NOTE: 33 ohm series termination resistors for each output are essential for operation.
For simplicity, series termination resistors are not shown for the outputs, but should be placed as close to the device as possible. It is most critical to have the 0.01 µF decoupling capacitors closest.

A = connect to VDDA
B = connect to VDDB
V = connect to VDD
G = connect to low inductance ground plane

Pin Descriptions

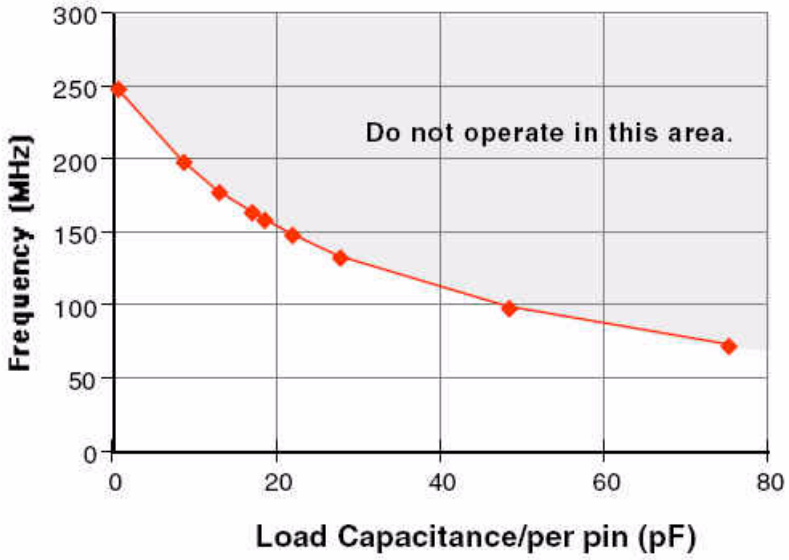
Pin Number	Pin Name	Pin Type	Pin Description
1	INA	Input	Clock input for eight A outputs.
2, 3, 4	QA0, QA1, QA2	Output	Clock A outputs.
5, 6	VDDA	Power	Power supply for QA outputs. Connect to a voltage from 2.5 V to VDD. Cannot exceed VDD.
7, 8	QA3, QA4	Output	Clock A outputs.
9, 10	GND	Power	Connect to ground.
11, 12, 13	QA5, QA6, QA7	Output	Clock A outputs.
14	OE	Input	Output Enable. Tri-states all clock outputs when this input is low. Internal pull-up to VDD.
15	VDD	Power	Power supply for inputs.
16, 17, 18	QB7, QB6, QB5	Output	Clock B outputs.
19, 20	GND	Power	Connect to ground.
21, 22	QB4, QB3	Output	Clock B outputs.
23, 24	VDDB	Power	Power supply for QB outputs. Connect to a voltage from 2.5 V to VDD. Cannot exceed VDD.
25, 26, 27	QB2, QB1, QB0	Output	Clock B outputs.
28	INB	Input	Clock input for eight B outputs.

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Maximum Speed

The maximum speed at which the chip can operate is limited by the power dissipation in the package. Graph 1 shows the operating frequency plotted against load capacitance per pin for a die temperature of 125°C. This is at VDD = VDDA = VDDB = 3.3 V, 70°C and with 33Ω series termination resistors.The termination resistors are essential because they allow a large proportion of the total power dissipated outside the package. Reducing or eliminating the series termination will cause an increase in die temperature. It is not recommended to operate the chip at die temperatures greater than 125°C. Also note that the load capacitance per pin must include PC board parasitics such as trace capacitance.

If not all outputs of the chip are used, it is possible to operate the chip faster with larger loads. Consult IDT for your specific requirement.



Graph 1
MK74CB218
Maximum Speed with all VDDs at 3.3V

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Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the MK74CB218. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Item	Rating
Supply Voltage, VDD (referenced to GND)	5.2 V
All Inputs and Outputs (referenced to GND)	-0.5 V to VDD+0.5 V
Ambient Operating Temperature	0 to +70° C
Storage Temperature	-65° C to 150° C
Soldering Temperature	260° C (max. of 20 seconds)

DC Electrical Characteristics

Unless stated otherwise, **VDD = 3.3 V ±10%**

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Operating Voltage	VDD		3.0	3.3	3.6	V
Operating Voltage	VDDA or VDDB		2.375		VDD	V
Operating Supply Current	IDD	At 100 MHz, No load		75		mA
Input High Voltage	V_{IH}	INA, INB pins	0.65VDD			V
Input Low Voltage	V_{IL}	INA, INB pins			0.35VDD	V
Input High Voltage	V_{IH}	OE pin	2.0			V
Input Low Voltage	V_{IL}	OE pin			0.8	V
Output High Voltage	V_{OH}	I_{OH} = -12 mA	VDD-0.4			V
Output High Voltage	V_{OH}	I_{OH} = -25 mA	2.4			V
Output Low Voltage	V_{OL}	I_{OL} = 25 mA			0.8	V
Output High Voltage	V_{OH}	VDD = 2.5 V, I_{OH} = -16 mA	2			V
Output Low Voltage	V_{OL}	VDD = 2.5 V, I_{OL} = 16 mA			0.5	V
Output Impedance				14		Ω
Short Circuit Current		Each output, VOUT=GND or VDD		100		mA
Input Capacitance	C_{IN}			7		pF
On-chip Pull-up Resistor	R_{PU}	OE		250		kΩ

Note: Short circuits may be applied indefintely, but only one output may be shorted at a time to prevent exceeding the power dissipation rating of this package.

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AC Electrical Characteristics

Unless stated otherwise, **VDD = 3.3 V ±10%**

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input Clock Frequency	F_{IN}	Note 3	0		200	MHz
Propagation Delay, 3.3 V		With load = 15 pF		3	6	ns
Output Clock Rise Time		20% to 80%, C_L=10 pF		1	2	ns
Output Clock Rise Time		VDD = 2.5 V, 20% to 80%, C_L=10 pF		2	3	ns
Output Clock Fall Time		80% to 20%, C_L=10 pF		1	2	ns
Output Clock Fall Time		VDD = 2.5 V, 80% to 20%, C_L=10 pF		2	3	ns
Output Duty Cycle		VDD = 3.3 V or 2.5 V, C_L=10 pF	40	50	60	%
Output Clock Rising Edge Skew		At VDD/2, Note 1		100	250	ps
Output Clock A to B Skew		At VDD/2, Note 2		100	250	ps
Output Enable Time		OE high to output on			20	ns
Output Disable Time		OE low to tri-state			20	ns

Notes:

1. Between any two A outputs, or any two B outputs, with equal loading.
2. Between any clock A output and any clock B output with INA connected to INB, and equal loading.
3. See discussion and graph of speed versus load.

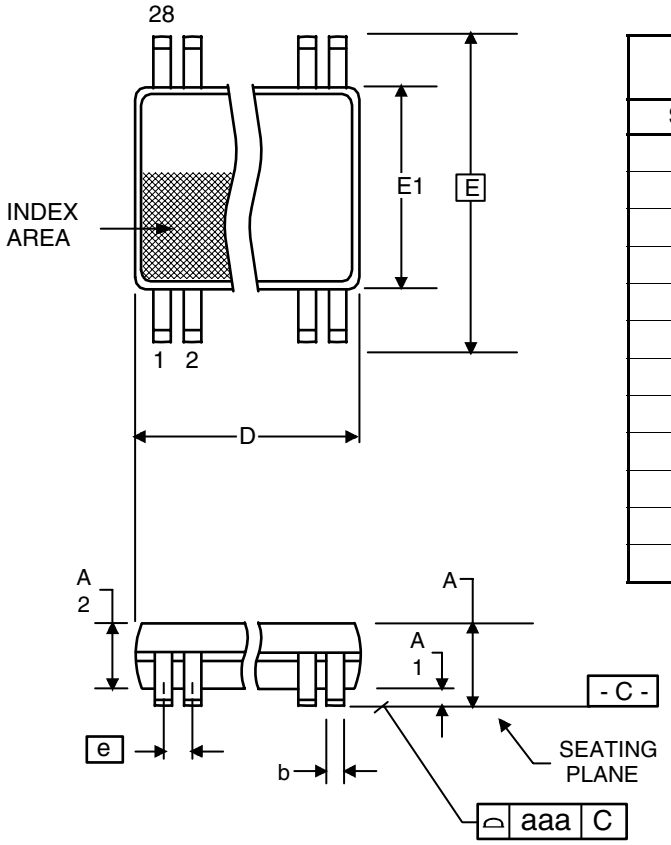
Thermal Characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Thermal Resistance Junction to Ambient	θ_{JA}	Still air		100		°C/W
	θ_{JA}	1 m/s air flow		80		°C/W
	θ_{JA}	3 m/s air flow		67		°C/W
Thermal Resistance Junction to Case	θ_{JC}			60		°C/W

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Package Outline and Package Dimensions (28-pin SSOP, 150 mil Body)

Package dimensions are kept current with JEDEC Publication No. 95, MO-153



	Millimeters		Inches	
Symbol	**Min**	**Max**	**Min**	**Max**
A	1.35	1.75	.053	.069
A1	0.10	0.25	.0040	.010
A2	--	1.50	--	.059
b	0.20	0.30	.008	.012
C	0.18	0.25	.007	.010
D	9.80	10.00	.386	.394
E	5.80	6.20	.228	.244
E1	3.80	4.00	.150	.157
e	0.635 Basic		0.025 Basic	
L	0.40	1.27	.016	.050
α	0°	8°	0°	8°
aaa	--	0.10	--	0.004

Ordering Information

Part / Order Number	Marking	Shipping Packaging	Package	Temperature
MK74CB218RLF	MK74CB218RLF	Tubes	28-pin SSOP	0 to +70° C
MK74CB218RLFTR	MK74CB218RLF	Tape and Reel	28-pin SSOP	0 to +70° C

Parts that are ordered with a "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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