MP201

Dying Gasp Storage and Release Control IC

The Future of Analog IC Technology

DESCRIPTION

The MP201 is a dying gasp storage and release controller. It charges storage capacitor from the input during normal operation. Once the storage capacitor is charged to the selected voltage, the charge is stopped, and the storage capacitor is separated from the input. The charging circuit maintains the storage voltage after the charge is completed.

The MP201 keeps monitoring the input voltage, and releases the charge from storage capacitor to input capacitor when the input voltage is lower than the selected release voltage. It regulates the input voltage to keep it close to release voltage for as long as possible.

The MP201 has built-in current limit circuit during the charging up of the storage capacitors. The storage and release voltage can be programmed to user's desired value by external resistors.

The MP201 comes in an SOIC-8 package and requires a minimum number of readily available standard external components.

FEATURES

- Wide 4.5V to 18V Input Operating Range
- 2.5A dumping current from Storage to VIN
- Built-in 260mA Current Limit for Charging Storage Capacitor
- User Programmable Storage and Release Voltage
- Dying Gasp FLAG Indicator
- Available in SOIC-8 package

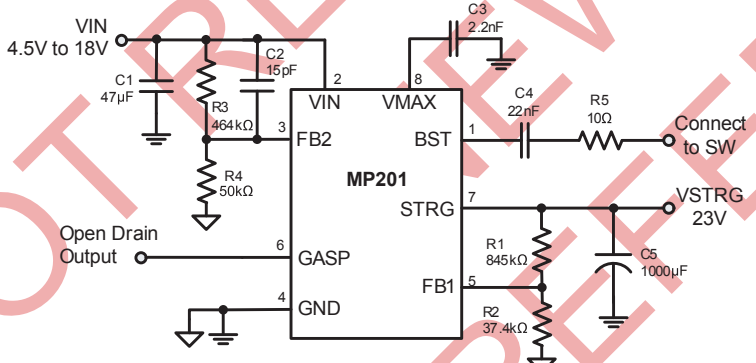
APPLICATIONS

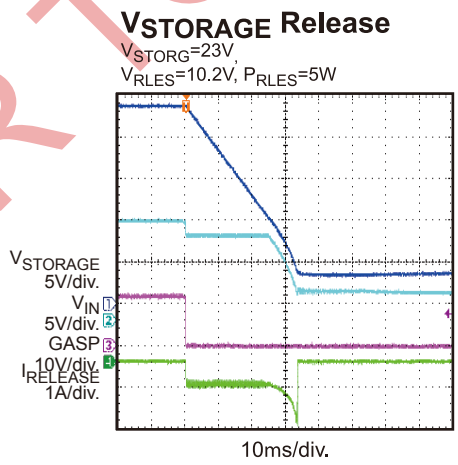
- Cable/DSL/PON Modems
- Home Gateway
- Access Point Networks

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TYPICAL APPLICATION





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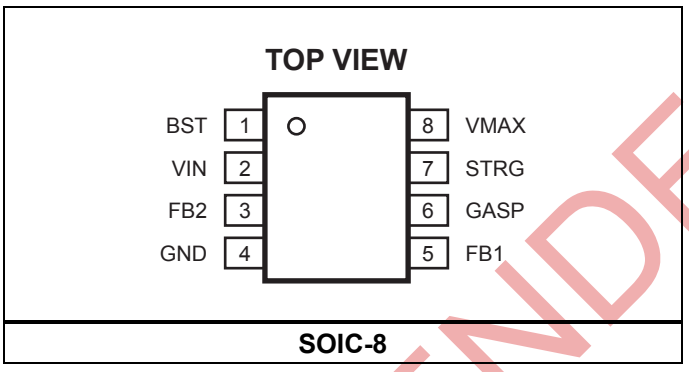
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ORDERING INFORMATION

Part Number*	Package	Top Marking
MP201DS	SOIC-8	MP201

* For Tape & Reel, add suffix –Z (eg.MP201DS–Z);
For RoHS compliant packaging, add suffix –LF (e.g. MP201DS–LF–Z)

PACKAGE REFERENCE



SOIC-8

ABSOLUTE MAXIMUM RATINGS (1)

V_{IN} .....-0.3V to 22V
V_{BST}. .....-0.3V to 40V
V_{BST}-V_{IN}.....-0.3V to 25V
V_{MAX}.....-0.3V to 42V
V_{MAX}-V_{IN}.....-0.3V to 25V
V_{STRG} .....-0.3V to 32V
V_{STRG}-V_{IN}.....-0.3V to 25V
V_{GASP} .....-0.3V to 22V
All Other Pins .....-0.3V to 6.5V
Junction Temperature .....150°C
Lead Temperature .....260°C
Continuous Power Dissipation (T_A = +25°C) (2)
..... 1.39W
Junction Temperature.....150°C

Recommended Operating Conditions (3)

Supply Voltage V_{IN} .....4.5V to 18V
Storage Voltage V_{STRG} .....
.....Vin to 2×V_{IN}-0.8V(32V max)
Operating Junction Temp. (T_J). -40°C to +125°C

Thermal Resistance (4)	θ_{JA}	θ_{JC}
SOIC-8	90	45 °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

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ELECTRICAL CHARACTERISTICS (5)

V_{IN} = 12V, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Input Supply Voltage Range	V_{IN}		4.5		18	V
Supply Current (Quiescent)	I_{IN}	V_{FB} = 1.1V		250	300	μA
VIN Under Voltage Lockout Threshold Rising	$INUV_{Vth}$		2.5	3.0	3.5	V
VIN Under Voltage Lockout Threshold Hysteresis	$INUV_{HYS}$			250		mV
Storage Feedback Voltage	V_{FB1}		0.97	1	1.03	V
Release Feedback Voltage	V_{FB2}		0.97	1	1.03	V
Vstorage Refresh Threshold-High	V_{FB1_H}			1.025	1.05	V
Vstorage Refresh Threshold-Low	V_{FB1_L}		0.95	0.975		V
Vstorage Refresh Threshold-Hysteresis	V_{FB1_Hys}			50		mV
Feedback Current	I_{FB}	V_{FB1}= V_{FB2}=1V		10	50	nA
GASP High Threshold(6)	VTH_{GASP}			1.05		V
GASP Low Threshold(6)	VTL_{GASP}			1		V
GASP Rising Delay Time	$GASP_{TdR}$			73		μs
GASP Falling Delay Time	$GASP_{TdF}$			0.7		μs
GASP Sink Current Capability	V_{GASP}	Sink 4mA		0.2	0.3	V
GASP Leakage Current	I_{GASP_LEAK}	V_{GASP}=3.3V		0.01	0.1	uA
Input Inrush Current Limit for Charging Storage Capacitor	$I_{PRECHARGE_LIMIT}$	V_{IN}=12V, Charging $C_{STORAGE}$ from 0 to V_{IN}	0.2	0.26	0.33	A
Current limit for Dumping Charge from CSTORAGE to V_{IN}	I_{DUMP_LIMIT}		2	2.5	3	A
Thermal Shutdown(7)	T_{SD}			150		ºC
Thermal Shutdown Hysteresis(7)	T_{HYS}			30		ºC

Notes:

5) Production test at +25°C. Specifications over the temperature range are guaranteed by design and characterization.

6) This voltage is FB2 voltage.

7) Guaranted by design

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PIN FUNCTIONS

Pin #	Name	Description
1	BST	Bootstrap. A capacitor and a resistor in series connected between this pin and DC/DC converter's SW node is required to charge storage capacitor.
2	VIN	Supply Voltage. The MP201 operates from a +4.5V to +18V input rail. Input decoupling capacitor is needed to decouple the input rail.
3	FB2	Feedback to set release voltage.
4	GND	System Ground. This pin is the reference ground of the regulated output voltage. For this reason care must be taken in PCB layout. Suggested to be connected to GND with copper and vias.
5	FB1	Feedback to set storage voltage.
6	GASP	Open drain output to indicate dying gasp operation is active.
7	STRG	Connect to storage capacitor for dying gasp storage and release operation.
8	VMAX	Internal Supply. A 2.2nF ceramic capacitor is required for decoupling.

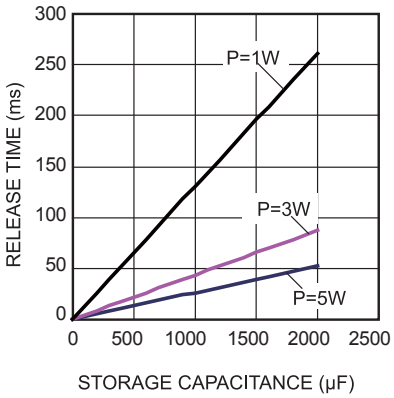
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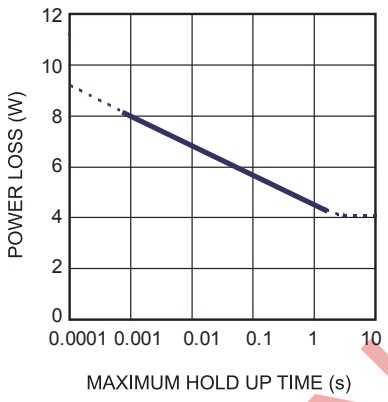
TYPICAL CHARACTERISTICS

V_{IN} = 12V, $V_{STORAGE}$ = 23V, $V_{RELEASE}$=10.2V, For DCDC Converter: P_{OUT}=5W, V_{OUT}=3.3V, T_A = +25ºC, unless otherwise noted.

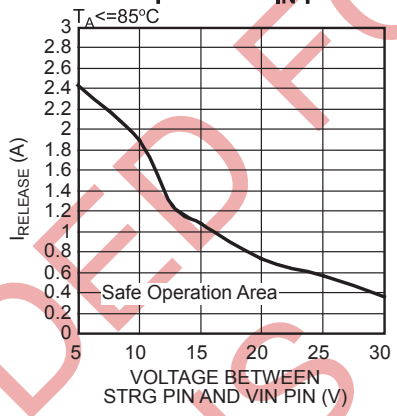
Release Time vs. Storage Capacitance



Thermal Performance



$I_{RELEASE}$ vs. Voltage between STRG pin and V_{IN} pin



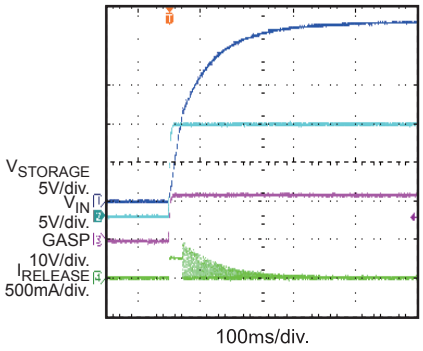
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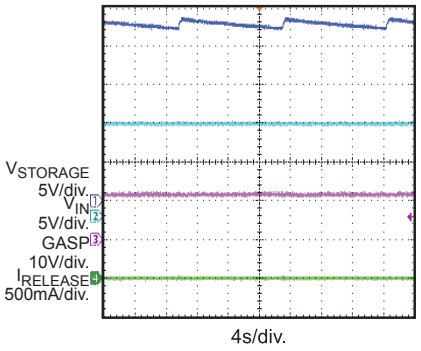
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, $V_{STORAGE}$ = 23V, $V_{RELEASE}$=10.2V, For DCDC Converter: P_{OUT}=5W, V_{OUT}=3.3V, T_A = +25°C, unless otherwise noted.

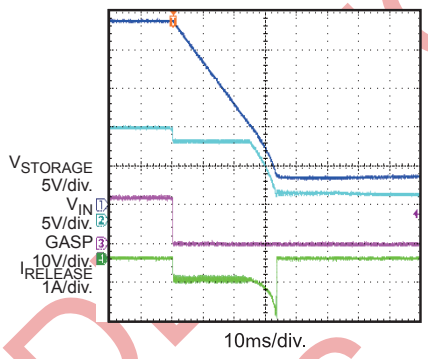
$V_{STORAGE}$ Charge Up



$V_{STORAGE}$ Refresh

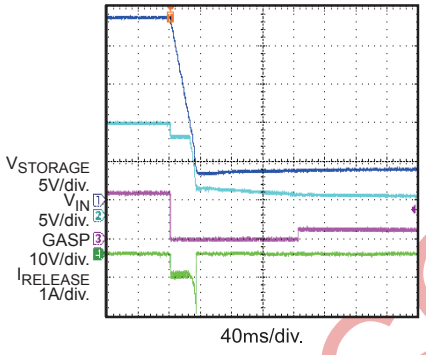


$V_{STORAGE}$ Release



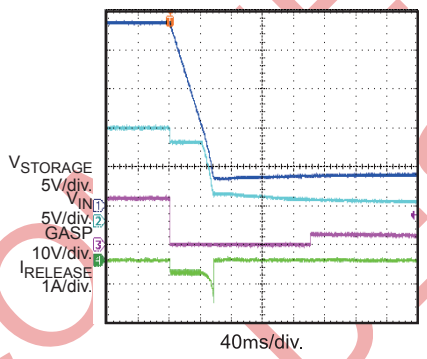
Release Time vs. Power

P_{OUT} = 5W



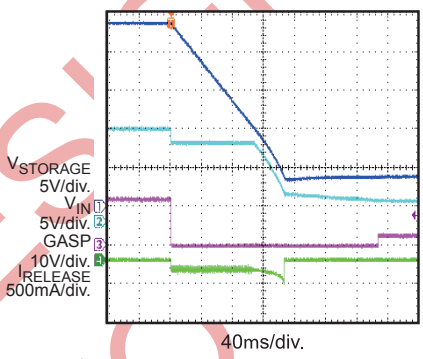
Release Time vs. Power

P_{OUT} = 3W



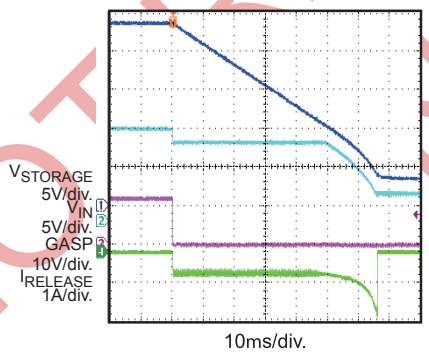
Release Time vs. Power

P_{OUT} = 1W



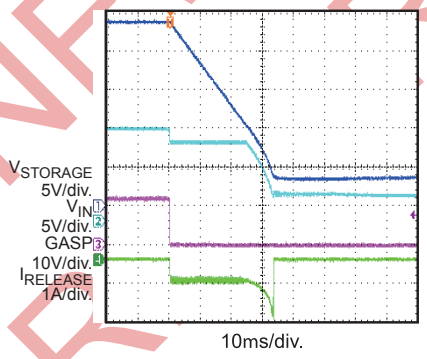
Release Time vs. Storage Cap

$C_{STORAGE}$ =2000µF



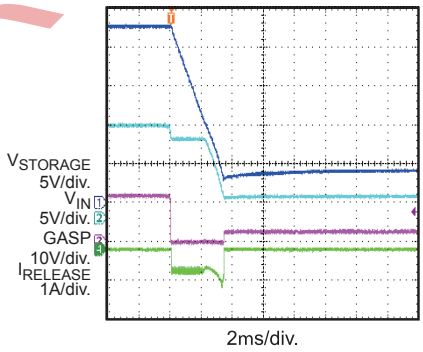
Release Time vs. Storage Cap

$C_{STORAGE}$ =1000µF



Release Time vs. Storage Cap

$C_{STORAGE}$ =100µF



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BLOCK DIAGRAM

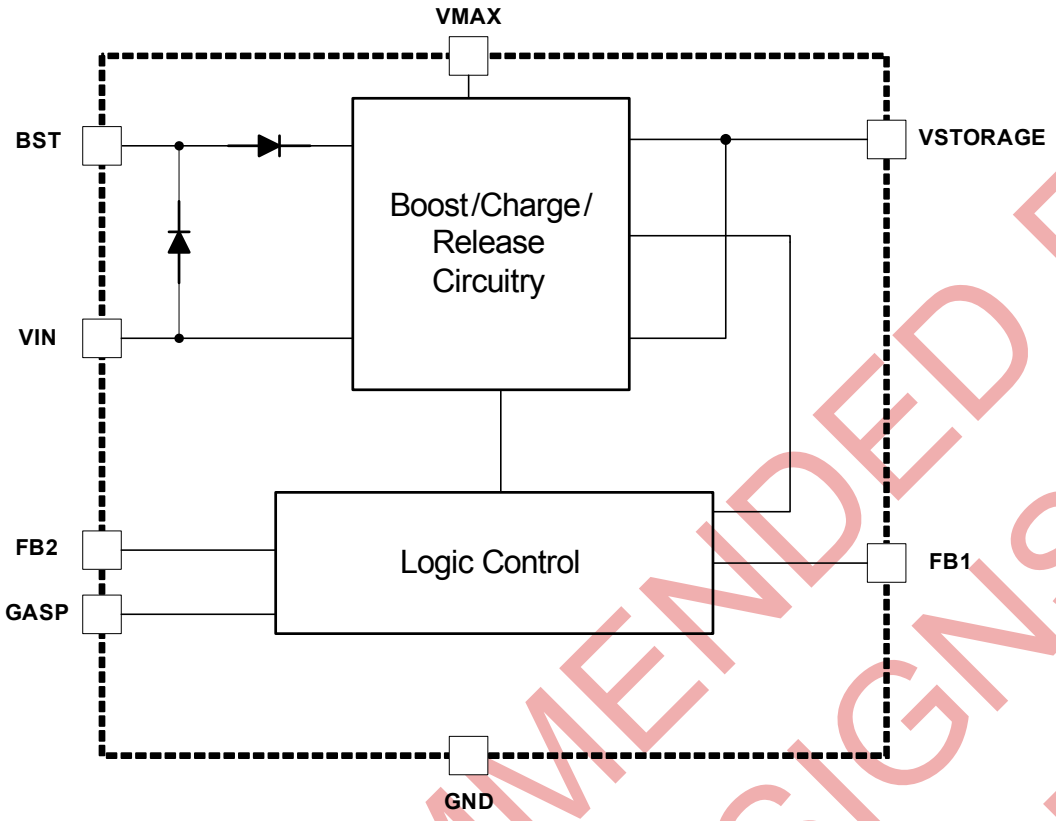


Figure 1 – Functional Block Diagram

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OPERATION

MP201 is a dying gasp storage and release control IC. It charges the storage capacitors from input supply during power start up and keeps refreshing the storage voltage at a regulated value during normal operation. MP201 continuously monitors the input voltage. Once the input voltage is lower than the programmed release voltage in the case of losing input power, it releases the charge from the storage capacitors to input, and keeps the input voltage regulated to the release voltage for as long as possible. It allows the system to respond to input power failure.

Start-Up

During the power start-up, there are two periods to charge the storage capacitors. In the first period, the MP201 pre-charges the large storage capacitors from 0 to nearly VIN with built-in inrush current limit. Once the storage voltage is close to the input voltage, the storage voltage is boosted and regulated at target voltage.

The BST pin of MP201 should connect to the DCDC switch node. Only after the DCDC is enabled, the MP201 will start boosting. Figure 2 shows the charging build-up process of MP201.

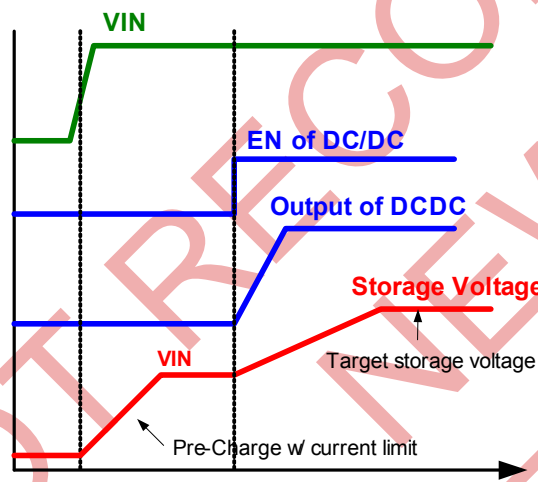


Figure 2 – Timing of Charging

Release

MP201 keeps monitoring the input voltage. Once the input voltage is lower than selected release voltage in the case of losing input power, MP201 moves the charge from high voltage storage capacitor to low input voltage capacitor. The release voltage can be determined by choosing appropriate input resistance divider. The maximum LDO release current can be as high as 2.5A. Until the storage capacitor voltage is near the input voltage, the input voltage loses its regulation and reduces further. A conceptual release process of MP201 is shown in Figure 3.

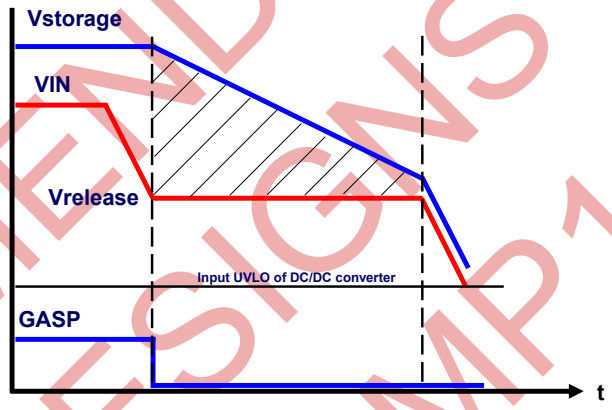


Figure 3 – Timing of Releasing

Gasp Indicator

When the FB2 voltage, feedback voltage for the input power, is higher than $1.05XV_{FB2}$, the GASP pin will be pulled high. Connect a resistor across VIN and GASP can drive GASP high. When the FB2 voltage is lower than $1.00XV_{FB2}$, the GASP voltage will be internally pulled low. GASP voltage can be used as a communication indicator signal which states input power availability.

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APPLICATION INFORMATION

SET STORAGE VOLTAGE

The storage voltage can be set by choosing appropriate external feedback resistors R1 and R2 which is shown in Figure 4.

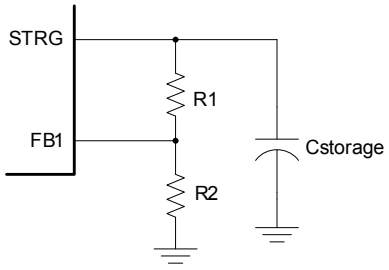


Figure 4 – Feedback Circuit for Storage Voltage

The storage voltage is determined by:

$$V_{STORAGE} = (1+\frac{R1}{R2}) \times V_{FB1}$$

Here is the example, if the storage voltage is set to be 20V, choose R2 to be 40kΩ, R1 will be then given by:

$$R1 = \frac{40k\Omega \times (20 - V_{FB2})}{V_{FB2}} = 760k\Omega$$

Table 1 lists the recommended resistors for different storage voltages.

Table 1 – Resistor Selection for Different Storage Voltages

$V_{STORAGE}$(V)	R1 (kΩ)	R2 (kΩ)
15	750	53.2
19	750	41.6
23	845	37.4

Select Release Voltage and Input Capacitors

The release voltage can be set by choosing external feedback resistors R3 and R4 which is shown in Figure 5.

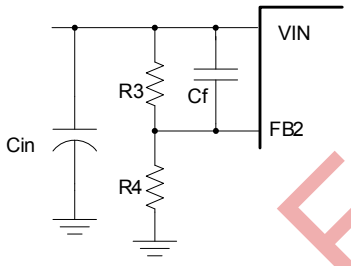


Figure 5 – Release Feedback Circuit

Similarly, the release voltage is set by:

$$V_{RELEASE} = (1+\frac{R3}{R4}) \times V_{FB2}$$

However, the selection of R3 and R4 not only determines the release voltage, but impacts the stability. Generally, choosing R3 to be 300~500kΩ is recommended for a stable performance with 47μF Cin. Table 2 lists the recommended resistors setup for different release voltages.

Table 2 – Resistor Selection for Different Release Voltages

$V_{RELEASE}$ (V)	R3 (kΩ)	R4 (kΩ)	Cf (pF)	C_{IN} (μF)
11	475	47.5	15	47
10.2	464	49.9	15	47
9.0	324	40.2	15	47

Select Storage Capacitor

The Storage Capacitor is for energy storage during normal operation and the energy will be released to VIN in case of losing input power. Typically, a general purpose electrolytic capacitor is recommended.

The voltage rating of storage capacitor needs to be higher than the targeted storage voltage. The voltage rating of storage capacitor can be fully utilized since the voltage on storage capacitor is very stable during normal operation. There will be less ripple current/voltage for most of the time during normal operation. The ripple current rating of storage cap can be less consideration.

The needed capacitance is dependent on how long the dying gasp time based on typically

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application. Assume the input release current is $I_{RELEASE}$ when input voltage is regulated at $V_{RELEASE}$ for the DCDC converter. The storage voltage of MP201 is $V_{STORAGE}$, and the required dying gasp time is T_{DASP}. The necessary storage capacitance can be calculated as following equation:

$$Cs = \frac{I_{RELEASE} \times T_{DASP}}{V_{STORAGE} - V_{RELEASE}}$$

If $I_{RELEASE}$=1A, T_D=20ms, $V_{STORAGE}$=20V, $V_{RELEASE}$=10V, the needed storage capacitance is 2000μF. Generally, the storage capacitance should be chosen a little bit large to avoid capacitance reduction at high voltage offset.

In typical xDSL applications using a 12V input supply, it is recommended to set the storage voltage higher than 20V to fully utilize the high voltage energy and minimize storage capacitance requirements. Generally, a 25V rated electrolytic capacitor can be used. The lifetime of electrolytic capacitors can be severely impacted by both environmental and electrical factors. One of the most critical electrical factors is the AC RMS ripple current through the capacitor which leads to increased capacitor core temperatures. Normally, for typical industrial uses, it is recommended to derate the capacitor voltage rating to 70%-80%. For example, a 25V rated electrolytic capacitor would be used for a 16V to 20V application.

However, since the MP201 tightly regulates the storage voltage, the storage capacitor almost has no AC ripple current going through it. The resulting refresh rate of the MP201 is very low which allows customers to safely use a 90% capacitor derating [8]. For example, a 25V electrolytic capacitor, can safely handle a storage voltage of up to 22V. Table 3 is some recommended storage electrolytic capacitors which can be used in typical xDSL application

PCB Layout Guide

PCB layout is very important to achieve stable operation. Please follow these guidelines and take the EVB board layout for references.

1) Connect the BST pin as close as possible to the SW node of DCDC converter through a resistor and a small ceramic capacitor. Try to avoid interconnect the feedback path.
2) Ensure all feedback connections are short and direct. Place the feedback resistors and compensation components as close to the chip as possible.
3) Keep the connection of the storage capacitors and STRG pin as short and wide as possible.

Table 3 – Recommended Storage Capacitors

Part #	Vender	Capacitance	Voltage	Operating Temp
25ME1500WX	Sanyo	1500μF	25V	-40 to +105°C
PEH526HAB4270M3	Kemet	2700μF	25V	-40 to +105°C
EEUFR1E152B	Panasonic	1500μF	25V	-40 to +105°C

Notes:

8) "Applying voltage does not affect the life time because the self heating by applying voltage can be ignored", from Sanyo.

Design Example

Below is a design example following the application guidelines for the specifications:

Table 4: Design Example

V_{IN}	12V to 18V
V_S	23V
$V_{RELEASE}$	10.2V

The detailed application schematic is shown in Figure 6. The typical performance and circuit waveforms have been shown in the Typical Performance Characteristics section. For more device applications, please refer to the related Evaluation Board Datasheets.

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TYPICAL APPLICATION CIRCUITS

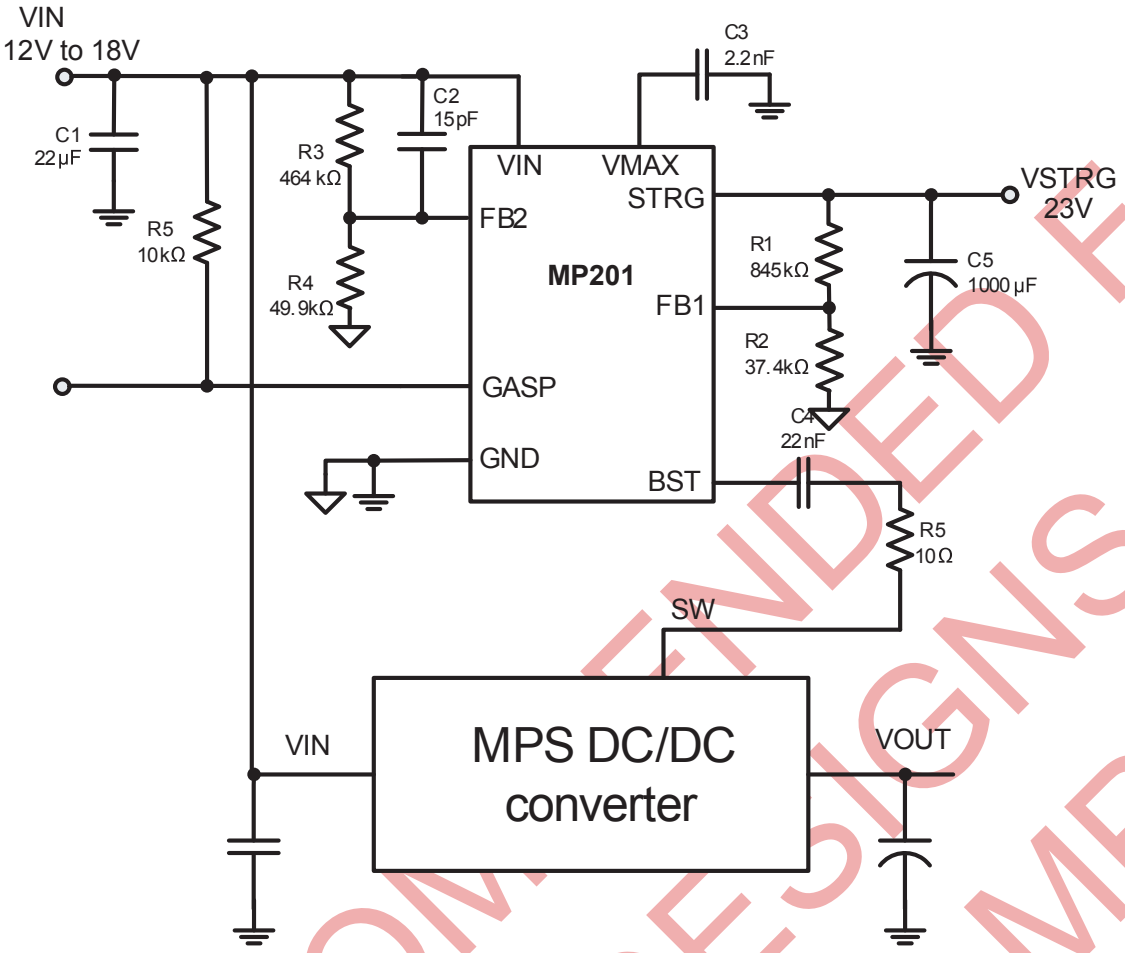


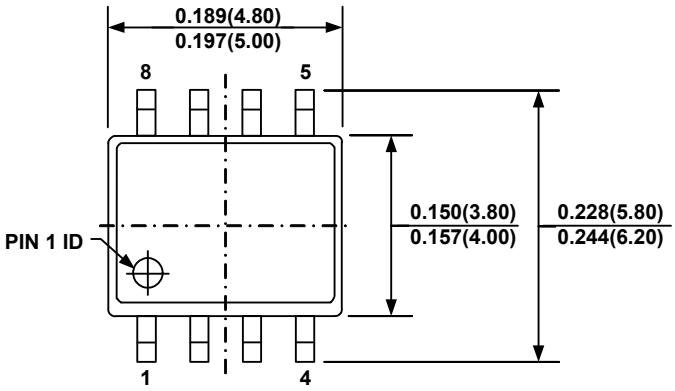
Figure 6 – MP201 Application Circuit

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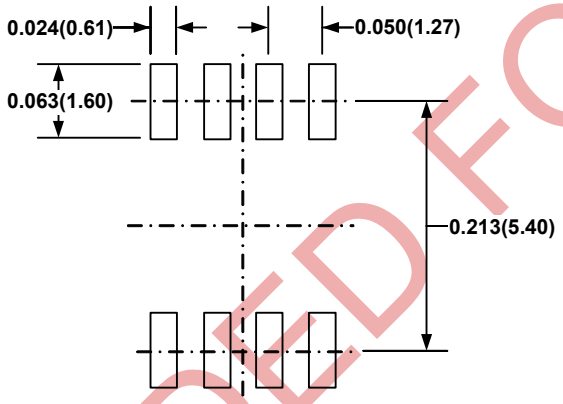
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PACKAGE INFORMATION

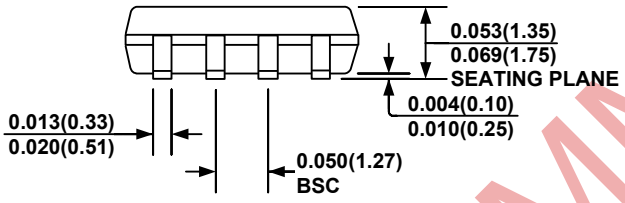
SOIC8



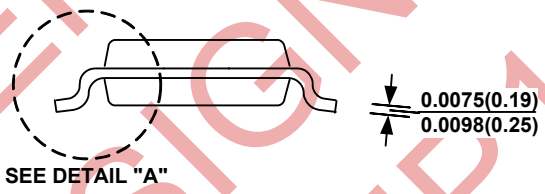
TOP VIEW



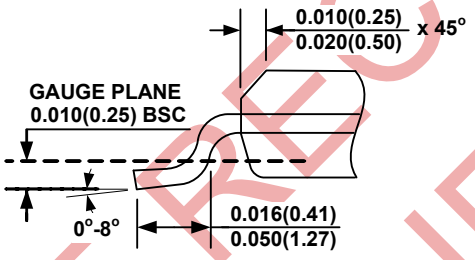
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW



DETAIL "A"

NOTE:

1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
5) DRAWING CONFORMS TO JEDEC MS-012, VARIATION AA.
6) DRAWING IS NOT TO SCALE.

NOT RECOMMENDED FOR NEW DESIGNS REFER TO MP111

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