MP2632

All-in-One, 3A Battery Charger with 3A Boost Current

DESCRIPTION

The MP2632 is a highly integrated, flexible, switch-mode battery charger with system power-path management and is designed for single-cell Li-ion or Li-polymer battery use in a wide range of applications.

The IC can operate in both charge mode and boost mode to allow for full system and battery power management.

The IC has an integrated IN-to-SYS pass-through path to pass the input voltage to the system. The pass-through path has built-in over-voltage and over-current protection and has a higher priority over the charging path.

When the input power is present, the device operates in charge mode. The MP2632 detects the battery voltage automatically and charges the battery in three phases: trickle current, constant current and constant voltage. Other features include charge termination and auto-recharge. The MP2632 also integrates both input current limit and input voltage regulation to manage input power and meet the priority of the system power demand.

In the absence of an input source, the IC switches to boost mode through PB to power SYS from the battery. In boost mode, OLIM programs the output current limit, and the IC turns off at light load automatically. The IC also uses output short-circuit protection to disconnect the battery from the load completely in the event of a short-circuit fault. The MP2632 resumes normal operation once the short-circuit fault is removed.

The 4-LED driver is integrated for voltage-based fuel gauge indication. Together with torch-light control, the MP2632 provides an all-in-one solution for power banks and similar applications without an external micro-controller.

The MP2632 is available in a 26-pin QFN (4mmx4mm) package.

FEATURES

- Up to 14V Sustainable Input Voltage
- 4.65V to 6V Operating Input Voltage Range
- Power Management Function, Integrated Input Current Limit, Input Voltage Regulation
- Up to 3A Programmable Charge Current
- Trickle-Charge Function
- Selectable 4.2V/4.35V/4.45V Charge Voltage with 0.5% Accuracy
- 4-LED Driver for Battery Fuel Gauge Indication
- Automatic Turn-Off at Light Load
- Input Source Detection
- Output Source Signaling
- Torch-Light Control
- Negative Temperature Coefficient Pin for Battery Temperature Monitoring
- Programmable Timer Back-Up Protection
- Thermal Regulation and Thermal Shutdown
- Internal Battery Reverse Leakage Blocking
- Integrated Over-Voltage Protection (OVP) and Over-Current Protection (OCP) for Pass-Through Path
- Reverse Boost Operation Mode for System Power
- Up to 3.0A Programmable Output Current Limit for Boost Mode
- Integrated Short-Circuit Protection (SCP) and Output Over-Voltage Protection for Boost Mode

APPLICATIONS

- Sub-Battery Applications
- Power-Bank Applications for Smart Phones
- Tablets and Other Portable Devices

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Analog Digital Adaptive Modulation (ADAM) is a trademark of Monolithic Power Systems, Inc.

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TYPICAL APPLICATION

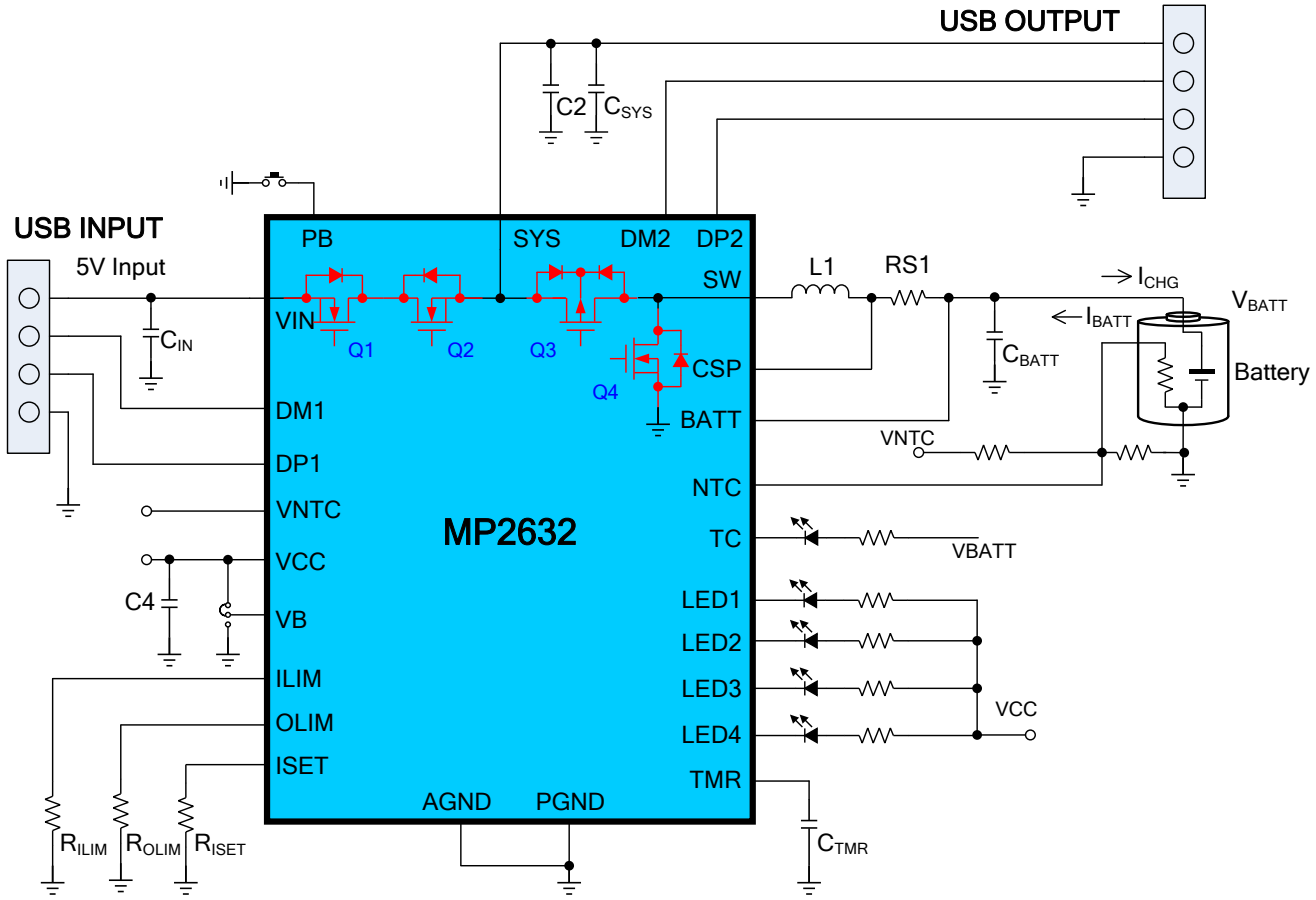


Table 1: Operation Mode Control

V_{IN} (V)	PB	Operation Mode	Q1, Q2	Q3	Q4
V_{BATT} + 300mV < V_{IN} < 6V	X	Charging	On	SW	SW
V_{IN} < V_{BATT} + 300mV	From H to L for >1.5ms	Discharging (boost)	Off	SW	SW
V_{IN} > 6V	X	OVP	Off	Off	Off
V_{IN} < 2V	H or L	Sleep	Off	Off	Off

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ORDERING INFORMATION

Part Number*	Package	Top Marking
MP2632GR	QFN-26 (4mmx4mm)	*See Below*

* For Tape & Reel, add suffix –Z (e.g. MP2632GR–Z)

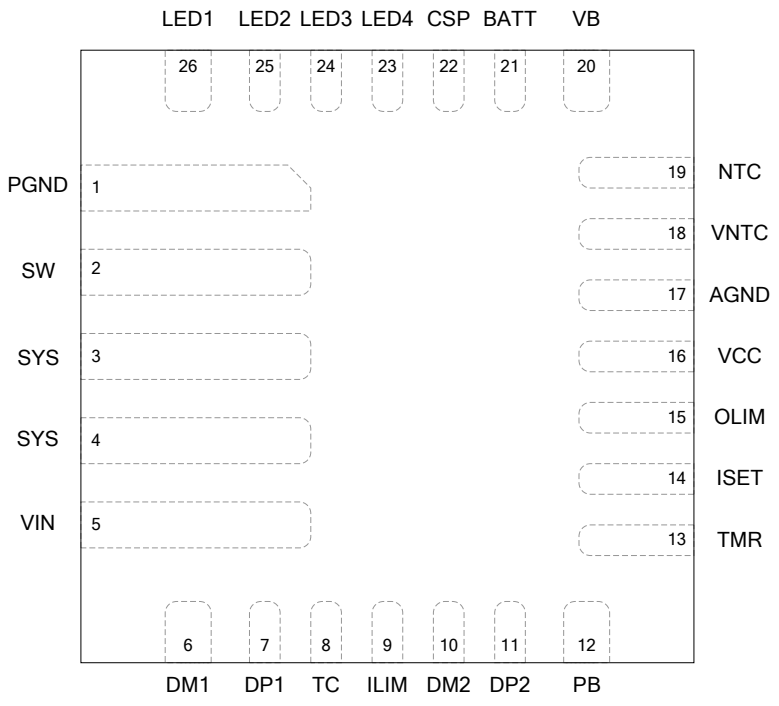
TOP MARKING

MPSYWW
MP2632
LLLLLL

MPS: MPS prefix
Y: Year code
WW: Week code
MP2632: Product code of MP2632GR
LLLLLL: Lot number

PACKAGE REFERENCE

TOP VIEW



QFN-26 (4mmx4mm)

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ABSOLUTE MAXIMUM RATINGS (1)

VIN to PGND ..... -0.3V to +14V
SYS to PGND ..... -0.3V to +6.5V
SW to PGND .....-0.3V (-2V for 20ns) to +6.5V
BATT to PGND……..... -0.3V to +6.5V
All other pins to AGND..... -0.3V to +6.5V
Continuous power dissipation (T_A = +25°C) (2) 2.84W
Junction temperature .....150°C
Lead temperature (solder) .....260°C
Storage temperature….. .....-65°C to +150°C

Recommended Operating Conditions (3)

Supply voltage (V_{IN}) ..... 4.65V to +6V
I_{IN} ..... Up to 3A
I_{SYS} ..... Up to 3A
I_{CHG} ..... Up to 3A
V_{BATT} ..... Up to 4.45V
Operating junction temp. (T_J) ... -40°C to +125°C

Thermal Resistance (4) θ_{JA} θ_{JC}

QFN-26 (4mmx4mm).....44 ..... 9 .... °C/W

NOTES:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

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ELECTRICAL CHARACTERISTICS

V_{IN} = 5.0V, RS1 = 10mΩ, T_A = +25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
IN-to-SYS NMOS on resistance	$R_{IN\ to\ SYS}$	VCC = 5V	49	55	62	mΩ
High-side PMOS on resistance	R_{H_DS}	VCC = 5V	20	26	31	mΩ
Low-side NMOS on resistance	R_{L_DS}	VCC = 5V	20	26	31	mΩ
High-side PMOS peak current limit	I_{PEAK_HS}	CC charge mode/boost mode	5.7	7	8.4	A
		TC charge mode	1.9	2.3	2.8	A
Low-side NMOS peak current limit	I_{PEAK_LS}		6.4	8	9.6	A
Switching frequency	F_{sw}		500	600	800	kHz
VCC UVLO	$V_{CC\ UVLO}$		1.96	2.16	2.36	V
VCC UVLO hysteresis				100		mV
Charge Mode						
Input quiescent current	I_{Q_IN}	Charge mode, I_{SYS} = 0, battery float		1.8	2.5	mA
Input current limit for DCP	I_{IN_LIMIT}	R_{ILIM} = 88.7k	380	435	490	mA
		R_{ILIM} = 49.9k	740	820	900	
		R_{ILIM} = 14.7k	2580	2840	3100	
Input current limit for SDP	I_{USB}	SDP is detected using DP1/DM1 detection	400	450	500	mA
Input over-voltage protection	$V_{IN\ OVP}$	V_{IN} rising	5.8	6.0	6.2	V
$V_{IN\ OVP}$ hysteresis		V_{IN} falling		250		mV
Input under-voltage lockout	V_{IN_UVLO}	V_{IN} rising	3.3	3.45	3.6	V
V_{UVLO} hysteresis		V_{IN} falling		155		mV
Input over-current threshold	$I_{IN\ OCP}$			5		A
Input over-current blanking time(5)	$T_{INOCBLK}$			200		µs
Input over-current recover time(5)	$T_{INRECVR}$			150		ms
Terminal battery voltage	V_{BATT_FULL}	Connect VB to GND	4.328	4.35	4.372	V
		Leave VB floating	4.179	4.2	4.221	
		Connect VB to VCC	4.428	4.45	4.472	
Recharge threshold	V_{RECH}	Connect to VB to GND	4.1	4.16	4.22	V
		Leave VB floating	3.95	4.02	4.08	
		Connect VB to VCC	4.19	4.26	4.32	
Trickle charge voltage threshold	V_{BATT_TC}	Connect VB to GND	3	3.07	3.13	V
		Leave VB floating	2.9	2.96	3.02	
		Connect VB to VCC	3.07	3.14	3.2	

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ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 5.0V, RS1 = 10mΩ, T_A = +25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Trickle charge hysteresis				220		mV
Battery over-voltage threshold	V_{BOVP}	As a percentage of V_{BATT_FULL}	101.5%	103.5%	105.5%	V_{BATT_FULL}
Constant charge (CC) current	I_{CC}	RS1 = 10mΩ, R_{ISET} = 150k	900	1000	1100	mA
		RS1 = 10mΩ, R_{ISET} = 75k	1800	2000	2200	
		RS1 = 10mΩ, R_{ISET} = 49.9k	2700	3000	3300	
Trickle charge current	I_{TC}		90	280	400	mA
Termination charge current	I_{BF}	RS1 = 10mΩ	90	200	300	mA
Input voltage regulation reference	V_{REG}		4.55	4.65	4.75	V
Boost Mode						
SYS voltage range		I_{SYS} = 100mA	5	5.1	5.2	V
Boost SYS over-voltage protection threshold	$V_{SYS(OVP)}$)	Threshold over V_{SYS} to turn off the converter during boost mode	5.6	5.8	6	V
SYS over-voltage protection threshold hysteresis		V_{SYS} falling from $V_{SYS(OVP)}$		330		mV
Boost quiescent current	I_{Q_BOOST}	I_{SYS} = 0, boost mode, in test mode with auto-off disabled			1.65	mA
Programmable boost output current-limit accuracy	I_{OLIM}	RS1 = 10mΩ, R_{OLIM} = 150k	0.9	1	1.1	A
		RS1 = 10mΩ, R_{OLIM} = 60.4k	2.34	2.5	2.66	
		RS1 = 10mΩ, R_{OLIM} = 49.9k	2.8	3	3.2	
SYS over-current blanking time[5]	$T_{SYSOCBLK}$			150		µs
SYS over-current recover time[5]	$T_{SYSRECVR}$			1.5		ms
System load to turn off boost	I_{NOLOAD}	Battery current in boost mode	50	85	120	mA
Light-load blanking time[5]				16		s
Weak battery threshold	V_{BAT_UVLO}	During boost		2.5	2.6	V
		Before boost starts		2.9	3.05	V
Sleep Mode						
Battery leakage current	$I_{LEAKAGE}$	V_{BATT} = 4.2V, SYS float, V_{IN} = 0V, not in boost mode		13	16	µA

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ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 5.0V, RS1 = 10mΩ, T_A = +25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Indication and Logic						
LED1, LED2, LED3, and LED4 output low voltage		Sinking 5mA			200	mV
TC output low voltage		Sinking 100mA			550	mV
LED1, LED2, LED3, LED4, TC leakage current		Connected to 5V			0.2	μA
INOVP, BOVP and NTC, fault blinking frequency(5)				1		Hz
PB input logic low voltage					0.4	V
PB input logic high voltage			1.4			V
Protection						
Trickle charge time		C_{TMR} = 0.1μF, remains in TC mode, I_{TC} = 250mA		16		Min
Total charge time		C_{TMR} = 0.1μF, I_{CHG} = 1A		390		Min
NTC low temp, rising threshold		R_{NTC} = NCP18XH103 (0°C)	65.2%	66.2%	67.2%	V_{SYS}
NTC low temp, rising threshold hysteresis				2.4%		
NTC high temp, rising threshold		R_{NTC} = NCP18XH103 (50°C)	34.7%	35.7%	36.7%	
NTC high temp, rising threshold hysteresis				2%		
Charging current foldback threshold(5)		Charge mode		120		°C
Thermal shutdown threshold(5)				150		°C
Input DP1/DM1 USB Detection						
DP1 voltage source	V_{DP_SRC}		0.5	0.6	0.7	V
Data connect detect current source	I_{DP_SRC}		7		13	μA
DM1 sink current	I_{DM_SINK}		50	100	150	μA
Leakage current input DP1/DM1	I_{DP_LKG}		-1		1	MA
	I_{DM_LKG}		-1		1	MA
Data detect voltage	V_{DAT_REF}		0.25		0.4	V
Logic low (logic threshold)	V_{LGC_LOW}				0.8	V
DM pull-down resistor				19		KΩ
Logic I/O Characteristics						
Low-logic voltage threshold	V_L				0.4	V
High-logic voltage threshold	V_H		1.3			V

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ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 5.0V, RS1 = 10mΩ, T_A = +25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Output DP2/DM2 USB Signaling						
BC1.2 DCP Mode						
DP2 and DM2 short resistance		V_{DP} = 0.8V, I_{DM} = 1mA		158	200	Ω
BC1.2 SDP Mode						
DP2 pull-down resistance			11	15	19	kΩ
DM2 pull-down resistance			11	15	19	kΩ
Divider Mode						
DP2 output voltage		V_{OUT} = 5V	2.6	2.7	2.8	V
DM2 output voltage		V_{OUT} = 5V	2.6	2.7	2.8	V
DP2/DM2 output impedance			26	31	36	kΩ
1.2V/1.2V Mode						
DP2/DM2 output voltage		V_{OUT} = 5V	1.21	1.26	1.31	V
DP2/DM2 output impedance			60	78	90	kΩ
Voltage-Based Fuel Gauge (V_{OREG} = 4.2V, Charge Mode)						
First level of battery voltage threshold			3.52	3.6	3.69	V
Hysteresis				500		mV
Second level of battery voltage threshold			3.7	3.8	3.91	V
Hysteresis				500		mV
Third level of battery voltage threshold			3.92	4.0	4.11	V
Hysteresis				500		mV
Voltage-Based Fuel Gauge (V_{OREG} = 4.2V, Discharge Mode)						
First level of battery voltage threshold			3.4	3.47	3.54	V
Hysteresis				500		mV
Second level of battery voltage threshold			3.55	3.62	3.69	V
Hysteresis				500		mV
Third level of battery voltage threshold			3.7	3.77	3.84	V
Hysteresis				500		mV
Fourth level of battery voltage threshold			3.85	3.92	3.99	V
Hysteresis				500		mV

NOTE:

5) Guaranteed by design.

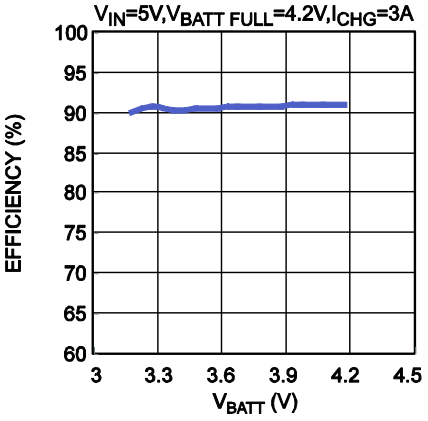
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TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 5V, C_{IN} = C_{BATT} = C_{SYS} = C2 = 22µF, L1 = 2.2µH, RS1 = 10mΩ, C4 = C_{TMR} = 0.1µF, battery simulator, unless otherwise noted.

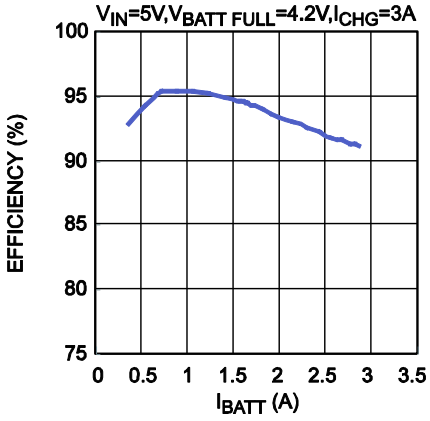
Constant Current Charge Efficiency

V_{IN}=5V,$V_{BATT\ FULL}$=4.2V,I_{CHG}=3A



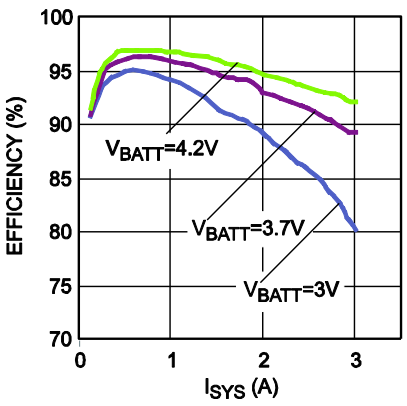
Constant Voltage Charge Efficiency

V_{IN}=5V,$V_{BATT\ FULL}$=4.2V,I_{CHG}=3A



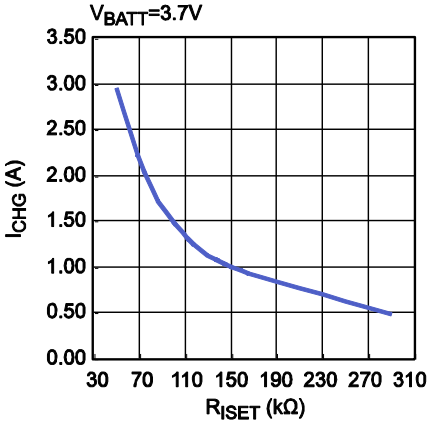
Boost Efficiency

R_{OLIM}=0

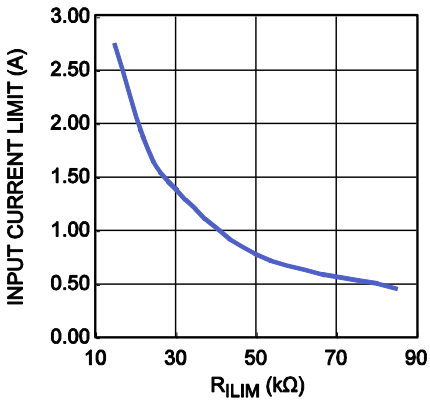


Programmble Charge Current, Charge Mode

V_{BATT}=3.7V

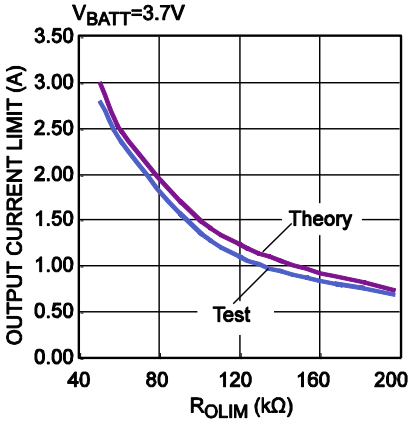


Programmble Input Current Limit, Charge Mode



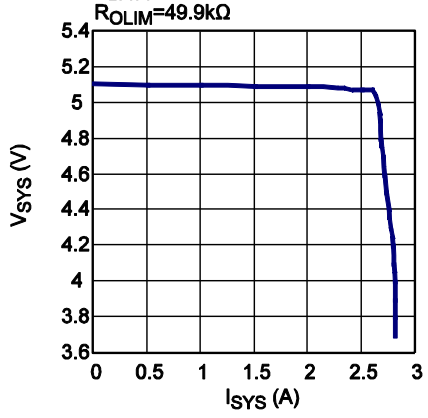
Programmble Output Current Limit, Boost Mode

V_{BATT}=3.7V



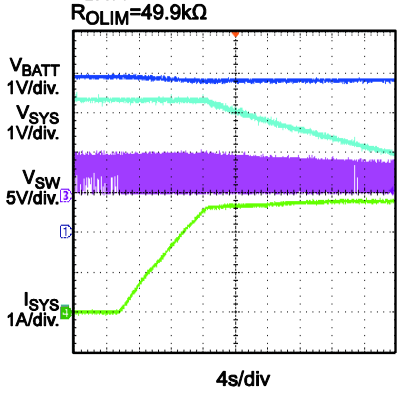
Boost Output U-I

V_{BATT}=3.7V, Ramp up ISYS, R_{OLIM}=49.9kΩ



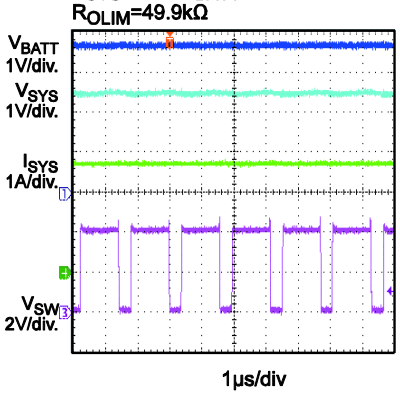
Boost Mode CC Function

V_{BATT}=3.7V, Ramp up ISYS, R_{OLIM}=49.9kΩ



Boost Mode CC Operation

V_{SYS}=4.5V,V_{BATT}=3.7V, ISYS=3A, R_{OLIM}=49.9kΩ



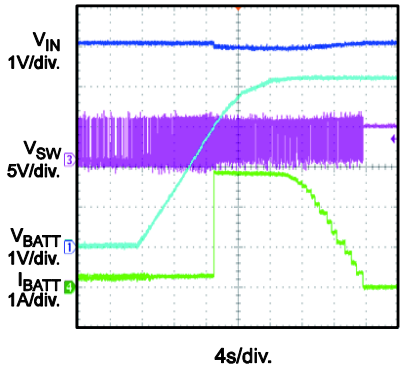
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TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

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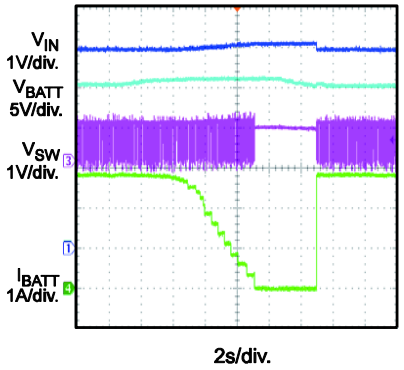
Battery Charge Curve

V_{BATT_FULL}=4.2V, I_{SYS}=0A, I_{CHG}=3.0A



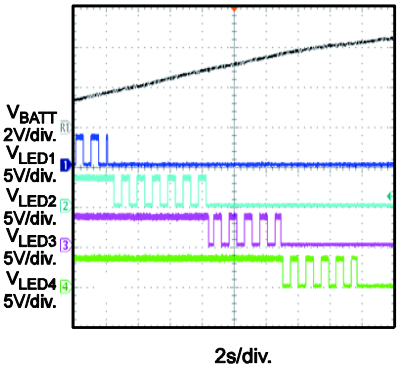
Auto-Recharge

V_{BATT_FULL}=4.2V, I_{SYS}=0A, I_{CHG}=3.0A



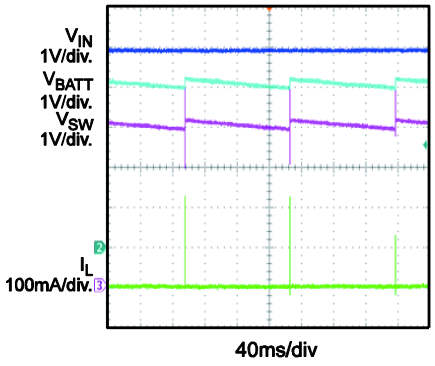
Indication during Charging

V_{BATT_FULL}=4.2V, I_{SYS}=0A, I_{CHG}=3.0A



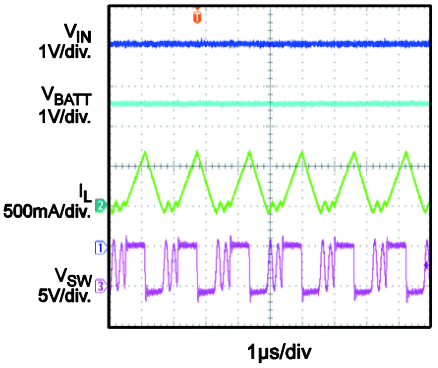
BATT Float Steady State

V_{BATT_FULL}=4.2V, I_{SYS}=0A



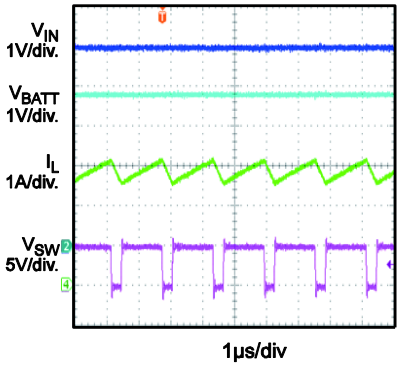
TC Charge Steady State

V_{BATT_FULL}=4.2V, I_{SYS}=0A,
V_{BATT} =2.6V



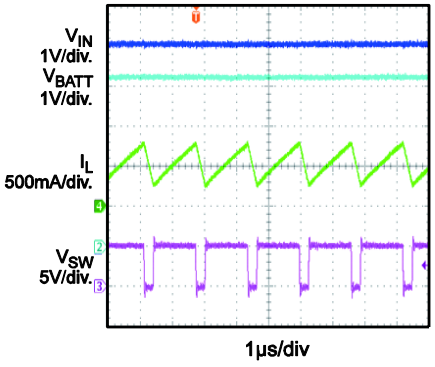
CC Charge Steady State

V_{BATT_FULL}=4.2V, I_{SYS}=0A,
V_{BATT} =3.7V



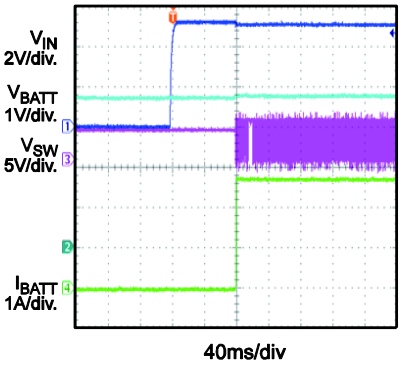
CV Charge Steady State

V_{BATT_FULL}=4.2V, I_{SYS}=0A,
V_{BATT} =4.2V



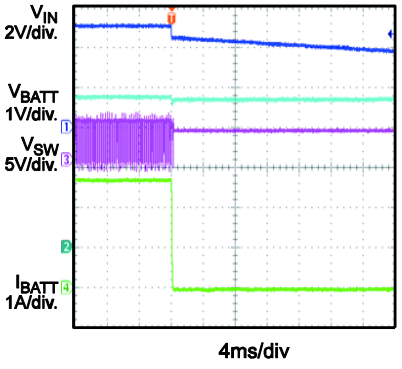
Power On, Charge Mode

V_{BATT_FULL}=4.2V, I_{SYS}=0A,
V_{BATT} =3.7V



Power Off, Charge Mode

V_{BATT_FULL}=4.2V, I_{SYS}=0A,
V_{BATT} =3.7V



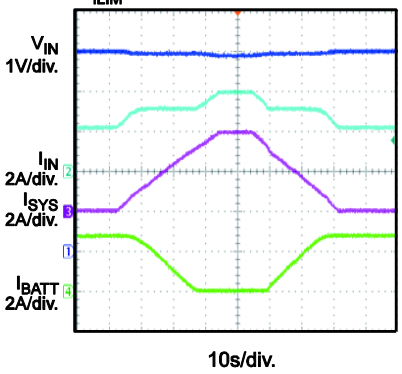
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TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, C_{IN} = C_{BATT} = C_{SYS} = C2 = 22µF, L1 = 2.2µH, RS1 = 10mΩ, C4 = C_{TMR} = 0.1µF, battery simulator, unless otherwise noted.

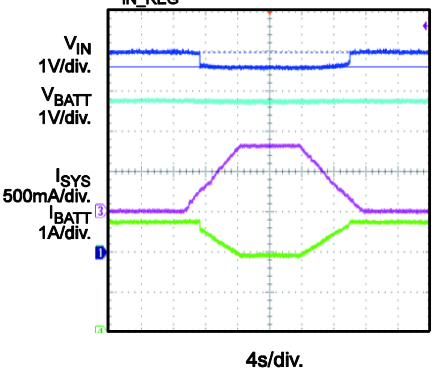
Input Current Limit

V_{BATT_FULL}=4.2V, V_{BATT} =3.7V, R_{ILIM}=14.7kΩ



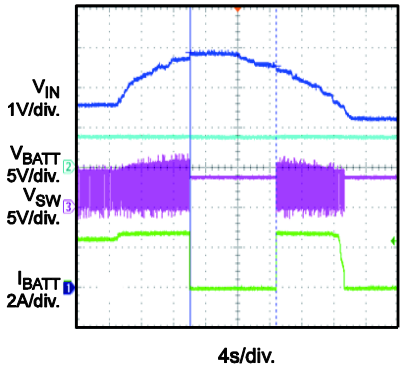
Input Voltage Regulation

V_{BATT_FULL}=4.2V, V_{BATT} =3.7V, V_{IN_REG}=4.65V



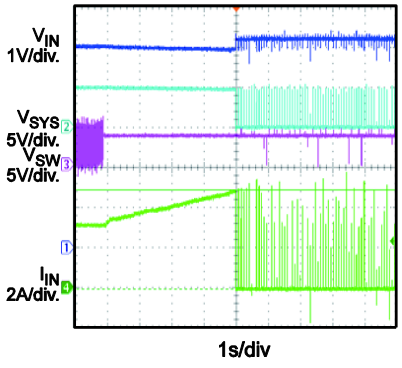
Input Over-Voltage Protection

V_{IN}=5V to 6V, V_{BATT} =3.7V



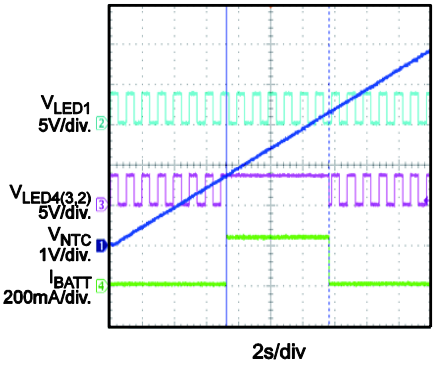
Input Over-Current Protection

V_{IN}=5V, Ramp up I_{SYS} to 4.2A, V_{BATT}=3.7V



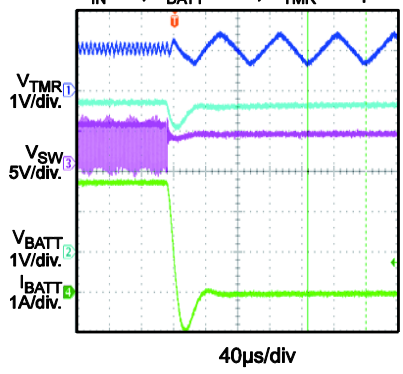
NTC Protection, Charge Mode

V_{IN}=5V, V_{BATT}=2.6V



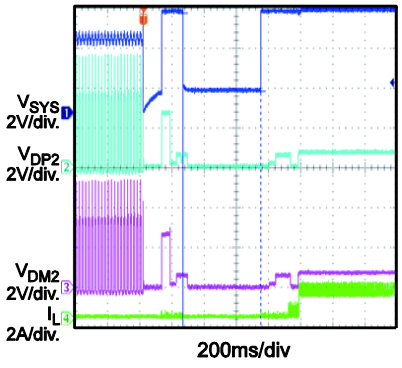
Timer Out Protection, Charge Mode

V_{IN}=5V, V_{BATT}=3.7V, C_{TMR}=150pF



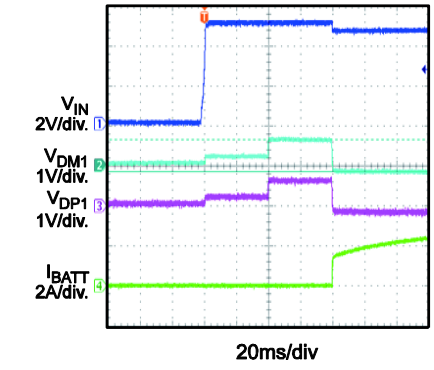
Boost Automatic On, Phone Insertion

V_{BATT} =4V



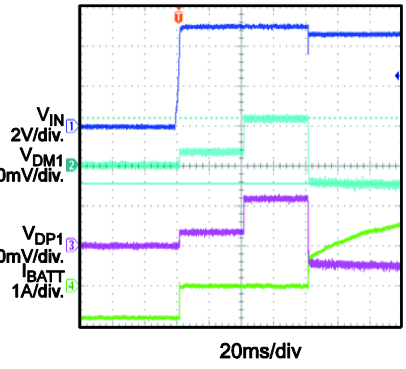
Input Adapter Insertion, No Load Connection

V_{BATT}=3.7V, R_{ILIMT}=14.7kΩ, R_{ISET}=49.9kΩ



Input Adapter Insertion, Phone Connected

V_{BATT}=3.7V, R_{ILIMT}=14.7kΩ, R_{ISET}=49.9kΩ



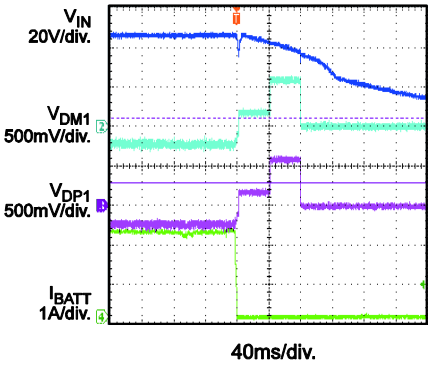
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TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, C_{IN} = C_{BATT} = C_{SYS} = C2 = 22µF, L1 = 2.2µH, RS1 = 10mΩ, C4 = C_{TMR} = 0.1µF, battery simulator, unless otherwise noted.

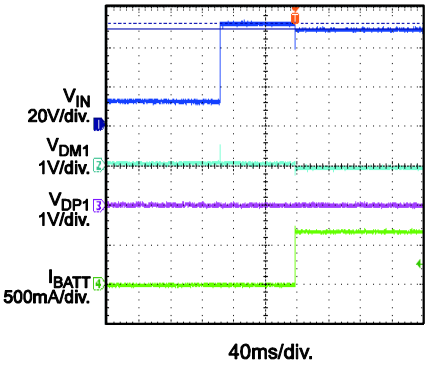
Input Adapter Removal, Phone Connected

V_{BATT}=3.7V, R_{ILIMT}=14.7k, R_{ISET}=49.9k



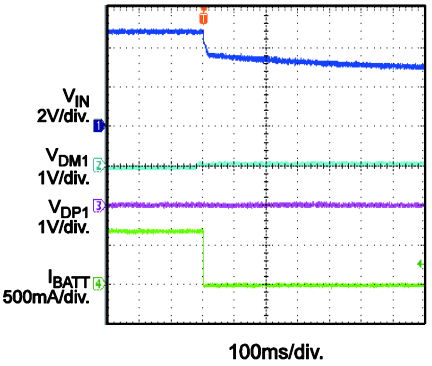
USB Insertion, No Load Connection

V_{BATT}=3.7V, R_{ILIMT}=14.7k, R_{ISET}=49.9k



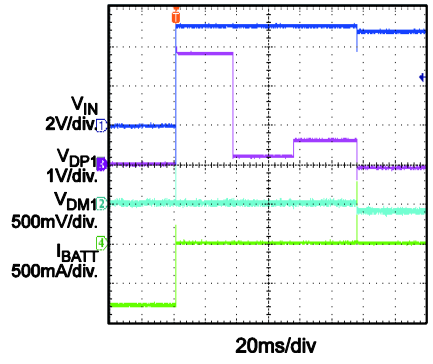
USB Removal, No Load Connection

V_{BATT}=3.7V, R_{ILIMT}=14.7k, R_{ISET}=49.9k



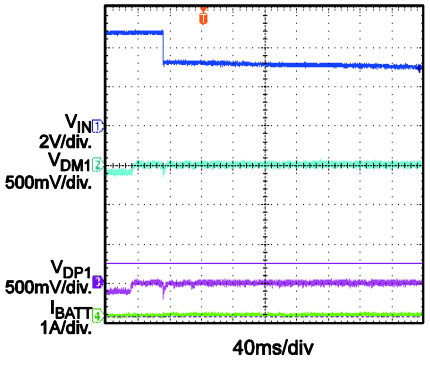
USB Insertion, Phone Connected

V_{BATT}=3.7V, R_{ILIMT}=14.7k, R_{ISET}=49.9k



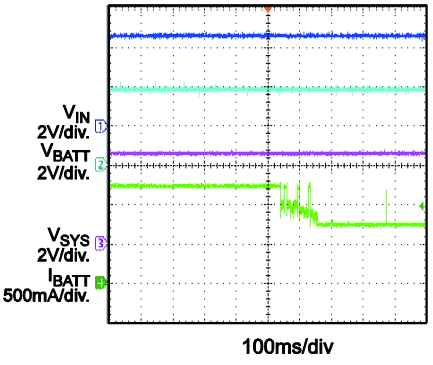
USB Removal, Phone Connected

V_{BATT}=3.7V, R_{ILIMT}=14.7k, R_{ISET}=49.9k



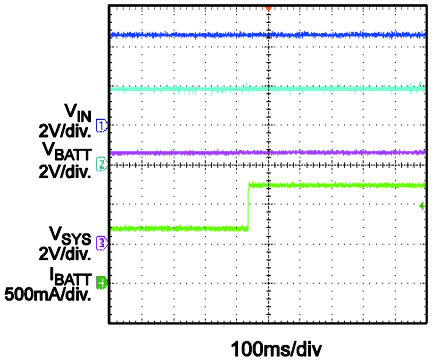
Phone Connected, Charging from Adapter

V_{BATT}=3.7V, R_{ILIMT}=14.7k, R_{ISET}=49.9k



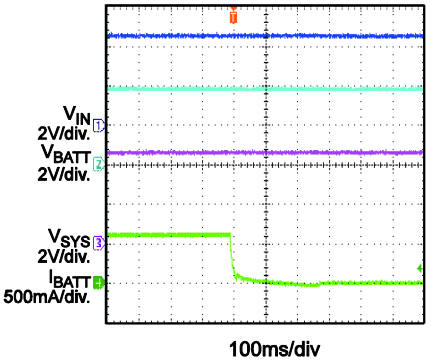
Phone Removed, Charging from Adapter

V_{BATT}=3.7V, R_{ILIMT}=14.7k, R_{ISET}=49.9k



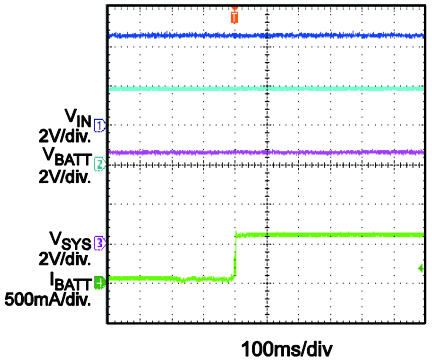
Phone Connected, Charging from USB

V_{BATT}=3.7V, R_{ILIMT}=14.7k, R_{ISET}=49.9k



Phone Removed, Charging from USB

V_{BATT}=3.7V, R_{ILIMT}=14.7k, R_{ISET}=49.9k

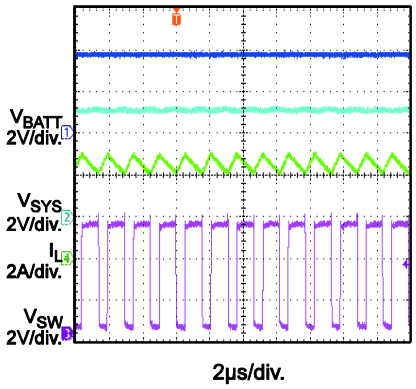


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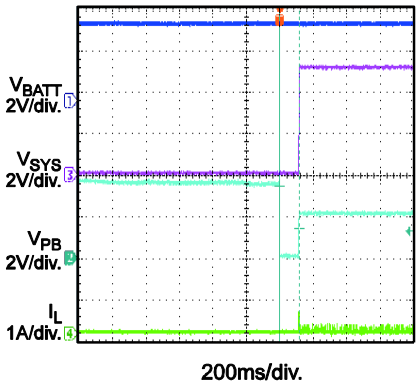
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, C_{IN} = C_{BATT} = C_{SYS} = C2 = 22µF, L1 = 2.2µH, RS1 = 10mΩ, C4 = C_{TMR} = 0.1µF, battery simulator, unless otherwise noted.

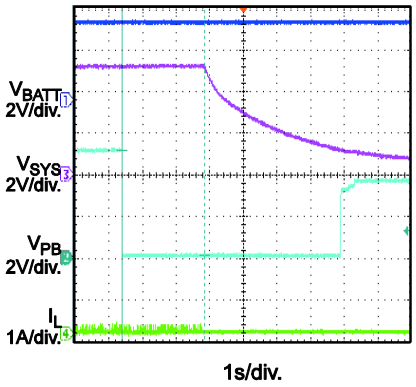
Boost Mode Steady State
V_{BATT}=3.7V, I_{SYS}=3A



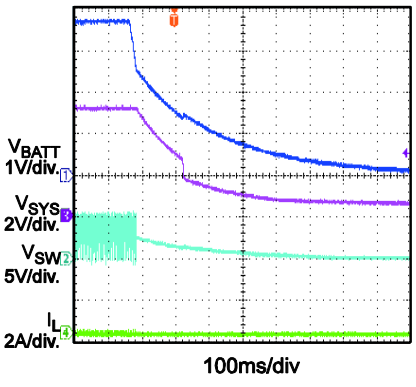
Power On by PB, Boost Mode
V_{BATT}=3.7V, I_{SYS}=0A



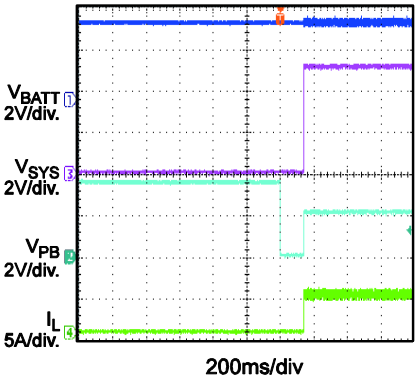
Power Off by PB, Boost Mode
V_{BATT}=3.7V, I_{SYS}=0A



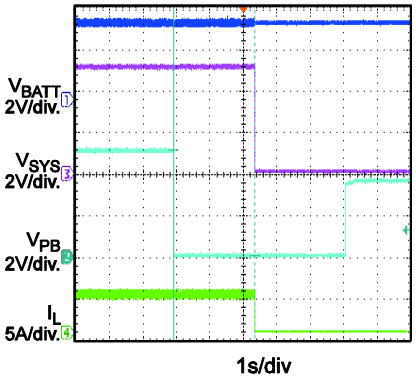
Power Off by Battery Removal, Boost Mode
V_{BATT}=3.7V, I_{SYS}=0A



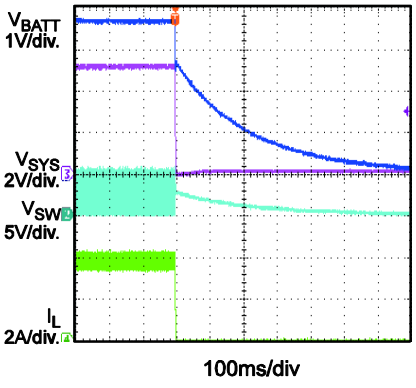
Power On by PB, Boost Mode
V_{BATT}=3.7V, I_{SYS}=3A



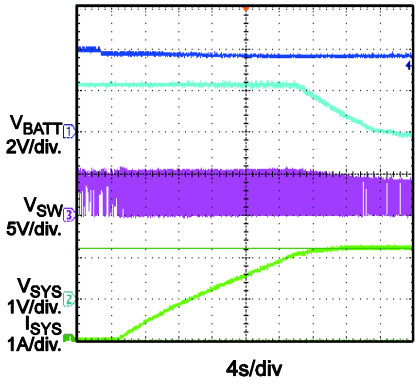
Power Off by PB, Boost Mode
V_{BATT}=3.7V, I_{SYS}=3A



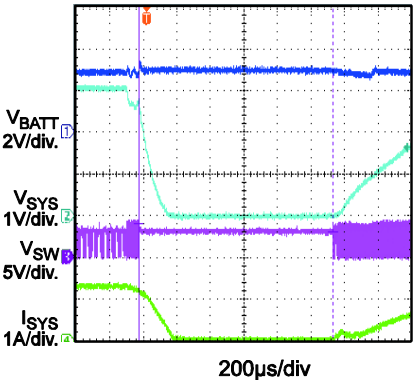
Power Off by Battery Removal, Boost Mode
V_{BATT}=3.7V, I_{SYS}=2.5A



SYS Output Current Limit, Boost Mode
V_{BATT}=3.7V, R_{OLIM}=60.4kΩ



Auto Restart after SYS OCP, Boost Mode
V_{BATT}=3.0V, R_{OLIM}=100kΩ

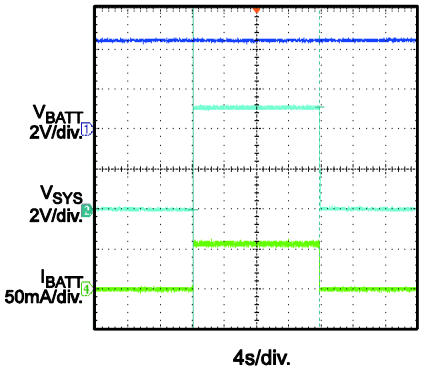


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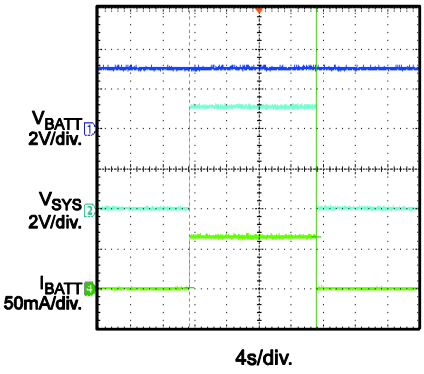
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, C_{IN} = C_{BATT} = C_{SYS} = C2 = 22µF, L1 = 2.2µH, RS1 = 10mΩ, C4 = C_{TMR} = 0.1µF, battery simulator, unless otherwise noted.

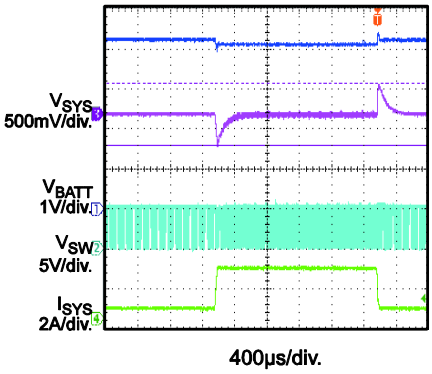
Light-Load Off Test
V_{BATT}=4.5V, I_{BATT}=55mA



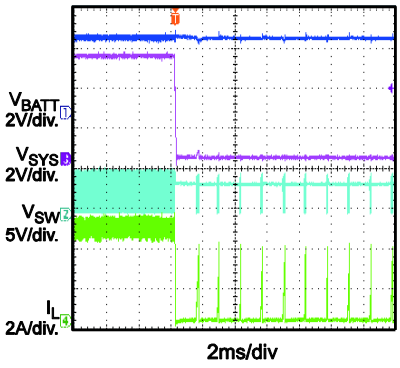
Light-Load Off Test
V_{BATT}=3.0V, I_{BATT}=65mA



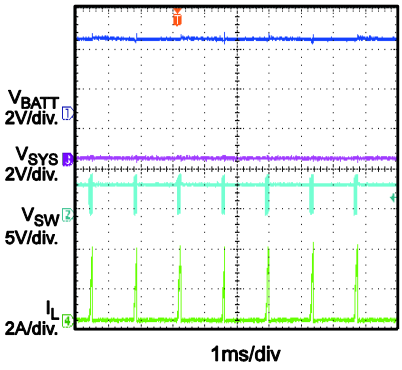
Load Transient
V_{BATT}=4.2V, I_{SYS}=0.5A-2.5A



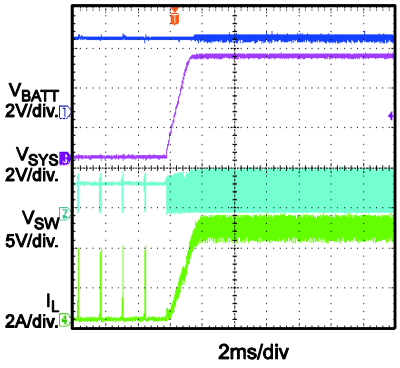
SYS Short-Circuit Entry
V_{BATT}=3.7V, I_{SYS}=3A



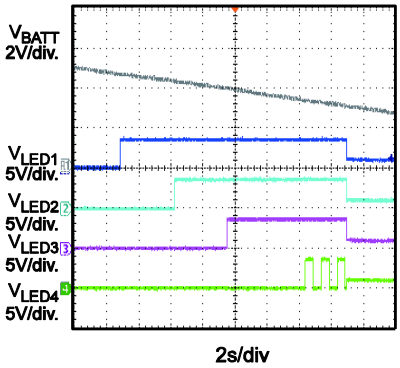
SYS Short Steady
V_{BATT}=3.7V, I_{SYS}=3A



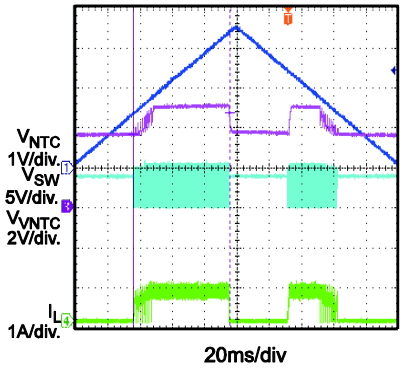
SYS Short-Circuit Recovery
V_{BATT}=3.7V, I_{SYS}=3A



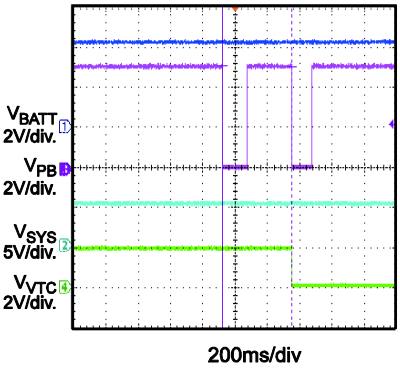
LED Indication during Discharging
V_{BATT} ramping down, I_{SYS}=3A



NTC Protection, Boost Mode
V_{BATT}=3.7V, I_{SYS}=1A



Torch Light
V_{BATT}=4.2V



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PIN FUNCTIONS

P/N	Name	I/O	Description
1	PGND	Power	**Power ground.**
2	SW	Power	**Switch output node.** It is not recommended to place vias on the SW plane during PCB layout.
3, 4	SYS	Power	**System output.** Place a ceramic capacitor of at least 22µF as close to SYS and PGND as possible. The total capacitance should not be lower than 44µF.
5	VIN	Power	**Adapter input.** Place a bypass capacitor close to VIN to prevent large input voltage spikes.
6	DM1	I	**Negative line of the input USB data line pair.** DM1 together with DP1 achieves the USB host. DM1 has automatic charging port detection.
7	DP1	I	**Positive line of the input USB data line pair.** DP1 together with DM1 achieves the USB host. DP1 has automatic charging port detection.
8	TC	O	**Torch control output.** TC is the open-drain structure. The internal driver MOSFET is on when PB is pulled low for more than 1.5ms twice within one second.
9	ILIM	I	**Input current setting.** Connect ILIM to GND with an external resistor to program an input current limit in charge mode when a dedicated charger is detected.
10	DM2	O	**Negative line of the output USB data line pair.** DM2 together with DP2 automatically provides the correct voltage signal for attached portable equipment to perform DCP detection.
11	DP2	O	**Positive line of the output USB data line pair.** DP2 together with DM2 automatically provides the correct voltage signal for attached portable equipment to perform DCP detection.
12	PB	I	**Push button input.** Connect a push button from PB to AGND. PB is pulled up by a resistor internally. When PB is set from high to low for more than 1.5ms, the boost is enabled and latched if V_{IN} is not available. LED1-4 are on for five seconds whenever PB is set from high to low for more than 1.5ms. If PB is set from high to low for more than 1.5ms twice within one second and the torch light is off, the torch light drive MOSFET is on and latched. However, if PB is set from high to low for more than 1.5ms twice within one second and the torch drive MOSFET is on, the torch light drive MOSFET is off. If PB is set from high to low for more than 2.5 seconds, this is defined as a long push, and boost is shut down manually.
13	TMR	I	**Oscillator period timer.** Connect a timing capacitor between TMR and GND to set the oscillator period. Short TMR to GND to disable the timer function.
14	ISET	I	**Programmable charge current.** Connect an external resistor to GND to program the charge current.
15	OLIM	I	**Programmable output current limit for boost mode.** Connect an external resistor to GND to program the system current in boost mode.

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PIN FUNCTIONS *(continued)*

P/N	Name	I/O	Description
16	VCC	I	**Internal circuit power supply.** Bypass VCC to GND with a ceramic capacitor no higher than 100nF.
17	AGND	I/O	**Analog ground.**
18	VNTC	O	**Pull-up voltage source for the NTC function.** VNTC is connected to VCC through an internal MOSFET. VNTC is disconnected from VCC during sleep mode. VNTC should be the pull-up voltage of the external NTC resistive divider.
19	NTC	I	**Negative temperature coefficient (NTC) thermistor.**
20	VB	I	**Programmable battery full voltage.** Leave VB floating for 4.2V. Connect VB to logic high for 4.45V. Connect VB to GND for 4.35V.
21	BATT	I	**Positive battery terminal/battery charge current sense negative input.**
22	CSP	I	**Battery charge current sense positive input.**
23	LED4	O	**LED4 together with LED1, LED2, and LED3 achieves the voltage-based fuel gauge indication.**
24	LED3	O	**LED3 together with LED1, LED2, and LED4 achieves the voltage-based fuel gauge indication.**
25	LED2	O	**LED2 together with LED1, LED3, and LED4 achieves the voltage-based fuel gauge indication.**
26	LED1	O	**LED1 together with LED2, LED3, and LED4 achieves the voltage-based fuel gauge indication.**

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BLOCK DIAGRAM

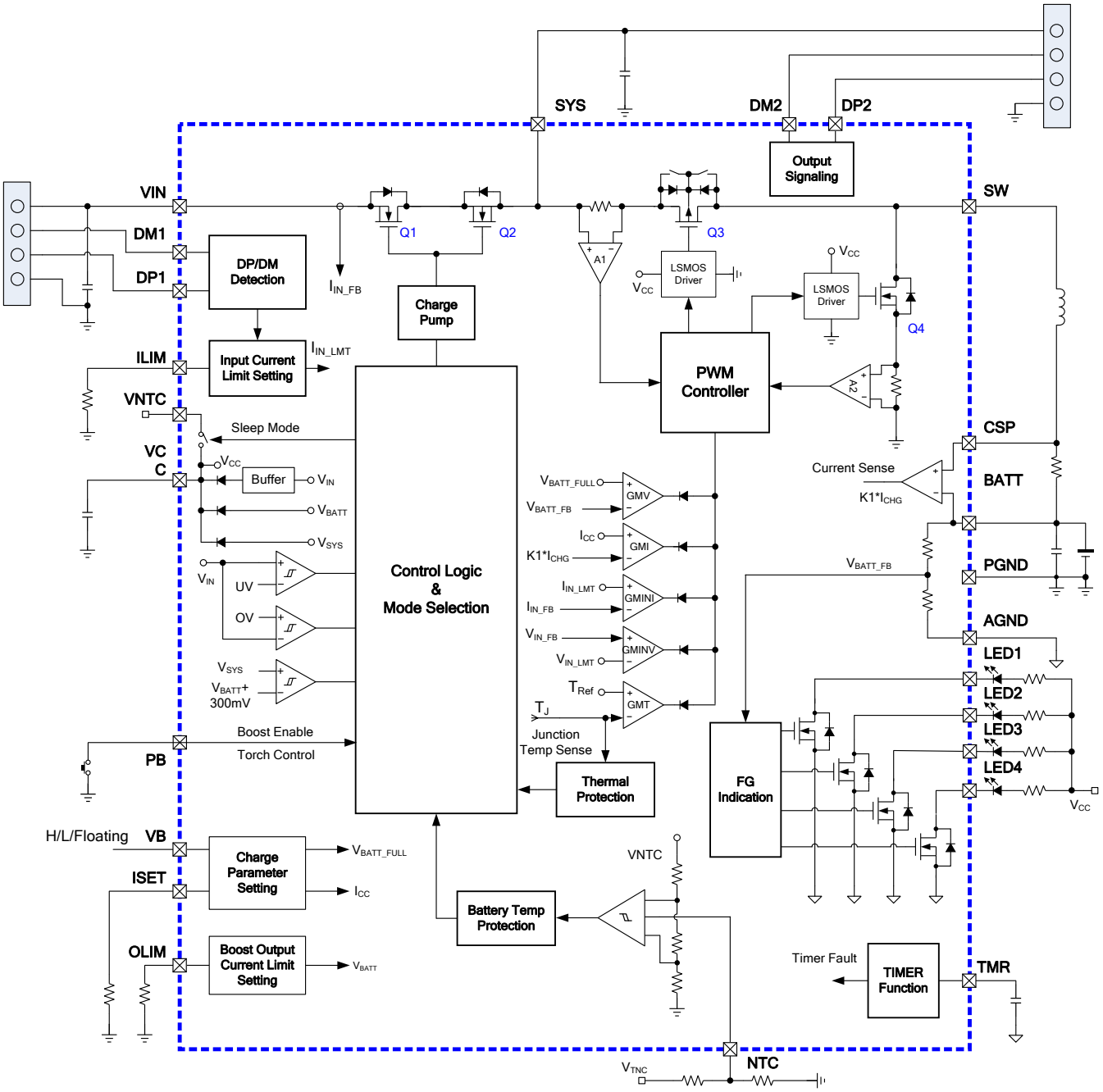


Figure 1: Functional Block Diagram in Charge Mode

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BLOCK DIAGRAM *(continued)*

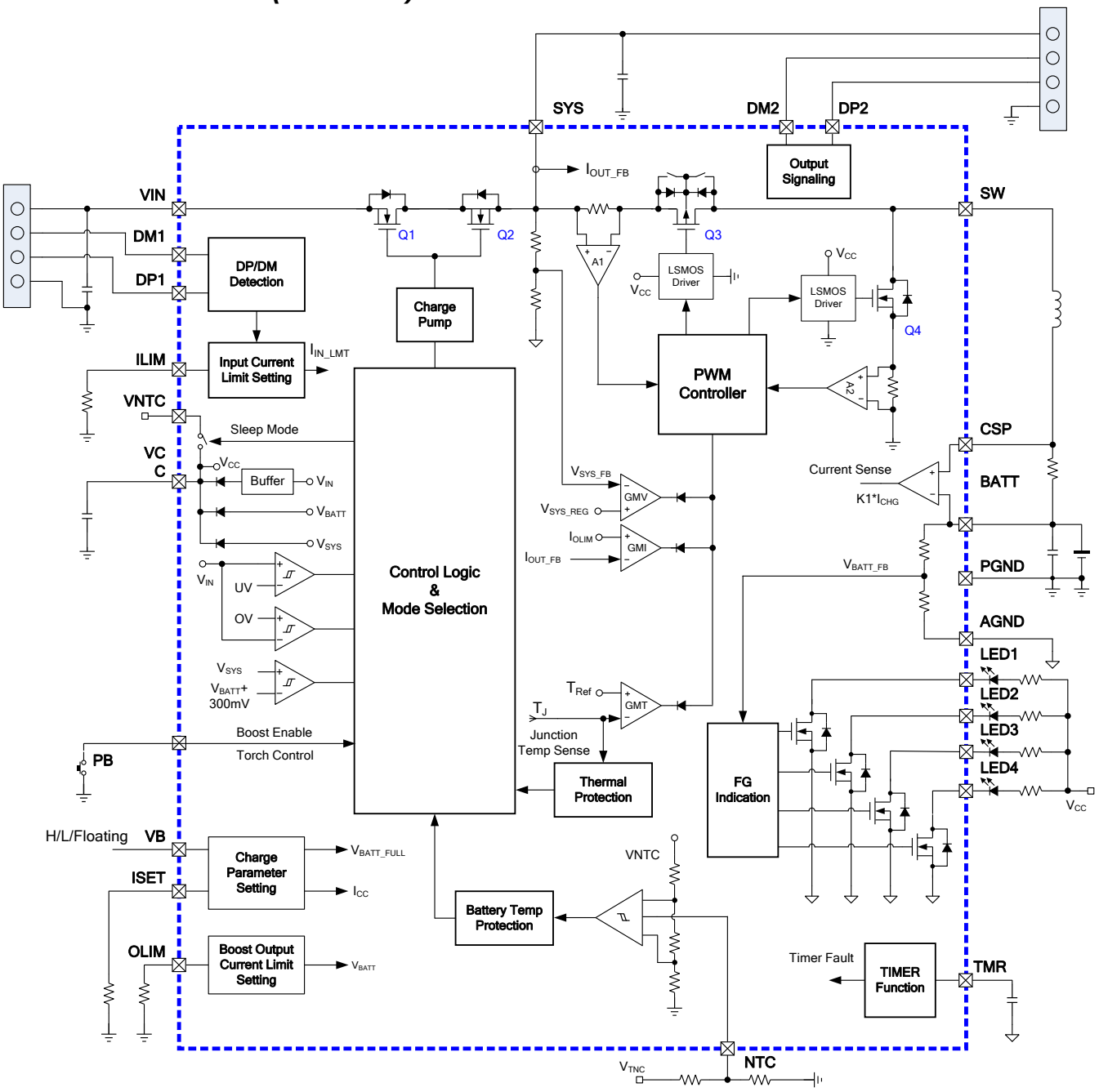


Figure 2: Functional Block Diagram in Boost Mode

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OPERATION FLOW CHART

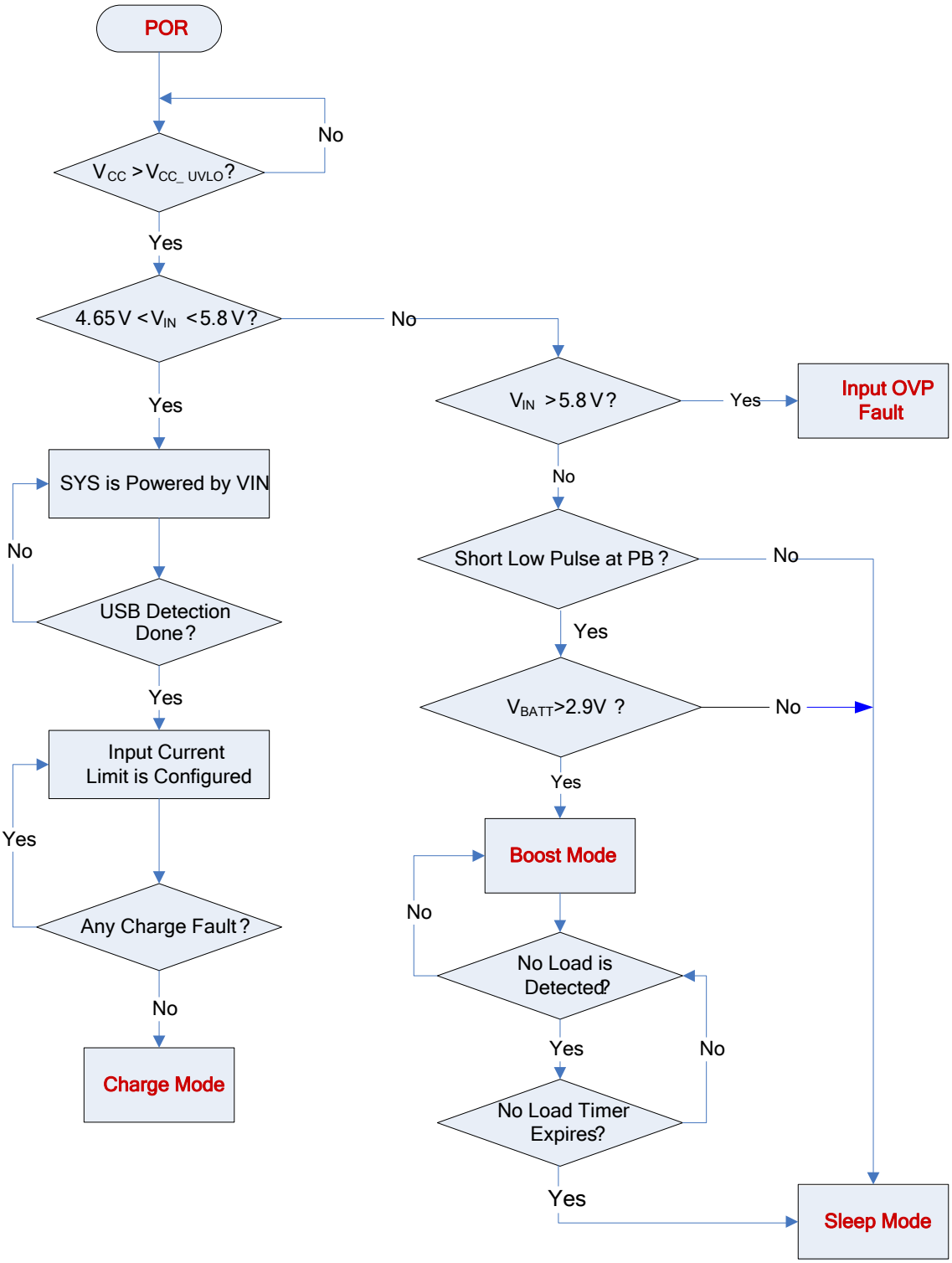


Figure 3: Mode Selection Flow Chart

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OPERATION FLOW CHART *(continued)*

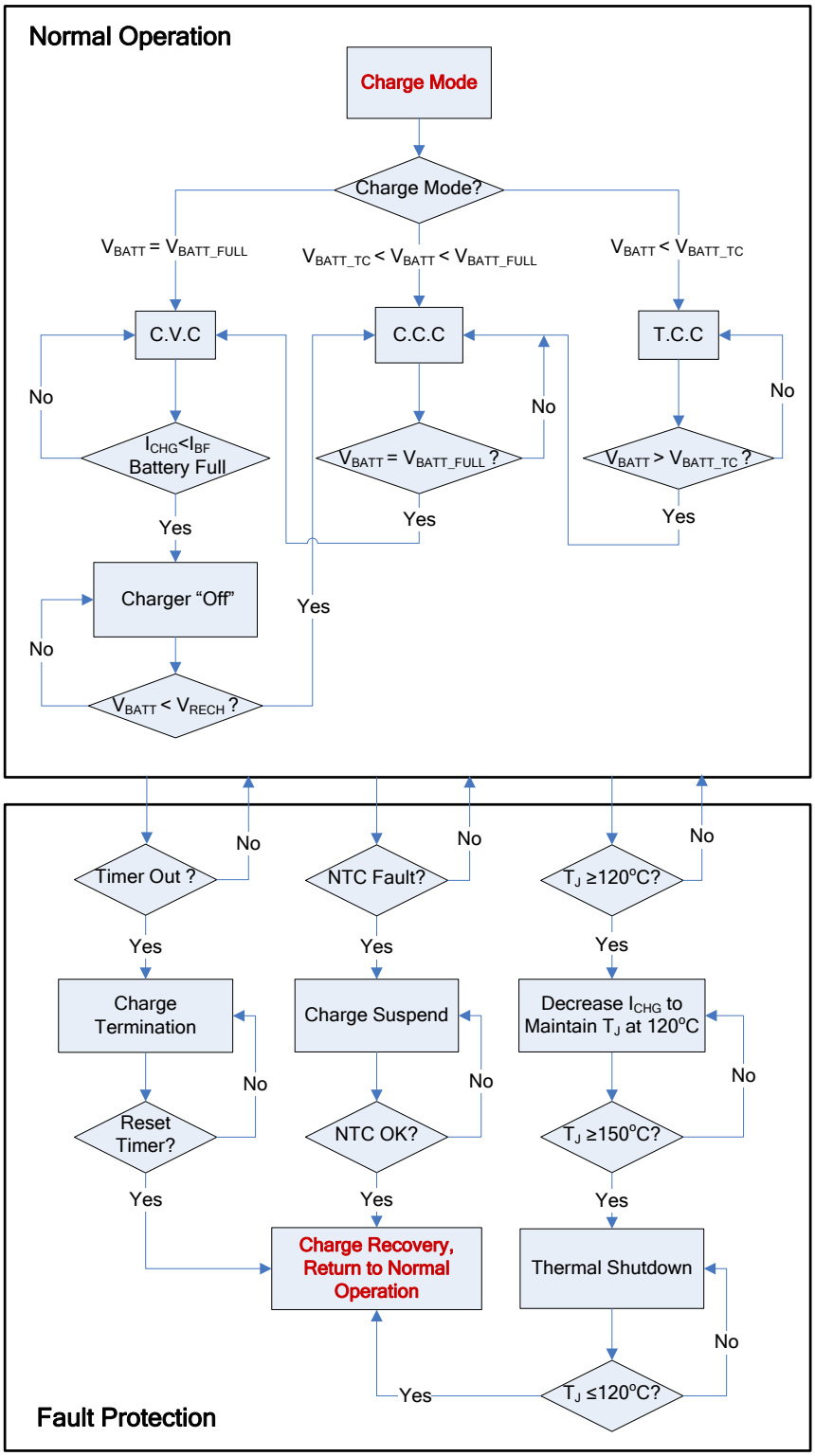


Figure 4: Normal Operation and Fault Protection in Charge Mode

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OPERATION FLOW CHART *(continued)*

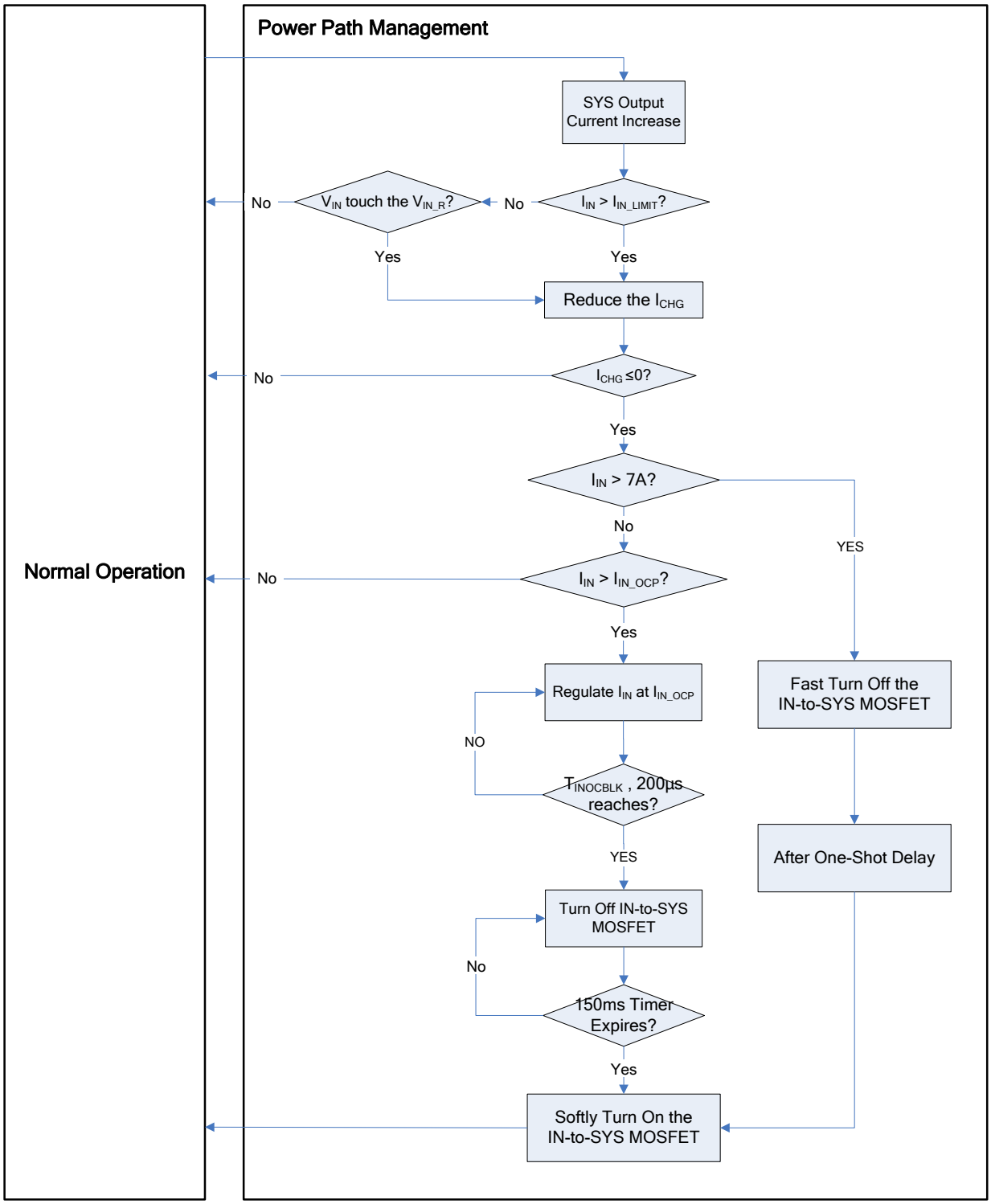


Figure 5: Power-Path Management in Charge Mode

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OPERATION FLOW CHART *(continued)*

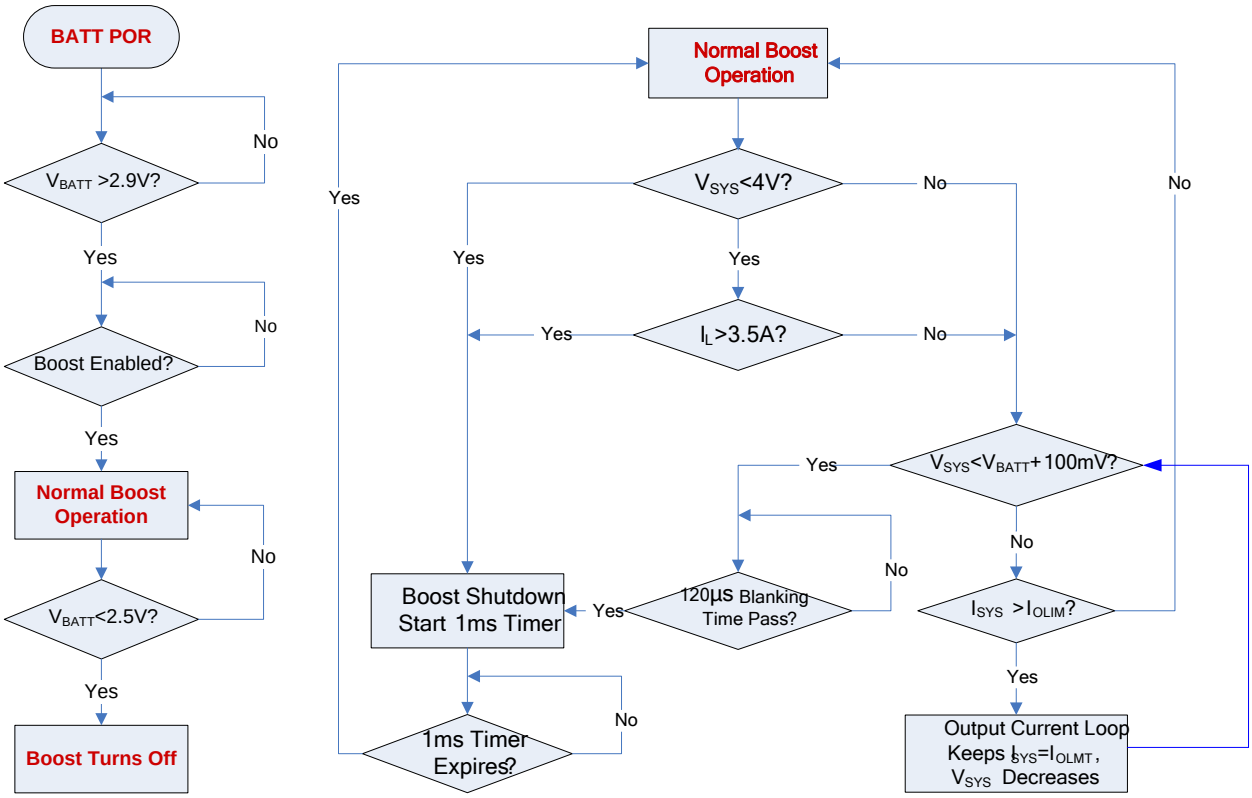


Figure 6: Operation Flow Chart in Boost Mode

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START-UP TIME FLOW IN CHARGE MODE

Condition: V_{IN} = 5V, V_{BATT} = 3.8V

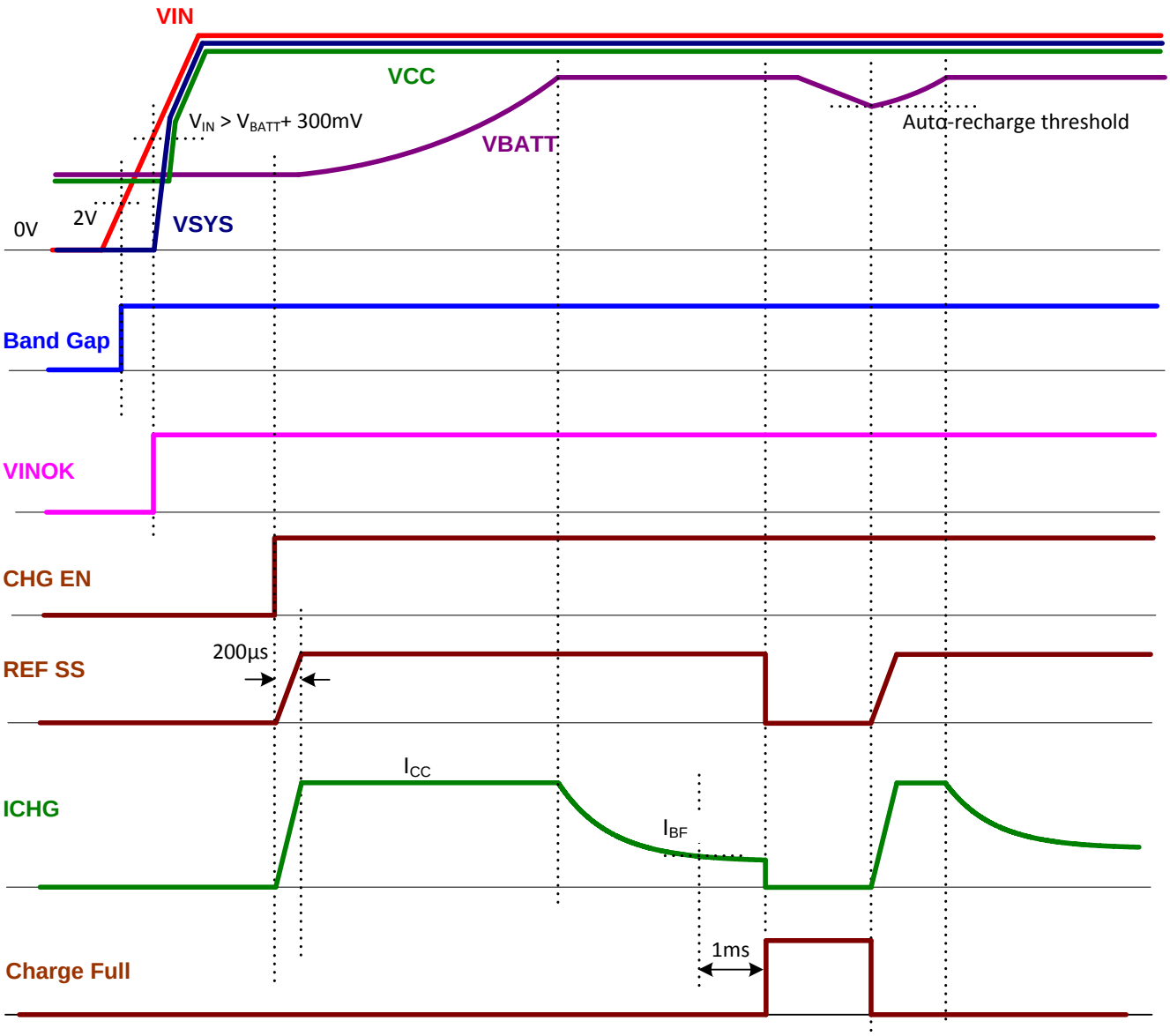


Figure 7: Input Power Start-Up Time Flow in Charge Mode

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START-UP TIME FLOW IN BOOST MODE

Condition: V_{IN} = 0V, V_{BATT} = 3.8V

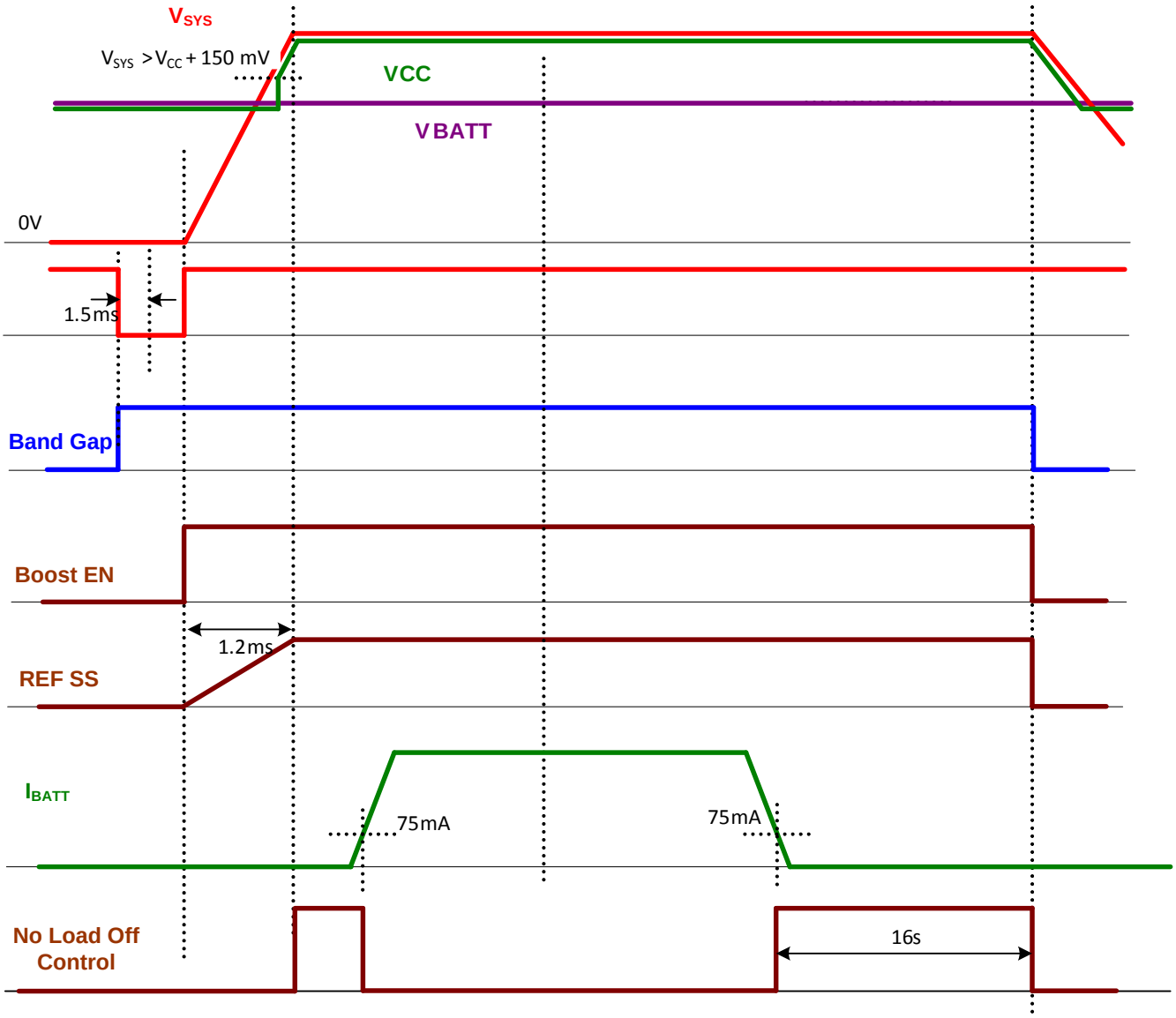


Figure 8: Boost Start-Up Time Flow in Boost Mode

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OPERATION

The MP2632 is a highly integrated, flexible, switch-mode battery charger with system power-path management designed for single-cell Li-ion or Li-polymer battery use in a wide range of applications. Depending on the status of the input, the IC can operate in three different modes: charge mode, boost mode, and sleep mode.

In charge mode, the IC can work with a single-cell Li-ion or Li-polymer battery. In boost mode, the IC boosts the battery voltage to V_{SYS} to power higher voltage system rails. In sleep mode, both charging and boost operations are disabled, and the device enters a power saving mode to help reduce overall power consumption. The IC monitors V_{IN} to allow smooth transitions between different modes of operation.

VCC Power Supply

The MP2632 has an external VCC power supply. VCC is powered by the highest voltage level out of V_{SYS}, V_{BATT}, and V_{IN} - 0.7V. An external capacitor is required to bypass VCC to GND. When VCC is higher than 2.2V, the internal control circuit is activated.

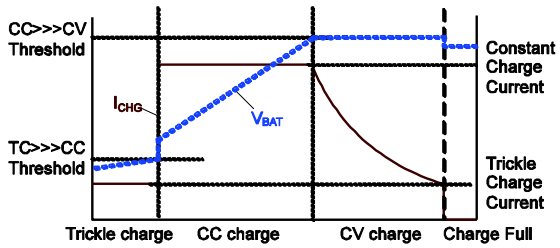
Charge Mode Operation

Charge Cycle (Trickle Charge → CC Charge → CV Charge)

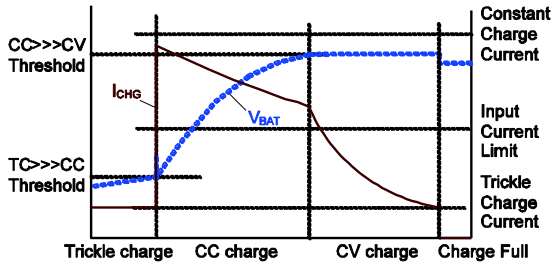
In charge mode, the IC uses five control loops to regulate the input current, input voltage, charge current, charge voltage, and device junction temperature. The IC charges the battery in three phases: trickle current (TC), constant current (CC), and constant voltage (CV).

When charge operation is enabled, all five loops are active, but only one dictates the IC behavior. A typical battery charge profile is shown in Figure 9a. The charger stays in TC charge mode until the battery voltage reaches a TC-to-CC threshold. Otherwise, the charger enters CC charge mode.

When the battery voltage rises to the CV mode threshold, the charger operates in constant voltage mode. Figure 9b shows a typical charge profile when the input current limit loop dominates during the CC charge mode. In this case, the charger maximizes the charging current due to the switching-mode charging solution, resulting in charging that is faster than a traditional linear charging solution.



a) Without input current limit



b) With input current limit

Figure 9: Typical Battery Charge Profile

Auto-Recharge

Once the battery charge cycle is completed, the charger remains off. During this time, the system load may consume battery power, or the battery may self-discharge. To ensure that the battery does not go into depletion, a new charge cycle begins automatically when the battery voltage falls below the auto-recharge threshold and the input power is present. The timer resets when the auto-recharge cycle begins.

If the input power restarts during the off-state after the battery is fully charged, the charge cycle starts and the timer resets regardless of what the battery voltage is.

Charge Current Setting

The external sense resistors (RS1 and R_{ISET}) program the battery charge current (I_{CHG}). Select R_{ISET} based on RS1.

To optimize the transfer efficiency, RS1 is recommended to be 10mΩ. The relationship between the R_{ISET} and I_{CHG} is shown in Equation (1):

$$I_{CHG}(A) = \frac{1500}{R_{ISET}(k\Omega) \times RS1(m\Omega)} \quad (1)$$

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Battery Over-Voltage Protection (OVP)

The IC has battery over-voltage protection (OVP). If the battery voltage exceeds the battery over-voltage threshold (103.5% of the battery's full voltage), charging is disabled. Under this condition, an internal 5kΩ dummy load draws a small current from BATT to reduce the battery voltage and protect the battery.

Timer Operation in Charge Mode

The IC uses an internal timer to terminate the charging. The timer remains active during the charging process. An external capacitor between TMR and GND programs the charge cycle duration.

If charging remains in TC mode beyond the trickle-charge time ($\tau_{TRICKLE_TMR}$), charging is terminated. For the MP2632, the charge current in TC mode is fixed at 265mA, and the sense resistor (RS1) is set to 10mΩ. The length of the trickle-charge period can be determined with Equation (2):

$$\tau_{TRICKLE_TMR} = 17mins \times \frac{C_{TMR}(\mu F)}{0.1\mu F} \quad (2)$$

The maximum total charge time can be calculated with Equation (3):

$$\tau_{TOTAL_TMR} = 7.55Hours \times \frac{C_{TMR}(\mu F)}{0.1\mu F} \times \frac{1A}{I_{CHG}(A) + 0.1} \quad (3)$$

Negative Temperature Coefficient (NTC) Input for Battery Temperature Monitoring

The IC has a built-in NTC resistance window comparator, which allows the IC to monitor the battery temperature via the battery-integrated thermistor during both charge and boost modes. Connect an appropriate resistor from VNTC to NTC and connect the thermistor from NTC to GND. The resistor divider determines the NTC voltage depending on the battery temperature. If the NTC voltage falls outside of the NTC window, the IC stops charging. The operation then restarts if the temperature goes back into the NTC window range. Please refer to the Application Information section on page 33 for the appropriate resistor selection.

VNTC Power Supply

The MP2632 has NTC protection in both boost mode and charge mode. To allow NTC protection in both boost mode and charge mode and to minimize the battery leakage current in sleep mode, the MP2632 uses a dedicated power supply pin for the pull-up voltage for the NTC protection function block. In boost mode and charge mode, VNTC is connected to VCC internally by a switch. In sleep mode, VNTC is disconnected from VCC to minimize the battery leakage current (see Figure 10).

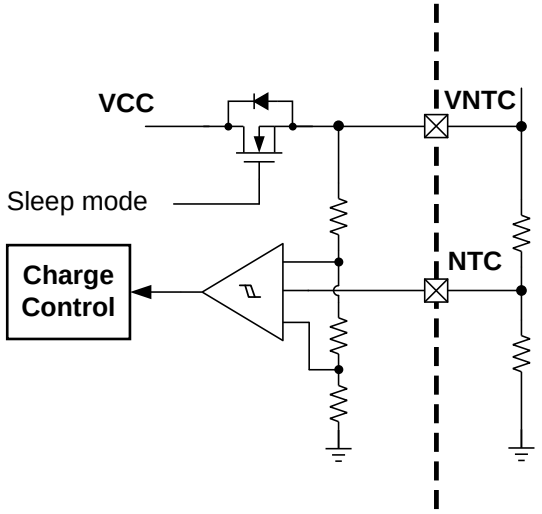


Figure 10: NTC Protection Block

Input DP1/DM1 USB Detection and Input Current Limit

Power devices (PDs) are able to draw current from the USB ports in personal computers to charge their batteries. If the portable device is attached to a USB host of the hub, then the USB specification requires the portable device to draw a limited current (usually 500mA). When the device is attached to a charging port, it is allowed to draw more than 1.5A.

The IC features input source detection to determine the input current limit according to the input source (USB or adapter) (see Figure 11).

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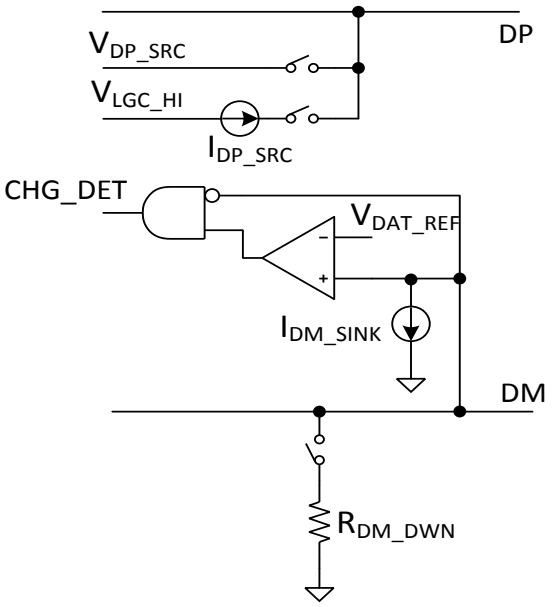


Figure 11: USB Port Detection

When the input source plugs in, the IC starts DP1/DM1 detection. DP1/DM1 detection has two steps: data contact detection (DCD) and primary detection. DCD uses a current source to detect when the data pins have made contact during an attach event. The protocol for data contact detection is as follows:

- The power device (PD) detects if V_{BUS} is asserted.
- The PD turns on DP I_{DP_SRC} and the DM pull-down resistor for 40ms.
- The PD waits for the DP line to be low.
- The PD turns off I_{DP_SRC} and the DM pull-down resistor when the DP line is detected to be low, or when the 40ms timer expires.

DCD allows the PD to start primary detection once the data pins have made contact. Once the data contact is detected, the IC jumps to the primary detection immediately. If the data contact is not detected, the IC jumps to the primary detection automatically after 300ms from the beginning of the DCD.

Primary detection is used to distinguish between the USB host (or SDP) and different types of charging ports.

During primary detection, the PD turns on V_{DP_SRC} on DP1 and I_{DM_SINK} on DM1. If the portable device is attached to a USB host, DM1 is low. If the power device is attached to CDP, DCP, or another dedicated charging port, DM1 remains high.

To be compatible with different capacities of the input source, the input current limit is recommended to be set using Table 2 if a 5V input is requested.

Table 2: Input Current Limit Setting

DP1/DM1 Detection	I_{IN_LMT}
Floating	500mA
SDP	500mA
CDP or DCP	Set through R_{ILIM}

The USB detection runs once V_{IN} is detected and is independent of the charge enable status. After the DP1/DM1 detection is done, the IC sets the input current limit as shown in Table 2.

When the detection algorithm is completed, the DP1 and DM1 signal lines enter a high-Z state with approximately 4pF of capacitive load.

External Input Current Limit Setting

The IC has a dedicated pin used to program the input current limit when CDP or DCP is detected. The current at ILIM is a fraction of the input current. The ILIM voltage indicates the average input current of the switching regulator as determined by the resistor value between ILIM and GND. As the input current approaches the programmed input current limit, the charge current is reduced to give priority to the system power.

The input current limit threshold can be determined with Equation (4):

$$I_{ILIM} = \frac{40(k\Omega)}{R_{ILIM}(k\Omega)}(A) \quad (4)$$

Input Voltage Regulation in Charge Mode

In charge mode, if the input power source is not sufficient for supporting both the charge current and the system load current, the input voltage decreases. As the input voltage internally approaches the 4.65V input voltage regulation threshold preset, the charge current is reduced to

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give priority to the system power and maintain proper regulation of the input voltage.

Integrated Over-Current Protection and Over-Voltage Protection for Pass-Through Path

The IC has an integrated IN-to-SYS pass-through path to allow direct connection of the input voltage to the system. Therefore, the IC monitors both the input current and voltage continuously. In the event of an overload, the charge current is reduced to ensure priority of the system power requirements.

The IC also features input over-current and over-voltage protection for the IN-to-SYS pass-through path.

Input Over-Current Protection (OCP)

When the total input current exceeds 5A, Q2 is controlled linearly to regulate the current (see Figure 12). If the current continues to exceed 5A after 200μs of blanking time, Q2 is turned off. In the event of the input current exceeding 7A, Q2 is turned off almost instantaneously and without any blanking time. This is done to protect both Q1 and Q2.

Input Over-Voltage Protection (OVP)

The IC has a built-in over-voltage threshold (V_{IN_OVP}). When the input voltage is higher than V_{IN_OVP}, an invalid input power source is detected by the IC. At this time, the IN-to-SYS pass-through path is turned off to prevent connecting to the wrong adapter.

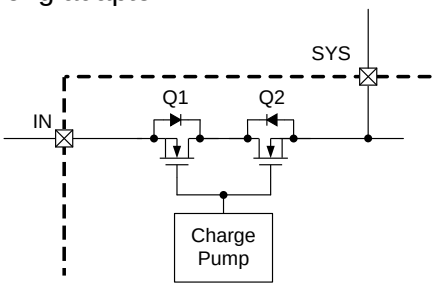


Figure 12: Integrated Pass-Through Path

Battery Short Protection

In charge mode, the MP2632 uses two inherent current-limit thresholds due to a peak-current-control strategy. CC and CV modes have a peak-current-limit threshold of 7A, while TC mode has a current-limit threshold of 4A. Therefore, the current limit threshold decreases to 4A when the battery voltage drops below the TC threshold. The switching frequency also decreases when the BATT voltage drops to 40% of the charge-full voltage.

Thermal Foldback Function

The IC implements thermal protection to prevent thermal damage to the IC and the surrounding components. An internal thermal sense and feedback loop decreases the programmed charge current automatically when the die temperature reaches 120°C. This function is called the charge-current-thermal foldback. This function protects against thermal damage and sets the charge current based on requirements, rather than worst-case conditions while ensuring safe operation. The part also includes thermal shutdown protection, where the charging process is stopped if the junction temperature rises to 150°C.

Non-Sync Operation Mode

During charging mode, the IC monitors the total input current flowing from IN to SYS continuously. When the input current is lower than 170mA, the low-side switch operates as a non-synchronous MOSFET.

Constant Off-Time Control for Large Duty Charging Operation

The IC has a built-in 600kHz frequency oscillator for the switching frequency. Unlike a traditional fixed-frequency peak-current control, the IC features a constant-off time control to support a constant current charge, even when the input voltage is very close to the battery voltage. The IC compares the high-side MOSFET sense current with the comp level continuously (see Figure 13). If the sense current does not reach the comp level within the original switching period, the next clock is delayed until the sense current reaches the comp level. As a result, the duty cycle is able to be extended as long as possible.

Indication for Fault Flag in Charge Mode

The MP2632 is designed with distinct indication separating the charging fault from the normal operation. At the charging fault, including INOVP, BOVP, and NTC fault, the four LED pins blink with a 1Hz frequency simultaneously (see Table 3).

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Table 3: Indication at Charge Mode

Operation Status	LED1 to LED4 State
Normal charging	Depending on the battery voltage, LEDx blinks at 1Hz, (refer to Fuel Gauge Indication section)
Charge full	LED1 to LED4 are all turned on
VIN UVLO	LED1 to LED4 are all turned off
VIN OVP, NTC fault, battery OVP	LED1 to LED4 are all blinking at 1Hz

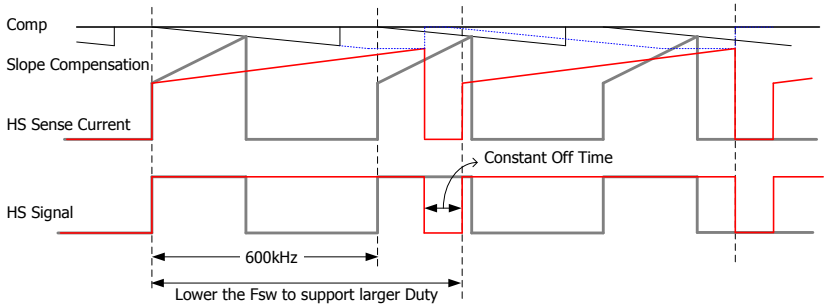


Figure 13: Constant-Off Time Operation Profile

Boost Mode Operation

Low-Voltage Start-Up

The minimum battery voltage required to start up the circuit in boost mode is 2.9V. Initially, when V_{SYS} is less than V_{BATT}, the IC works in down mode. In this mode, the synchronous P-FET stops switching and its gate connects to V_{BATT} statically. The P-FET stays off for as long as the voltage across the parasitic C_{DS} (V_{SW}) is lower than V_{BATT}. When the voltage across C_{DS} exceeds V_{BATT}, the synchronous P-FET enters linear mode, allowing the inductor current to decrease and flow into SYS. Once V_{SYS} exceeds V_{BATT}, the P-FET gate is released, and normal closed-loop PWM operation is initiated. In boost mode, the battery voltage can drop as low as 2.5V without affecting circuit operation.

SYS Disconnect and Inrush Limiting

The IC can achieve true output disconnect by eliminating body diode conduction of the internal P-FET rectifier. V_{SYS} can go to 0V during shutdown, drawing no current from the input source. It also allows for inrush current limiting at start-up, minimizing surge currents from the input supply. To optimize the benefits of the output disconnect, avoid connecting an external Schottky diode between SW and SYS.

Board layout is extremely critical for minimizing voltage overshoot at SW due to stray inductance. Keep the output filter capacitor as close to SYS as possible, and use very low ESR/ESL ceramic capacitors tied to a good ground plane.

Boost Output Voltage Setting

In boost mode, the IC programs the output voltage internally according to the load connected to SYS (5.1V or 5.2V) and provides built-in output over-voltage protection (OVP) to protect the device and other components against damage when V_{SYS} goes beyond 6V. Once output over-voltage occurs, the IC turns off the boost converter. When the voltage on V_{SYS} drops to a normal level, the boost converter restarts again when PB is set from high to low for more than 1.5ms.

Boost Output Current Limiting

The IC integrates a programmable output current limit function in boost mode. If the boost output current exceeds this programmable limit, the output current is limited at this level and the SYS voltage begins to drop down. OLIM programs the current limit threshold up to 3.0A, per Equation (5):

$$I_{OLIM}(A) = \frac{1500}{R_{OLIM}(k\Omega) \times RS1(m\Omega)} \quad (5)$$

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The MP2632 can operate in CC mode when the current limit is reached, and V_{IN} does not drop to the down mode threshold (V_{BATT} + 100mV) (see Figure 14).

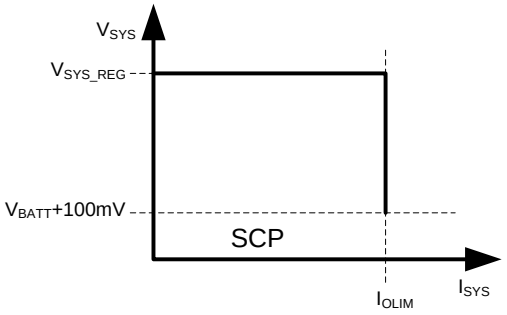


Figure 14: Boost Output U-I Curve

The MP2632 not only has CC mode during the charging process, but also has CC mode operation in boost mode for various applications.

SYS to BATT Block Protection

When there is no V_{IN} and the boost mode is not on, the part is in sleep mode. The HS switch implements the body switch function, which connects the body diode of the switch to the high-voltage side of SW and SYS, which blocks the external voltage on SYS from flooding into the battery.

SYS Output Over-Current Protection (OCP)

The IC integrates a three-phase output over-current protection.

1. Phase one (boost mode output current limit): When the output current exceeds the programmed output current limit, the output constant current loop controls the output current, the output current remains at its limit (I_{OLIM}), and V_{SYS} decreases.
2. Phase two (down mode): When V_{SYS} drops below V_{BATT} + 100mV and the output current loop remains in control, the boost converter enters down mode and shuts down after 120μs of blanking time.
3. Phase three (short-circuit mode): When V_{SYS} drops below 4.0V (2V during boost soft start), the boost converter shuts down immediately once the inductor current hits the foldback peak-current limit of the low-side N-FET. The boost converter can also recover automatically after a 1ms deglitch period.

Thermal Shutdown Protection

The thermal shutdown protection is also active in boost mode. Once the junction temperature rises higher than 150°C, the IC enters thermal shutdown and does not resume normal operation until the junction temperature drops below 120°C.

Automatic Off at Light Load

The boost turns off automatically if the load current at BATT is below the typical 75mA value for 16 seconds.

The MP2632 also features a long-push action on PB to shut down the boost manually. A low push on PB longer than 2.5 seconds is defined as a long push (see Figure 14 for PB action).

Automatic Output DP2/DM2 Signaling

In boost mode, the IC sets the DP2/DM2 signal based on the load applied on USB2. In pass-through mode, DP2 and DM2 are set according to DP1/DM1 detection results.

In boost mode, DM2/DP2 are set based on three types of signals: DM2/DP2 separately biased with a 2.7V voltage signal (default), DM2/DP2 shorted, and DM2/DP2 shorted with a 1.2V bias.

In pass-through mode, DM2/DP2 are connected together if the dedicated charger ports are detected, and pulled down to ground separately with a 15kΩ resistor if SDP is identified.

Torch Control

If the internal torch drive FET is off when PB is pulled from high to low for more than 1.5ms twice within one second, the drive FET is turned on. Conversely, if the torch drive FET is on, the drive FET is turned off.

Once the torch light is turned on, the automatic off function is blocked.

PB Control

PB is used to control the enable of boost mode. Pull PB from high to low for more than 1.5ms to enable boost mode; pull PB from high to low for 2.5s to disable boost mode.

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Automatic On when Load is Applied

The boost turns on automatically when PB is pulled from high to low for more than 1.5ms, or when the load is plugged in to USB2 using the PB control.

To detect the USB load plug-in, the RC network is connected to the USB port shield floating in the PCB. Once the USB load is inserted, the USB connector shield is grounded through the USB load. A short pulse (high to low for more than 1.5ms) is generated in PB, resulting in the start of boost.

An RC network can also be connected in V_{BUS} of the USB output port. During load insertion, the load input cap generates a high-to-low pulse for more than 1.5ms to start the boost (see Figure 15). The circuit in the dash frame is the automatic load detection circuit. M2 is used to decouple the USB port from the V_{SYS} cap (C2, C_{SYS}), and M1 is used to drive M2.

Once a phone is plugged in, the voltage at C_{USB} is pulled down because the input cap inside the phone is far larger than C_{USB}, so the falling edge is delivered to PB to enable boost automatically.

M3 is used to cut off PB to and from the USB port when boost is turned on. The PB state is not affected by the spec of the inserted load of the USB port. Choose M3 with a low turn-on threshold (-0.7V is recommended) which can ensure that it is fully on when the load is inserted and that its on resistance does not cause too much of a voltage drop.

4-LED Driver for Voltage-Based Fuel Gauge

The IC provides 4-LED drivers for a voltage-based fuel gauge. The driver is connected to an internal open-drain FET. The 4-LED indication values are shown in Table 4.

The LED threshold can be programmed using a fuse. Each threshold can be adjusted from 150mV to 200mV with 50mV steps from their default value.

The LED threshold is also adjusted automatically based on the V_{BAT_REG} setting. The V_{OREG} difference is considered to be offset for LED thresholds.

During the voltage measurement, the battery impedance (50mΩ) should be compensated based on the battery current to get a precise battery voltage for fuel gauge indication.

Indication for Fault Flag in Boost Mode

To minimize the power consumption of the battery, the indication is active once PB is short-pushed in normal discharge operation, and turns off after five seconds automatically.

Table 4: Indication at Discharge Mode

Operation status	LED1 to LED4 state
Normal discharging	Depending on the battery voltage, LEDx is turned off. (refer to Fuel Gauge Indication section)
NTC fault	LED1 to LED4 are all blinking at 1Hz

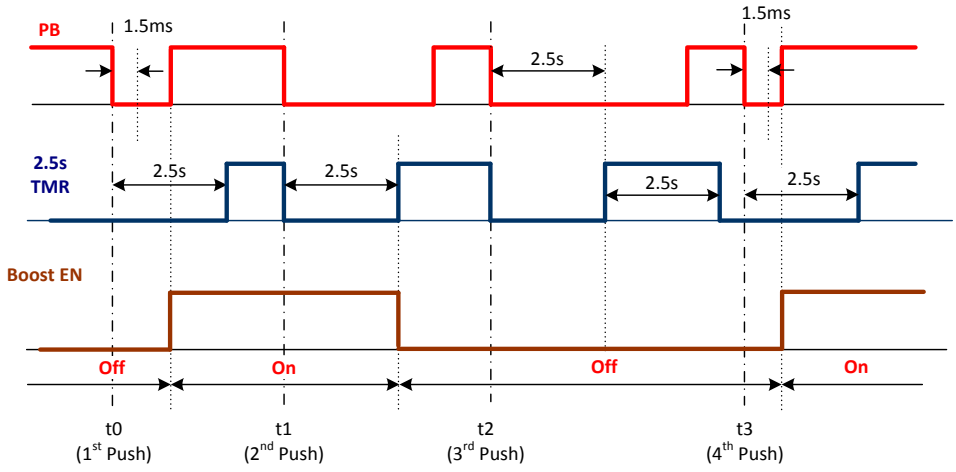


Figure 15: PB Action Profile

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Table 5: Indication during Normal Operation

Mode	V_{BATT}	SOC	LED1	LED2	LED3	LED4
Charging	V_{BATT} < 3.6V	<25%	Flash	Off	Off	Off
	[3.6V, 3.8V)	[25%, 50%)	On	Flash	Off	Off
	[3.8V, 4.0V)	[50%, 75%)	On	On	Flash	Off
	CV mode, [4.0V, 4.2V), not terminated	[75%, 100%)	On	On	On	Flash
	V_{BATT} ≥ 4.0, terminated	100%	On	On	On	On
Discharging (All off after 5s)	V_{BATT} ≥ 3.92V	>75%	On	On	On	On
	[3.77V, 3.92V)	[50%, 75%)	On	On	On	Off
	[3.62V, 3.77V)	[25%, 50%)	On	On	Off	Off
	[3.47V, 3.62V)	[5%, 25%)	On	Off	Off	Off
	[V_{BAT_ULVO}, 3.47V)	[1%, 5%)	Flash	Off	Off	Off
	V_{BATT} < V_{BAT_UVLO}	<1%	Off	Off	Off	Off

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APPLICATION INFORMATION

Setting the Charge Current in Charge Mode

In charge mode, both the external sense resistor (RS1) and the resistor (R_{ISET}) connect to ISET to set the charge current (I_{CHG}) of the MP2632 (see the Typical Application circuit on page 2). Given the expected I_{CHG} and RS1 values, R_{ISET} can be calculated with Equation (6):

$$I_{CHG}(A) = \frac{1500}{R_{ISET}(k\Omega) \times RS1(m\Omega)} \quad (6)$$

For example, if I_{CHG} = 3.0A and RS1 = 10mΩ, then R_{ISET} = 49.9kΩ.

Given a 10mΩ RS1, Table 6 lists the expected R_{ISET} values for the typical charge current.

Table 6: Charging Current vs. R_{ISET}

R_{ISET} (kΩ)	Charge Current (A)
150	1.0
100	1.5
75	2.0
60	2.5
49.9	3.0

Setting the Input Current Limit in Charge Mode

In charge mode, connect a resistor from ILIM to AGND to program the input current limit if a dedicated charger (CDP or DCP) is detected. The relationship between the input current limit and setting resistor is shown in Equation (7):

$$I_{ILIM} = \frac{40(k\Omega)}{R_{ILIM}(k\Omega)}(A) \quad (7)$$

R_{ILIM} must exceed 14.7kΩ so that I_{IN_LIM} is in the range of 0A to 2.7A.

NTC Function in Charge Mode

An internal resistor divider sets the low temperature threshold (V_{TL}) and high temperature threshold (V_{TH}) at 66.6% of V_{SYS} and 35% of V_{SYS}, respectively (see Figure 16). For a given NTC thermistor, select an appropriate R_{T1} and R_{T2} to set the NTC window with Equation (8) and Equation (9):

$$\frac{V_{TL}}{V_{SYS}} = \frac{R_{T2}//R_{NTC_Cold}}{R_{T1} + R_{T2}//R_{NTC_Cold}} = TL = 66.6\% \quad (8)$$

$$\frac{V_{TH}}{V_{SYS}} = \frac{R_{T2}//R_{NTC_Hot}}{R_{T1} + R_{T2}//R_{NTC_Hot}} = TH = 35\% \quad (9)$$

Where R_{NTC_Hot} is the value of the NTC resistor at the upper bound of its operating temperature range, and R_{NTC_Cold} is its lower bound.

The two resistors R_{T1} and R_{T2} determine the upper and lower temperature limits independently. This flexibility allows the IC to operate with most NTC resistors for different temperature range requirements. Calculate R_{T1} and R_{T2} with Equation (10) and Equation (11):

$$R_{T1} = \frac{R_{NTC_Hot} \times R_{NTC_Cold} \times (TL - TH)}{TH \times TL \times (R_{NTC_Cold} - R_{NTC_Hot})} \quad (10)$$

$$R_{T2} = \frac{(TL - TH) \times R_{NTC_Cold} \times R_{NTC_Hot}}{(1 - TL) \times TH \times R_{NTC_Cold} - (1 - TH) \times TL \times R_{NTC_Hot}} \quad (11)$$

For example, the NCP18XH103 thermistor has the following electrical characteristics:

- At 0°C, R_{NTC_Cold} = 27.445kΩ
- At 50°C, R_{NTC_Hot} = 4.1601kΩ

Based on Equation (17) and Equation (18), an R_{T1} value of 6.65kΩ and an R_{T2} value of 25.63kΩ are suitable for an NTC window between 0°C and 50°C. Approximate values are R_{T1} = 6.65kΩ and R_{T2} = 25.5kΩ.

If no external NTC is available, connect R_{T1} and R_{T2} to keep the voltage on NTC within the valid NTC window (e.g.: R_{T1} = R_{T2} = 10kΩ).

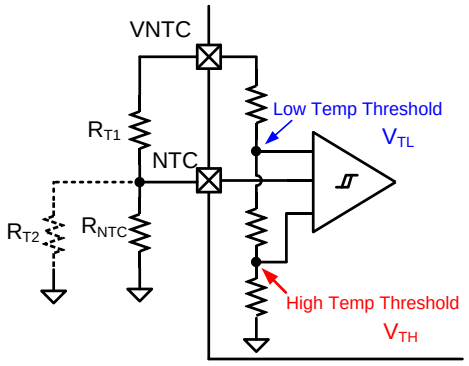


Figure 16: NTC Function Block

For convenience, an NTC thermistor design spreadsheet has also been provided.

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Setting the Output Current Limit in Boost Mode

In boost mode, connect a resistor from OLIM to AGND to program the output current limit. The relationship between the output current limit and the setting resistor is shown in Equation (12):

$$I_{OLIM}(A) = \frac{1500}{R_{OLIM}(k\Omega) \times RS1(m\Omega)} \quad (12)$$

The output current limit of the boost can be programmed up to 3.0A.

Given a 10mΩ RS1, Table 7 lists the expected R_{OLIM} values for the typical output current limit.

Table 7: Output Current vs. R_{OLIM}

R_{OLIM} (kΩ)	Output Current (A)
150	1.0
100	1.5
75	2.0
60	2.5
49.9	3.0

Selecting the Inductor

The inductor selection trades off between cost, size, and efficiency. A lower inductance value corresponds with a smaller size, but results in higher current ripples, higher magnetic hysteretic losses, and higher output capacitances. However, a higher inductance value benefits from lower ripple currents and smaller output filter capacitors, but results in a higher inductor DC resistance (DCR) loss. Choose an inductor that does not saturate under the worst-case load condition.

In charge mode, the MP2632 works as a buck converter. The required inductance can be estimated with Equation (13):

$$L = \frac{V_{IN} - V_{BATT}}{\Delta I_{L_MAX}} \times \frac{V_{BATT}}{V_{IN} \times f_S} \quad (13)$$

Where V_{IN} is the typical input voltage, V_{BATT} is the CC charge threshold, f_S is the switching frequency, and ΔI_{L_MAX} is the maximum peak-to-peak inductor current, which is usually designed at 30% - 40% of the CC charge current.

With a typical 5V input voltage, if there is a 35% inductor current ripple at the corner point between the trickle charge and the CC charge (V_{BATT} = 3V, I_{CHG} = 2.5A), then the inductance is 2.2μH.

In boost mode, the MP2637 works as a boost converter. The required inductance value can be calculated with Equation (14), Equation (15), and Equation (16):

$$L = \frac{V_{BATT} \times (V_{SYS} - V_{BATT})}{V_{SYS} \times f_S \times \Delta I_{L_MAX}} \quad (14)$$

$$\Delta I_{L_MAX} = (30\% - 40\%) \times I_{BATT(MAX)} \quad (15)$$

$$I_{BATT(MAX)} = \frac{V_{SYS} \times I_{SYS(MAX)}}{V_{BATT} \times \eta} \quad (16)$$

Where V_{BATT} is the minimum battery voltage, f_{SW} is the switching frequency, and ΔI_{L_MAX} is the peak-to-peak inductor ripple current (approximately 30% of the maximum battery current ($I_{BATT(MAX)}$)), $I_{SYS(MAX)}$ is the system current, and η is the efficiency.

The worst case occurs if the battery voltage is 3V, there is a 30% inductor current ripple, and the typical system voltage is V_{SYS} = 5V. Then, the inductance is 1.5μH when the efficiency is 90%.

For best results, use an inductor with an inductance of 2.2μH with a DC current rating no lower than the peak current of the MOSFET. For higher efficiency, minimize the inductor's DC resistance.

Selecting the Input Capacitor (C_{IN})

The input capacitor (C_{IN}) reduces both the surge current drawn from the input and the switching noise from the device. The input capacitor impedance at the switching frequency should be less than the input source impedance to prevent the high-frequency switching current from passing to the input. Ceramic capacitors with X7R dielectrics are recommended because of their low ESR and small temperature coefficients. For most applications, a 22μF capacitor is sufficient.

Selecting the System Capacitor (C_{SYS})

Select the system capacitor (C_{SYS}) based on the demand of the system current ripple. In charge mode, C_{SYS} acts as the input capacitor of the buck converter. The input current ripple can be calculated with Equation (17):

$$I_{RMS_MAX} = I_{SYS_MAX} \times \frac{\sqrt{V_{TC} \times (V_{IN_MAX} - V_{TC})}}{V_{IN_MAX}} \quad (17)$$

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In boost mode, C_{SYS} is the output capacitor of the boost converter. C_{SYS} keeps the system voltage ripple small and ensures feedback loop stability. The system current ripple can be calculated with Equation (18):

$$I_{RMS_MAX} = I_{SYS_MAX} \times \frac{\sqrt{V_{TC} \times (V_{SYS_MAX} - V_{TC})}}{V_{SYS_MAX}} \quad (18)$$

Since the input voltage is passed to the system directly, V_{IN_MAX} is equal to V_{SYS_MAX}, and both charge mode and boost mode have the same system current ripple.

When I_{CC_MAX} equals 2A, V_{TC} equals 3V, V_{IN_MAX} equals 6V, and the maximum ripple current is 1A. Select the system capacitors based on the ripple-current temperature rise, not exceeding 10°C. For best results, use low ESR ceramic capacitors with X7R dielectrics and small temperature coefficients. For most applications, use three 22µF capacitors.

Selecting the Battery Capacitor (C_{BATT})

C_{BATT} is in parallel with the battery to absorb the high-frequency switching ripple current. In charge mode, the capacitor (C_{BATT}) is the output capacitor of the buck converter. The output voltage ripple is then calculated with Equation (19):

$$\Delta r_{BATT} = \frac{\Delta V_{BATT}}{V_{BATT}} = \frac{1 - V_{BATT} / V_{SYS}}{8 \times C_{BATT} \times f_{SW}^{2} \times L} \quad (19)$$

In boost mode, C_{BATT} is the input capacitor of the boost converter. The input voltage ripple is the same as the output voltage ripple from Equation (19).

Both charge mode and boost mode have the same battery voltage ripple. C_{BATT} can be calculated with Equation (20):

$$C_{BATT} = \frac{1 - V_{TC} / V_{SYS_MAX}}{8 \times \Delta r_{BATT_MAX} \times f_{SW}^{2} \times L} \quad (20)$$

To guarantee ±0.5% BATT voltage accuracy, the maximum BATT voltage ripple must not exceed 0.5% (e.g.: 0.1%). The worst case occurs at the minimum battery voltage of the CC charge with the maximum input voltage. For example, V_{SYS_MAX} = 6V, V_{CC_MIN} = V_{TC} = 3V, L = 2.2µH, f_S = 600kHz, Δr_{BATT_MAX} = 0.1%, and C_{BATT} is 22µF.

A 22µF ceramic capacitor with X7R dielectrics is sufficient.

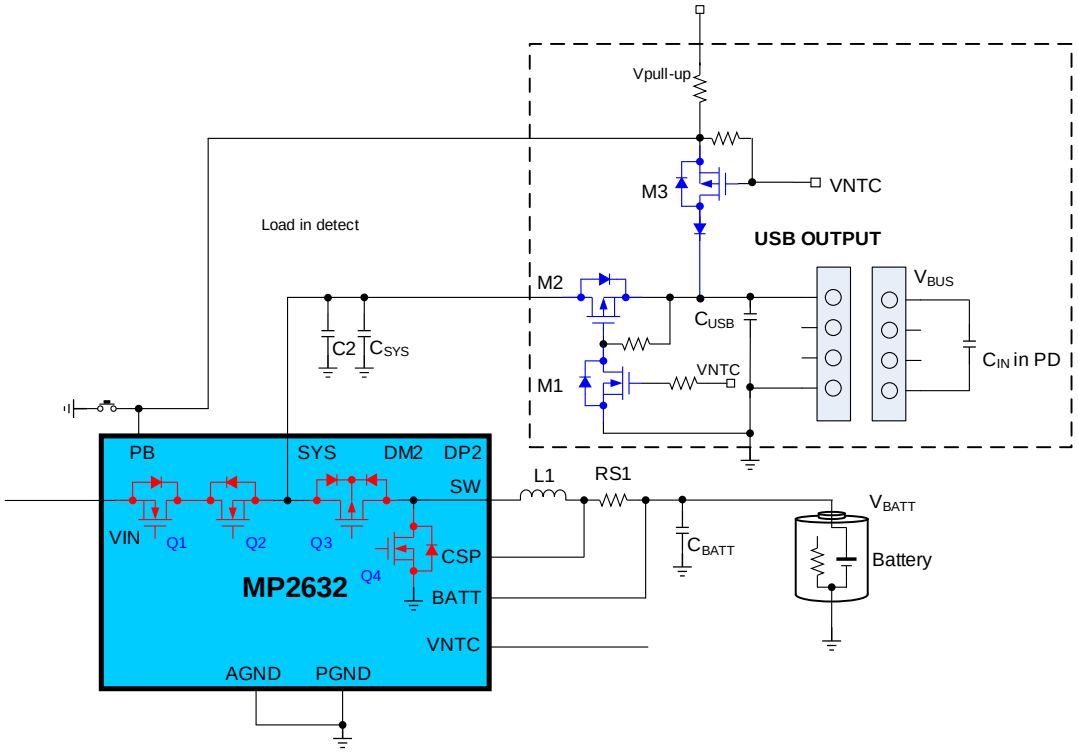
PCB Layout Guidelines

Efficient PCB layout is critical for meeting specified noise, efficiency, and stability requirements. The following design considerations can improve circuit performance:

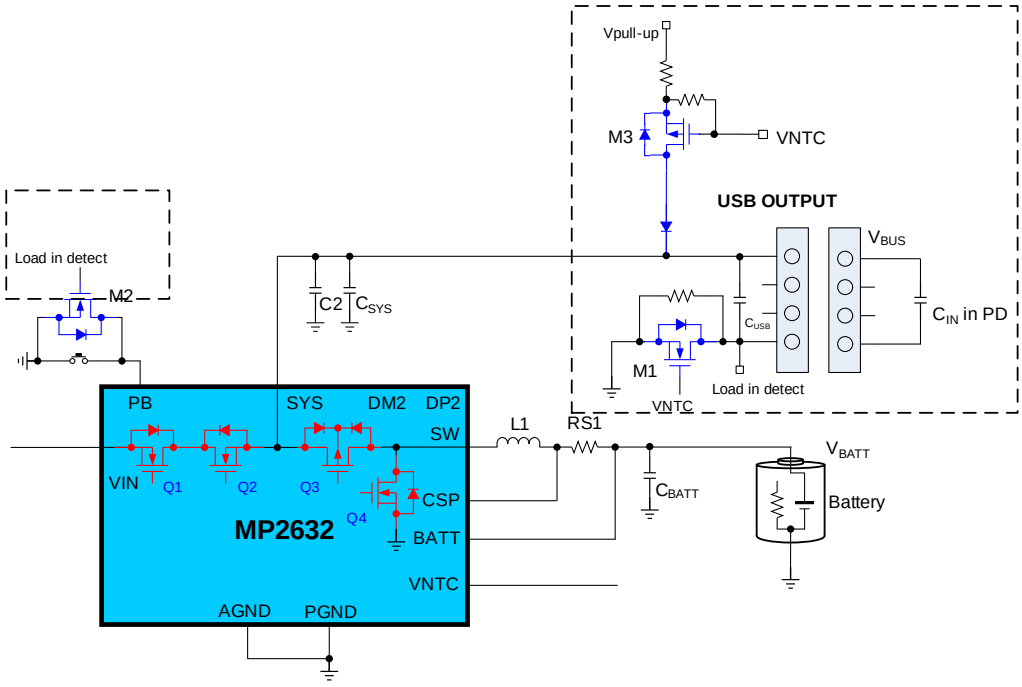
1. Route the power stage adjacent to their grounds.
2. Minimize the high-side switching node (SW, inductor) trace lengths in the high-current paths.
3. Keep the switching node short and away from all small control signals, especially the feedback network.
4. Place the input capacitor as close to V_{IN} and PGND as possible.
5. Place the local power input capacitors connected from SYS to PGND as close to the IC as possible.
6. Place the output inductor close to the IC.
7. Connect the output capacitor between the inductor and PGND of the IC.
8. Connect the power pads for VIN, SYS, SW, BATT, and PGND to as many coppers planes on the board as possible for high-current applications.
   This improves thermal performance because the board conducts heat away from the IC.
9. Connect a ground plane directly to the return of all components through vias (e.g.: two vias per capacitor for power-stage capacitors, and one via per capacitor for small-signal components).
   A star ground design approach is typically used to keep circuit block currents isolated (power-signal/control-signal), which reduces noise-coupling and ground-bounce issues. A single ground plane for this design provides good results.
10. Place the ISET, OLIM, and ILIM resistors very close to their respective IC pins.

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TYPICAL APPLICATION CIRCUITS



a) High-Side MOSFET Solution



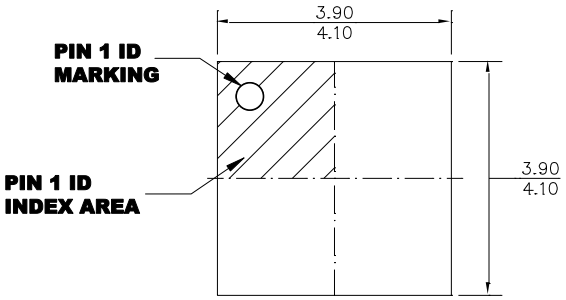
b) Low-Side MOSFET Solution

Figure 17: **Load Detection Circuit**

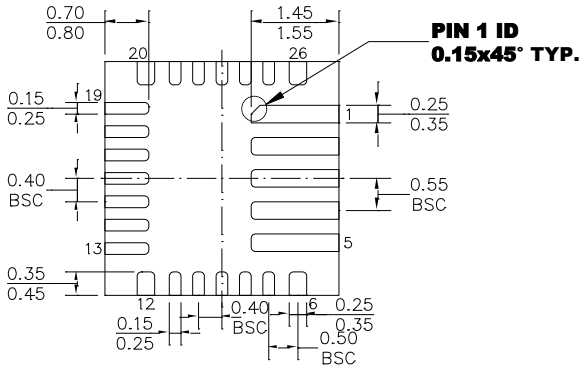
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PACKAGE INFORMATION

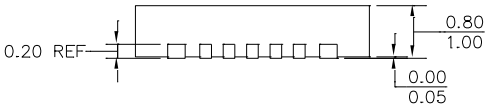
QFN-26 (4mmx4mm)



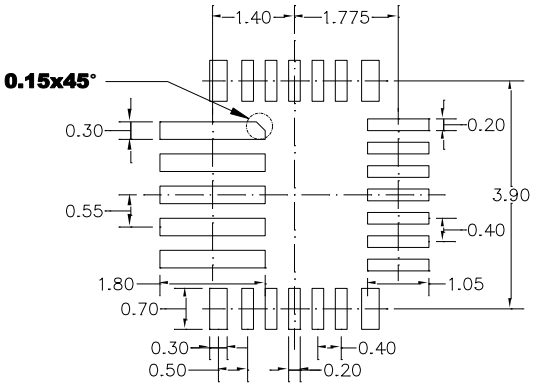
TOP VIEW



BOTTOM VIEW



SIDE VIEW



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