MP2665A

21V, 1A, Battery Charger for Single-Cell Li-Ion Batteries with I²C Control, Power Path Management, and Shipping Mode

DESCRIPTION

The MP2665A is a highly integrated, single-cell Li-ion/Li-polymer battery charger with system power path management. It is targeted at space-constrained portable applications. This device takes input power from either an AC adapter or a USB port to supply the system load and charge the battery simultaneously. The charger features pre-charge, constant current (CC) fast charge, constant voltage (CV) regulation, charge termination, and automatic recharge.

Power path management ensures that the system is continuously powered by automatically selecting the input, the battery, or both to power the system. Power path management is accomplished using a low-dropout (LDO) regulator connected from the input to the system, as well as a 100mΩ switch connected from the battery to the system. This function separates the charging current from the system load, which allows for proper charge termination and keeps the battery in full charge mode.

The MP2665A provides system short-circuit protection (SCP) by limiting the current from the input to the system, as well as the current from the battery to the system. This feature is especially critical to prevent the Li-ion battery from being damaged due to excessively high currents. An on-chip battery under-voltage lockout (UVLO) threshold cuts off the path between the battery and the system if the battery voltage drops below the configurable battery UVLO threshold. This prevents the Li-ion battery from being overly discharged. An integrated I²C interface allows the MP2665A to configure the following charging parameters: input current limit, input voltage regulation limit, charging current, battery regulation voltage, safety timer, and battery UVLO threshold.

The MP2665A is available in a QFN-12 (2.5mmx3mm) package.

FEATURES

- USB-Compliant, I²C-Configurable Charger for Single-Cell Li-Ion/Polymer Batteries
- 21V Maximum Input Voltage Rating with Over-Voltage Protection (OVP)
- Complete Power Path Management to Simultaneously Power the System and Charge the Battery
- **Fully Configurable Charging Parameters:**
  - 50mA to 1A Input Current Limit
  - 3.88V to 5.08V Input Voltage Loop to Support Weak Adapters
  - ±0.5% Charging Termination Voltage Accuracy
  - 16mA to 896mA Fast Charge Current
  - 2.5mA to 62mA Pre-Charge and Termination Current
- I²C Interface to Set Charging Parameters and Report INT/Statuses
- Ultra-Low Battery Leakage Current in Shipping Mode
- **Robust Safety Features:**
  - Built-in Charging Protections Including Battery Temperature Monitoring and Configurable Timer
  - Configurable Thermal Regulation
  - Configurable Watchdog Timer
  - PCB Over-Temperature Protection
  - Configurable Over Discharge Current Protection
- System Reset Function
- OTP Back Registers to Set Default Power-On Configuration
- Available in a QFN-12 (2.5mmx3mm) Package

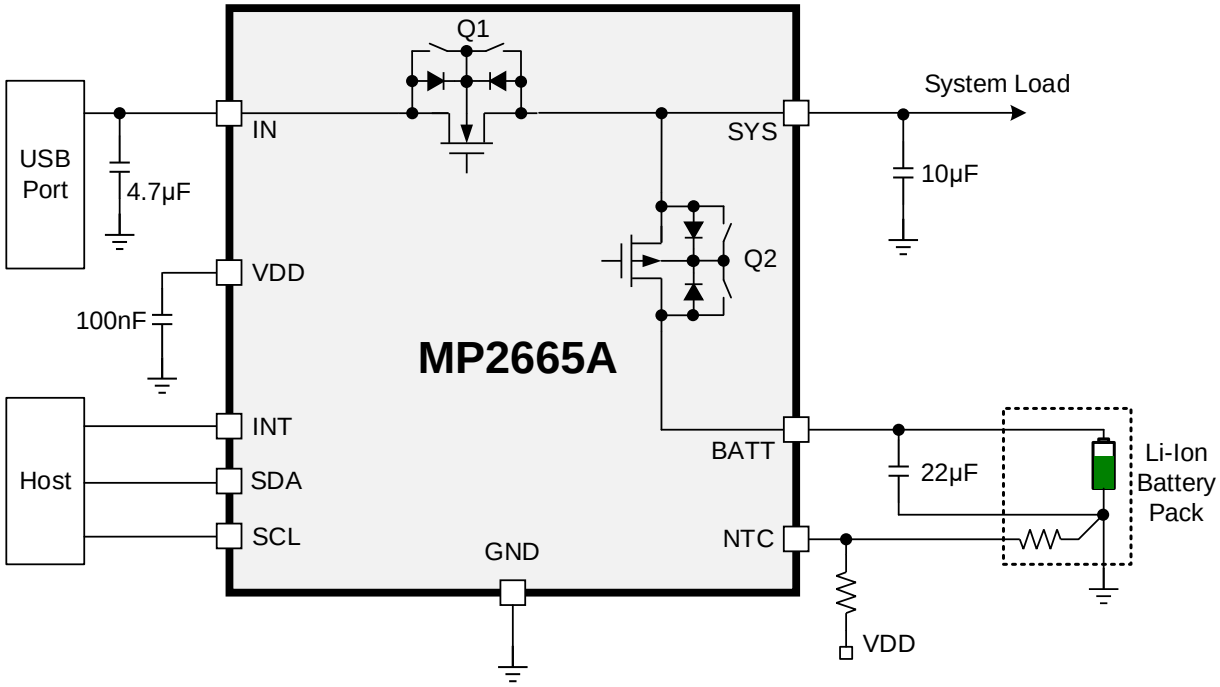
APPLICATIONS

- Wearable Devices
- Smart Handheld Devices
- Fitness Accessories
- Smartwatches

All MPS parts are lead-free, halogen-free, and adhere to the RoHS directive. For MPS green status, please visit the MPS website under Quality Assurance. “MPS”, the MPS logo, and “Simple, Easy Solutions” are trademarks of Monolithic Power Systems, Inc. or its subsidiaries.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

TYPICAL APPLICATION



MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MP2665AGQB-xxxx**	QFN-12 (2.5mmx3mm)	*See Below*	1
EVKT-MP2665A	Evaluation kit	-	

* For Tape & Reel, add suffix -Z (e.g. MP2665AGQB-xxxx-Z).

** "-xxxx" is the register setting option. The factory default is "-0000." This content can be viewed in the I²C register map. Contact an MPS FAE to obtain an "-xxxx" value.

TOP MARKING

BXJ
YWW
LLL

BXJ: Product code of MP2665AGQB
Y: Year code
WW: Week code
LLL: Lot number

EVALUATION KIT EVKT-MP2665A

EVKT-MP2665A kit contents (items below can be ordered separately):

#	Part Number	Item	Quantity
1	EV2665A-QB-00A	MP2665A evaluation board	1
2	EVKT-USBI2C-02-BAG	Includes one USB to I²C communication interface, one USB cable, and one ribbon cable	1
3	Online resources	Include datasheet, user guide, product brief, and GUI	1

Order directly from MonolithicPower.com or our distributors.

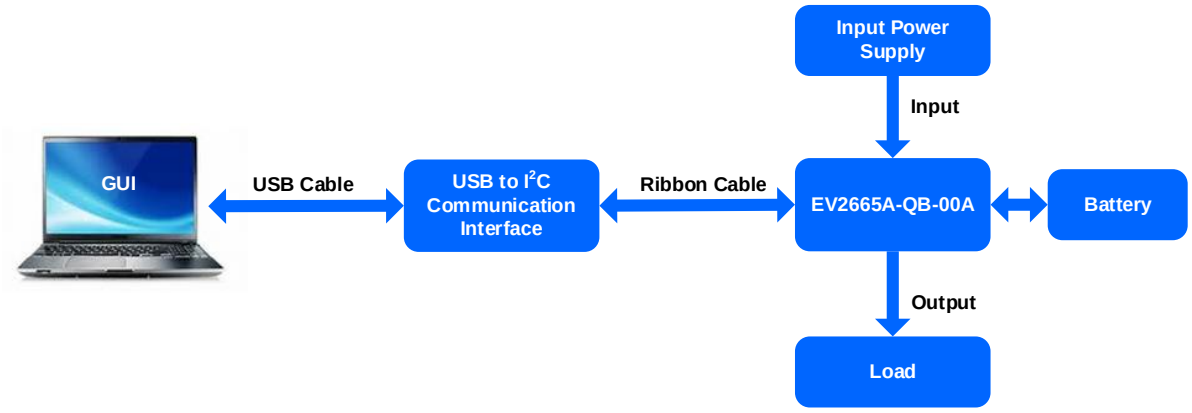
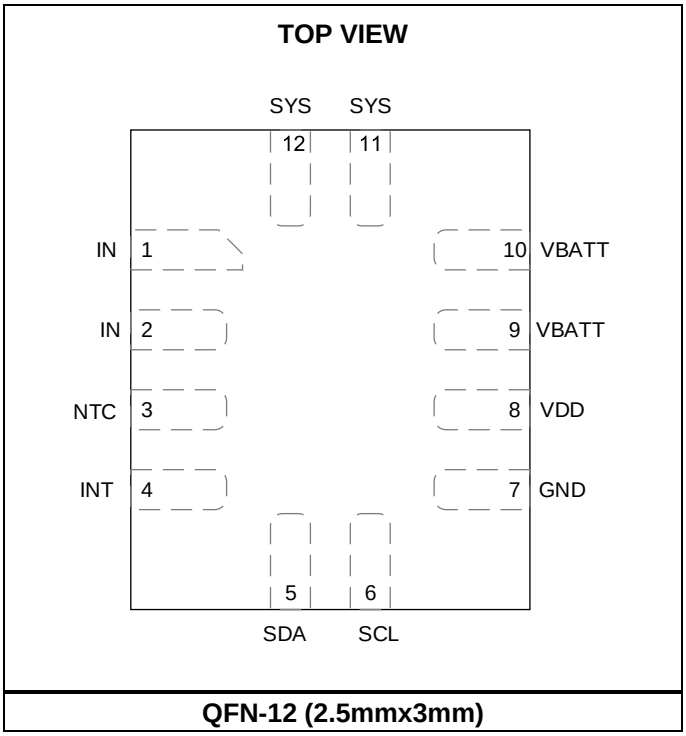


Figure 1: EVKT-MP2665A Evaluation Kit Set-Up

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

PACKAGE REFERENCE



QFN-12 (2.5mmx3mm)

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

PIN FUNCTIONS

Pin #	Name	I/O (1)	Description
1, 2	IN	P	**Input power pin.** Place a ceramic capacitor from IN to GND, as close as possible to the IC.
3	NTC	AI	**Temperature-sense input.** Connect a negative temperature coefficient thermistor to the NTC pin. Configure the hot and cold temperature thresholds with a resistor divider connected from VDD to NTC to GND. Charging is suspended when the NTC pin is out of range.
4	INT	AIO	**Interrupt signal.** INT can send a charging status and fault interrupt signal to the host. INT is also used to disconnect the system from the battery. If INT is pulled low for longer than t_{RST_DGL} (about 16s), the battery FET turns off and turns on again automatically after t_{RST_DUR} (about 4s), regardless of the INT state. Both t_{RST_DGL} and t_{RST_DUR} can be configured via the I²C interface.
5	SDA	DIO	**I²C interface data.** Connect SDA to the logic rail through a 10kΩ resistor.
6	SCL	DI	**I²C interface clock.** Connect SCL to the logic rail through a 10kΩ resistor.
7	GND	P	**Ground.**
8	VDD	P	**Internal control power supply pin.** Connect a 100nF ceramic capacitor from the VDD pin to GND. No external load is allowed.
9, 10	BATT	P	**Battery pin.** Place a ceramic capacitor from BATT to GND, as close as possible to the IC.
11, 12	SYS	P	**System power supply.** Place a ceramic capacitor from SYS to GND, as close as possible to the IC.

Note:

1) AI = analog input, AIO = analog input/output, DI = digital input, DIO = digital input/output, P = power.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

ABSOLUTE MAXIMUM RATINGS (2)

IN .....-0.3V to +21V
BATT to GND.....-0.3V to +6.0V
SYS to GND....-0.3V to +5.3V (+5.5V for 500µs)
All other pins to GND .....-0.3V to +5.2V
Continuous power dissipation (T_A = 25°C) (3) 1.67W
Junction temperature .....150°C
Lead temperature (solder) .....260°C
Storage temperature..... -65°C to +150°C

ESD Ratings

Human body model (HBM) 2000V
Charged device model (CDM).....750V

Recommended Operating Conditions (4)

Supply voltage (V_{IN})...4.35V to 5.5V (USB Input)
I_{IN}.....Up to 1A
I_{DSCHG}.....Up to 3.2A (5)
I_{CC}.....Up to 896mA
V_{BATT_REG} .....Up to 4.545V
Operating junction temp (T_J).... -40°C to +125°C

Thermal Resistance (6) θ_{JA} θ_{JC}

QFN-12 (2.5mmx3mm)..... 60 ..... 13....°C/W

Notes:

2) Exceeding these ratings may damage the device.
3) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can cause excessive die temperature, and the device may go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
4) The device is not guaranteed to function outside of its operating conditions.
5) Guaranteed by design.
6) Measured on JESD51-7, 4-layer PCB.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

ELECTRICAL CHARACTERISTICS

V_{IN} = 5.0V, V_{BATT} = 3.5V, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Input Source and Battery Protection						
Input under-voltage lock-out threshold	V_{IN_UVLO}	Input falling	3.6	3.7	3.8	V
Input under-voltage lock-out threshold hysteresis		Input rising		170		mV
Input over-voltage protection threshold	V_{IN_OVP}	Input rising threshold	6.1	6.4	6.7	V
Input over-voltage protection threshold hysteresis				350		mV
Input vs. battery voltage headroom threshold	V_{HDRM}	Input rising vs. battery	80	120	160	mV
Input vs. battery voltage headroom threshold hysteresis				85		mV
Battery under-voltage lockout threshold	V_{BATT_UVLO}	BATT voltage falling, REG01h, bits[2:0] = 000	2.2	2.4	2.6	V
		BATT voltage falling, REG01h, bits[2:0] = 100	2.6	2.76	2.92	
		BATT voltage falling, REG01h, bits[2:0] = 111	2.9	3.03	3.2	
BATT under voltage threshold hysteresis		V_{BATT_UVLO} = 2.76V		210		mV
Battery over-voltage protection threshold	V_{BATT_OVP}	Rising, higher than V_{BATT_REG}		110		mV
Battery over-voltage protection hysteresis				50		
Power Path Management						
Regulated system output voltage accuracy	$V_{SYS_REG_ACC}$	V_{IN} = 5.5V, R_{SYS} = 100Ω, I_{BATT} = 0A, REG07h, bits[3:0] = 0000, V_{SYS_REG} = 4.2V	-2		+2	%
		V_{IN} = 5.5V, R_{SYS} = 100Ω, I_{BATT} = 0A, REG07h, bits[3:0] = 0010, V_{SYS_REG} = 4.3V	-2		+2	%
		V_{IN} = 5.5V, R_{SYS} = 100Ω, I_{BATT} = 0A, REG07h, bits[3:0] = 1001, V_{SYS_REG} = 4.65V	-2		+2	%
		V_{IN} = 5.5V, R_{SYS} = 100Ω, I_{BATT} = 0A, REG07h, bits[3:0] = 1111, V_{SYS_REG} = 4.95V	-2		+2	%
Input current limit	I_{IN_LIM}	REG00h, bits[3:0] = 0000, I_{IN_LIM} = 50mA	30	40	50	mA
		REG00h, bits[3:0] = 0011, I_{IN_LIM} = 140mA	112	126	140	
		REG00h, bits[3:0] = 0110, I_{IN_LIM} = 460mA	420	440	460	
		REG00h, bits[3:0] = 1110 ,I_{IN_LIM} = 940mA	840	890	940	
		REG00h, bits[3:0] = 1111, I_{IN_LIM} = 1000mA	900	950	1000	

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 5.0V, V_{BATT} = 3.5V, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Input minimum voltage regulation	V_{IN_MIN}	REG00h, bits[7:4] = 0000, V_{IN_MIN} = 3.88V	3.6	3.88	4.2	V
		REG00h, bits[7:4] = 0110, V_{IN_MIN} = 4.36V	4.1	4.36	4.7	
		REG00h, bits[7:4] = 1001, V_{IN_MIN} = 4.60V	4.3	4.6	4.9	
		REG00h, bits[7:4] = 1111, V_{IN_MIN} = 5.08V	4.8	5.08	5.4	
IN to SYS switch on resistance	R_{ON_Q1}	V_{IN} = 4.5V, I_{SYS} = 100mA		290		mΩ
Input quiescent current	I_{IN_Q}	V_{IN} = 5.1V, EN_HIZ = 0, CEB = 0, charging enabled, I_{BATT} = 0A, I_{SYS} = 0A		1.8		mA
		V_{IN} = 5.1V, EN_HIZ = 0, CEB = 1, charging disabled, I_{BATT} = 0A, I_{SYS} = 0A		1.6		
Input suspend current	I_{IN_SUSP}	V_{IN} = 5.5V, EN_HIZ = 1, CEB = 0, charging enabled		0.7	1.5	mA
Battery quiescent current	I_{BATT_Q}	V_{IN} = 5V, CEB = 0, I_{SYS} = 0A, charging done, V_{BATT} = 4.35V		43		µA
		V_{IN} = GND, CEB = 1, I_{SYS} = 0A, V_{BATT} = 4.35V, disable the PCB OTP function, not including the current from the external NTC resistor		6.5	8	
		V_{IN} = GND, CEB = 1, I_{SYS} = 0A, V_{BATT} = 4.35V, enable PCB OTP function, not include the current from external NTC resistor		14	21	
		V_{IN} = GND, CEB = 1, I_{SYS} = 0A, V_{BATT} = 4.35V, enable PCB OTP function, not include the current from external NTC resistor, enable watchdog		22.5		
		V_{BATT} = 4.5V, V_{IN} = V_{SYS} = GND, FET_DIS = 1, shipping mode			350	nA
Battery FET on resistance	R_{ON_Q2}	V_{IN} = GND, V_{BATT} = 3.5V, I_{SYS} = 100mA		100		mΩ
Battery FET discharge current limit	I_{DSCHG}	REG03h, bits[7:4] = 0001, I_{DSCHG} = 400mA		480		mA
		REG03h, bits[7:4] = 1001, I_{DSCHG} = 2000mA		2000 (7)		
		REG03h, bits[7:4] = 1111, I_{DSCHG} = 3200mA		3200 (7)		
SYS reverse to BATT switch leakage		V_{SYS} = 4.65V, V_{IN} = 5V, V_{BATT} = GND, EN_HIZ = 1, CEB = 1, charging disabled			1	µA
Ideal diode forward voltage in supplement mode	V_{FWD}	50mA discharge current		28.5		mV
Shipping mode						
Enter shipping mode deglitch time	t_{SMEN_DGL}	REG06h, bit[5] is set from 0 to 1, REG09h, bits[7:6] = 00		1		s
Exit shipping mode by INT or V_{IN} plug in	t_{SMEX_DGL}	INT is pulled low		2		s

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 5.0V, V_{BATT} = 3.5V, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Auto-Reset Mode						
Reset by INT	t_{RST_DGL}	REG01h, bits[7:6] = 00		8		s
		REG01h, bits[7:6] = 10		16		
Battery FET off lasting time	t_{RST_DUR}	REG01h, bit[5] = 0		2		s
		REG01h, bit[5] = 1		4		
Battery Charger						
Battery charge voltage regulation	V_{BATT_REG}	REG04h, bits[7:2] = 000000, V_{BATT_REG} = 3.6V	3.582	3.6	3.618	V
		REG04h, bits[7:2] = 101000, V_{BATT_REG} = 4.2V	4.179	4.2	4.221	
		REG04h, bits[7:2] = 110010, V_{BATT_REG} = 4.38V	4.358	4.38	4.4	
		REG04h, bits[7:2] = 111110, V_{BATT_REG} = 4.53V	4.522	4.53	4.568	
Fast charge current	I_{CC}	REG02h, bits[5:0] = 000000, I_{CC} = 16mA	12.5	15.5	18.5	mA
		REG02h, bits[5:0] = 001011, I_{CC} = 168mA	139	160	181	
		REG02h, bits[5:0] =001111, I_{CC} = 224mA	193	216	239	
		REG02h, bits[5:0] =100011, I_{CC} = 504mA	467	504	536	
		REG02h, bits[5:0] =110001, I_{CC} = 700mA	654	704	754	
		REG02h, bits[5:0] = 111111, I_{CC} = 896mA	790	900	1000	
Pre-charge current	I_{PRE}	I_{PRE} = I_{TERM}	2.5		62	mA
Charge termination current threshold	I_{TERM}	REG03h, bits[3:0] = 0000, I_{TERM} = 2.5mA	1.5	2.5	3.5	mA
		REG03h, bits[3:0] = 0001, I_{TERM} = 7.5mA	6	7.5	9	
		REG03h, bits[3:0] = 0101, I_{TERM} = 22mA	20	22	24	
		REG03h, bits[3:0] = 1111, I_{TERM} = 62mA	56	62	70	
Termination deglitch time	t_{TERM_DGL}			3.2		s
Pre-charge to fast charge threshold	V_{BATT_PRE}	V_{BATT} rising, REG04h, bit[1] = 1, V_{BATT_PRE} = 3.0V	2.9	3.0	3.1	V
Pre-charge to fast charge threshold hysteresis				90		mV
Battery automatic recharge voltage threshold	V_{RECH}	Below V_{BATT_REG}, REG04h, bit[0] = 0	60	100	140	mV
		Below V_{BATT_REG}, REG04h, bit[0] = 1	145	200	245	
Battery automatic recharge deglitch time	t_{RECH_DGL}			200		ms

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 5V, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Thermal						
Junction temperature regulation (7)	T_{J_REG}	Thermal regulation threshold REG07h, bits[5:4] = 11 (120°C)		120		°C
Thermal shutdown threshold (7)	T_{J_SHDN}			150		°C
Thermal shutdown hysteresis (7)				20		°C
NTC pin output current	I_{NTC}	CEB = 0, NTC = 3V	-1	0	+1	µA
NTC cold temp rising threshold	V_{COLD}	As a percentage of V_{DD}	63	65	68	%
NTC cold temp rising threshold hysteresis				55		mV
NTC hot temp falling threshold	V_{HOT}	As a percentage of V_{DD}	31	33	35	%
NTC hot temp falling threshold hysteresis				70		mV
NTC hot temp falling threshold for PCB OTP	V_{HOT_PCB}	As a percentage of V_{DD}	30	33	35	%
NTC hot temp falling threshold hysteresis for PCB OTP				85		mV
Logic I/O Pin Characteristics						
Low logic voltage threshold	V_L				0.4	V
High logic voltage threshold	V_H		1.3			V
I²C Interface (SDA, SCL)						
Input high threshold level	V_{IL}	V_{PULL_UP} = 1.8V, SDA and SCL	1.3			V
Input low threshold level	V_{IH}	V_{PULL_UP} = 1.8V, SDA and SCL			0.4	V
Output low threshold level	V_{OL}	I_{SINK} = 5mA			0.4	V
I²C clock frequency	f_{SCL}				400	kHz
Clock Frequency and Watchdog Timer						
Clock frequency	f_{CLK}			131		kHz
Watchdog timer	t_{WDT}	REG05h, bits[6:5] = 11		160		s

Note:

7) Guaranteed by design

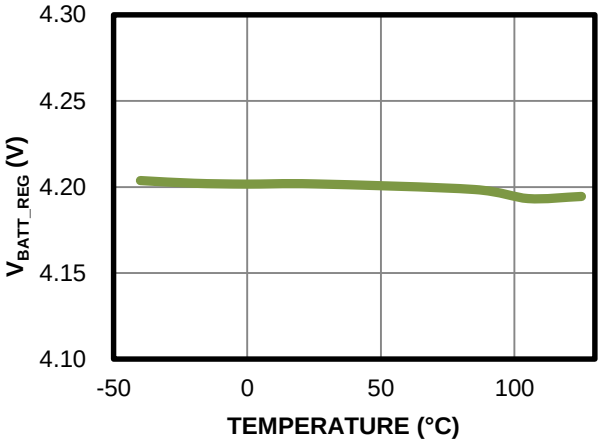
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 5V, T_A = 25°C, I_{IN_LIM} = 940mA, I_{CC} = 224mA, V_{IN_MIN} = 4.36V, V_{SYS_REG} = 4.65V, unless otherwise noted.

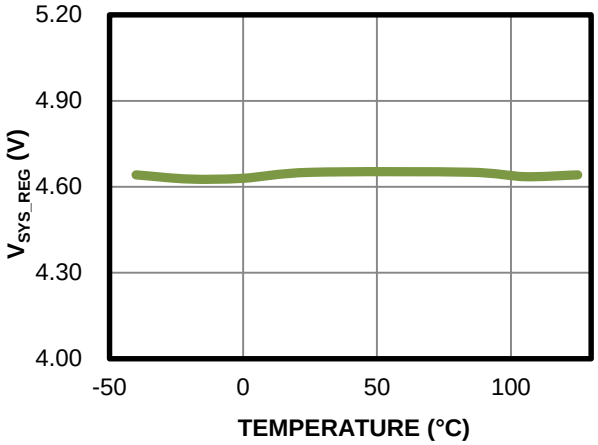
Battery Regulation Voltage vs. Temperature

V_{BATT_REG} = 4.2V

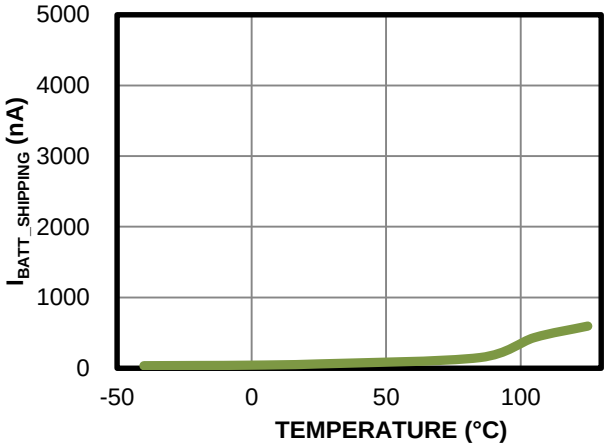


System Regulation Voltage vs. Temperature

V_{SYS_REG} = 4.65V

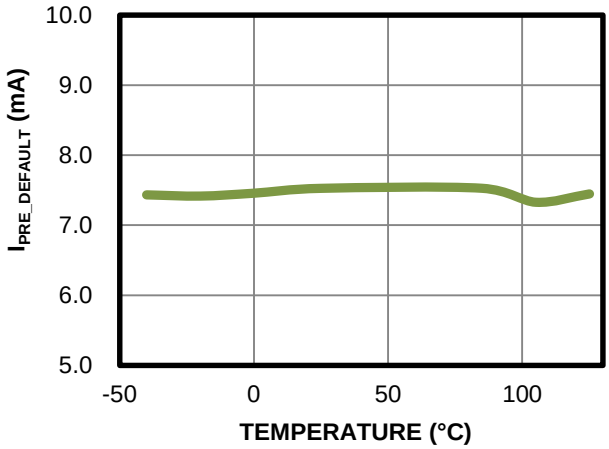


Battery Current under Shipping Mode vs. Temperature



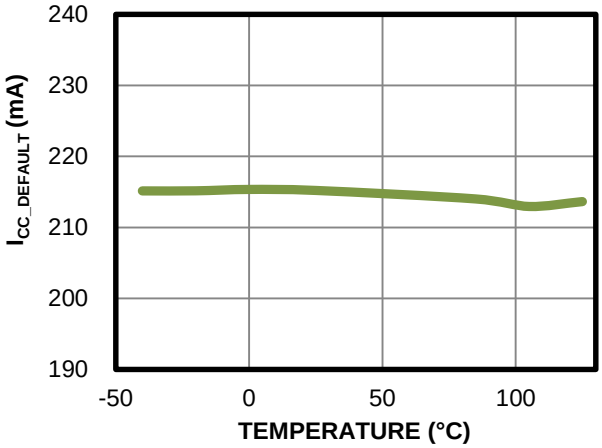
Pre-Charge Current vs. Temperature

I_{PRE} = 7.5mA



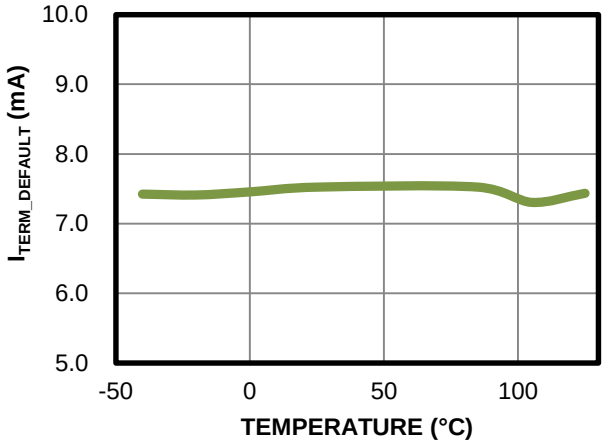
Fast Charge Current vs. Temperature

I_{CC} = 224mA



Battery Termination Current vs. Temperature

I_{TERM} = 7.5mA

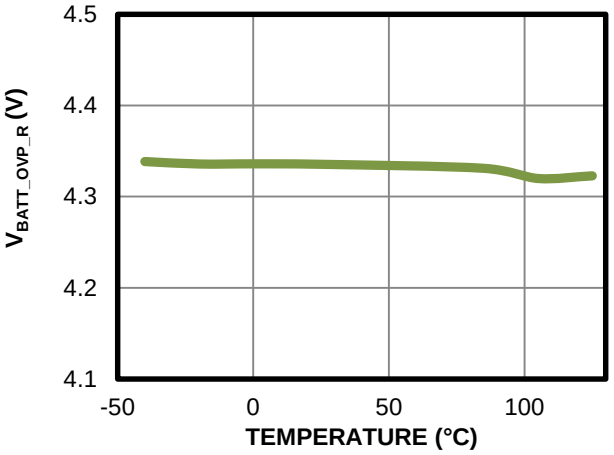


MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

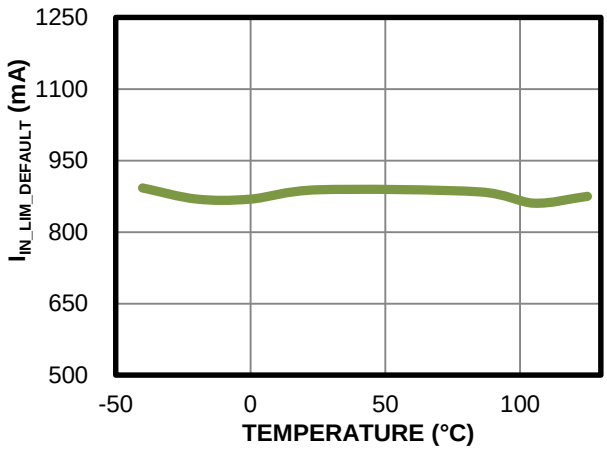
V_{IN} = 5V, T_A = 25°C, I_{IN_LIM} = 940mA, I_{CC} = 224mA, V_{IN_MIN} = 4.36V, V_{SYS_REG} = 4.65V, unless otherwise noted.

Battery OVP Voltage vs. Temperature



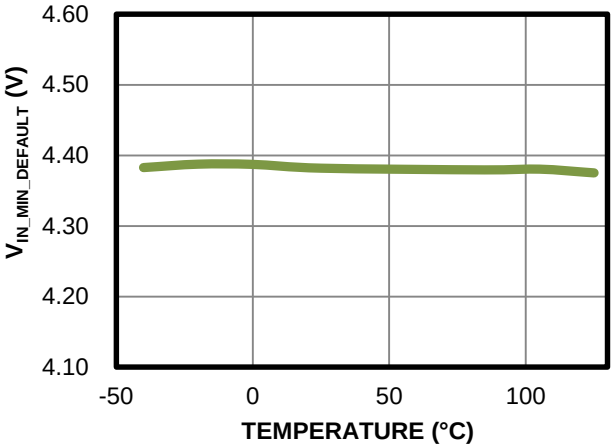
Input Current Limit vs. Temperature

I_{IN_LIM} = 940mA



Input Minimum Voltage vs. Temperature

V_{IN_MIN} = 4.36V



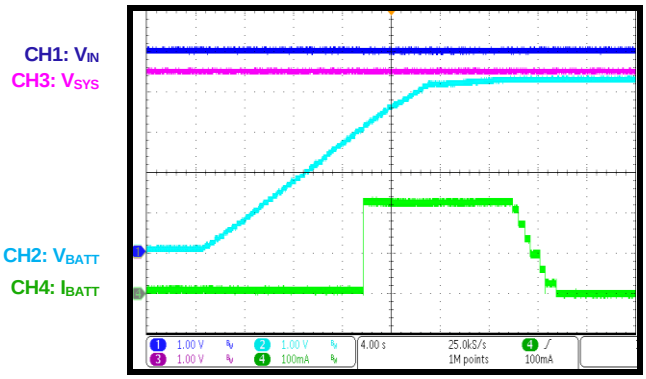
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, T_A = 25°C, I_{IN_LIM} = 460mA, I_{CC} = 224mA, V_{IN_MIN} = 4.36V, V_{SYS_REG} = 4.65V, unless otherwise noted.

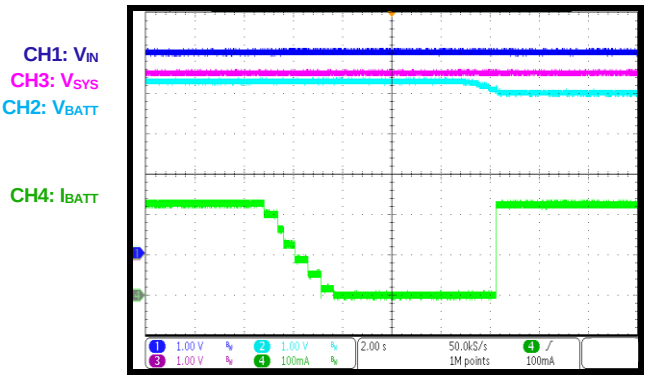
Battery Charge Curve

V_{SYS_REG} = 4.5V, I_{SYS} = 0A



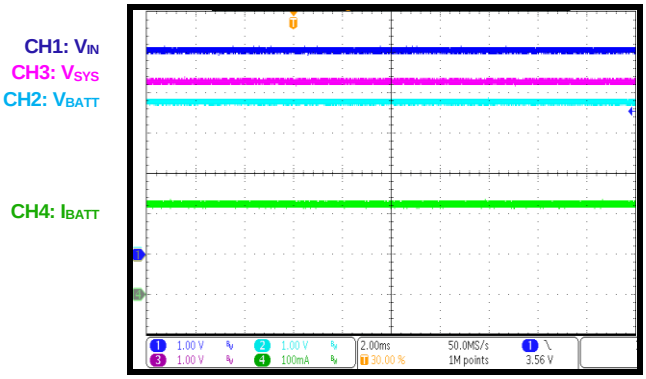
Automatic Recharge

V_{SYS_REG} = 4.5V, I_{SYS} = 0A



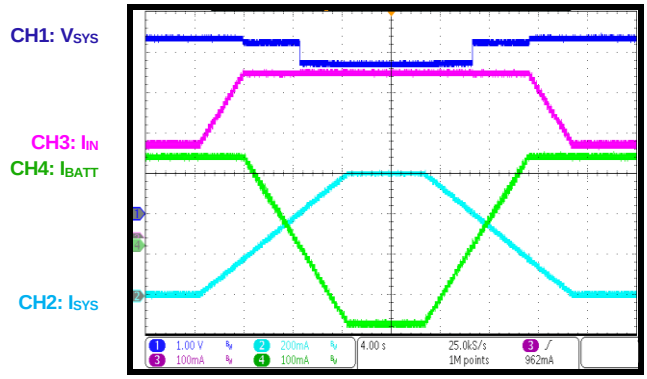
CC Charge Steady State

V_{BATT} = 3.7V, I_{SYS} = 0A



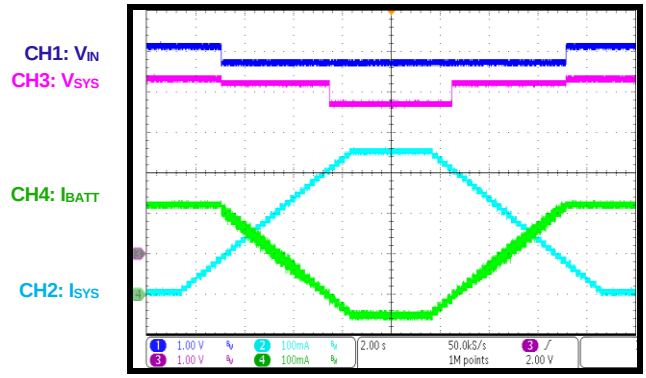
Input Current-Limit based PPM

V_{BATT} = 3.7V



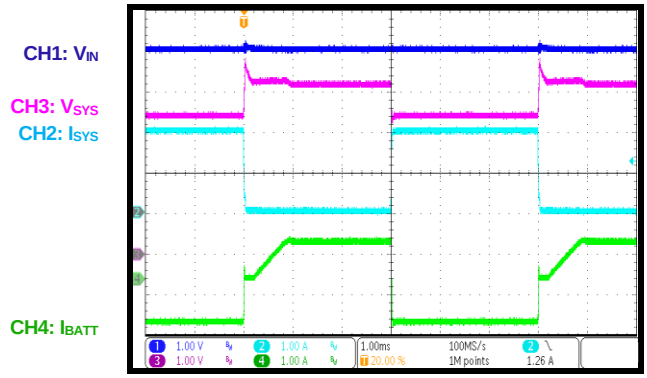
Input Voltage Regulation based PPM

V_{IN_MIN} = 4.6V, V_{IN} = 5V/300mA, V_{BATT} = 3.7V



SYS Load Transient Response

I_{IN_LIM} = 1A, I_{CC} = 896mA, V_{IN} = 5V, V_{BATT} = 3.7V, I_{SYS} = 0A to 2A



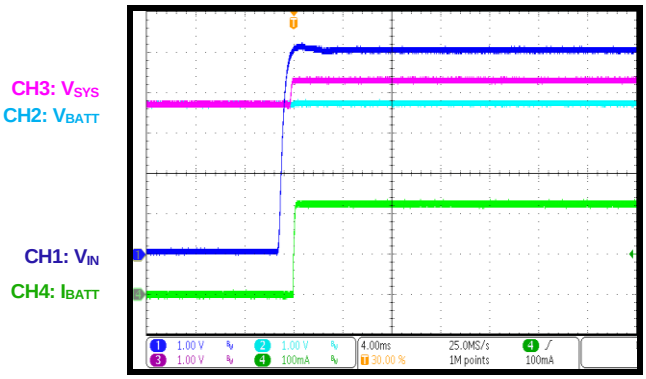
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, T_A = 25°C, I_{IN_LIM} = 460mA, I_{CC} = 224mA, V_{IN_MIN} = 4.36V, V_{SYS_REG} = 4.65V, unless otherwise noted.

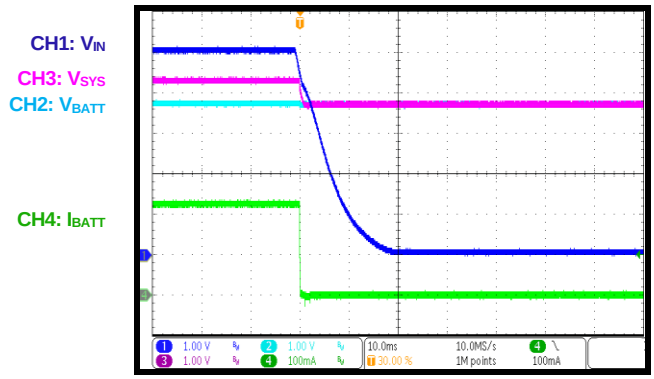
Start-Up

V_{BATT} = 3.7V, I_{SYS} = 0A



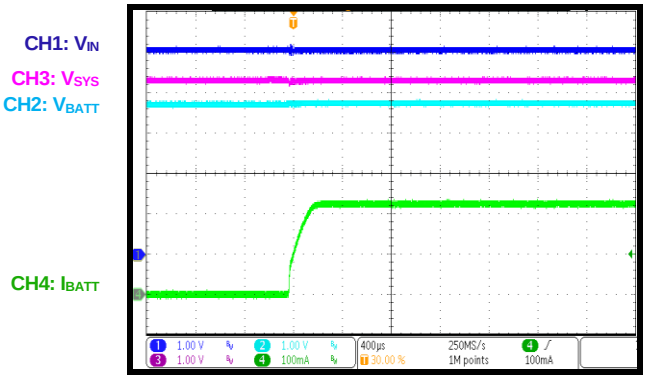
Shutdown

V_{BATT} = 3.7V, I_{SYS} = 0A



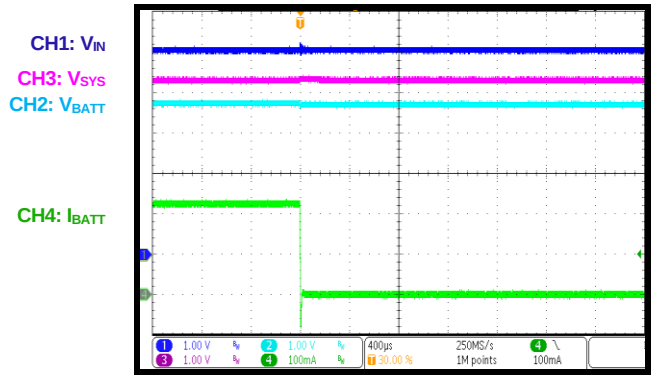
Charging Enabled

V_{BATT} = 3.7V, I_{SYS} = 0A



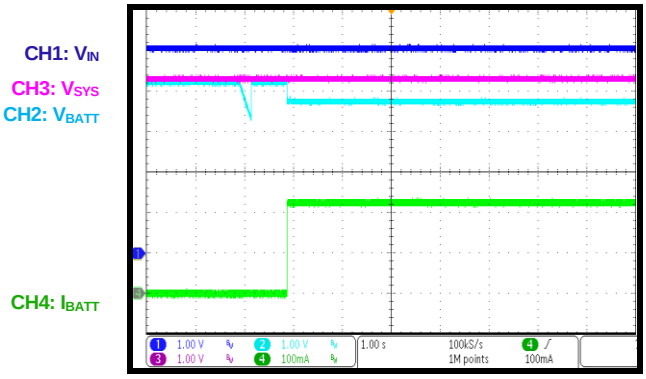
Charging Disabled

V_{BATT} = 3.7V, I_{SYS} = 0A



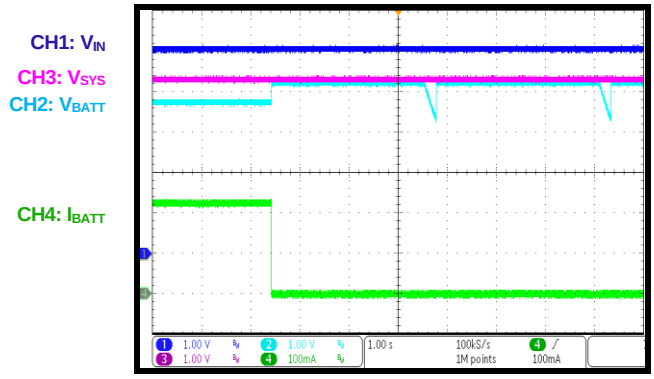
BATT Insertion

V_{BATT} = 3.7V, I_{SYS} = 0A



BATT Removal

V_{BATT} = 3.7V, I_{SYS} = 0A



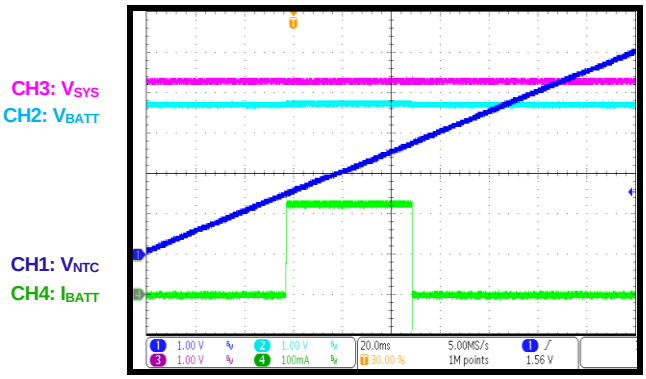
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, T_A = 25°C, I_{IN_LIM} = 460mA, I_{CC} = 224mA, V_{IN_MIN} = 4.36V, V_{SYS_REG} = 4.65V, unless otherwise noted.

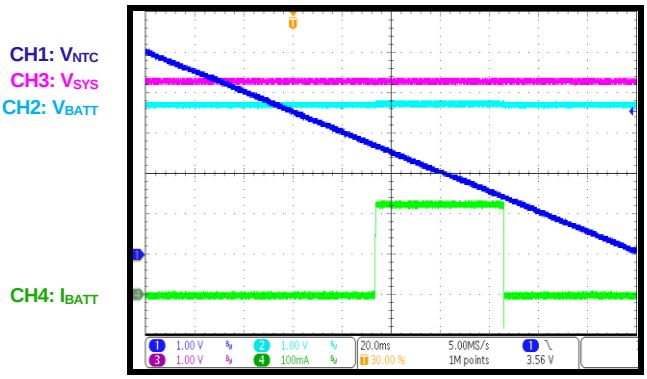
NTC Rising

V_{BATT} = 3.7V, I_{SYS} = 0A, PCB OTP disabled



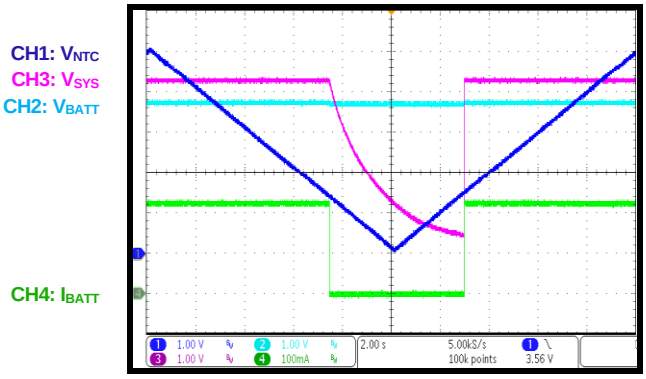
NTC Falling

V_{BATT} = 3.7V, I_{SYS} = 0A, PCB OTP disabled



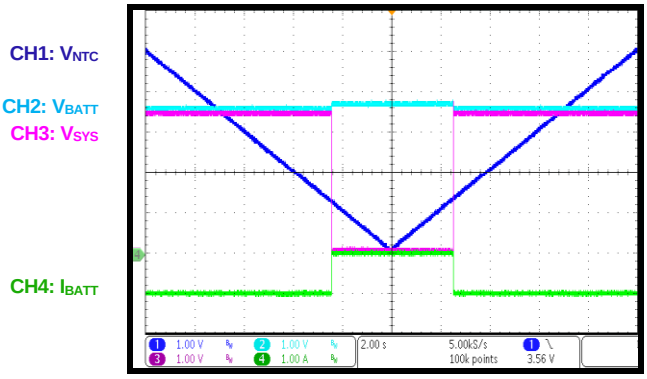
PCB OTP ing Charging Mode

V_{BATT} = 3.7V, I_{SYS} = 0A, PCB OTP enabled



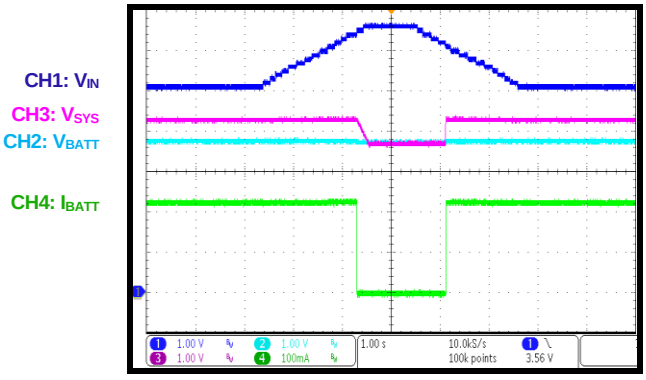
PCB OTP in Discharging Mode

V_{IN} = 0V, V_{BATT} = 3.7V, I_{SYS} = 1A, PCB OTP enabled



V_{IN} OVP Operation

V_{BATT} = 3.7V, I_{SYS} = 0A



MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

FUNCTIONAL BLOCK DIAGRAM

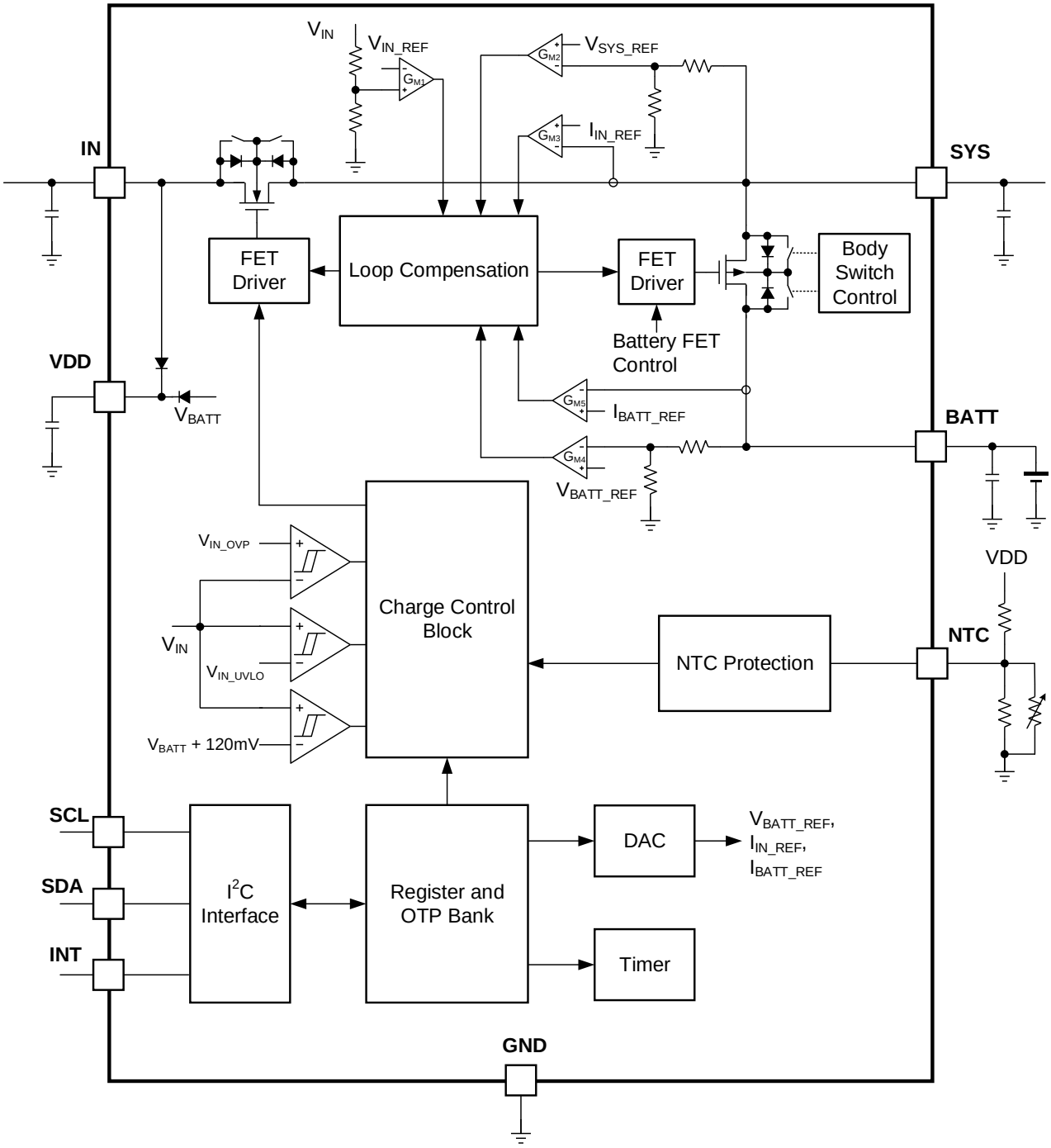


Figure 2: Functional Block Diagram

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

OPERATION

Introduction

The MP2665A is an I²C-controlled single-cell Li-ion or Li-polymer battery charger with complete power path management. The full charge function features constant current pre-charge (PRE.C), constant current (CC) fast charge, and constant voltage (CV) regulation, charge termination, automatic recharge, and a built-in timer. The power path function allows the input source to power the system and charge the battery simultaneously. The system load requirement always has priority over the charge current. When the input power is limited due to an input current limit or input voltage limit, the MP2665A automatically reduces the charge current until the battery supplements the system load.

The MP2665A integrates a 290mΩ LDO FET between the IN and SYS pins, and a 100mΩ battery FET between the SYS and BATT pins.

In charging mode, the on-chip, 100mΩ battery FET works as a full-featured linear charger with pre-charge, fast charge, CV charge, charge termination, automatic recharge, NTC monitoring, built-in timer control, and thermal protection. The charge current can be configured via the I²C interface. The MP2665A adjusts the charge current when the die temperature exceeds the thermal regulation threshold (about 120°C).

When the input power cannot power the system load in supplement mode, the 100mΩ battery FET turns on to connect the battery to the system load. When the input is removed, the 100mΩ battery FET fully turns on, so the battery can power up the system.

Once the system load is sufficient, the remaining current charges the smart power path management battery. When the demand exceeds the input power capacity, the MP2665A reduces the charging current or uses power from the battery to satisfy the system load.

Figure 3 shows the power path management structure.

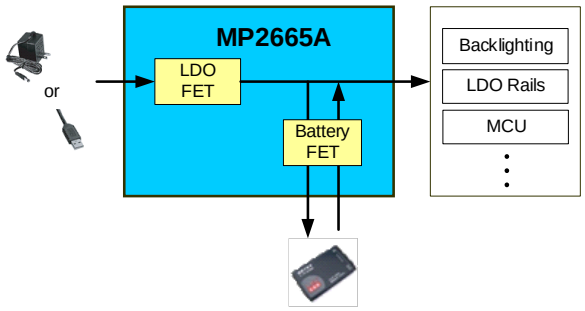


Figure 3: Power Path Management Structure

Power Supply

The internal bias circuit is powered from the higher voltage between the IN and BATT pins. When IN or BATT rise above their respective under-voltage lockout (UVLO) threshold, the sleep comparator, battery depletion comparator and the battery FET driver are active. Then the I²C interface is ready for communication, and all the registers are reset to the default value. The host can access all the registers at this point.

Input Over-Voltage Protection (OVP) and Under-Voltage Lockout (UVLO)

The MP2665A has an input over-voltage protection (OVP) threshold and input under-voltage lockout (UVLO) threshold. Once the input voltage (V_{IN}) rises above or drops below its normal range, the LDO FET (Q1) turns off immediately.

When V_{IN} is identified as a good source, a 200µs immunity timer activates. If the input power is good after 200µs, the system starts up. Otherwise, Q1 remains off.

Figure 4 shows the operation profile.

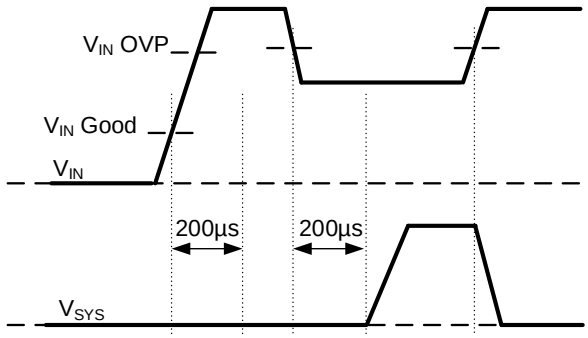


Figure 4: Input Power Detection Operation Profile

Figure 5 shows the battery charge profile.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

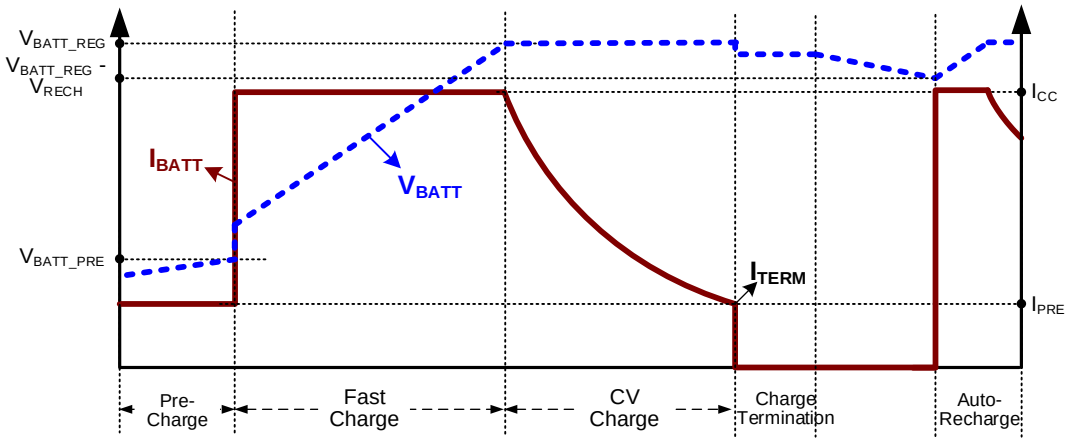


Figure 5: Battery Charge Profile

Power Path Management

The MP2665A employs a pass-through power path structure with the battery FET (Q2) by decoupling the system from the battery, which allows for separate control between the system and the battery. The system is given the priority to start up even with a deeply discharged or missing battery. This means that input power is available with a deeply depleted battery, and the system voltage is always regulated to V_{SYS_REG} by the integrated LDO FET.

Figure 2 on page 14 shows the direct power structure, which is comprised of a frond-end LDO FET between the IN and SYS pins, and a battery FET between the SYS and BATT pins. The LDO FET and battery FET can be controlled by I²C.

Table 1: FET Control via the I²C

FET On/Off Changed By Control	Hi-Z Mode and Charge Control	
	Set EN_HIZ to 1	Set CEB to 1
LDO FET	Off	x
Battery FET (charging)	x (8)	Off
Battery FET (discharging)	x	x

Note:

8) x means not applicable.

System voltage control is described in greater detail below:

- If the input voltage exceeds V_{SYS_REG}, the system voltage is regulated to V_{SYS_REG}.
- When the input voltage is below V_{SYS_REG}, the LDO FET is fully on with input current limiting.

V_{SYS_REG} can be configured through REG07h, bits[3:0].

Battery Charge Profile

The MP2665A provides three main charging phases: pre-charge, fast current charge, and constant voltage charge (see Figure 5).

Phase 1 (pre-charge): The MP2665A safely pre-charges the deeply depleted battery until the battery voltage reaches the pre-charge to fast charge threshold (V_{BATT_PRE}).

The pre-charge current can be configured through REG03h, bits[3:0]. If V_{BATT_PRE} is not reached before the pre-charge timer (2hrs) expires, the charge cycle ends, and a corresponding timeout fault signal asserts.

Phase 2 (fast charge): When the battery voltage exceeds V_{BATT_PRE}, the device enters a fast charge phase. The fast charge current can be configured via REG02h, bits[5:0].

Phase 3 (constant voltage charge): When the battery voltage rises to the battery full voltage (V_{BATT_REG}) set via REG04h, bits[7:2], the charge mode changes from constant current (CC) mode to constant voltage (CV) mode, and the charge current begins to decrease.

Assuming the termination function (EN_TERM) set via REG05h, bit[4] = 1, the charge cycle is considered to be complete when the following conditions are met:

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

- The charge current (I_{BATT}) reaches the termination current threshold (I_{TERM}), and a 3.2s delay timer is initiated.
- I_{BATT} is always below (I_{TERM} + I_{TERM_HYS}) during this 3.2s period.

The charge status is updated to charging done once the 3.2s delay timer expires.

The termination charge current (I_{TERM}) threshold can be configured by REG03h, bits[3:0].

The charge current is terminated if TERM_TMR set via REG05h, bit[0] = 0. Otherwise the charge current continues tapering off even after the charging status is changed to charging done.

If EN_TERM = 0, the termination function is disabled and all the above actions are invalid (see Table 2).

Table 2: Termination Function Selection

EN_TERM	TERM_TMR	3.2s After I_{BATT} Reaches I_{TERM} in CV Mode	
		Operation	Charge Status
0	x (9)	Charge in CV mode	Charge
1	0	Charging done	Charging done
1	1	Charge in CV mode	Charge Done

Note:

9) "x" means not applicable.

During the charging process, the actual charge current may be less than what is set by the register due to other loop regulations, such as dynamic power management (DPM) regulation (e.g. input voltage, input current), or thermal regulation. Termination does not occur if any of the above conditions are active (or if the device is operating in supplement mode).

A new charge cycle starts when the following conditions are valid:

- The input power is recycled
- Battery charging is enabled by the I²C
- Automatic recharge initiates
- No thermistor fault at NTC has occurred
- No safety timer fault has occurred
- No battery over-voltage event has occurred
- The battery FET is not forced to turn off

Automatic Recharge

When the battery is fully charged and charging is terminated, the battery may be discharged due to system consumption or self-discharge. When the battery voltage is discharged below the recharge threshold, and V_{IN} is still in the operation range, the MP2665A automatically starts a new charging cycle without manually restarting a charging cycle.

The automatic recharge function is enabled when EN_TERM = 1 and TERM_TMR = 0.

Battery Over-Voltage Protection (OVP)

The built-in battery over-voltage (OV) limit is about 110mV above V_{BATT_REG}. If a battery OV event occurs, the MP2665A immediately suspends charging and asserts a fault.

Input Current and Input Voltage Based Power Management

To meet the input source (typically a USB) maximum current limit specification, the MP2665A features input current based power management that continuously monitors the input current. The total input current limit can be configured via the I²C to prevent the input source from being overloaded.

If the preset input current limit exceeds the input source rating, the backup input voltage based power management also prevents the input source from being overloaded. If either the input current limit or the input voltage limit is reached, the FET (Q1) between IN and SYS is regulated such that the total input power is limited. As a result, the system voltage drops. Once the system voltage from to (V_{SYS_REG} - 135mV) and (V_{IN} - 295mV), the charge current is reduced to prevent the system voltage from dropping further.

The voltage based dynamic power management (DPM) regulates the input voltage to V_{IN_MIN} when the load exceeds the input power capacity.

Battery Supplement Mode

If DPM regulates the input voltage, the charge current drops to keep the input current or input voltage under regulation. If the charge current

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

drops to zero and the input source is still overloaded due to a heavy system load, the system voltage starts to decrease. Once the system voltage falls 30mV below the battery voltage, the MP2665A enters battery supplement mode, and ideal diode mode is enabled. The battery FET is regulated to maintain (V_{BATT} - V_{SYS}) at 28.5mV when the supplement current (I_{DSCHG} x R_{ON_BATT}) is lower than 28.5mV. If I_{DSCHG} x R_{ON_BATT} exceeds 28.5mV, the battery FET fully turns on. While the system load decreases, and V_{SYS} exceeds V_{BATT} + 20mV, ideal diode mode is disabled. Figure 6 shows the dynamic power management and battery supplement mode operation profile.

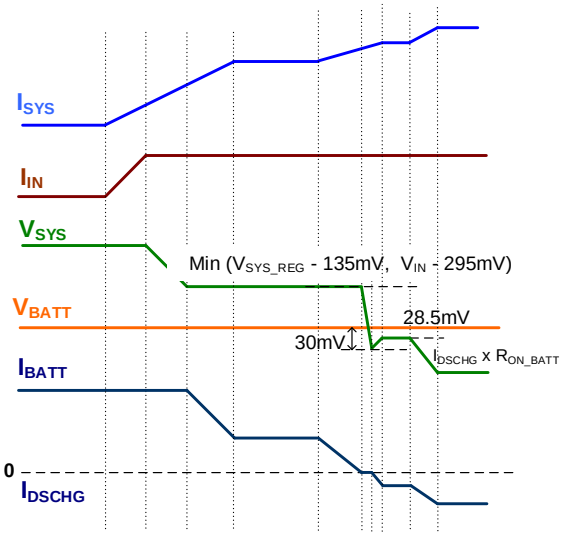


Figure 6: Dynamic Power Management and Battery Supplement Operation Profile

When the input voltage is not available, the MP2665A operates in discharge mode. In discharge mode, the battery FET is always fully on to reduce power loss.

Battery Regulation Voltage

The battery voltage for the constant voltage regulation phase is V_{BATT_REG}. When battery is floating, the BATT pin voltage varies between (V_{BATT_REG} - V_{RECH}) and V_{BATT_REG}.

Thermal Regulation and Thermal Shutdown

The MP2665A continuously monitors the internal junction temperature to maximize power delivery and avoid overheating the chip. When the internal junction temperature reaches the preset limit of T_{J_REG} (about 120°C), the IC starts to reduce the charge current to prevent higher power dissipation. The multiple thermal regulation thresholds (from 60°C to 120°C) help the system design meet the thermal requirements for different applications. The junction temperature regulation threshold can be set via REG07h, bits[5:4].

If the junction temperature reaches 150°C, both Q1 and Q2 turn off.

NTC (Negative Temperature Coefficient) Temperature Sensor

The NTC pin allows the MP2665A to sense the battery temperature using the thermistor (typically available in the battery pack) to ensure that the chip operates in a safe operating environment. An appropriate resistor should be connected from VDD to NTC, while the thermistor should be connected from NTC to ground. The voltage on the NTC pin is determined by the resistor divider, and the divide ratio depends on the temperature. The IC internally sets a pre-determined upper and lower bound on the divide ratio for the NTC cold and NTC hot thresholds.

The MP2665A is set to use the NTC function by default. This function can be changed via the I²C (see Table 3).

Table 3: NTC Function Selection

I²C Control		Function
EN_NTC	EN_PCB OTP	
0	x (10)	Disabled
1	1	NTC
1	0	PCB OTP

Note:

10) "x" means not applicable.

If PCB over-temperature protection (OTP) is selected, and the NTC pin voltage is below the NTC hot threshold, both the LDO FET and battery FET are off. A PCB OTP fault also sets the NTC_FAULT bit (REG09h, bit[1]) to 1 to indicate if a fault has occurred. Operation resumes once the NTC pin voltage exceeds the NTC hot threshold.

The NTC function only works in charge mode. Once the NTC pin voltage falls out of this divide ratio (meaning the temperature is outside the safe operating range), the MP2665A stops charging and reports the change on the status

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

bits. Charging automatically resumes after the temperature falls back into the safe range.

Safety Timer

The pre-charge and fast charge safety timer prevent extended charging cycles due to abnormal battery conditions. The safety timer is 2hrs when the battery voltage is below V_{BATT_PRE}. The fast charge safety timer starts when the battery enters fast charge. The fast charge safety timer can be configured and enabled through the I²C.

The following actions restart the safety timer:

- A new charge cycle is initiated
- Charge toggling is enabled
- Hi-Z toggling is disabled

Host Mode and Default Mode

The MP2665A is a host-controlled device. After power-on reset (POR), the device starts in the watchdog timer expiration state or default mode. All the registers are in their default settings.

The watchdog timer works in both charge and discharge mode. The register returns to its default value when the watchdog timer runs out. When the watchdog timer runs out in both charge and discharge mode, the system is reset.

To save the quiescent current in discharge mode, the watchdog timer can be turned off during discharge mode by setting REG05h, bit[7] to 0.

Any write to the MP2665A transits the device to host mode. All the charge parameters are configurable. If the watchdog timer (REG05h, bits[6:5]) is not disabled, the host has to reset the watchdog timer regularly by writing 1 to REG02h, bit[6] before the watchdog timer expires to keep the device in host mode. Once the watchdog timer expires, the IC goes back to default mode. The watchdog timer limit can also be configured or disabled via host control.

When REG05h, bits[6:5] is set to 00, the watchdog timer is disabled under both charge mode and discharge mode, regardless of what REG05h, bit[7] is set to.

The MP2665A can enter default mode if any of the following conditions are valid:

- The input is refreshed without a battery
- A battery is reinserted if there is no input voltage
- REG02h, bit[7] is reset

Battery Discharge Function

If a battery is connected and the input source is missing, the battery FET turns fully on when V_{BATT} exceeds the V_{BATT_UVLO} threshold. The 100mΩ battery FET minimizes conduction loss during discharge. The quiescent current is as low as 6.5μA in this mode. The low on resistance and quiescent current extend the battery's run time.

Over Discharge Current Protection

The MP655A provides over discharge current protection in discharge mode and supplement mode. If I_{DSCHG} exceeds the configurable discharge current limit (default at 3.2A), after a 60μs delay, the battery FET turns off and the part goes into hiccup mode due to over-current protection (OCP). The discharge current limit can be set high to 3.2A through the I²C. If the discharge current reaches the internal fixed current limit (about 3.7A), the battery FET turns off and starts hiccup mode immediately.

Similarly, when the battery voltage falls below the configurable V_{BATT_UVLO} threshold (about 2.76V by default), the battery FET turns off to prevent over discharge.

System Short-Circuit Protection (SCP)

The MP2665A features SYS node short-circuit protection for both the IN to SYS path and the BATT to SYS path.

The system voltage is continuously monitored. If V_{SYS} is below 1.5V, the system SCP for both the IN to SYS path and the BATT to SYS path are active. Meanwhile, I_{DSCHG} drops to 1/2 of the original value. The two paths are described in greater detail below:

1. IN to SYS path: Once I_{IN} exceeds the protection threshold, both the LDO FET and the battery FET turn off immediately, and the MP2665A enters hiccup mode. If the maximum current limit is not reached, but the set input current limit is reached, I_{IN} is regulated to I_{IN_LIM}, and hiccup mode starts

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

after a 60us delay. The interval for hiccup mode is 800µs.

2. BATT to SYS path: Once I_{BATT} exceeds the 3.7A protection threshold, both the LDO FET and the battery FET turn off immediately, and the MP2665A enters hiccup mode. If the battery discharge current limit threshold is reached, hiccup mode also starts after a 60µs delay. The interval for hiccup mode is 800µs.

For more details, see Figure 20 on page 37.

If a system short circuit occurs when both the input and battery are present, the protection mechanism for both paths work simultaneously, though the protection that is triggered first initiates hiccup mode.

Interrupt to Host (INT)

The MP2665A has an alert mechanism that can output an interrupt signal via the INT pin to notify the system of the operation by outputting a 256µs, low-state INT pulse. The below events trigger the INT output:

- Good input source detected (PG_STAT)
- Charging completed
- Charging status change
- Any fault in REG09h (e.g. watchdog timer fault, input fault, thermal fault, safety timer fault, battery over-voltage protection fault, NTC fault) has occurred

If a fault occurs, the device sends out an INT pulse and latches the fault state in REG09h. After the fault is removed, the fault bit can be released to 0 after the host reads REG09h. The NTC fault does not latch, and it always reports the current thermistor conditions.

The INT signal can be masked when the corresponding control bit is set. This means that INT can stay high even if a fault occurs. To mask the INT signal, set the INT control bit in REG06h, bits[4:0].

Battery Disconnection Function

In the application has a battery that cannot be removed, disconnect the battery from the system for shipping mode to allow the system power to be reset during the application. The MP2665A provides both shipping mode and system reset mode for different applications (see Table 4).

The MP2665A has a register bit (FET_DIS) for battery disconnection control. If this bit is set to 1, the MP2665A enters shipping mode after a delay time that can be configured by REG09h, bits[7:6]. The battery FET turns off and the FET_DIS bit is refreshed to 0 after the battery FET turns off. By pulling down the INT pin or plugging in the input adapter for 2s, the part can wake up from shipping mode.

Table 4: Shipping Mode Control

Items	Enter Shipping Mode	Exit Shipping Mode	
	Set FET_DIS to 1	INT High to Low for 2s	VIN Plug In
LDO FET	x (11)	x	On
Battery FET (charging)	Off (t_{SMEN_DGL} later)	On	On (2s later)
Battery FET (discharging)	Off (t_{SMEN_DGL} later)	On	On (2s later)

Note:

11) “x” means not applicable.

The IC can reuse the INT pin to cut off the path from the battery to manually reset the system. Once the logic on the INT pin is set low for more than t_{RST_DGL} (which can be configured by REG01h, bits[7:6]), the battery is disconnected from the system by turning off the battery FET. This off state lasts for t_{RST_DUR}, which can be configured by REG01h, bit[5]. Then the battery FET automatically turns on, and the system is powered by the battery again. During the off period, the INT pin is not limited to being either high or low.

The MP2665A can reset the system by controlling the INT pin. Figure 7 shows the system reset function.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

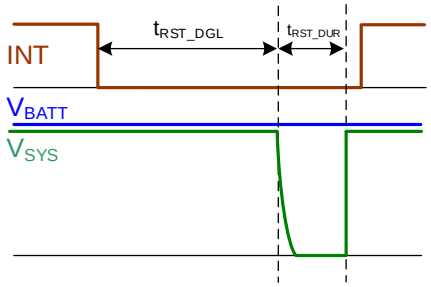


Figure 7: System Reset Function Operation Profile

SERIES INTERFACE

The IC uses an I²C-compatible interface for set the charging parameters and instantaneously report the device status. The I²C is a two-wire serial interface with two required bus lines: a serial data line (SDA) and a serial clock line (SCL). Both the SDA and SCL lines are open drains that must be connected to the positive supply voltage via a pull-up resistor.

The MP2665A operates as a slave device, receiving control inputs from the master device, such as a microcontroller (MCU). The SCL line is always driven by the master device. The I²C interface supports both standard mode (up to 100 kbit/s), and fast mode (up to 400 kbit/s).

All transactions begin with a start (S) condition and are terminated by a stop (P) condition. The start and stop conditions are always generated by the master. A high to low transition on the SDA line while SCL is high defines a start condition. A low to high transition on the SDA line when SCL is high defines a stop condition (see Figure 8).

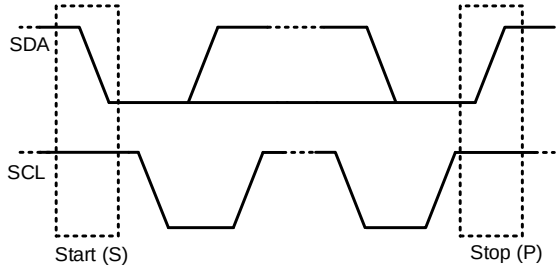


Figure 8: Start and Stop Conditions

For data validity, the data on the SDA line must be stable during the high period of the clock. The high or low state of the SDA line can only change when the clock signal on the SCL line is low. Every byte on the SDA line must be 8 bits long. The number of bytes that can be transmitted per transfer is unrestricted. Data is first transferred with the most significant bit (MSB) (see Figure 9).

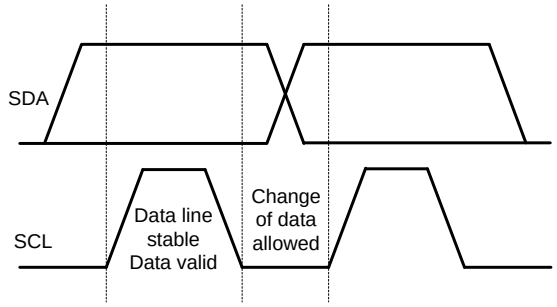


Figure 9: Bit Transfer on the I²C Bus

Each byte has to be followed by an acknowledge (ACK) bit that is generated by the receiver. The ACK bit signals to the transmitter that the byte was successfully received.

The ACK signal is defined as when the transmitter releases the SDA line during the acknowledge clock pulse. Then the receiver can pull the SDA line low, and the SDA line remains low during the high period of the ninth clock.

If the SDA line is high during the ninth clock, this is defined as a not acknowledge (NACK) signal. The master can then generate either a stop condition to abort the transfer, or a repeated start (Sr) condition to start a new transfer.

After the start signal is received, a slave address is sent. This address is 7 bits long, followed by the eighth data direction bit (R/W). A zero indicates a transmission (write), and a one indicates a request for data (read). Figure 10 shows the address bit arrangement.

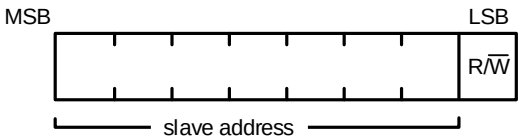


Figure 10: 7-Bit Address

Figure 11, Figure 12, Figure 13, Figure 14, and Figure 15 on page 22 show the detailed sequences.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

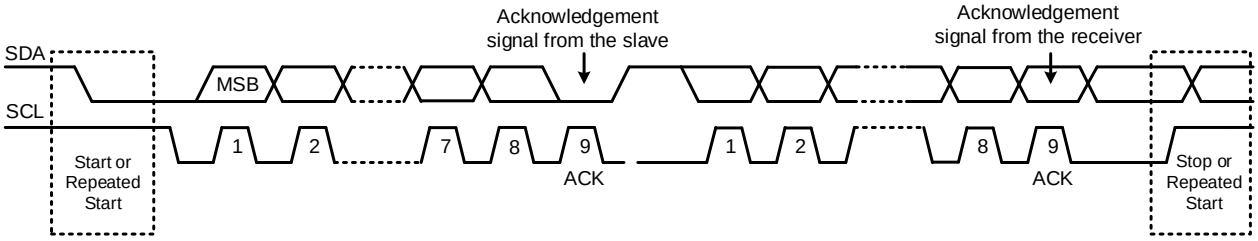


Figure 11: Data Transfer on the I²C Bus

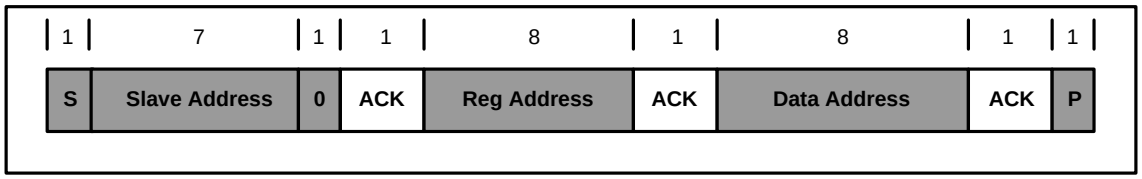


Figure 12: Single Write

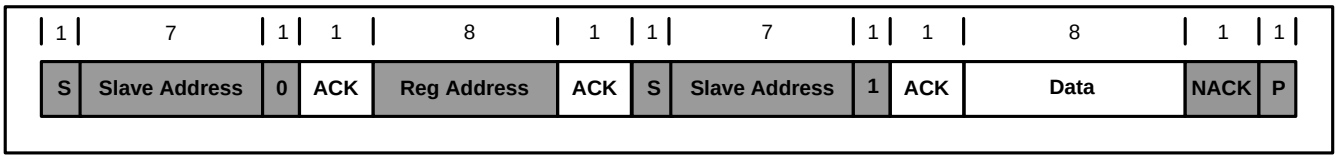


Figure 13: Single Read

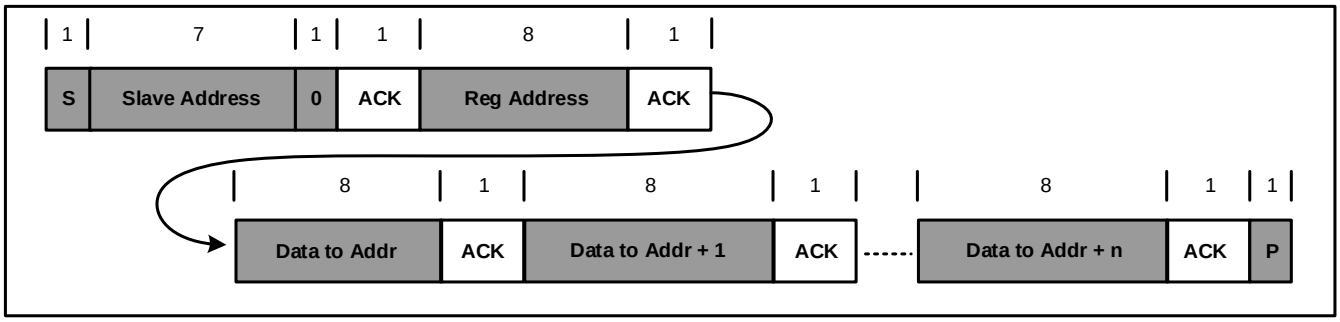


Figure 14: Multi-Write



Figure 15: Multi-Read

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

I²C REGISTER MAP

IC Address: REG08h (reserved certain trim options)

Register Name	Address	R/W	Description	Default
REG00h	0x00	R/W	Input source control register	0110 0110
REG01h	0x01	R/W	Power connection control register	1010 1100
REG02h	0x02	R/W	Charge current setting register	0000 1111
REG03h	0x03	R/W	Discharge/termination current limit setting register	1111 0001
REG04h	0x04	R/W	Charge termination voltage setting register	1010 0011
REG05h	0x05	R/W	Charge termination/timer control register	0011 1000
REG06h	0x06	R/W	Miscellaneous operation control register	1100 0000
REG07h	0x07	R/W	Thermal/system voltage regulation setting register	1011 1001
REG08h	0x08	R	Charge status register	0100 0000
REG09h	0x09	R/W	Fault register	0000 0000
REG0Ah	0x0A	N/A	Address for the one-time programmable (OTP) register	0000 0000

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

REG00h

Bits	Bit Name	POR	Reset by REG_RST	Reset by WTD	R/W	Description	Comments
7	V_{IN_MIN}[3]	0	Y	N	R/W	640mV	Offset: 3.88V Range: 3.88V to 5.08V Default: 0110 (4.36V)
6	V_{IN_MIN}[2]	1	Y	N	R/W	320mV	
5	V_{IN_MIN}[1]	1	Y	N	R/W	160mV	
4	V_{IN_MIN}[0]	0	Y	N	R/W	80mV	
3	I_{IN_LIM}[3]	1	Y	N	R/W	480mA	Sets the input current limit. If I_{IN_LIM} ≤ 170mA: Offset: 50mA Step: 30mA Range: 0000 to 0100 (50mA to 170mA) If I_{IN_LIM} > 170mA: Offset: 100mA Step: 60mA Range: 0101 to 1111 (400mA to 1000mA) Default: 1110 (940mA)
2	I_{IN_LIM}[2]	1	Y	N	R/W	120mA: I_{IN_LIM} ≤ 170mA 240mA: I_{IN_LIM} > 170mA	
1	I_{IN_LIM}[1]	1	Y	N	R/W	60mA: I_{IN_LIM} ≤ 170mA 120mA: I_{IN_LIM} > 170mA	
0	I_{IN_LIM}[0]	0	Y	N	R/W	30mA: I_{IN_LIM} ≤ 170mA 60mA: I_{IN_LIM} > 170mA	

REG01h

Bits	Bit Name	POR	Reset by REG_RST	Reset by WTD	R/W	Description	Comments
7	t_{RST_DGL}[1]	1	Y	Y	R/W	00: 8s 01: 12s 10: 16s 11: 20s	Sets how long the INT signal should be pulled low to disconnect the battery. Default: 10 (16s)
6	t_{RST_DGL}[0]	0	Y	Y	R/W		
5	t_{RST_DUR}	1	Y	Y	R/W	0: 2s 1: 4s	Battery FET lasts off time before auto-on Default: 1 (4s)
4	EN_HIZ (12)	0	Y	Y	R/W	0: Disabled 1: Enabled	Default: 0 (disabled)
3	CEB	1	Y	Y	R/W	0: Charge enabled 1: Charge disabled	Configures the charge. Default: 1 (charge disabled)
2	V_{BATT_UVLO}[2]	1	Y	Y	R/W	360mV	Sets the battery under-voltage lockout (UVLO) threshold. Offset: 2.4V Range: 2.4V to 3.03V Default: 100 (2.76V)
1	V_{BATT_UVLO}[1]	0	Y	Y	R/W	180mV	
0	V_{BATT_UVLO}[0]	0	Y	Y	R/W	90mV	

Note:

12) This bit only controls when the LDO FET turns on and off.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

REG02h

Bits	Bit Name	POR	Reset by REG_RST	Reset by WTD	R/W	Description	Comments
7	REGISTER_ RESET	0	Y	N	R/W	0: Keep the current setting 1: Reset	Default: 0 (keep the current setting)
6	I²C_ WATCHDOG_ TIMER_RESET	0	Y	Y	R/W	0: Normal 1: Reset	Default: 0 (normal)
5	I_{CC}[5]	0	Y	Y	R/W	448mA	Sets the fast charge current. If I_{CC} ≤ 80mA: Offset: 16mA Step: 16mA Range: 000000 to 000100 (16mA to 80mA) If I_{CC} > 80mA: Offset: 14mA Step: 14mA Range: 000101 to 111111 (84mA to 896mA) Default: 001111 (224mA)
4	I_{CC}[4]	0	Y	Y	R/W	224mA	
3	I_{CC}[3]	1	Y	Y	R/W	112mA	
2	I_{CC}[2]	1	Y	Y	R/W	64mA: I_{CC} ≤ 80mA 56mA: I_{CC} > 80mA	
1	I_{CC}[1]	1	Y	Y	R/W	32mA: I_{CC} ≤ 80mA 28mA: I_{CC} > 80mA	
0	I_{CC}[0]	1	Y	Y	R/W	16mA: I_{CC} ≤ 80mA 14mA: I_{CC} > 80mA	

REG 03h

Bits	Bit Name	POR	Reset by REG_RST	Reset by WTD	R/W	Description	Comments
7	I_{DSCHG}[3]	1	Y	Y	R/W	1600mA	Sets the BATT to SYS discharge current limit. Offset: 200mA Range: 400mA to 3.2A Valid range: 0001 to 1111 Default: 1111 (3200mA)
6	I_{DSCHG}[2]	1	Y	Y	R/W	800mA	
5	I_{DSCHG}[1]	1	Y	Y	R/W	400mA	
4	I_{DSCHG}[0]	1	Y	Y	R/W	200mA	
3	I_{TERM}[3]	0	Y	Y	R/W	32mA	Sets the termination current. If I_{TERM} ≤ 17.5mA: Offset: 2.5mA Step: 5mA Range: 0000 to 0011 (2.5mA to 17.5mA) If I_{TERM} > 17.5mA: Offset: 2mA Step:4mA Range: 0100 to 1111 (18mA to 62mA) Default: 0001 (7.5mA)
2	I_{TERM}[2]	0	Y	Y	R/W	16mA	
1	I_{TERM}[1]	0	Y	Y	R/W	10mA: I_{TERM} ≤ 17.5mA 8mA: I_{TERM} > 17.5mA	
0	I_{TERM}[0]	1	Y	Y	R/W	5mA: I_{TERM} ≤ 17.5mA 4mA: I_{TERM} > 17.5mA	

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

REG04h

Bits	Bit Name	POR	Reset by REG_RST	Reset by WTD	R/W	Description	Comments
7	V_{BATT_REG}[5]	1	Y	Y	R/W	480mV	Sets the battery regulation voltage. Offset: 3.60V Range: 3.60V to 4.545V Default: 4.2V (101000)
6	V_{BATT_REG}[4]	0	Y	Y	R/W	240mV	
5	V_{BATT_REG}[3]	1	Y	Y	R/W	120mV	
4	V_{BATT_REG}[2]	0	Y	Y	R/W	60mV	
3	V_{BATT_REG}[1]	0	Y	Y	R/W	30mV	
2	V_{BATT_REG}[0]	0	Y	Y	R/W	15mV	
1	V_{BATT_PRE}	1	Y	Y	R/W	0: 2.8V 1: 3.0V	Pre-charge to fast charge threshold Default: 1 (3V)
0	V_{RECH}	1	Y	Y	R/W	0: 100mV 1: 200mV	Battery recharge threshold (below V_{BATT_REG}) Default: 1 (200mV)

REG05h

Bits	Bit Name	POR	Reset by REG_RST	Reset by WTD	R/W	Description	Comments
7	EN_WD_DISCHG	0	Y	N	R/W	0: Disabled 1: Enabled	Enables watchdog control in discharge mode. Default: 0 (disabled)
6	WATCHDOG[1]	0	Y	Y	R/W	00: Timer disabled 01: 40s 10: 80s 11: 160s	Sets the I²C watchdog timer limit. If bits[6:5] = 00, then the watchdog timer is disabled, regardless of bit[7]. If bits[6:5] are set to 00 via the OTP, then the watchdog flag is not triggered and the system does not reset after the watchdog timer expires. Default: 01 (40s)
5	WATCHDOG[0]	1	Y	Y	R/W		
4	EN_TERM	1	Y	Y	R/W	0: Disabled 1: Enabled	Enables termination control. Default: 1 (enabled)
3	EN_TIMER	1	Y	Y	R/W	0: Disabled 1: Enabled	Enables the safety timer. Default: 1 (enabled)
2	CHG_TMR[1]	0	Y	Y	R/W	00: 20hrs 01: 5hrs 10: 8hrs 11: 12hrs	Sets the fast charge timer. Default: 00 (20hrs)
1	CHG_TMR[0]	0	Y	Y	R/W		
0	TERM_TMR	0	Y	Y	R/W	0: Disabled 1: Enabled	Controls the termination timer (when TERM_TMR is enabled, the IC does not suspend the charge current after charge termination). Default: 0 (disabled)

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

REG06h

Bits	Bit Name	POR	Reset by REG_RST	Reset by WTD	R/W	Description	Comments
7	EN_NTC	1	Y	Y	R/W	0: Disabled 1: Enabled	Default: 1 (enabled)
6	TMR2X_EN	1	Y	Y	R/W	0: Disable the 2x extended safety timer during PPM; 1: Enable the 2x extended safety timer during PPM	Default: 1 (enabled)
5	FET_DIS (13)	0	Y	N	R/W	0: Enabled 1: Turned off	Default: 0 (enabled)
4	PG_INT_ CONTROL	0	Y	Y	R/W	0: On 1: Off	Default: 0 (on)
3	EOC_INT_ CONTROL	0	Y	Y	R/W	0: On 1: Off	Charge completed INT mask control Default: 0 (on)
2	CHG STATUS_ INT_CONTROL	0	Y	Y	R/W	0: On 1: Off	Charging status change INT mask control (Charging status contain: not charging, pre-charge and charge) Default: 0 (on)
1	NTC_INT_ CONTROL	0	Y	Y	R/W	0: On 1: Off	Default: 0 (on)
0	BATTOVP_ INT_CONTROL	0	Y	Y	R/W	0: On 1: Off	Default: 0 (on)

Note:

13) This bit only controls the turn on/off function of the battery FET, including charge and discharge.

REG07h

Bits	Bit Name	POR	Reset by REG_RST	Reset by WTD	R/W	Description	Comments
7	EN_PCB_OTP	1	Y	Y	R/W	0: Enabled 1: Disabled	Enables PCB over-temperature protection (OTP). Default: 1 (disabled)
6	EN_VINLOOP	0	Y	Y	R/W	0: Enabled 1: Disabled	Default: 0 (enabled)
5	T_{J_REG}[1]	1	Y	Y	R/W	00: 60°C 01: 80°C 10: 100°C 11: 120°C	Sets the thermal regulation threshold Default: 11 (120°C)
4	T_{J_REG}[0]	1	Y	Y	R/W		
3	V_{SYS_REG}[3]	1	Y	N	R/W	400mV	Sets the system regulation voltage. Offset: 4.2V Range: 4.2V to 4.95V Default: 1001 (4.65V)
2	V_{SYS_REG}[2]	0	Y	N	R/W	200mV	
1	V_{SYS_REG}[1]	0	Y	N	R/W	100mV	
0	V_{SYS_REG}[0]	1	Y	N	R/W	50mV	

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

REG08h

Bits	Bit Name	POR	Reset by REG_RST	Reset by WTD	R/W	Description	Comments
7	WATCHDOG_FAULT	0	NA	NA	R	0: Normal 1: Watchdog timer expiration	Default: 0 (normal)
6	REV[1]	1	NA	NA	R	00: Reserved 01: Reserved 10: MP2665A 11: Reserved	Indicates the revision number. Default: 10 (MP2665A)
5	REV[0]	0	NA	NA	R		
4	CHG_STAT[1]	0	NA	NA	R	00: Not charging 01: Pre-charge 10: Charge 11: Charge done	Default: 00 (not charging)
3	CHG_STAT[0]	0	NA	NA	R		
2	PPM_STAT	0	NA	NA	R	0: No PPM 1: In PPM	Default: 0 (no PPM)
1	PG_STAT	0	NA	NA	R	0: Power fail 1: Power good	PG is set to 1 when V_{IN} is beyond its thresholds. V_{IN} should exceed V_{BATT} + V_{HDRM}. Default: 0 (power fail)
0	THERM_STAT	0	NA	NA	R	0: No thermal regulation 1: In thermal regulation	Default: 0 (no thermal regulation)

REG09h

Bits	Bit Name	POR	Reset by REG_RST	Reset by WTD	R/W	Description	Comments
7	EN_SHIPPING_DGL[1]	0	Y	N	R/W	00: 1s 01: 2s 10: 4s 11: 8s	Sets the shipping mode deglitch time. Default: 00 (1s)
6	EN_SHIPPING_DGL[0]	0	Y	N	R/W		
5	VIN_FAULT	0	NA	NA	R	0: Normal 1: Input fault (OVP or bad source)	When V_{IN} rises above or drops below its thresholds, this bit is set to 1. Default: 0 (normal)
4	THEM_SD	0	NA	NA	R	0: Normal 1: Thermal shutdown	Default: 0 (normal)
3	BAT_FAULT	0	NA	NA	R	0: Normal 1: Battery over-voltage protection (OVP) has occurred	Default: 0 (normal)
2	STMR_FAULT	0	NA	NA	R	0: Normal 1: Safety timer expiration	Default: 0 (normal)
1	NTC_FAULT[1]	0	NA	NA	R	0: Normal 1: NTC hot	Default: 0 (normal)
0	NTC_FAULT[0]	0	NA	NA	R	0: Normal 1: NTC cold	Default: 0 (normal)

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

REG0Ah (14)

Bits	Bit Name	POR	Reset by REG_RST	Reset by WTD	R/W	Description	Comments
7	ADDR[1]	0	NA	NA	NA	00: 08h 01: 0Ah 10: 0Ch 11: 0Eh	Indicates the IC address. Default: 00 (08h)
6	ADDR[0]	0	NA	NA	NA		
5	VINOVP	0	NA	NA	NA	0: 6.4V 1: 13.6V	Sets the V_{IN} over-voltage protection (OVP) threshold. Default: 0 (6.4V)
4	RESERVED	0	NA	NA	NA		
3	RESERVED	0	NA	NA	NA		
2	RESERVED	0	NA	NA	NA		
1	RESERVED	0	NA	NA	NA		
0	RESERVED	0	NA	NA	NA		

Note:

14) This register is for the one-time programmable (OTP) memory, and it is not accessible.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

OTP MAP

#	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]
0x00	N/A				I_{IN_LIM}[3]	N/A		
0x01	N/A				CEB	N/A		
0x02	N/A		I_{CC}: 16mA to 896mA					
0x03	N/A				I_{TERM}: 2.5mA to 62mA			
0x04	V_{BATT_REG}: 3.6V to 4.545V (15mV/step)						N/A	
0x05	N/A	WATCHDOG		N/A				
0x07	EN_PCB_OTP	EN_VINLOOP	N/A					
0x0A	ADDRESS		VINOVP	N/A				

OTP DEFAULT

OTP Items	Default
I_{IN_LIM}	940mA
CEB	Disable
I_{CC}	224mA
I_{TERM}	7.5mA
V_{BATT_REG}	4.2V
WATCHDOG	40s
EN_PCB OTP	Disable
EN_VINLOOP	Enable
ADDRESS	08h
VINOVP	6.4V

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

STATE CONVERSION CHART

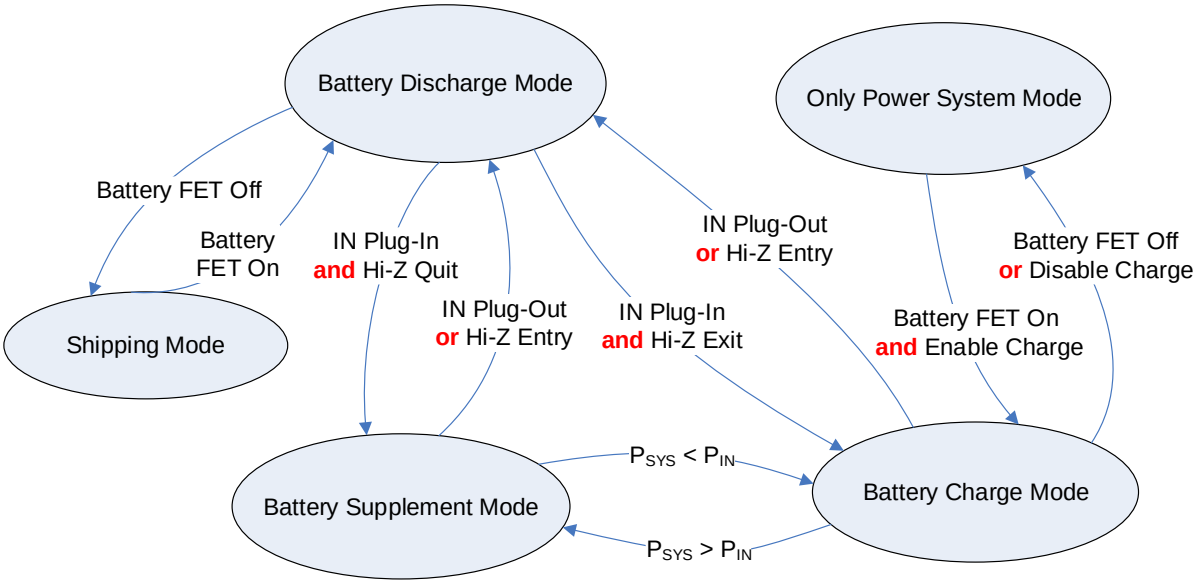


Figure 16: State Machine Conversion

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

CONTROL FLOWCHARTS

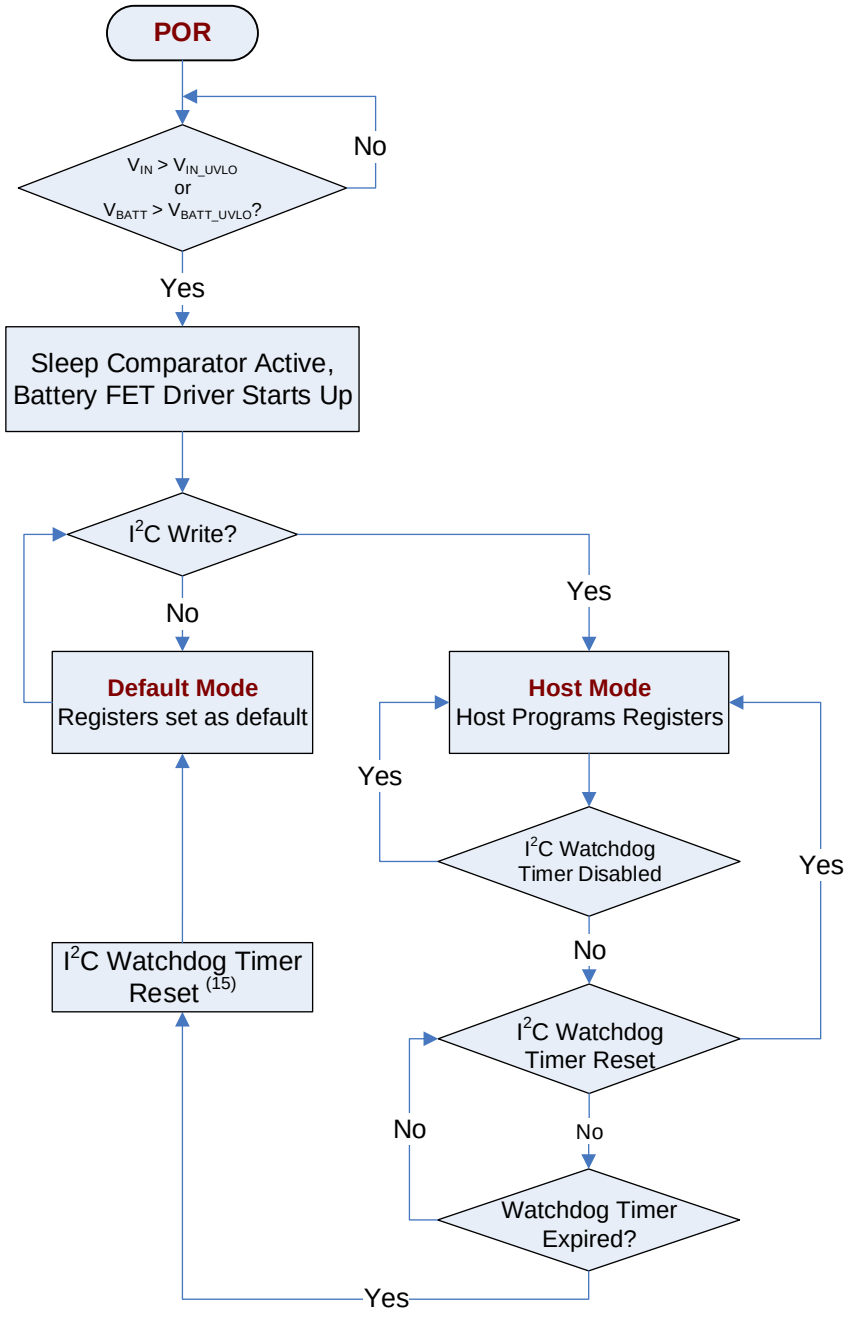


Figure 17: Default Mode and Host Mode Selection

Note:

15) Once the watchdog timer has expired, the I²C watchdog timer must be reset, or the watchdog timer is not valid in the next cycle.

.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

CONTROL FLOWCHARTS *(continued)*

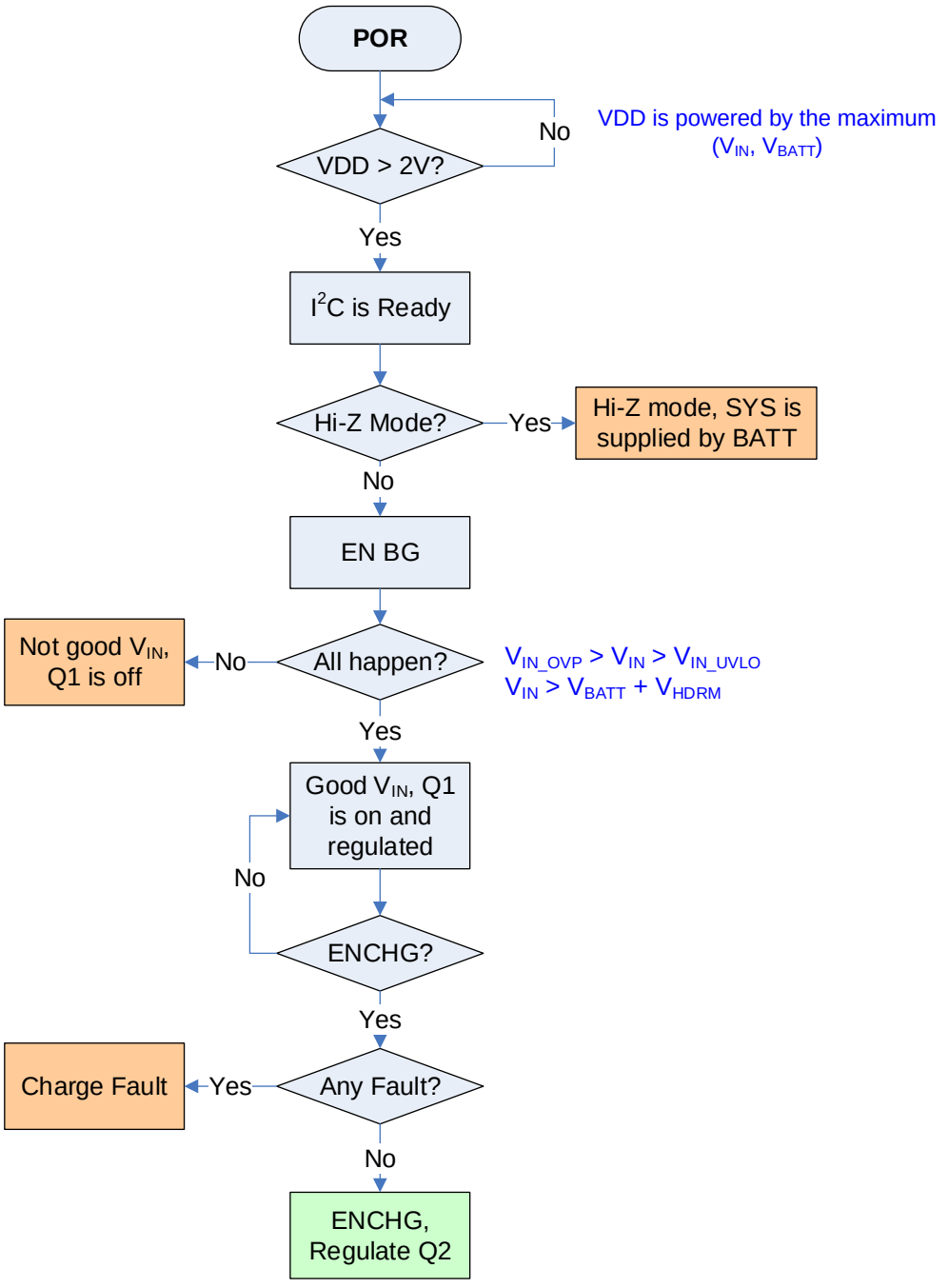


Figure 18: Input Power Start-Up Flowchart

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

CONTROL FLOWCHARTS *(continued)*

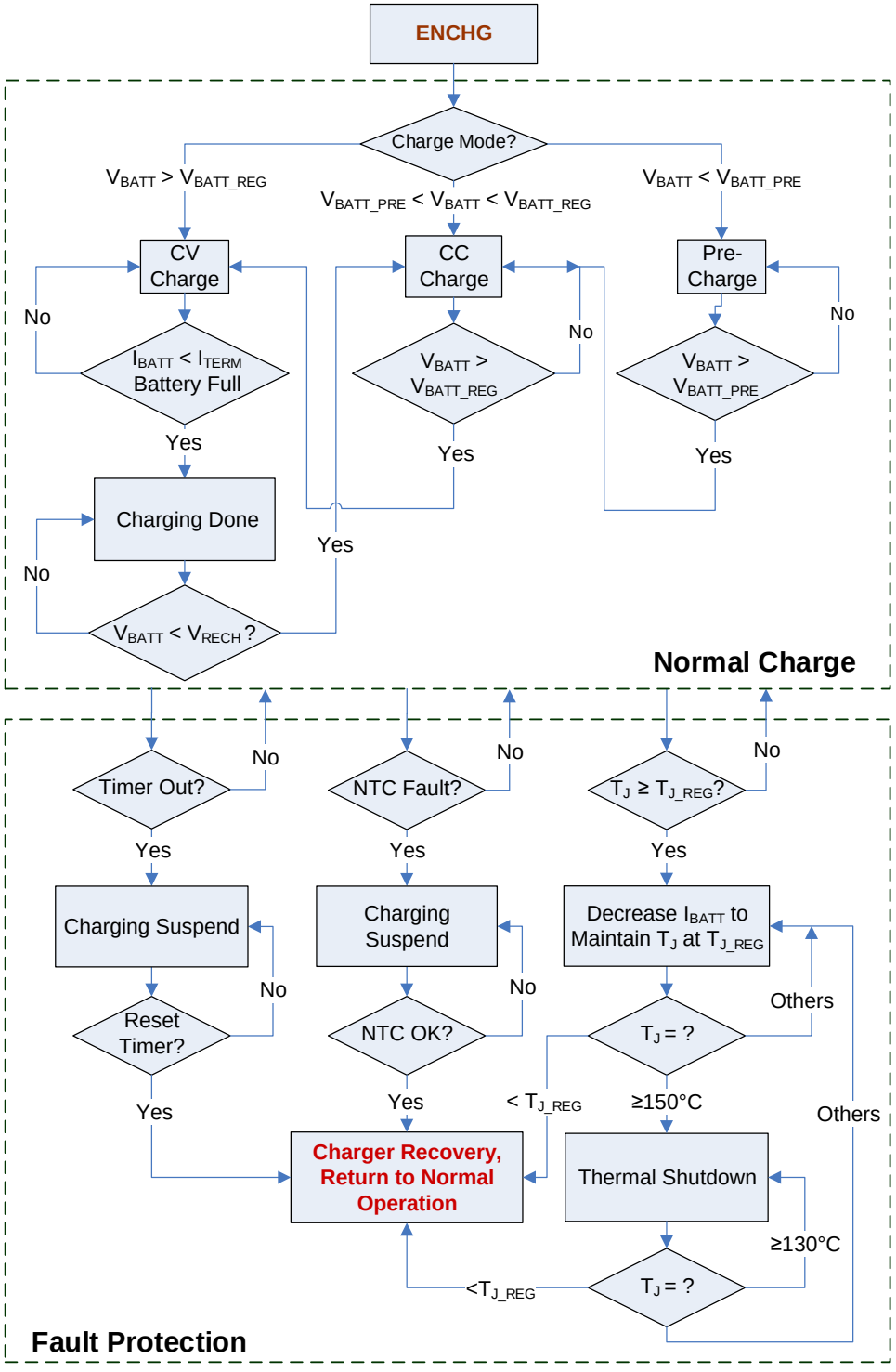


Figure 19: Charging Process

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

CONTROL FLOWCHARTS *(continued)*

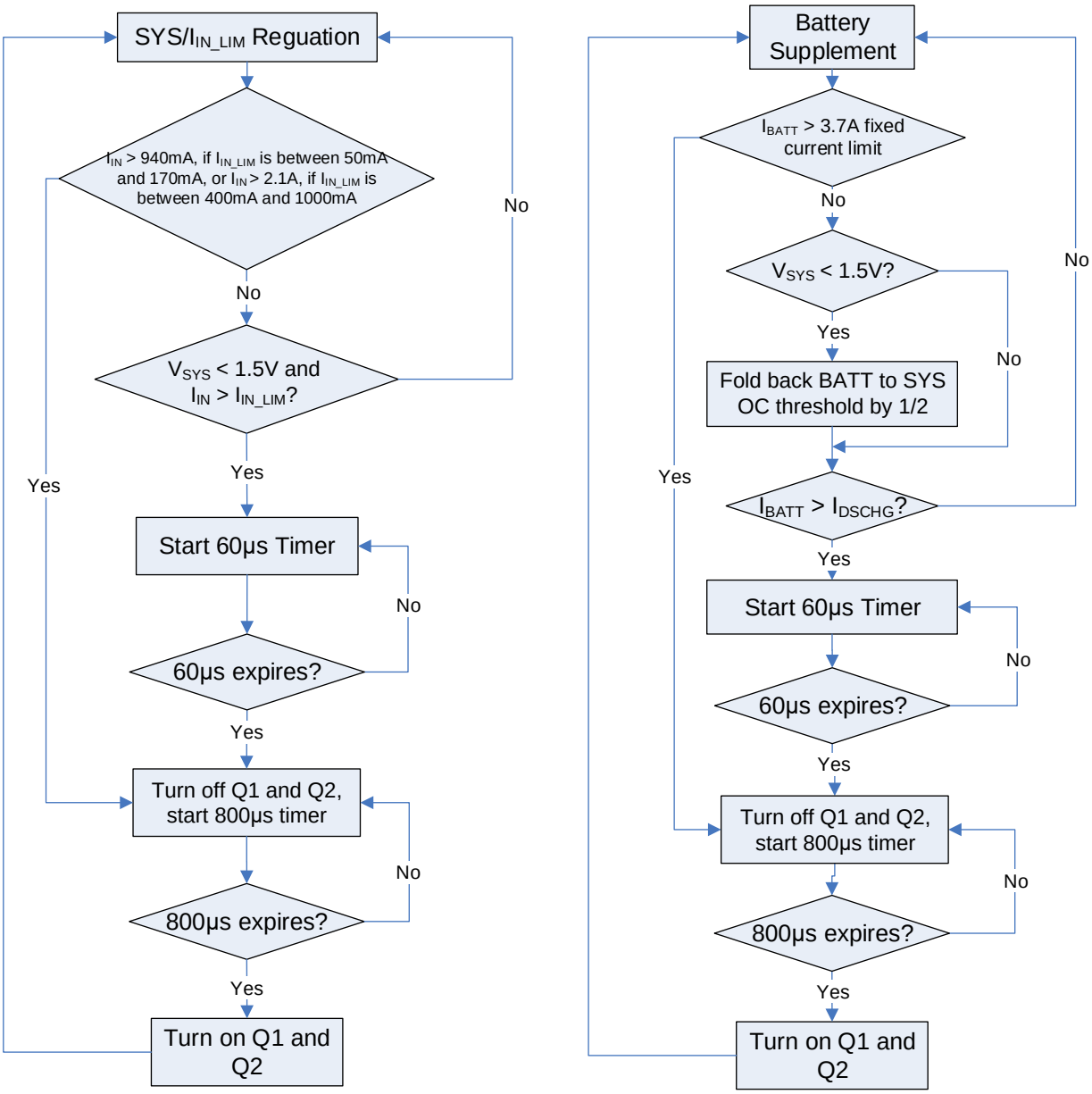


Figure 20: System Short-Circuit Protection (SCP)

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

APPLICATION INFORMATION

Selecting the NTC Resistor

The NTC pin uses a resistor divider connected to the input source (VDD) to sense the battery temperature. The two resistors (R_{T1} and R_{T2}) allow the high temperature limit and low temperature limit to be configured independently (see Figure 21). This means the MP2665A can meet most NTC resistor and temperature operation range requirements with the addition of two resistors.

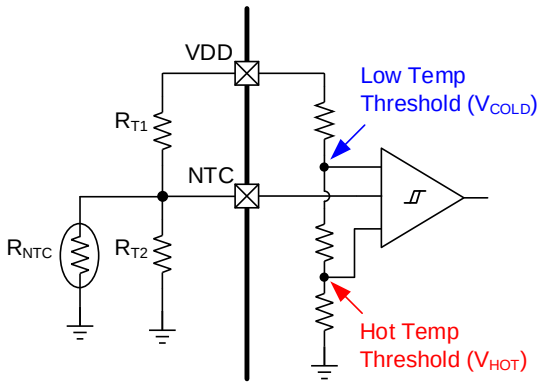


Figure 21: NTC Functional Block

For a given NTC thermistor, the R_{T1} and R_{T2} values depend on the type of the NTC resistor. R_{T2} and R_{T1} can be calculated with Equation (1) and Equation (2), respectively:

$$R_{T2} = \frac{(V_{COLD} - V_{HOT}) \times R_{NTCH} \times R_{NTCL}}{(V_{HOT} - V_{COLD}V_{HOT}) \times R_{NTCL} - (V_{COLD} - V_{COLD}V_{HOT}) \times R_{NTCH}} \quad (1)$$

$$R_{T1} = \frac{1\text{-}V_{COLD}}{V_{COLD}} \times (R_{T2} // R_{NTCL}) \quad (2)$$

Where R_{NTCH} is the value of the NTC resistor at the high temperature, and R_{NTCL} is the value of the NTC resistor at the low temperature.

For example, for the thermistor NCP18XH103, R_{NTCL} is 27.219kΩ at 0°C, and R_{NTCH} is 4.161kΩ at 50°C. Use Equation (1) and Equation (2) to calculate R_{T1} = 7.33kΩ and R_{T2} = 27.22kΩ. Assume that the NTC window is between 0°C and 50°C, then use the V_{COLD} and V_{HOT} values from the Electrical Characteristics section on page 10.

Selecting the External Capacitor

Like most low-dropout regulators, the MP2665A requires external capacitors for regulator stability and voltage spike immunity. The device is specifically designed for portable applications requiring minimum board space and smallest components, these capacitors must be selected for optimal performance.

Selecting the Input Capacitor

A minimum 4.7µF input capacitor must be connected between IN to GND for stable operation across the full load current range. The output capacitance can have a higher capacitance than the input, as long as the input is at least 4.7µF.

Selecting the Output Capacitor

The MP2665A is designed specifically to work with a very small ceramic output capacitor. A >10µF ceramic capacitor with X5R or X7R dielectrics is recommended for the application circuit. The output capacitor should be connected between the SYS and GND pins with a thick trace and small loop area.

Selecting the BATT to GND Capacitor

Place a >22µF ceramic capacitor with X5R or X7R dielectrics from the BATT pin to GND.

Selecting the VDD to GND Capacitor

The capacitor between VDD and GND stabilizes the VDD voltage so that VDD can power the internal control and logic circuit. The typical value of this capacitor is about 100nF.

PCB Layout Guidelines

1. Place the external capacitors as close to the IC as possible for the smallest input inductance and the ground impedance.
2. The PCB trace to connect the capacitor between VDD and GND should be put very close to the IC.
3. The GND-to-I²C wire should be clean, and it should not be be placed close to GND.
4. The I²C wires should be placed in parallel.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

TYPICAL APPLICATION CIRCUIT

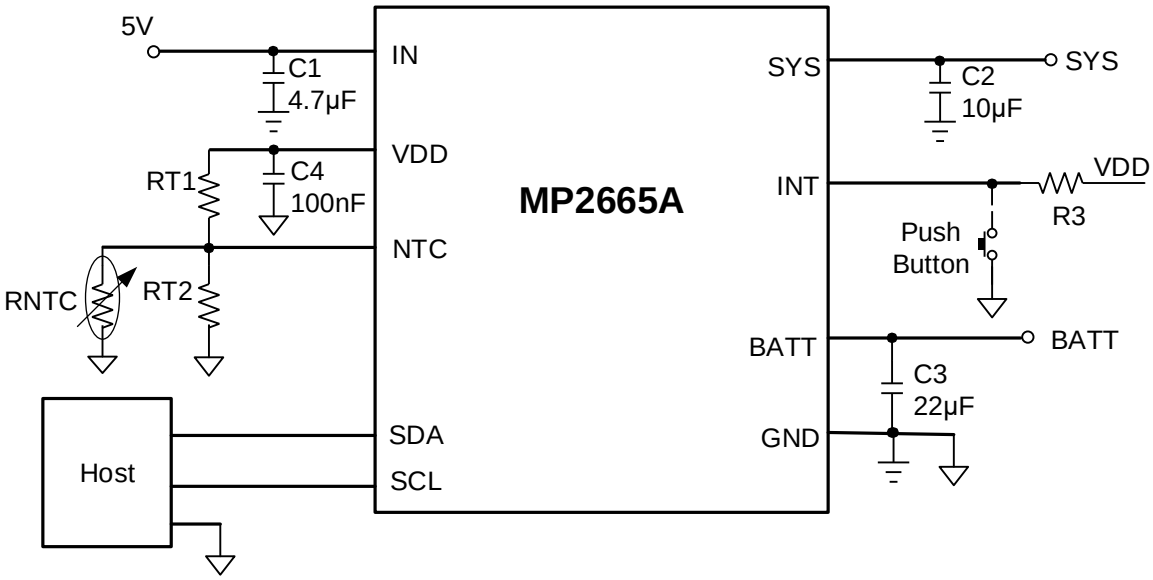


Figure 22: MP2665A Typical Application Circuit with 5V Input

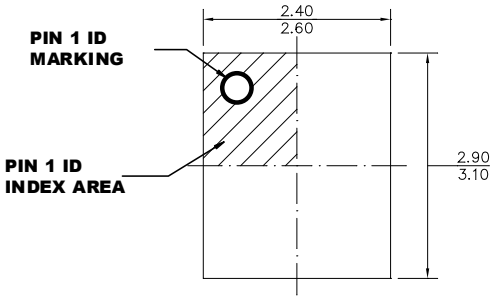
Table 5: The Key BOM from Figure 22

Qty	Ref	Value	Description	Package	Manufacturer
1	C1	4.7µF	Ceramic capacitor, 16V, X5R OR X7R	0603	Any
1	C2	10µF	Ceramic capacitor, 16V, X5R OR X7R	0805	Any
1	C3	22µF	Ceramic capacitor, 16V, X5R OR X7R	0805	Any
1	C4	100nF	Ceramic capacitor, 16V, X5R OR X7R	0603	Any

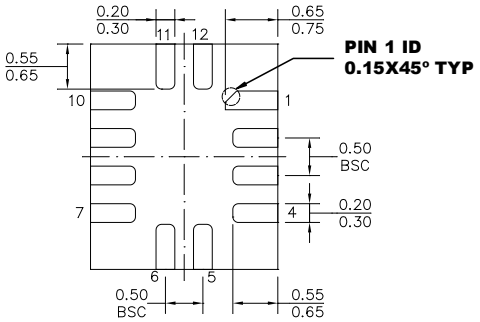
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

PACKAGE INFORMATION

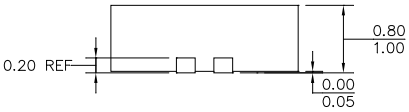
QFN-12 (2.5mmx3mm)



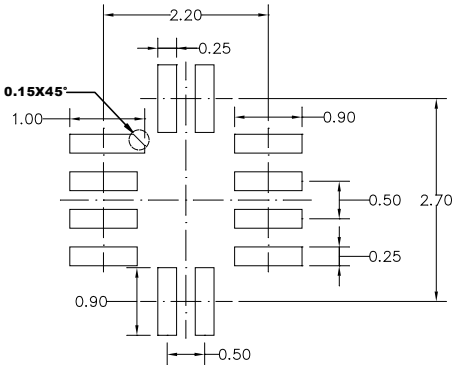
TOP VIEW



BOTTOM VIEW



SIDE VIEW



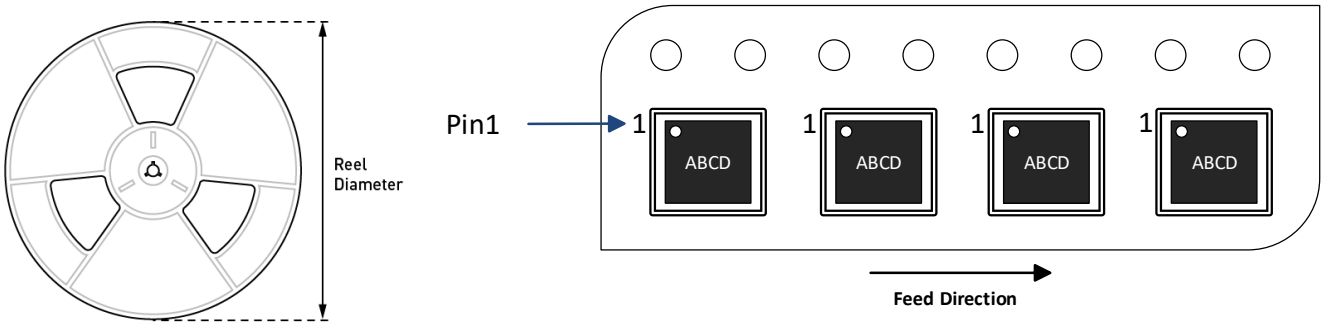
RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
3) JEDEC REFERENCE IS MO-220.
4) DRAWING IS NOT TO SCALE.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP2665AGQB-xxxx-Z	QFN-12 (2.5mmx3mm)	5000	N/A	N/A	13in	12mm	8mm

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	8/16/2021	Initial Release	-
1.1	4/28/2022	Minor grammar edits	1
		Updated WATCHDOG[1] and WATCHDOG[0] in REG05h	28

Notice: The information in this document is subject to change without notice. Users should warrant and guarantee that third-party Intellectual Property rights are not infringed upon when integrating MPS products into any application. MPS will not assume any legal responsibility for any said applications.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.