MP2667

5V USB, 1000mA, I²C-Controlled Linear Charger with Power Path Management for Single-Cell, Li-Ion Battery in QFN Package

DESCRIPTION

The MP2667 is a highly integrated, single-cell, Li-ion/Li-polymer battery charger with system power path management for space-limited portable applications. The MP2667 takes input power from either an AC adapter or a USB port to supply the system load and charge the battery simultaneously. The charger function features constant current pre-charge, constant current fast charge (CC) and constant voltage (CV) regulation, charge termination, and auto-recharge.

The power path management function ensures continuous power to the system by automatically selecting the input, battery, or both to power the system. This power stage features a low-dropout regulator from the input to the system and a 100mΩ switch from the battery to the system. Power path management separates the charging current from the system load, which allows for proper charge termination and keeps the battery in full-charge mode.

The MP2667 provides a system short-circuit protection (SCP) function by limiting the current from the input to the system and the battery to the system. This feature is especially critical for preventing the Li-ion battery from being damaged due to excessively high currents. An on-chip battery under-voltage lockout (UVLO) cuts off the path between the battery and the system if the battery voltage drops below the programmable battery UVLO threshold. This prevents the Li-ion battery from being over-discharged. An integrated I²C control interface allows the MP2667 to program the charging parameters, such as the input current limit, input minimum voltage regulation, charging current, battery regulation voltage, safety timer, and battery UVLO.

The MP2667 is available in a 10-pin QFN (2mmx2mm) package.

FEATURES

- Compatible with 5V USB Power Sources
- Fully Autonomous Charger for Single-Cell Li-Ion/Li-Polymer Batteries
- Complete Power Path Management for Simultaneously Powering the System and Charging the Battery
- Programmable Input Current Limit and Minimum Input Voltage Regulation Thresholds
- ±0.5% Charging Voltage Accuracy
- 13V Maximum Voltage for the Input Source
- I²C Interface for Programming Charging Parameters and Status Reporting
- Fully Integrated Power Switches and No External Blocking Diode Required
- Built-In Robust Charging Protection Including Battery Temperature Monitoring and Programmable Timer
- Built-In Battery Disconnection Function for Shipping Mode
- Thermal Limiting Regulation on the Chip
- Available in an Ultra-Compact QFN-10 (2mmx2mm) Package

APPLICATIONS

- Wearable Devices
- Smart Handheld Devices
- Fitness Accessories
- Smartwatches
- Bluetooth Headphones

All MPS parts are lead-free, halogen-free, and adhere to the RoHS directive. For MPS green status, please visit the MPS website under Quality Assurance. “MPS”, the MPS logo, and “Simple, Easy Solutions” are registered trademarks of Monolithic Power Systems, Inc. or its subsidiaries.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2019 MPS. All Rights Reserved.

TYPICAL APPLICATION

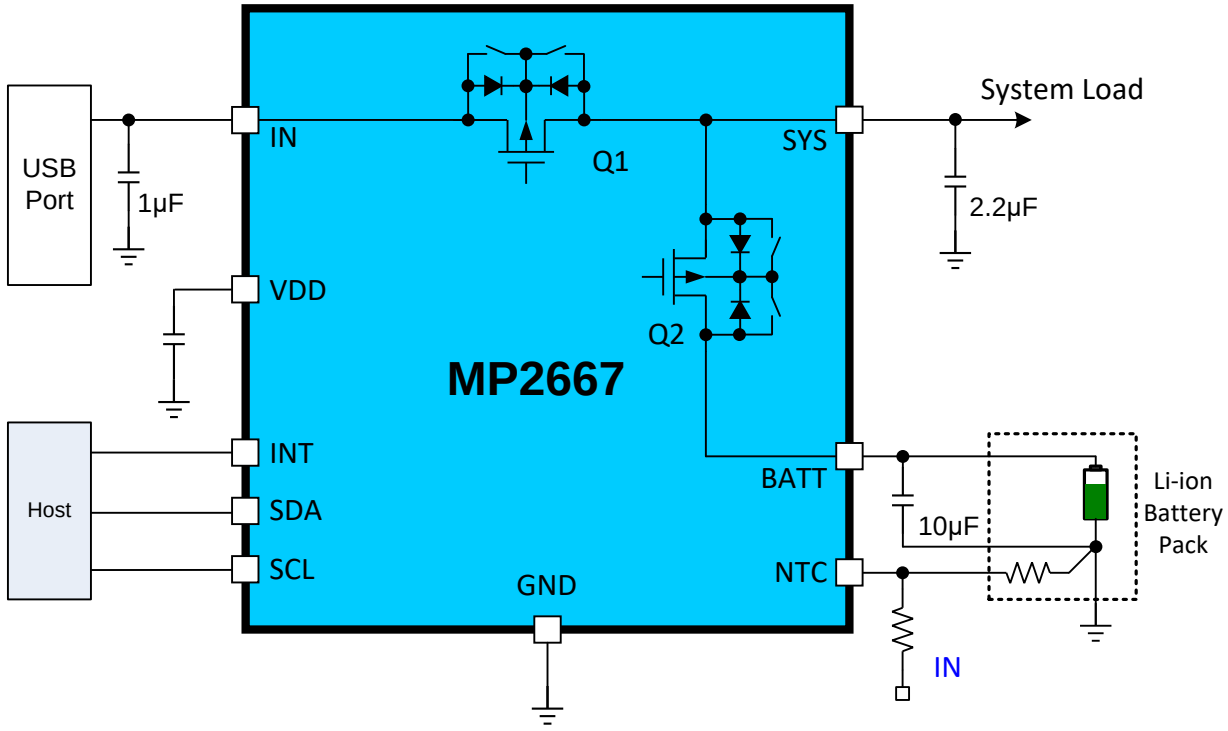


Table 1: Operation Mode Table

FET On/Off Change By Control	I²C Control		
	HZ = 1	CEB = 1	FET_DIS = 1*
	Enter Hi-Z Mode	Charge Control	Enter Shipping Mode
LDO FET	Off	x	x
Battery FET (charging)	x	Off	Off
Battery FET (discharging)	x	x	Off

x = N/A

* FET_DIS goes back to 0 when the battery FET is off.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2019 MPS. All Rights Reserved.

ORDERING INFORMATION

Part Number*	Package	Top Marking
MP2667GG-xxxx**	QFN-10 (2mmx2mm)	*See Below*
EVKT-MP2667	Evaluation kit	*See Below*

* For Tape & Reel, add suffix –Z (e.g. MP2667GG-xxxx–Z).
** "xxxx" is the configuration code identifier for the register settings. For the default case, the number is "0000." Each "x" can have a hexadecimal value between 0 and F. Contact an MPS FAE to create this unique number, even if ordering the "0000" code.

TOP MARKING

JQY
LLL

JQ: Product code of MP2667GG
Y: Year code
LLL: Lot number

EVALUATION KIT EVKT-MP2667

EVKT-MP2667 kit contents (items below can be ordered separately):

#	Part Number	Item	Quantity
1	EV2667-C-00A	MP2667 evaluation board	1
2	EVKT-USBI2C-02-bag	Include one USB to I²C communication interface, one USB cable, and one ribbon cable	1
3	Online resources	Include datasheet, user guide, product brief, and GUI	1

Order direct from MonolithicPower.com or our distributors.

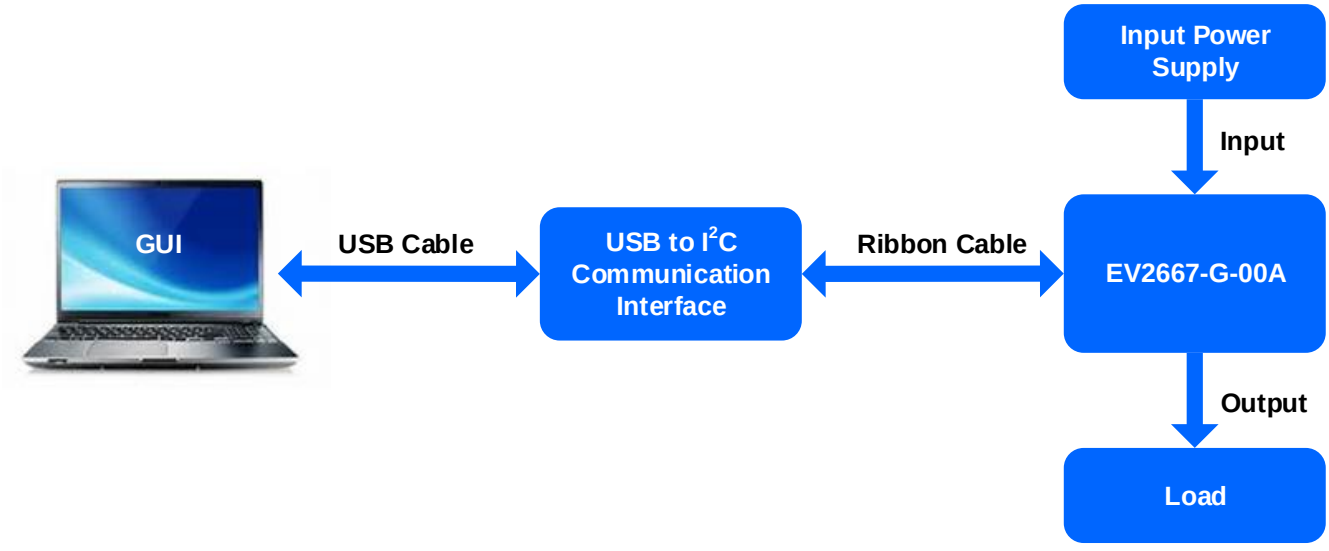
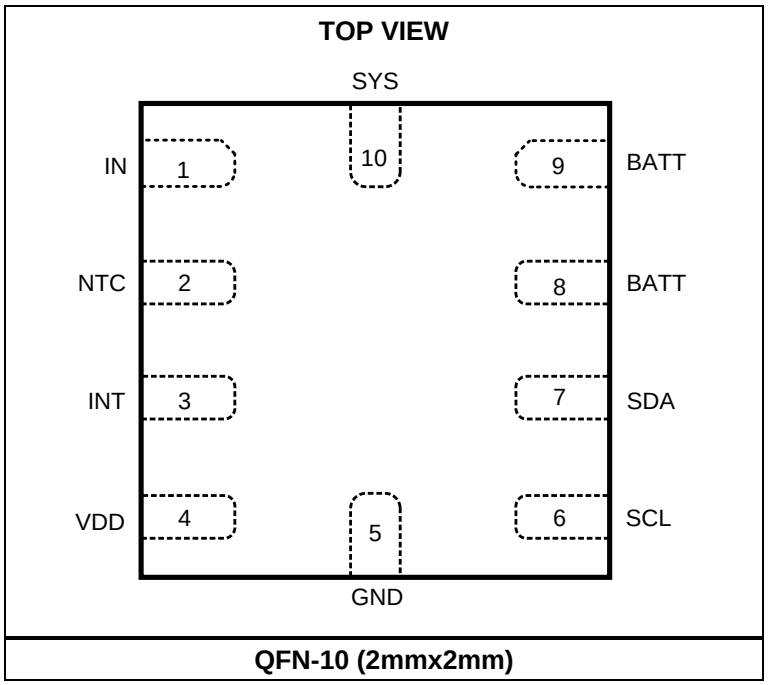


Figure 1: EVKT-MP2667 Evaluation Kit Set-Up

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2019 MPS. All Rights Reserved.

PACKAGE REFERENCE



QFN-10 (2mmx2mm)

PIN FUNCTIONS

Pin #	Name	I/O	Description
1	IN	Power	**Input power pin.** Place a ≥1μF ceramic capacitor from IN to GND, as close to the IC as possible.
2	NTC	I	**Temperature sense input.** Connect a negative temperature coefficient thermistor to NTC. Program the hot and cold temperature window with a resistor divider from IN to NTC to GND. The charge is suspended when NTC is out of range.
3	INT	O	**Interrupt output.** INT can send the charging status and fault interrupt signal to the host. INT is also used to disconnect the system from the battery. Pull INT from high to low for >8s to disconnect the battery from the system. The external pull-up resistor at INT must be greater than 100kΩ.
4	VDD	I	**Internal control power supply.** Connect a ceramic capacitor (0.1μF) from VDD to GND. No external load is allowed.
5	GND	Power	**Ground.**
6	SCL	I/O	**I²C interface clock.** Connect SCL to the logic rail through a 10kΩ resistor.
7	SDA	I/O	**I²C interface data.** Connect SDA to the logic rail through a 10kΩ resistor.
8, 9	BATT	Power	**Battery pin.** Place a ceramic capacitor from BATT to GND, as close to the IC as possible.
10	SYS	Power	**System power supply.** Place a ceramic capacitor from SYS to GND, as close to the IC as possible.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2019 MPS. All Rights Reserved.

ABSOLUTE MAXIMUM RATINGS (1)

V_{IN} .....-0.3V to +13V
All other pins to GND .....-0.3V to +6.0V
Continuous power dissipation (T_A = +25°C) (2)
..... 1.25W
Junction temperature .....150°C
Lead temperature (solder) .....260°C
Storage temperature..... -65°C to +150°C

Recommended Operating Conditions (3)

Supply voltage (V_{IN}) .....4.35V to 5.5V
(USB input)
I_{IN}.....Up to 1A
I_{SYS} .....Up to 1.6A
I_{CHG}.....Up to 1A
V_{BATT}.....Up to 4.545V
Operating junction temp (T_J).... -40°C to +125°C

Thermal Resistance (4) θ_{JA} θ_{JC}

QFN-10 (2mmx2mm)..... 80.... 16... °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2019 MPS. All Rights Reserved.

ELECTRICAL CHARACTERISTICS

V_{IN} = 5.0V, V_{BATT} = 3.5V, T_A = +25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Input Source and Battery Protection						
Input voltage range	V_{IN}				13	V
Input operation voltage	V_{IN}		4.35	5.0	5.5	V
Battery input voltage (5)	V_{BATT}				4.5	V
Input over-voltage protection trigger threshold	V_{IN_OVP}	Input rising threshold	5.85	6.00	6.15	V
Input over-voltage protection recover threshold				367		mV
Input under-voltage lockout threshold	V_{IN_UVLO}	Input rising threshold	3.8	3.9	4.0	V
Input under-voltage lockout threshold hysteresis				180		mV
Input vs. battery voltage headroom threshold	V_{HDRM}	Input rising vs. battery	90	110	130	mV
Input vs. battery voltage headroom threshold hysteresis				66		mV
Battery under-voltage lockout threshold	V_{BATT_UVLO}	Battery voltage falling, programmable, V_{BATT_UVLO} = 2.8V	2.6	2.8	3.0	V
Battery UVLO range		Programmable using I²C	2.4		3.1	V
Battery under-voltage threshold hysteresis		V_{BATT_UVLO} = 2.8V		227		mV
Battery over-voltage protection threshold	V_{BATT_OVP}	Rising, higher than V_{BATT_REG}		128		mV
		Falling, higher than V_{BATT_REG}		63		
Power Path Management						
System regulation voltage	V_{SYS_REG}	V_{IN} = 5.5V, I_{SYS} = 10mA, I_{CHG} = 0A	4.85	5.00	5.15	V
Input current limit range		I²C programmable	77		993	mA
Input current limit	I_{IN_LIM}	REG00[2:0] = 000 - 77mA	59	68	77	mA
		REG00[2:0] = 001 - 118mA	95	107	118	
		REG00[2:0] = 011 - 470mA	410	440	470	
		REG00[2:0] = 111 - 993mA	875	934	993	
Input minimum voltage regulation	V_{IN_MIN}	I²C-programmable range	3.88		5.08	V
		I²C setting V_{IN_MIN} = 4.20V	4.10	4.20	4.30	
		I²C setting V_{IN_MIN} = 4.60V	4.50	4.60	4.70	
SYS output voltage	V_{SYS}	Charging mode, V_{IN} = 5.5V, V_{BATT} = 3.7V	4.85	5.00	5.15	V
		Supplement mode, V_{BATT} = 3.7V, I_{BATT} = 100mA	3.6			
		V_{IN} < V_{IN_UVLO} and V_{BATT} < V_{BATT_UVLO}	0			

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2019 MPS. All Rights Reserved.

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 5.0V, V_{BATT} = 3.5V, T_A = +25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
IN to SYS switch on resistance	R_{ON_Q1}	V_{IN} = 5V, I_{SYS} = 100mA		300	400	mΩ
Input quiescent current	I_{IN_Q}	V_{IN} = 5.5V, CE = L, enable, I_{CHG} = 0A, I_{SYS} = 0A		642		µA
		V_{IN} = 5.5V, CE = H, charge disabled		482		
Battery quiescent current	I_{BATT_Q}	V_{IN} = 5V, CE = L, I_{SYS} = 0A, V_{BATT} = 4.3V		33		µA
		V_{IN} = 0V, CE = H, I_{SYS} = 0A, V_{BATT} = 4.35V		11	14	
		V_{BATT} = 4.5V, V_{IN} = V_{SYS} = GND, disconnect mode		4.512	5.055	
BFET on resistance	R_{ON_Q2}	V_{IN} < 2V, V_{BATT} = 3.5V, I_{SYS} = 100mA		100	150	mΩ
Battery current regulation in discharge mode	I_{DSCHG}	Program range	100		1600 (5)	mA
BFET switch leakage		V_{BATT} = 4.5V, V_{IN} = V_{SYS} = GND, disconnect mode			1	µA
SYS reverse to BATT switch leakage		V_{SYS} = 5V, V_{IN} = 4.5V, V_{BATT} = GND, CE = H			1.3	µA
Battery discharge function controlled by INT (5)	t_{INT}	INT pull low lasting time to turn off the battery discharge function		8		s
		Battery FET lasts for the off time before auto-on		500		ms
Battery Charger						
Battery voltage regulation (V_{BATT_REG} = 4.2V)	V_{BATT}	T = 25°C, I_{BATT} = 15mA	4.179	4.200	4.221	V
Battery charge voltage regulation	V_{BATT_REG}	Programmable using I²C	3.600		4.545	V
		V_{BATT_REG} = 3.6V, REG04[7:2] = 000000, T_A = 25°C	3.582	3.600	3.618	
		V_{BATT_REG} = 3.6V, REG04[7:2] = 000000, T_A = -40°C to +85°C	3.574		3.626	
		V_{BATT_REG} = 4.2V, REG04[7:2] = 101000, T_A = 25°C	4.179	4.200	4.221	
		V_{BATT_REG} = 4.2V, REG04[7:2] = 101000, T_A = -40°C to +85°C	4.170		4.230	
		V_{BATT_REG} = 4.35V, REG04[7:2] = 110010, T_A = 25°C	4.328	4.350	4.372	
		V_{BATT_REG} = 4.35V, REG04[7:2] = 110010, T_A = -40°C to +85°C	4.319		4.381	

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2019 MPS. All Rights Reserved.

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 5.0V, V_{BATT} = 3.5V, T_A = +25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Fast charge current	I_{CC}	V_{IN} = 5V, V_{BATT} = 3.8V, programmable range	26		1049 (5)	mA
		V_{IN} = 5V, V_{BATT} = 3.8V, I_{CC} [4:0] = 26mA, T_A = 25°C	19	26	33	
		V_{IN} = 5V, V_{BATT} = 3.8V, I_{CC} [4:0] = 26mA, T_A = -40°C to +85°C	19		33	
		V_{IN} = 5V, V_{BATT} = 3.8V, I_{CC} [4:0] = 257mA, T_A = 25°C	239	253	267	
		V_{IN} = 5V, V_{BATT} = 3.8V, I_{CC} [4:0] = 257mA, T_A = -40°C to +85°C	235		269	
		V_{IN} = 5V, V_{BATT} = 3.8V, I_{CC} [4:0] = 818mA, T_A = 25°C	764	816	868	
		V_{IN} = 5V, V_{BATT} = 3.8V, I_{CC} [4:0] = 818mA, T_A = -40°C to +85°C	750		875	
Junction temperature regulation (5)	T_{J_REG}	Junction temperature regulation REG06[1:0] = 11 – T_{J_REG} = 120°C		120		°C
Pre-charge current	I_{PRE}	I_{TERM} [1:0] = 24mA, T_A = 25°C	6	15	25	mA
		I_{TERM} [1:0] = 24mA, T_A = -40°C to +85°C	4		27	
		I_{TERM} [1:0] = 52mA, T_A = 25°C	27	40	52	
		I_{TERM} [1:0] = 52mA, T_A = -40°C to 85°C	26		53	
Charge termination current threshold	I_{TERM}	Program range	24		108	mA
		I_{CC} [4:0] ≤ 521mA, (REG02[4] = 0), I_{TERM} [1:0] = 24mA, T_A = 25°C	7	14	20	mA
		I_{CC} [4:0] ≤ 521mA, (REG02[4] = 0), I_{TERM} [1:0] = 24mA, T_A = -40°C to +85°C	6		21	
		I_{CC} [4:0] ≤ 521mA, (REG02[4] = 0), I_{TERM} [1:0] = 52mA, T_A = 25°C	19	26	33	
		I_{CC} [4:0] ≤ 521mA, (REG02[4] = 0), I_{TERM} [1:0] = 52mA, T_A = -40°C to +85°C	17		35	
		I_{CC} [4:0] ≥ 554mA, (REG02[4] = 1), I_{TERM} [1:0] = 24mA, T_A = 25°C	20	28	36	
		I_{CC} [4:0] ≥ 554mA, (REG02[4] = 1), I_{TERM} [1:0] = 24mA, T_A = -40°C to +85°C	17		37	
		I_{CC} [4:0] ≥ 554mA, (REG02[4] = 1), I_{TERM} [1:0] = 52mA, T_A = 25°C	42	52	63	
		I_{CC} [4:0] ≥ 554mA, (REG02[4] = 1), I_{TERM} [1:0] = 52mA, T_A = -40°C to +85°C	39		68	
Pre-charge to fast charge threshold	V_{BATT_PRE}	V_{BATT} rising, set V_{BATT_PRE} = 3.0V	2.8	3.0	3.1	V
Pre-charge to fast charge threshold hysteresis				97		mV
Auto-recharge battery voltage threshold	V_{RECH}	REG04[0] = 0	140	170	220	mV
		REG04[0] = 1	270	320	370	

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2019 MPS. All Rights Reserved.

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 5V, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Thermal Protection						
Thermal shutdown threshold (5)	T_{J_SHDN}			150		°C
Thermal shutdown hysteresis (5)				20		°C
NTC output current	I_{NTC}	CE = L, V_{NTC} = 3V	-100	0	100	nA
NTC cold temperature rising threshold	V_{COLD}	As a percentage of V_{IN}	64	66	68	%
NTC cold temperature rising threshold hysteresis				30		mV
NTC hot temperature falling threshold	V_{HOT}	As a percentage of V_{IN}	33	35	37	%
NTC hot temperature falling threshold hysteresis				65		mV
Logic I/O Pin Characteristics (5)						
Low logic voltage threshold	V_L				0.4	V
High logic voltage threshold	V_H		1.3			V
I²C Interface (SDA, SCL)						
Input high voltage level	V_{IH}	V_{PULL_UP} = 1.8V, SDA and SCL	1.3			V
Input low voltage level	V_{IL}	V_{PULL_UP} = 1.8V, SDA and SCL			0.4	V
Output low voltage level	V_{OL}	I_{SINK} = 5mA			0.4	V
I²C clock frequency	f_{SCL}				400	kHz
Digital Clock and Watchdog Timer						
Digital clock 2	f_{DIG2}			32		kHz
Watchdog timer	t_{WDT}	Programmable (REG05[5:4] = 11)	140	165	190	s
Safety timer for fast charging cycle (5)	t_{TMR_FAST}	Programmable (REG05[2:1] = 00), t_{TMR_FAST} = 20hrs		20		hrs
		Programmable (REG05[2:1] = 01), t_{TMR_FAST} = 5hrs		5.0		
		Programmable (REG05[2:1] = 10), t_{TMR_FAST} = 8hrs		8.0		
		Programmable (REG05[2:1] = 11), t_{TMR_FAST} = 12hrs		12.0		

Note:

5) Guaranteed by design.

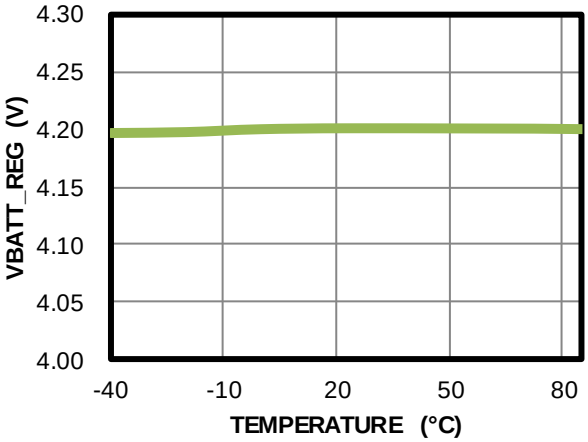
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2019 MPS. All Rights Reserved.

TYPICAL CHARACTERISTICS

V_{IN} = 5V, T_A = 25°C, I_{IN_LIM} = 470mA, I_{CC} = 257mA, V_{IN_MIN} = 4.6V, unless otherwise noted.

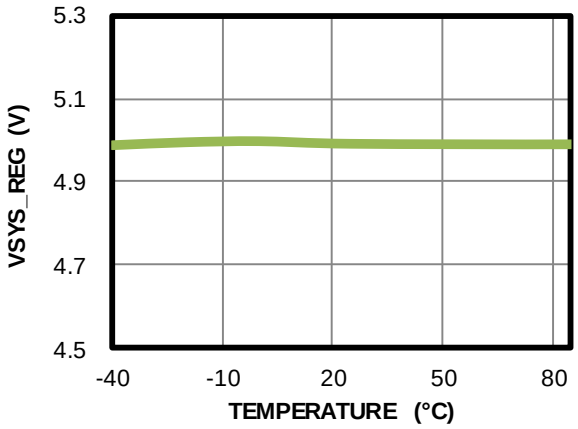
Battery Regulation Voltage vs. Temperature

V_{BATT_REG} = 4.2V

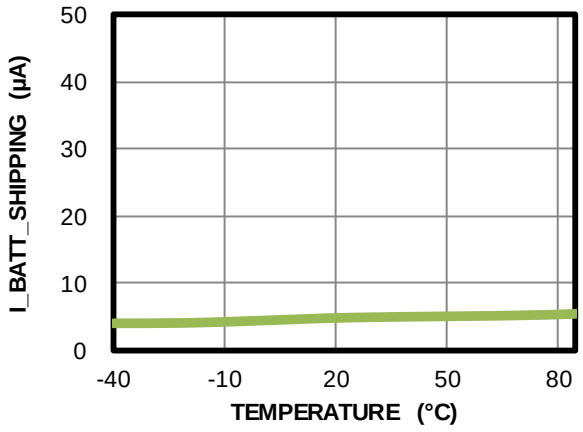


System Regulation Voltage vs. Temperature

V_{SYS_REG} = 5V

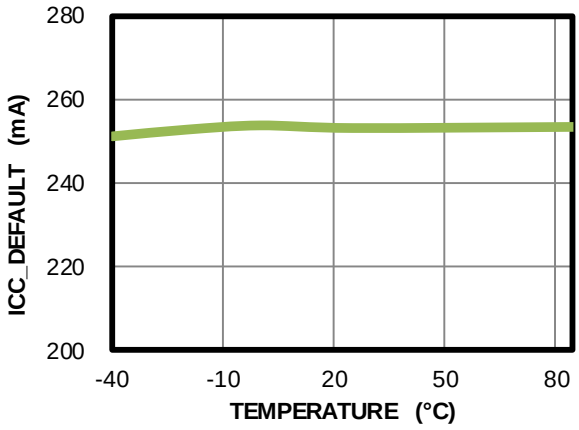


Battery Current under Shipping Mode vs. Temperature



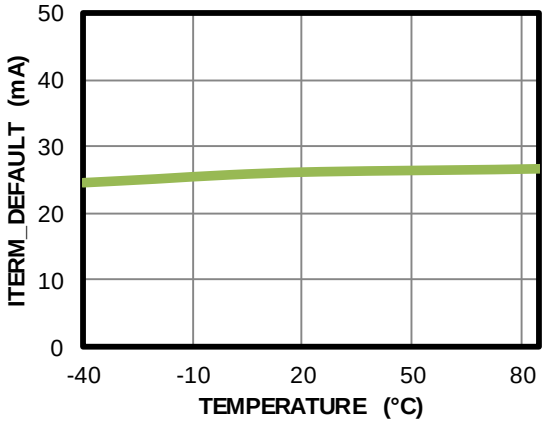
CC Charge Current vs. Temperature

I_{CC} = 257mA



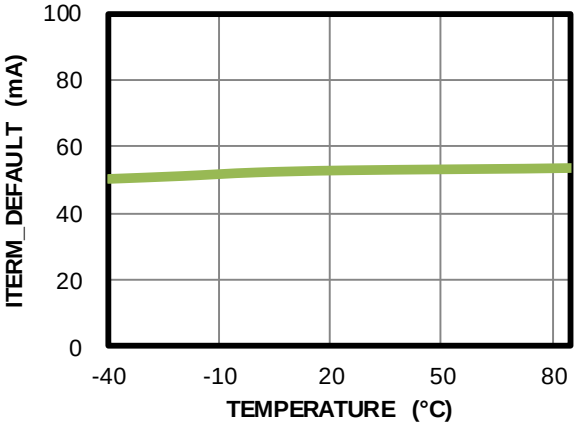
Battery Termination Current vs. Temperature

I_{TERM} = 52mA @ I_{IN_LIM} = 470mA, I_{CC} = 257mA



Battery Termination Current vs. Temperature

I_{TERM} = 52mA @ I_{IN_LIM} = 734mA, I_{CC} = 620mA



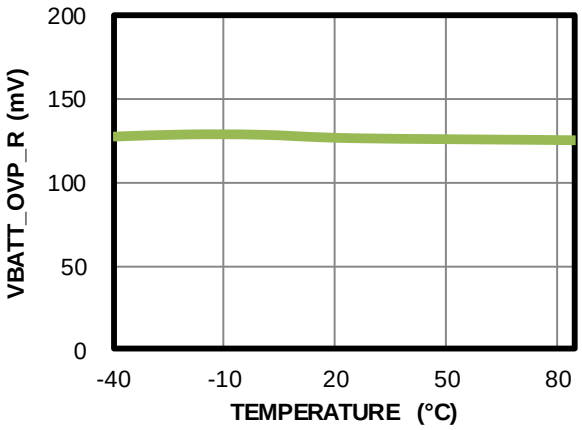
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2019 MPS. All Rights Reserved.

TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 5V, T_A = 25°C, I_{IN_LIM} = 470mA, I_{CC} = 257mA, V_{IN_MIN} = 4.6V, unless otherwise noted.

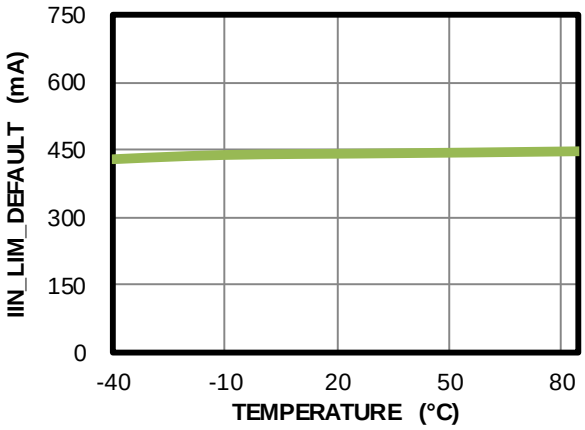
Battery OVP Voltage vs. Temperature

Rising, higher than V_{BATT_REG}



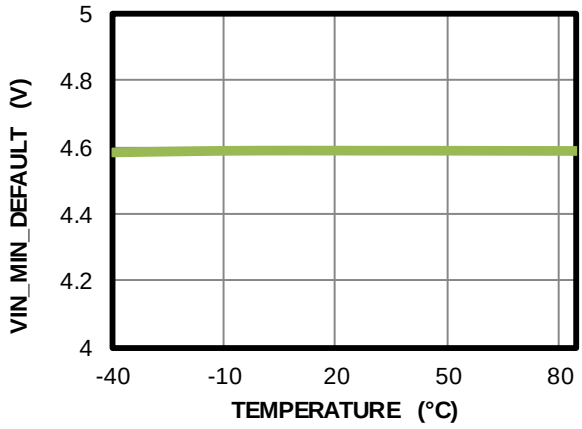
Input Current Limit vs. Temperature

I_{IN_LIM} = 470mA



Input Minimum Voltage vs. Temperature

V_{IN_MIN} = 4.6V



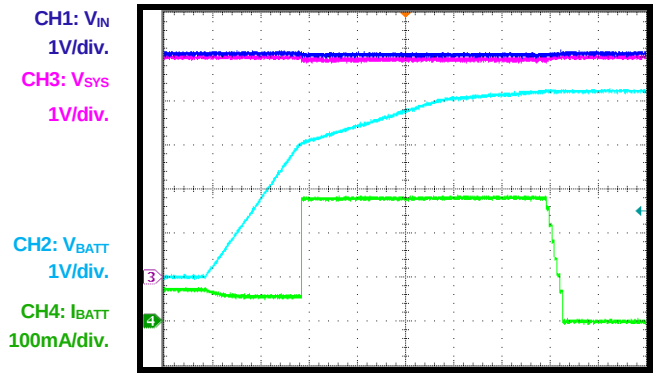
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2019 MPS. All Rights Reserved.

TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 5V, T_A = 25°C, I_{IN_LIM} = 470mA, I_{CC} = 257mA, V_{IN_MIN} = 4.6V, unless otherwise noted.

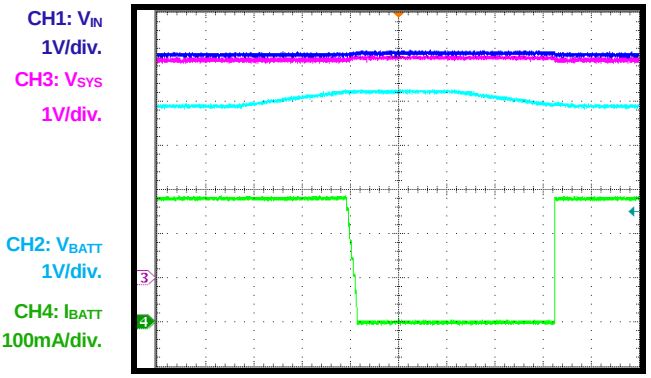
Battery Charge Curve

I_{SYS} = 0A



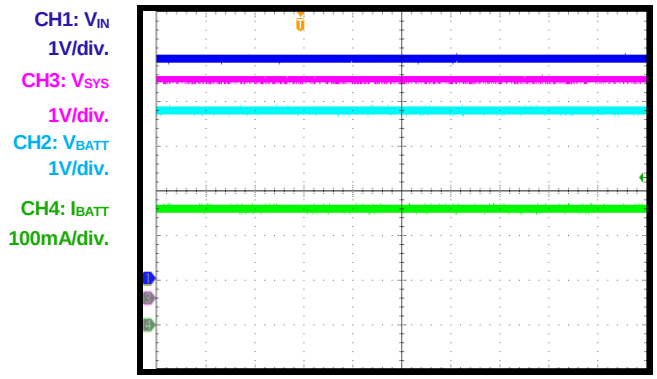
Auto-Recharge

I_{SYS} = 0A



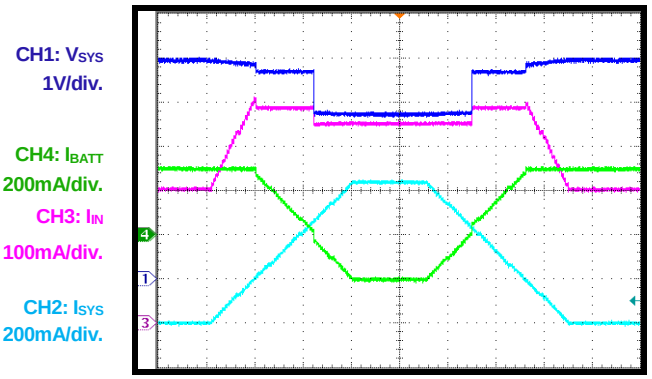
CC Charge Steady State

V_{BATT} = 3.7V, I_{SYS} = 0A



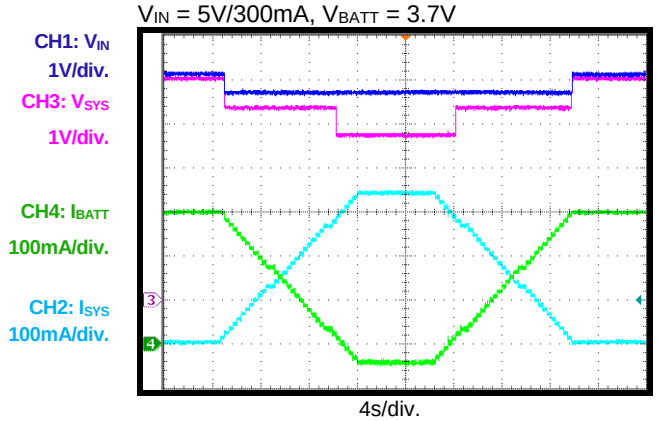
Input Current Limit-Based PPM

V_{BATT} = 3.7V



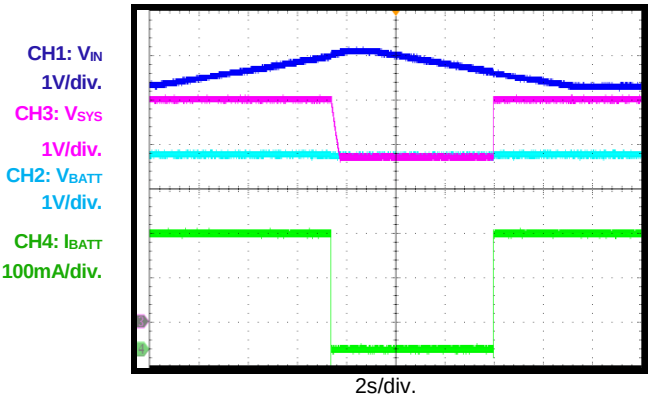
Input Voltage Regulation-Based PPM

V_{IN} = 5V/300mA, V_{BATT} = 3.7V



V_{IN} OVP Operation

V_{BATT} = 3.7V, I_{SYS} = 0A



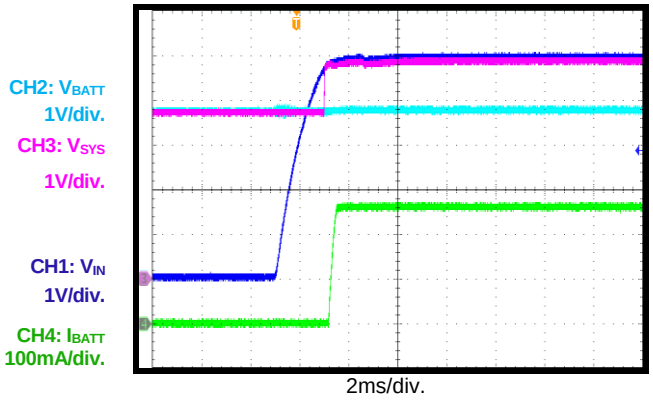
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2019 MPS. All Rights Reserved.

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, T_A = 25°C, I_{IN_LIM} = 470mA, I_{CC} = 257mA, V_{IN_MIN} = 4.6V, unless otherwise noted.

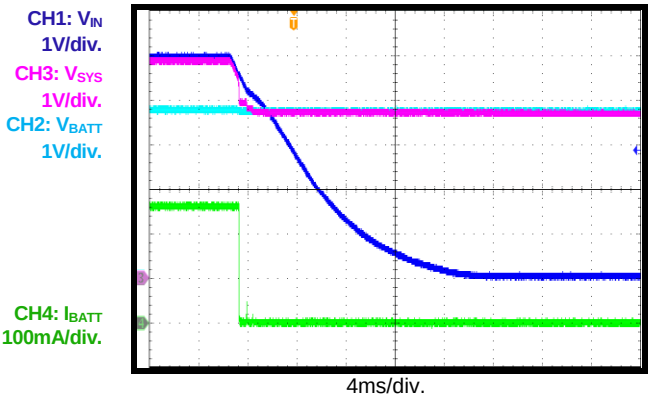
Power-On

V_{BATT} = 3.7V, I_{SYS} = 0A



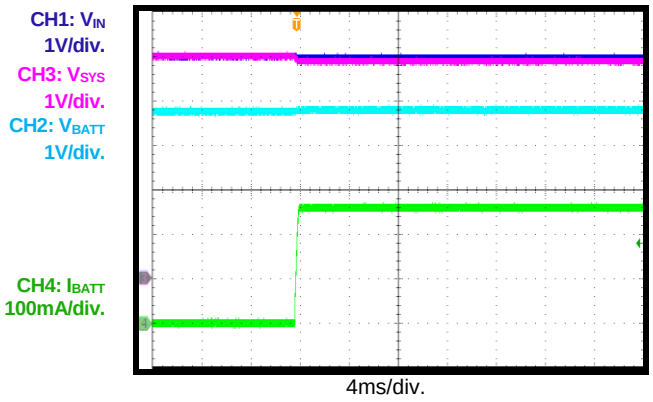
Power-Off

V_{BATT} = 3.7V, I_{SYS} = 0A



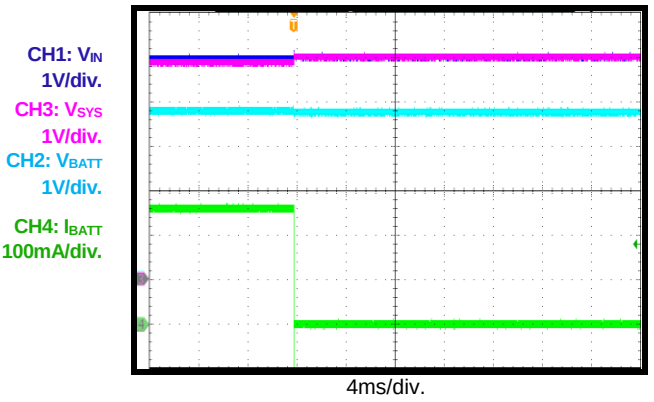
Charge Enable

V_{BATT} = 3.7V, I_{SYS} = 0A



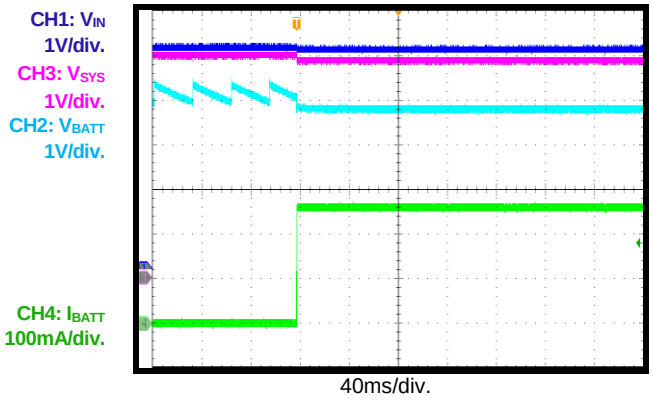
Charge Disable

V_{BATT} = 3.7V, I_{SYS} = 0A



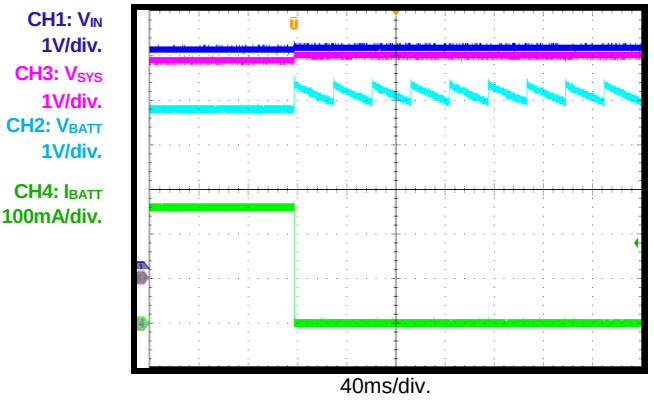
BATT Insertion

V_{BATT} = 3.7V, I_{SYS} = 0A



BATT Removal

V_{BATT} = 3.7V, I_{SYS} = 0A



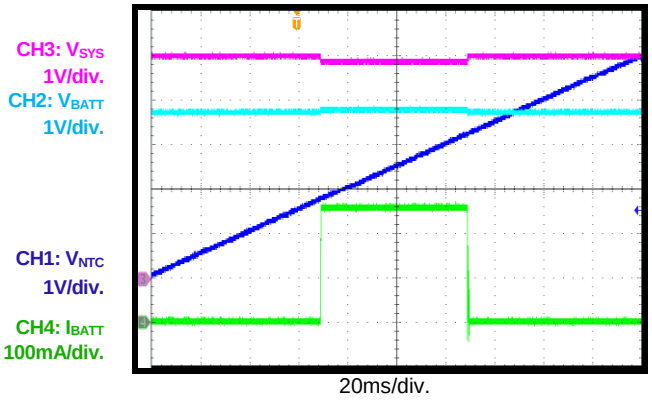
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2019 MPS. All Rights Reserved.

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, T_A = 25°C, I_{IN_LIM} = 470mA, I_{CC} = 257mA, V_{IN_MIN} = 4.6V, unless otherwise noted.

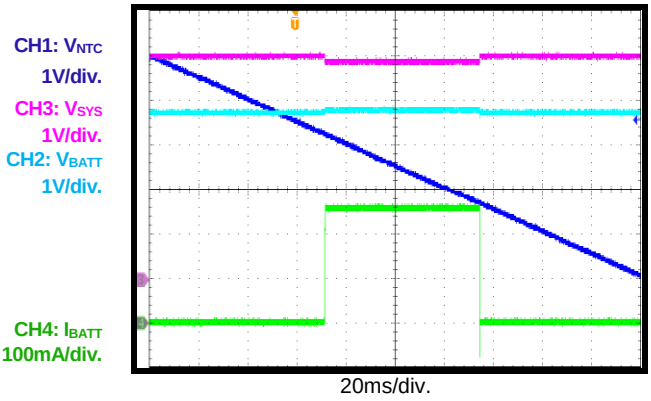
NTC Rising

V_{BATT} = 3.7V, I_{SYS} = 0A



NTC Falling

V_{BATT} = 3.7V, I_{SYS} = 0A



MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2019 MPS. All Rights Reserved.

FUNCTIONAL BLOCK DIAGRAM

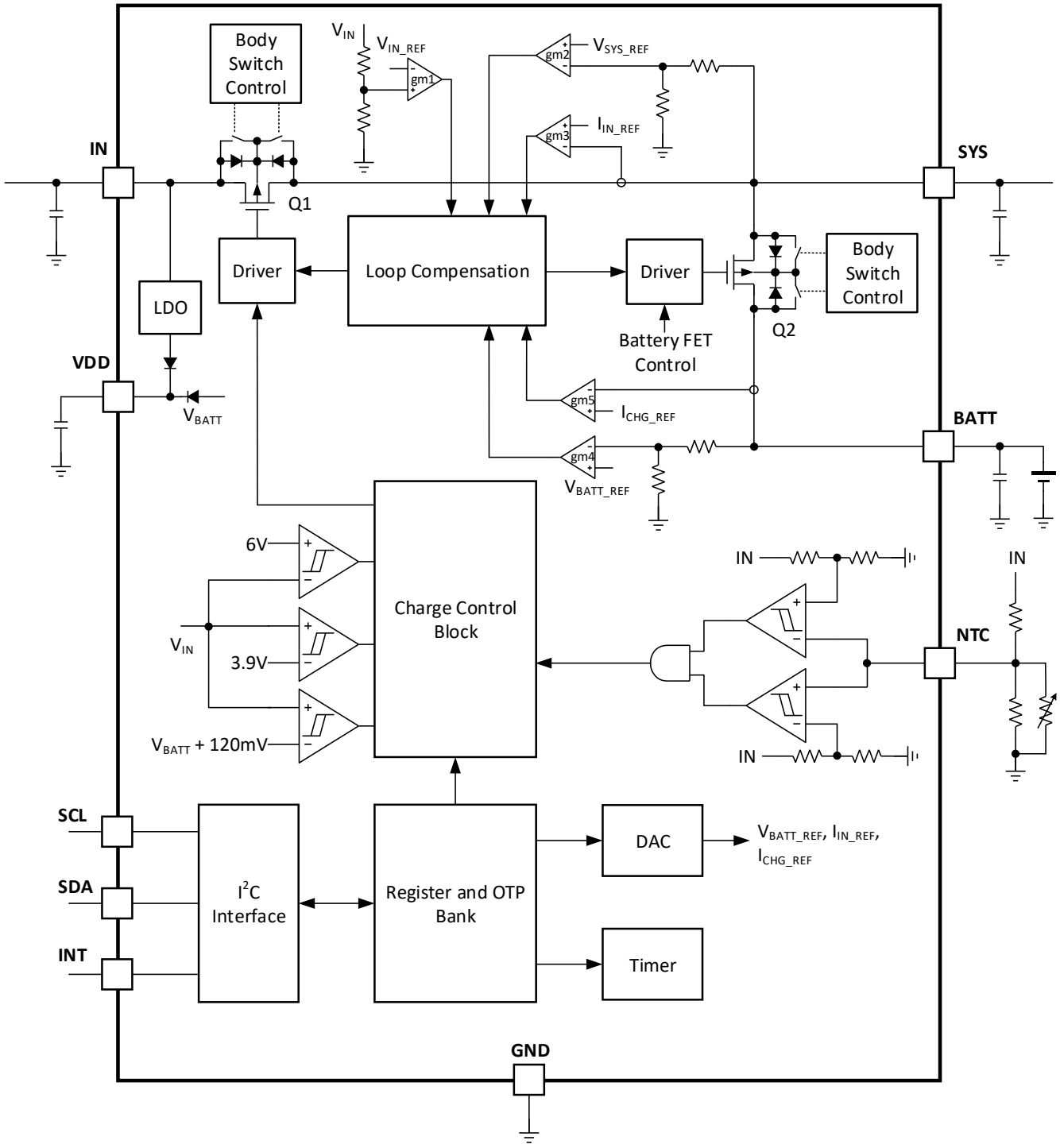


Figure 2: Functional Block Diagram

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2019 MPS. All Rights Reserved.

OPERATION

The MP2667 is an I²C-controlled, single-cell, Li-ion or Li-polymer battery charger with complete power path management. The full charge function features fast charge (CC) and constant voltage (CV) regulation, pre-charge (PRE.C), charge termination, auto-recharge, and a built-in timer. The power path function allows the input source to power the system and charge the battery simultaneously. If the power source cannot supply enough current to the system load and to charge the battery, then the charge current will be reduced until it is necessary for the battery to supplement system power.

The IC integrates a 300mΩ LDO FET between IN and SYS, and a 100mΩ battery FET between SYS and BATT.

During charging mode, the on-chip 100mΩ battery FET works as a full-featured linear charger with pre-charging, CC and CV charging, charge termination, auto-recharging, NTC monitoring, built-in timer control, and thermal protection. The charge current can be programmed via the I²C interface. The IC limits the charge current when the die temperature exceeds the programmable thermal regulation threshold (120°C default).

When the input power is not sufficient for powering the system load, the MP2667 enters supplement mode by fully turning on the 100mΩ battery FET. When the input is removed, the 100mΩ battery FET is also fully turned on, allowing the battery to power up the system.

When the system load is satisfied, the remaining current is used to charge the battery. The IC reduces the charging current or uses power from the battery to satisfy the system load when its demand is over the input power capacity, or if either the input current or voltage loops are active.

Figure 3 shows the power path management structure for the MP2667.

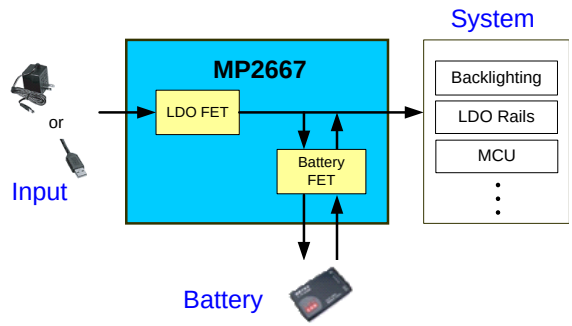


Figure 3: Power Path Management Structure

Power Supply

The internal bias circuit of the IC is powered from the higher voltage of IN or BATT. When IN or BATT rises above the respective under-voltage lockout (UVLO) threshold, the sleep comparator, battery depletion comparator, and battery FET driver are active. The I²C interface is ready for communication, and all registers are reset to the default value. The host can access all registers.

Input OVP and UVLO

The MP2667 has an input over-voltage protection (OVP) threshold and an input UVLO threshold. Once the input voltage transitions out of the normal input voltage range, the Q1 FET immediately turns off.

When the input voltage is identified as a good source, a 200µs immunity timer is active. If the input power is normal until the 200µs timer expires, the system starts up. Otherwise, Q1 remains off (see Figure 4).

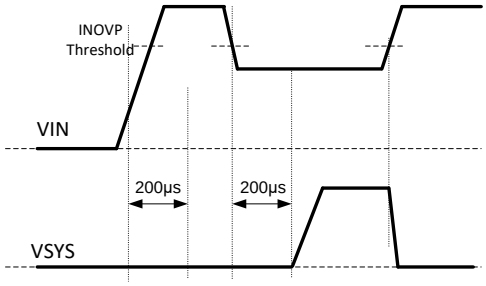


Figure 4: Input Power Detection Operation

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2019 MPS. All Rights Reserved.

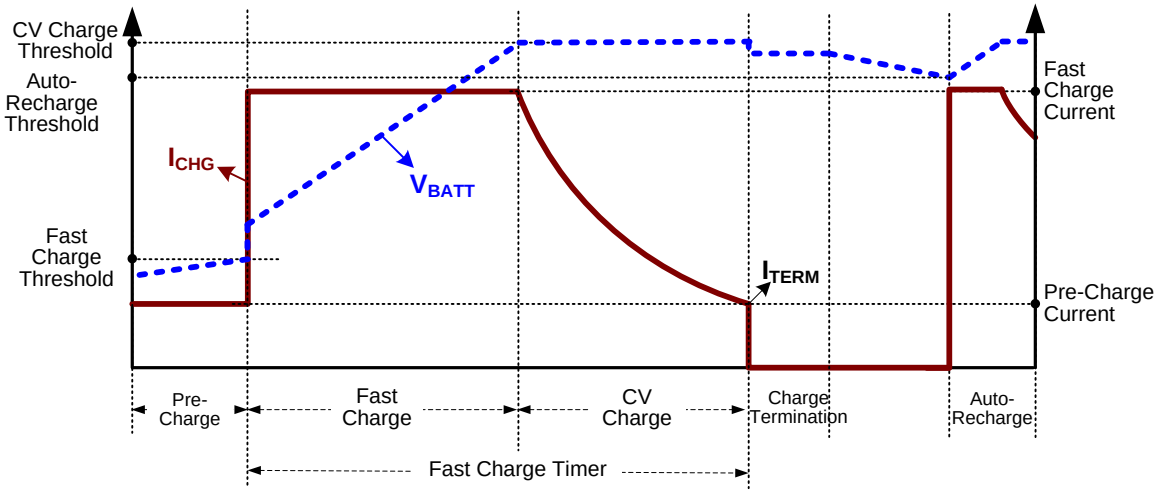


Figure 5: Battery Charge Profile

Power Path Management

The IC employs a direct power path structure with the battery FET decoupling the system from the battery, which allows for separate control between the system and the battery. The system is given the priority to start up even with a deeply discharged or missed battery. When the input power is available, even with a depleted battery, the system voltage is always regulated to V_{SYS_REG} by the integrated LDO FET.

The direct power structure is composed of a front-end LDO FET between the IN and SYS pins and a battery FET between the SYS and BATT pins (see Figure 3).

The input LDO (using an LDO FET) provides power to the system, which drives the system load directly and charges the battery through the battery FET.

For the system voltage control, when the input voltage is higher than V_{SYS_REG}, the system voltage is regulated to V_{SYS_REG}. When the input voltage is lower than V_{SYS_REG}, the LDO FET is fully on in dropout with an input current limit.

Battery Charge Profile

The IC provides three main charging phases: pre-charge, fast charge, and constant-voltage charge (see Figure 5).

1. Phase 1 (constant current pre-charge): The IC can safely pre-charge the deeply depleted battery until the battery voltage reaches the pre-charge to fast charge threshold (V_{BATT_PRE}). The pre-charge current is programmable via REG03 bit[1:0]. If V_{BATT_PRE} is not reached before the pre-charge timer (2hrs) expires, the charge cycle is stopped, and a corresponding timeout fault signal is asserted.
2. Phase 2 (constant current fast charge): When the battery voltage exceeds V_{BATT_PRE}, the IC enters a constant-current charge (fast charge) phase. The fast charge current is programmable via REG02 bit[4:0].
3. Phase 3 (constant-voltage charge): When the battery voltage rises to the pre-programmable charge full voltage (V_{BATT_REG}), set via REG04 bit[7:2], the charge mode changes from CC mode to CV mode, and the charge current begins to taper off.

Table 2 shows the end of charge (EOC) current threshold (I_{TERM}) value setting.

Table 2: I_{TERM} Value Table

Reg02 Bit[4]	I_{TERM} Value
0 ($I_{CC_SETTING}$ ≤ 521mA)	50% * I_{TERM} [1:0]
1 ($I_{CC_SETTING}$ ≥ 554mA)	I_{TERM} [1:0]

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2019 MPS. All Rights Reserved.

Once the charge current reaches the EOC current threshold (I_{TERM}) and the CV loop is still dominated, the IC has three possible actions after a 500µs delay, depending on the settings of EN_TERM (REG05 bit[6]) and TERM_TMR (reg05 bit[0]):

1. EN_TERM = 1, TERM_TMR = 0, (default spec): The IC terminates the charge and changes the charge status to Charge Done.
2. EN_TERM = 1, TERM_TMR = 1: The IC changes the charge status to Charge Done, but the charge current continues tapering off until it reaches 0.
3. EN_TERM = 0, TERM_TMR = x: The charge status stays at Charge, but the charge current continues tapering off until it reaches 0.

During the charging process, the actual charge current may be less than the register setting due to other loop regulations, such as dynamic power management (DPM) regulation or thermal regulation. See the Input Current- and Input Voltage-Based Power Management section for details.

If I_{TERM} is not reached before the safety charge timer expires (see Safety Timer section on page 19), the charge cycle stops and the corresponding timeout fault signal is asserted.

The following conditions can start a new charge cycle:

- The input power is recycled
- Battery charging is enabled by the I²C
- Auto-recharge kicks in

However, the following conditions can stop a charge cycle:

- No thermistor fault at NTC
- No safety timer fault
- No battery over-voltage
- Battery FET is not forced to turn off

Automatic Recharge

When the battery is fully charged and charging is terminated, the battery may be discharged due to system consumption or a self-discharge. When the battery voltage is discharged below the recharge threshold, and V_{IN} is still in the operating range, the IC begins another new charging cycle automatically without the requirement of restarting a charging cycle manually. The auto-recharge function is valid only when EN_TERM = 1 and TERM_TMR = 0.

Battery Over-Voltage Protection (OVP)

The IC is designed with a built-in battery over-voltage limit about 120mV higher than V_{BATT_REG}. When the battery over-voltage event occurs, the IC immediately suspends charging and asserts a fault.

Input Current- and Input Voltage-Based Power Management

To meet the input source (usually USB) maximum current limit specification, the IC uses an input current-based power management by monitoring the input current continuously. The total input current limit can be programmable via the I²C to prevent the input source from overloading.

If the pre-set input current limit is higher than the rating of the input source, backup input voltage-based power management also works to prevent the input source from being overloaded. If either the input current limit or the input voltage regulation is reached, the Q1 FET between IN and SYS is regulated so that the total input power is limited. As a result, the system voltage drops. Once the system declines to the minimum value of 4.8V or V_{SYS_REG} - 320mV, the charge current is reduced to prevent the system voltage from dropping further.

The voltage-based dynamic power management (DPM) regulates the input voltage to V_{IN_MIN} when the load is over the input power capacity. V_{IN_MIN} is set via the I²C, and should be at least 500mV higher than V_{BATT_REG} to ensure stable operation of the regulator.

Battery Supplement Mode

The charge current is reduced to keep the input current or input voltage in regulation when DPM occurs. If the charge current is at zero and the input source is still overloaded due to a heavy system load, the system voltage starts to fall off. Once the system voltage falls below the battery voltage, the IC enters battery supplement mode. When the system voltage is 30mV below the battery voltage, the ideal diode mode is enabled. The battery FET is regulated to maintain

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2019 MPS. All Rights Reserved.

V_{BATT} - V_{SYS} at 22.5mV. If the voltage drop of the battery FET (I_{DSCHG} * R_{ON_BATT}) is greater than 22.5mV, the battery FET is fully turned on to keep the ideal forward voltage. When the system load decreases and V_{SYS} is higher than V_{BATT} + 20mV, ideal diode mode is disabled.

Figure 6 shows the dynamic power management and battery supplement mode operation profile.

When V_{IN} is not available, the IC operates in discharge mode, and the battery FET is always fully on to reduce loss.

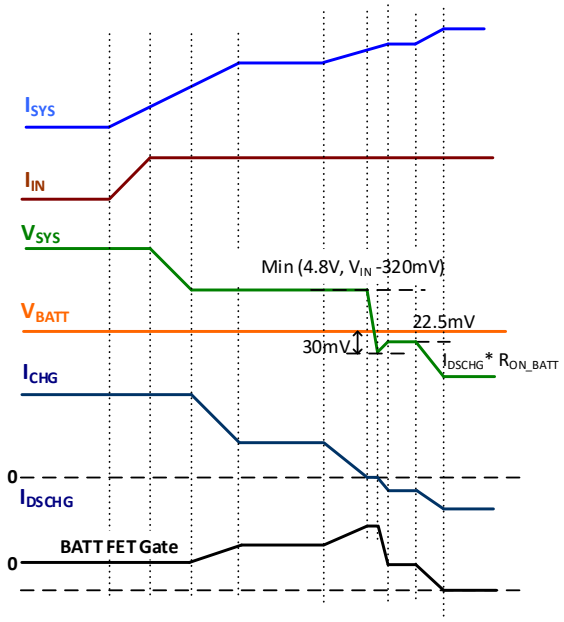


Figure 6: Dynamic Power Management and Battery Supplement Operation Profile

Battery Charge Full Voltage

The battery voltage for the constant voltage regulation phase is V_{BATT_REG}. When V_{BATT_REG} is 4.2V, it has a ±0.5% accuracy over the ambient temperature range of 0°C to +50°C. When the battery is removed, the battery voltage is between V_{BATT_REG} - V_{RECH} and V_{BATT_REG}.

Thermal Regulation and Thermal Shutdown

The IC monitors the internal junction temperature continuously to maximize power delivery and prevent the chip from overheating. When the internal junction temperature reaches the pre-set limit of T_{J_REG} (default 120°C), the IC reduces the charge current to prevent higher power dissipation. The multiple thermal regulation thresholds from 60°C to 120°C help the system design meet the thermal requirement in different applications. The junction temperature regulation threshold is set via REG06 bit[1:0]. When the junction temperature reaches 150°C, both Q1 and Q2 turn off.

Negative Temperature Coefficient (NTC) Temperature Sensor

NTC allows the IC to sense the battery temperature using the thermistor, usually available in the battery pack, to ensure a safe operating environment for the chip. Connect appropriately valued resistors from VDD to NTC to ground. The resistor divider works with a thermistor connected from NTC to ground. The voltage on NTC is determined by the resistor divider, whose divide ratio depends on the battery temperature. The IC sets a pre-determined upper and lower bound of the divide ratio internally for NTC cold and NTC hot.

The NTC function works in charge mode only. Once the NTC voltage falls out of the divide ratio (the temperature is outside the safe operating range), the IC stops the charging. Charging resumes automatically after the temperature falls back into the safe range.

Safety Timer

The IC provides both a pre-charge and a fast charge safety timer to prevent extended charging cycles due to abnormal battery conditions. The pre-charge safety timer is 2 hours when the battery voltage is below V_{BATT_PRE}. The fast charge safety timer begins when the battery enters fast charging. Figure 5 shows the definition of the fast charge timer. The fast charge safety timer is programmed through the I²C. The safety timer feature can be disabled via the I²C.

The following actions restart the safety timer:

- A new charge cycle is initiated
- REG01 bit[3] is written from 0 to 1 (charge enable)
- REG05 bit[3] is written from 0 to 1 (safety timer enable)
- REG01 bit[7] is written from 0 to 1 (software reset)

During PPM, the charge current is reduced because of insufficient input power (input

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2019 MPS. All Rights Reserved.

current limit, input voltage limit), and the timer period can be extended by 2 times through setting TMR2X_EN (REG06 bit[6]) as 1.

1. TMR2X_EN = 1: Enable 2x extended safety timer during PPM
2. TMR2X_EN = 0, (default spec): Disable 2x extended safety timer during PPM

This feature avoids a false trigger indication for bad battery indication when there is little charge current delivered to the battery as a result of insufficient input power.

Host Mode and Default Mode

The IC is a host-controlled device. After the power-on reset, the IC starts up in the watchdog timer expiration state or default mode. All registers are in the default settings.

Any write to the IC switches it into host mode. All charge parameters are programmable. If the watchdog timer (REG05 [5:4]) is not disabled, the host must reset the watchdog timer regularly by writing 1 to REG01 bit[6] before the watchdog timer expires to keep the device in host mode. Once the watchdog timer expires, the IC returns to default mode. The watchdog timer limit can also be programmed or disabled by the host control. When there is no V_{IN}, the watchdog timer is suspended.

Operation also changes to default mode when any of the following conditions occur:

- Refresh input without battery
- Re-insert battery with no V_{IN}
- Register reset REG01 bit[7] is reset

Battery Discharge Function

If the battery is connected and the input source is missing, the battery FET is fully on when V_{BATT} is above the V_{BATT_UVLO} threshold. The 100mΩ battery FET minimizes conduction loss during discharge. The quiescent current of the IC is as low as 11μA in this mode. The low on resistance and low quiescent current help extend the running time of the battery.

Over-Discharge Current Protection

The IC has an over-discharge current protection in discharge mode and supplement mode. Once I_{BATT} exceeds the programmable discharge current limit (default 1.0A), the battery FET is regulated to limit the discharge current.

Similarly, when the battery voltage falls below the programmable V_{BATT_UVLO} threshold (default 2.8V), the battery FET is turned off to prevent over-discharge.

System Short-Circuit Protection (SCP)

The MP2667 features SYS node short-circuit protection (SCP) for both the IN to SYS path and the BATT to SYS path.

The system voltage is monitored continuously. Once V_{SYS} is below 1.5V, the over-current protection threshold for the BATT to SYS path is limited to 2A (fast off). For details, see Figure 12.

If the system short-circuit occurs when both the input and the battery are present, the protection mechanisms for both paths work, with the faster one (the IN to SYS path protection mechanism) dominating the hiccup operation.

Interrupt to Host (INT)

The IC also has an alert mechanism, which can output an interrupt signal via the INT pin to notify the system of the operation by outputting a 256μs low-state INT pulse. Any of the following events will trigger the INT output:

- Good input source detected
- UVLO or input OVP charge completed
- Charging status change
- Any fault in reg08 (watchdog timer fault, input fault, thermal fault, safety timer fault, battery OVP fault, NTC fault)

When any fault occurs, the IC sends out an INT pulse and latches the fault state in reg08. After the IC exits the fault state, the fault bit can be released to 0 after the host reads reg08. The NTC fault is not latched and always reports the current thermistor conditions.

Note that the INT needs the external pull-up resistor for its open-drain connection. A resistance of 100kΩ or greater is recommended.

Battery Disconnection Function

In applications where the battery is not removable, it is essential to disconnect the battery from the system to shipping mode, in

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2019 MPS. All Rights Reserved.

stock mode, or to system reset mode, depending on the application (see Table 3).

1. Shipping Mode:

   Entering shipping mode: The register bit FET_DIS (REG06 bit[5]), makes the IC enter shipping mode. During normal operation, the battery FET is turned on (the bit is 0). If this bit is set to 1 through the I²C, the battery FET is turned off, and the MP2667 enters shipping mode.

   The FET_DIS bit is reset to 0 automatically after the battery FET is turned off.

   Exiting shipping mode: The IC can exit shipping mode by pulling INT down for a very short time (>500ms).

2. Reset Mode:

   The IC can use INT to cut off the path from the battery to the system under the condition needed to reset the system manually.

   If the battery FET is on, once the logic at INT is set to low for more than 8s, the battery is disconnected from the system by turning off the battery FET. The battery can be connected in and out of the system by controlling INT (see Figure 7).

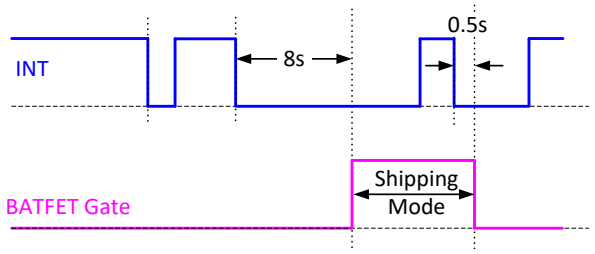


Figure 7: Disconnection Function Operation Profile

Table 3: Battery Disconnection Control

FET On/Off Change by Control	INT Pin	
	H to L for 8s	H to L for 500ms
	Reset Mode	Exit Shipping Mode
LDO FET	x	x
Battery FET (charging)	Off	On
Battery FET (discharging)	Off	On

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2019 MPS. All Rights Reserved.

I²C REGISTER MAP

IC Address: 09h

Input Source Control Register / Address: 00h (Default: 0100 1011)

Bit	Symbol	Description	Read/Write	Default
Bit 7	EN_HIZ (6)	0: Disable 1: Enable	Read/Write	Default: Disable (0)
Input Minimum Voltage Regulation				
Bit 6	V_{IN_MIN} [3]	640mV	Read/Write	Offset: 3.88V Range: 3.88V to 5.08V Default: 4.60V (1001)
Bit 5	V_{IN_MIN} [2]	320mV		
Bit 4	V_{IN_MIN} [1]	160mV		
Bit 3	V_{IN_MIN} [0]	80mV		
Input Current Limit				
Bit 2	I_{IN_LIM} [2]	000: 77mA 001: 118mA 010: 345mA 011: 470mA 100: 540mA 101: 635mA 110: 734mA 111: 993mA	Read/Write	Default: 470mA (011)
Bit 1	I_{IN_LIM} [1]			
Bit 0	I_{IN_LIM} [0]			

Note:

6) This bit only controls the on and off of the LDO FET.

Power-On Configuration Register / Address: 01h (Default: 0000 0100)

Bit	Symbol	Description	Read/Write	Default
Bit 7	Register reset	0: Keep current setting 1: Reset	Read/Write	Keep current register setting (0)
Bit 6	I²C watchdog timer reset	0: Normal 1: Reset	Read/Write	Normal (0)
Bit 5	Reserved			
Bit 4	Reserved			
Charger Configuration				
Bit 3	CEB	0: Charge enable 1: Charge disable	Read/Write	Charge enable (0)
Battery UVLO Threshold				
Bit 2	V_{BATT_UVLO} [2]	0.4V	Read/Write	Offset: 2.4V Range: 2.4V to 3.1V Default: 2.8V (100)
Bit 1	V_{BATT_UVLO} [1]	0.2V		
Bit 0	V_{BATT_UVLO} [0]	0.1V		

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2019 MPS. All Rights Reserved.

I²C REGISTER MAP *(continued)*

Charge Current Control Register / Address: 02h (Default: 0000 0111)

Bit	Symbol	Description	Read/Write	Default
Bit 7	Reserved			
Bit 6	Reserved			
Bit 5	Reserved			
Fast Charge Current Setting				
Bit 4	I_{CC} [4]	528mA	Read/Write	Offset: 26mA Range: 26mA to 1049mA Default: 257mA (00111)
Bit 3	I_{CC} [3]	264mA		
Bit 2	I_{CC} [2]	132mA		
Bit 1	I_{CC} [1]	66mA		
Bit 0	I_{CC} [0]	33mA		

Discharge / Termination Current / Address: 03h (Default: 0100 1001)

Bit	Symbol	Description	Read/Write	Default
Bit 7	Reserved			
BATT to SYS Discharge Current Limit				
Bit 6	I_{DSCHG}[3]	800mA	Read/Write	Offset: 100mA Range: 100mA to 1.6A Default: 1.0A (1001)
Bit 5	I_{DSCHG} [2]	400mA		
Bit 4	I_{DSCHG} [1]	200mA		
Bit 3	I_{DSCHG} [0]	100mA		
Bit 2	Reserved			
Terminal Current				
Bit 1	I_{TERM} [1]	56mA	Read/Write	Offset: 24mA Range: 24mA to 108mA Default: 52mA (01)
Bit 0	I_{TERM} [0]	28mA		

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2019 MPS. All Rights Reserved.

I²C REGISTER MAP *(continued)*

Charge Voltage Control Register / Address: 04h (Default: 1010 0011)

Bit	Symbol	Description	Read/Write	Default
Battery Regulation Voltage				
Bit 7	V_{BATT_REG} [5]	480mV	Read/Write	Offset: 3.60V Range: 3.60V to 4.545V Default: 4.2V (101000)
Bit 6	V_{BATT_REG} [4]	240mV		
Bit 5	V_{BATT_REG} [3]	120mV		
Bit 4	V_{BATT_REG} [2]	60mV		
Bit 3	V_{BATT_REG} [1]	30mV		
Bit 2	V_{BATT_REG} [0]	15mV		
Pre-Charge to Fast Charge Threshold				
Bit 1	V_{BATT_PRE}	0: 2.8V 1: 3.0V	Read/Write	3.0V (1)
Battery Recharge Threshold (below V_{BATT_REG})				
Bit 0	V_{RECH}	0: 150mV 1: 300mV	Read/Write	300mV (1)

Charge Termination / Timer Control Register / Address: 05h (Default: 0100 1010)

Bit	Symbol	Description	Read/Write	Default
Bit 7	Reserved			
Termination Setting (Control of the Termination is Allowed or Not)				
Bit 6	EN_TERM	0: Disable 1: Enable	Read/Write	Enable (1)
I²C Watchdog Timer Limit				
Bit 5	WATCHDOG [1]	00: Disable timer 01: 40s 10: 80s 11: 160s	Read/Write	Disable timer (00)
Bit 4	WATCHDOG [0]			
Safety Timer Setting				
Bit 3	EN_TIMER	0: Disable 1: Enable	Read/Write	Enable timer (1)
Safety Timer for Fast Charging Cycle				
Bit 2	CHG_TMR [1]	00: 20hrs 01: 5hrs 10: 8hrs 11: 12hrs	Read/Write	5hrs (01)
Bit 1	CHG_TMR [0]			
Termination Timer Control (When TERM_TMR is Enabled, the IC Will Not Suspend the Charge Current After Charge Termination)				
Bit 0	TERM_TMR	0: Disable 1: Enable	Read/Write	Disable (0)

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2019 MPS. All Rights Reserved.

I²C REGISTER MAP *(continued)*

Miscellaneous Operation Control Register / Address: 06h (Default: 0000 1011)

Bit	Symbol	Description	Read/Write	Default
Bit 7	Reserved			
Bit 6	TMR2X_EN	0: Disable 2x extended safety timer during PPM 1: Enable 2x extended safety timer during PPM	Read/Write	Disable (0)
Bit 5	FET_DIS (7)	0: Enable 1: Turn off	Read/Write	Enable (0)
Bit 4	Reserved			
Bit 3	EN_NTC	0: Disable 1: Enable	Read/Write	Enable (1)
Bit 2	Reserved			
Thermal Regulation Threshold				
Bit 1	T_{J_REG} [1]	00: 60°C 01: 80°C 10: 100°C 11: 120°C	Read/Write	Default: 120°C (11)
Bit 0	T_{J_REG} [0]			

Note:

7) This bit only controls the on and off of the battery FET, including charge and discharge.

System Status Register / Address: 07h (Default: 0000 0000)

Bit	Symbol	Description	Read/Write	Default
Bit 7	Reserved			
Revision				
Bit 6	Rev [1]	Revision number	Read-only	(00)
Bit 5	Rev [0]			
Bit 4	CHG_STAT [1]	00: Not charging 01: Pre-charge 10: Charge 11: Charge done	Read-only	Not charging (00)
Bit 3	CHG_STAT [0]			
Bit 2	PPM_STAT	0: No PPM 1: In PPM	Read-only	No PPM (0) (no power-path management happens)
Bit 1	PG_STAT	0: Power fail 1: Power good	Read-only	Not power good (0)
Bit 0	THERM_STAT	0: No thermal regulation 1: In thermal regulation	Read-only	Normal (0)

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2019 MPS. All Rights Reserved.

I²C REGISTER MAP *(continued)*

Fault Register / Address: 08h (Default: 0000 0000)

Bit	Symbol	Description	Read/Write	Default
Bit 7	Reserved			
Bit 6	WATCHDOG_ FAULT	0: Normal 1: Watchdog timer expiration	Read-only	Normal (0)
Bit 5	VIN_FAULT	0: Normal 1: Input fault (OVP or bad source)	Read-only	Normal (0)
Bit 4	THEM_SD	0: Normal 1: Thermal shutdown	Read-only	Normal (0)
Bit 3	BAT_FAULT	0: Normal 1: Battery OVP	Read-only	Normal (0)
Bit 2	STMR_FAULT	0: Normal 1: Safety timer expiration	Read-only	Normal (0)
Bit 1	Reserved			
Bit 0	Reserved			

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2019 MPS. All Rights Reserved.

ONE-TIME PROGRAMMING MAP

#	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x02	N/A			I_{CC}: 26mA to 1049mA / 33mA step				
0x03	N/A						I_{TERM}	
0x04	V_{BATT_REG}: 3.6V to 4.545V / 15mV step						N/A	
0x05	N/A		WATCHDOG		N/A			

ONE-TIME PROGRAMMING DEFAULT

One-Time Programmable Items	Default
I_{CC}	257mA
I_{TERM}	52mA
V_{BATT_REG}	4.2V
WATCHDOG	Disable timer

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2019 MPS. All Rights Reserved.

STATE CONVERSION CHART

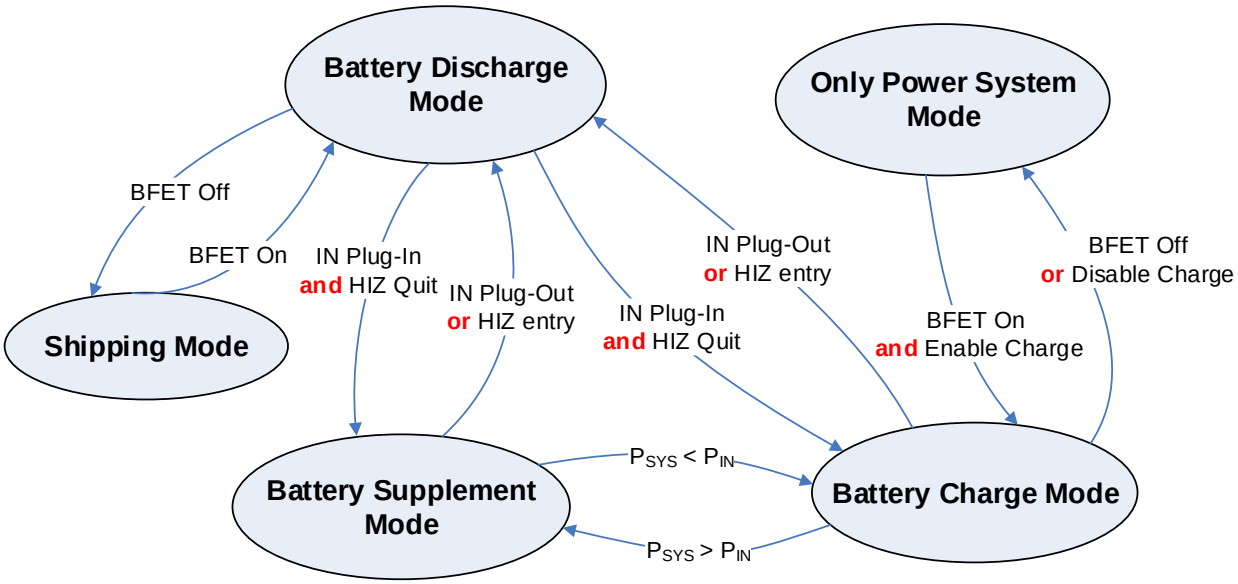


Figure 8: State Machine Conversion

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2019 MPS. All Rights Reserved.

CONTROL FLOWCHART

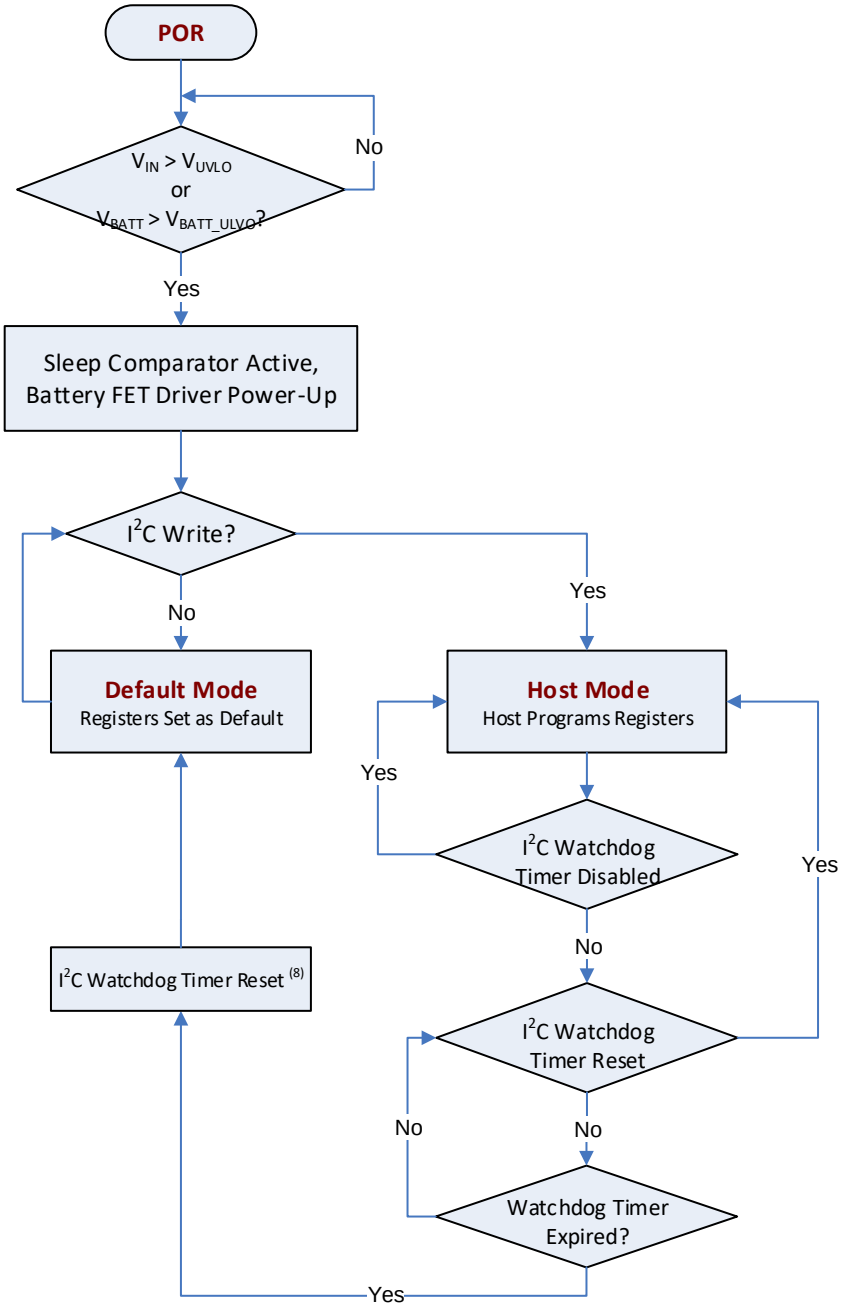


Figure 9: Default Mode and Host Mode Selection (9)

Note:

8) Once the watchdog timer expires, the I²C watchdog timer reset is required, or the watchdog timer is not valid in the next cycle.
9) The watchdog timer is held when V_{IN} is not present.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2019 MPS. All Rights Reserved.

CONTROL FLOWCHART *(continued)*

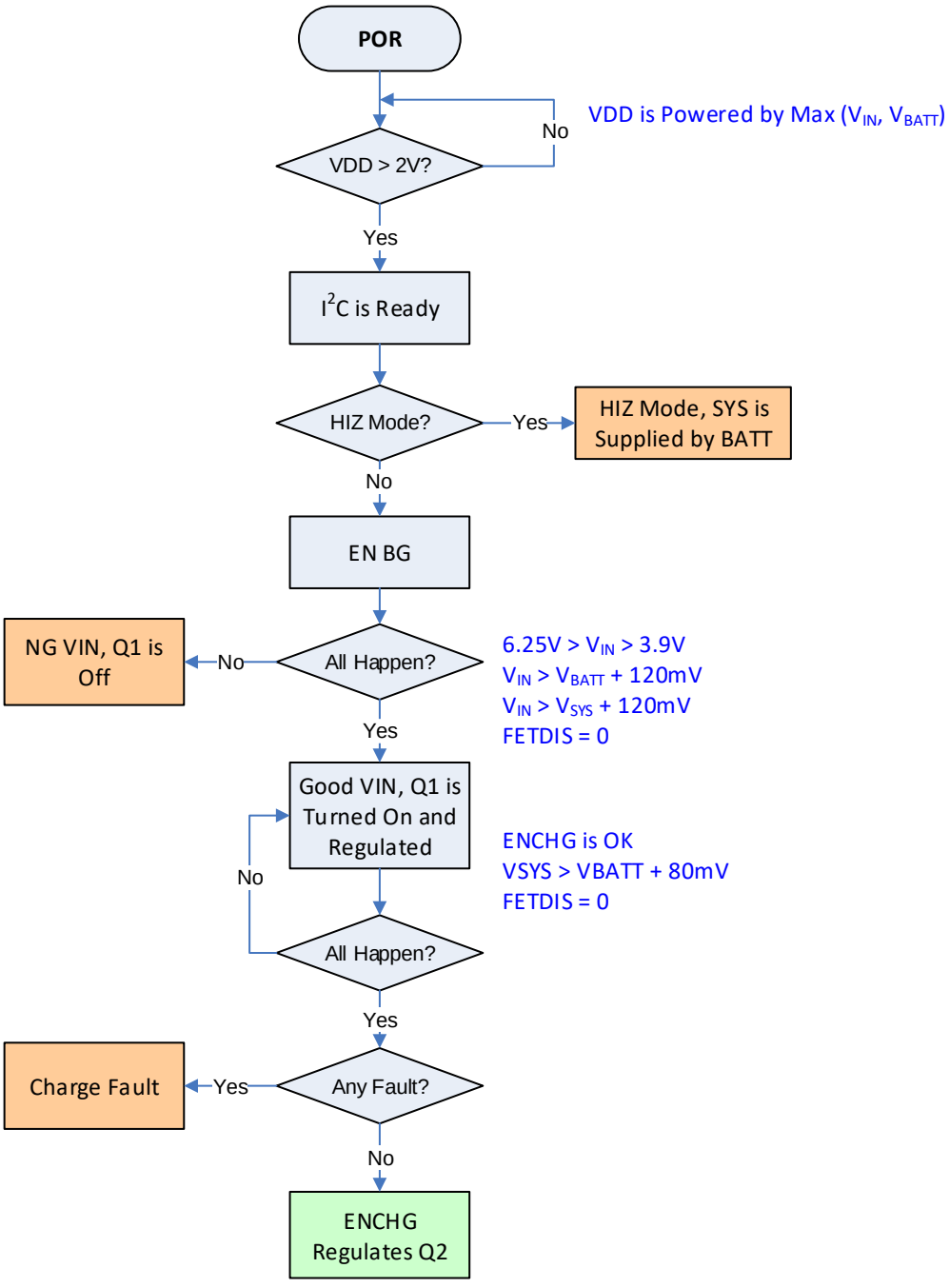


Figure 10: Input Power Start-Up Flowchart

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2019 MPS. All Rights Reserved.

CONTROL FLOWCHART *(continued)*

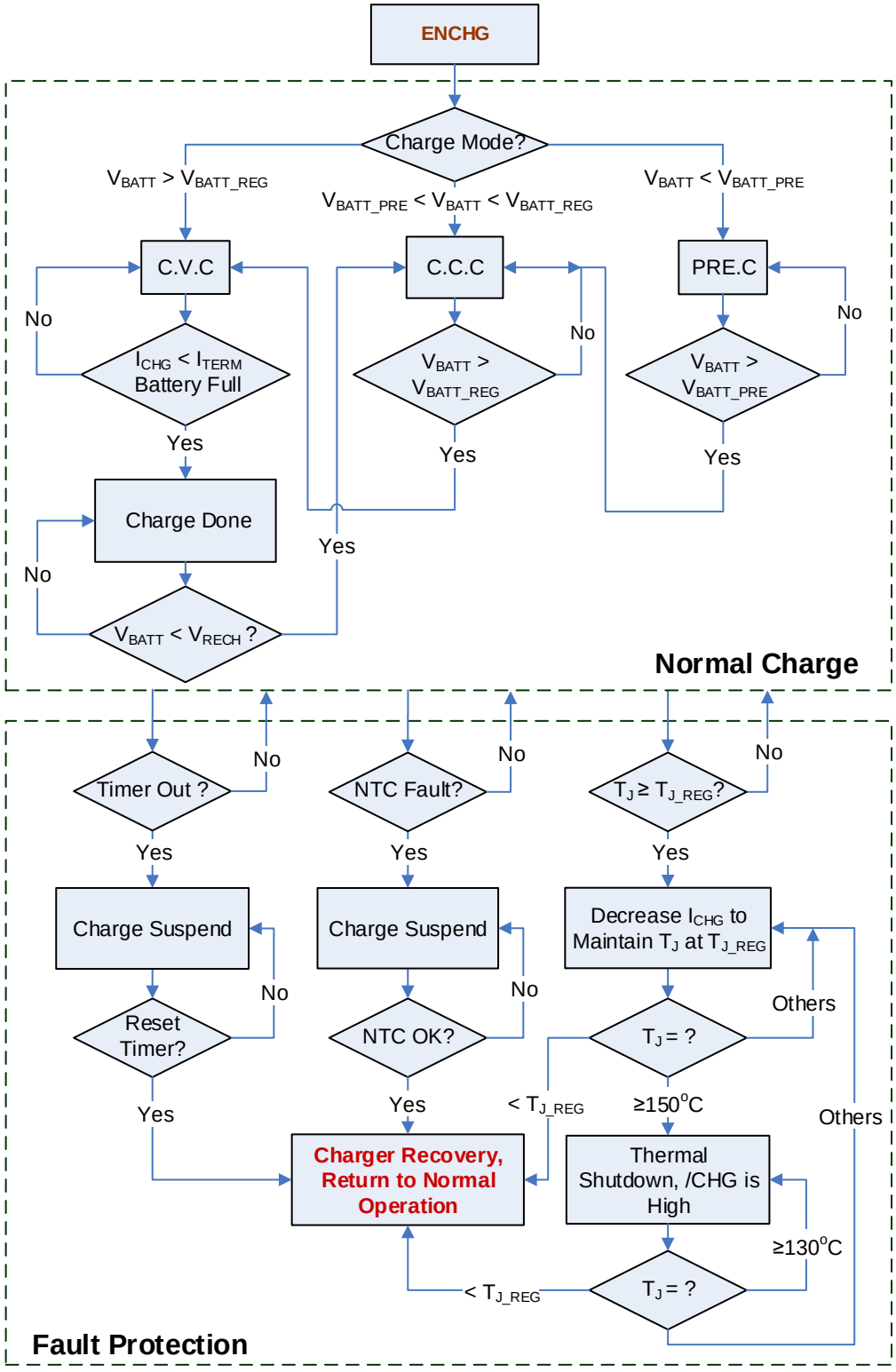


Figure 11: Charging Process

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2019 MPS. All Rights Reserved.

CONTROL FLOWCHART *(continued)*

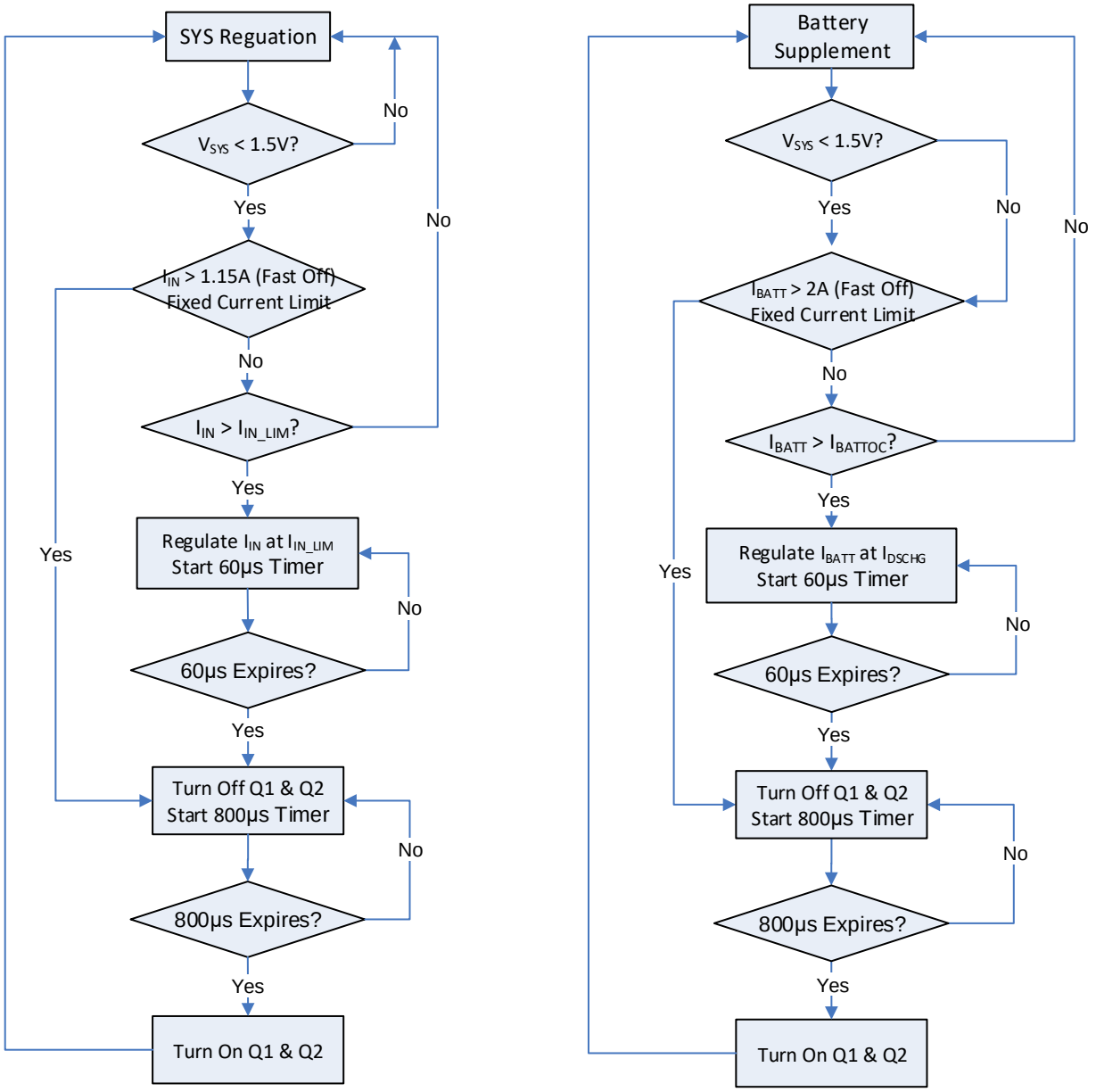


Figure 12: System Short-Circuit Protection

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2019 MPS. All Rights Reserved.

APPLICATION INFORMATION

Selecting a Resistor for the NTC Sensor

Figure 13 shows an internal resistor divider reference circuit to limit the low-temperature threshold and high-temperature threshold at V_{HOT} and V_{COLD}, respectively.

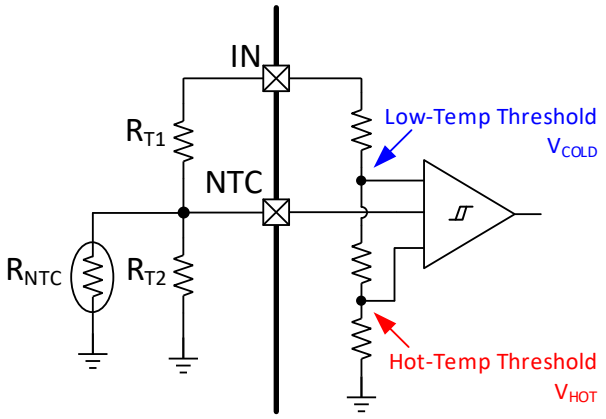


Figure 13: NTC Function Block

For a given NTC thermistor, set the NTC window by selecting appropriate R_{T1} and R_{T2} values with Equation (1) and Equation (2):

$$\frac{R_{T2} // R_{NTC_Cold}}{R_{T1} + R_{T2} // R_{NTC_Cold}} = V_{COLD} \quad (1)$$

$$\frac{R_{T2} // R_{NTC_Hot}}{R_{T1} + R_{T2} // R_{NTC_Hot}} = V_{HOT} \quad (2)$$

Where R_{NTC_Hot} is the NTC resistor value at the high end of the required temperature operation range, and R_{NTC_Cold} is the NTC resistor value at a low temperature. The two resistors (R_{T1} and R_{T2}) allow the high-temperature limit and low-temperature limit to be programmed independently. With this feature, the MP2667 can fit most NTC resistor types and different temperature operation range requirements.

The R_{T1} and R_{T2} values depend on the type of NTC resistor used. For example, for the thermistor 103AT-2, R_{NTC_Cold} is 27.28kΩ at 0°C, and R_{NTC_Hot} is 4.16kΩ at 50°C.

Equation (1) and Equation (2) can be used to calculate R_{T1} = 6.59kΩ and R_{T2} = 24.07kΩ, assuming that the NTC window is between 0°C and 50°C, and using the V_{COLD} and V_{HOT} values from the EC table.

Selecting the External Capacitor

Like most low-dropout regulators, the MP2667 requires external capacitors for regulator stability and voltage spike immunity. The device is designed specifically for portable applications requiring minimal board space and small components. These capacitors must be selected correctly for optimal performance.

An input capacitor is required for stability. A minimum 1µF capacitor must be connected between IN to GND for stable operation over the entire load current range. There can be more output capacitance than input as long as the input is at least 1µF.

The IC is designed specifically to work with a very small ceramic output capacitor (typically 2.2µF). A minimum 2.2µF ceramic capacitor with X5R or X7R type dielectrics is suitable in the MP2667 application circuit. The output capacitor should be connected between SYS and GND with thick traces and small loop area.

A capacitor from BATT to GND is also necessary for the MP2667, and the typical capacitance value is 10µF. A ceramic capacitor with X5R or X7R type dielectrics at least 10µF is suitable for the application circuit.

A capacitor between VDD and GND is used to stabilize the VDD voltage to power the internal control and logic circuit. The typical value of this capacitor is 100nF.

PCB Layout Guidelines

Efficient PCB layout is critical for stable operation of the MP2667. For best results, follow the guidelines below:

1. Place the external capacitors as close to the IC as possible to ensure the smallest input inductance and ground impedance.
2. Place the PCB trace connecting the capacitor between VDD and GND as close as possible to the IC.
3. Keep the signal GND for the I²C wire clean.
4. Route the I²C wires (SDA and SCL) parallel with each other.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2019 MPS. All Rights Reserved.

TYPICAL APPLICATION CIRCUIT

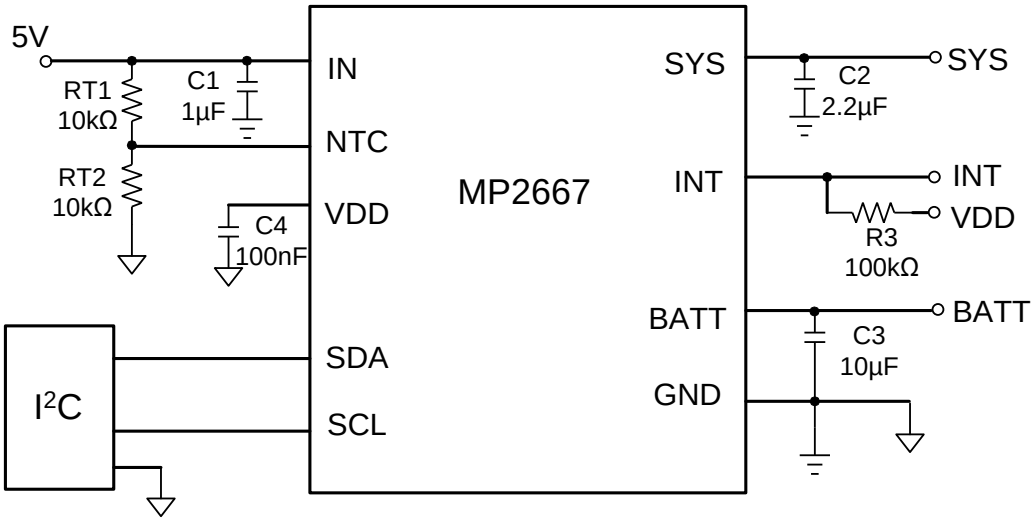


Figure 14: MP2667 Typical Application Circuit with 5V Input

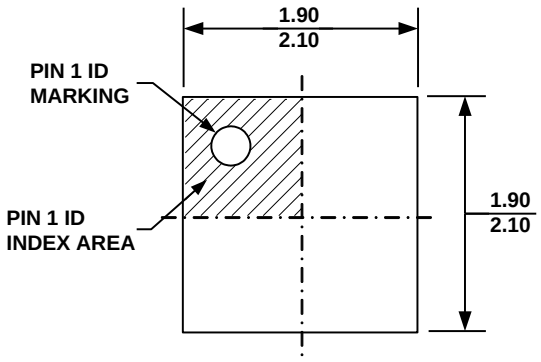
Table 4: The Key BOM of Figure 14

Qty	Ref	Value	Description	Package	Manufacture
1	C1	1µF	Ceramic capacitor, 16V, X5R or X7R	0603	Any
1	C2	2.2µF	Ceramic capacitor, 16V, X5R or X7R	0603	Any
1	C3	10µF	Ceramic capacitor, 16V, X5R or X7R	0603	Any
1	C4	100nF	Ceramic capacitor, 16V, X5R or X7R	0603	Any
2	R_{T1}, R_{T2}	10kΩ	Film resistor, 1%	0603	Any

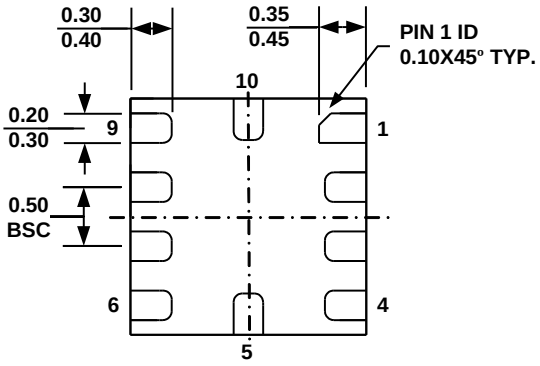
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2019 MPS. All Rights Reserved.

PACKAGE INFORMATION

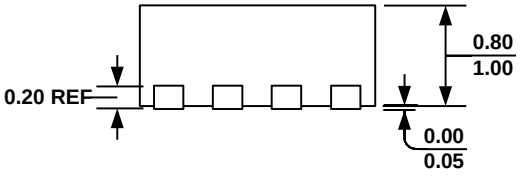
QFN-10 (2mmx2mm)



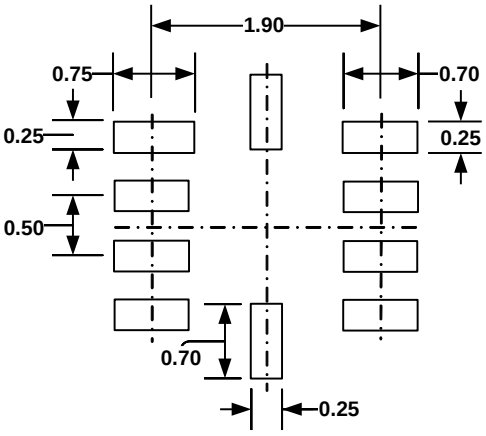
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETER MAX.
4) JEDEC REFERENCE IS MO-220, VARIATION VCCD.
5) DRAWING IS NOT TO SCALE.

NOTICE: The information in this document is subject to change without notice. Please contact MPS for current specifications. Users should warrant and guarantee that third-party Intellectual Property rights are not infringed upon when integrating MPS products into any application. MPS will not assume any legal responsibility for any said applications.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2019 MPS. All Rights Reserved.