MP2672A

Boost Charger with Cell Balance for 2-Cell Lithium-Ion Batteries in Series

DESCRIPTION

The MP2672A is a highly integrated, flexible switch-mode battery charger IC for Lithium-ion batteries with two cells in series. This makes it applicable for a wide range of portable applications.

When an input power supply is present, the MP2672A operates in boost mode to charge the battery with two cells in series. When charging is enabled, the MP2672A automatically detects the battery voltage and charges the battery in three phases: pre-charge, constant current charge, and constant voltage charge. Other features include charge termination and auto-recharge.

The device also has a narrow voltage DC (NVDC) power structure. With a deeply discharged battery, the MP2672A regulates the system output to a minimum voltage level. This powers the system instantly while simultaneously charging the battery via the battery FET.

The MP2672A provides a cell balance function. It can monitor the voltage across each cell, then equalize the cell's voltages if the difference between the two cells exceeds the mismatch threshold.

The device has two configuration modes: standalone mode and host-control mode. In standalone mode, the charging parameters can be configured by hardware pins. In host-control mode, the charging parameters can be configured by the I^2C registers.

Diverse and robust protections include a thermal regulation loop to decrease the charge current in case the junction temperature exceeds the thermal loop threshold, and battery temperature protection that is compliant with JEITA standards. Other safety features include input over-voltage protection (OVP), battery OVP, thermal shutdown, battery temperature monitoring, a watchdog timer, and a configurable backup timer to prevent prolonged charging of a dead battery.

The MP2672A is available in a QFN-18 (2mmx3mm) package.

FEATURES

- 4.0V to 5.75V Operating Input Voltage
- Up to 14V Sustainable Voltage
- Up to 2A Configurable Charge Current for Battery with 2 Cells in Series
- Compatible with Host-Control or Standalone Mode
- NVDC Power Path Management
- Configurable Input Voltage Limit
- Configurable Charge Voltage with 0.5% Accuracy
- No External Sense Resistor Required
- Integrated Cell-Balancing Circuit for Mismatched Cells
- Preconditioning for Fully Depleted Battery
- Flexible New Charging Cycle Initiation
- Charging Operation Indicator in Standalone Mode
- Missing Battery Detection in Host-Control Mode
- I^2C Port for Flexible System Parameter Setting and Status Reporting in Host-Control Mode
- Negative Temperature Coefficient (NTC) Pin for Temperature Monitoring Compliant with JEITA Standards
- Built-In Charging Protection and Configurable Safety Timer
- MOSFET Cycle-by-Cycle Over-Current Protection (OCP)
- Thermal Regulation and Thermal Shutdown
- Available in a QFN-18 (2mmx3mm) Package

APPLICATIONS

- Portable Handheld Solutions
- Point-of-Sale (POS) Machines
- Bluetooth Speakers
- E-Cigarettes
- General 2-Cell Applications

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TYPICAL APPLICATIONS

Standalone Mode

Use a resistor to connect the CV pin to AGND. Set the battery-full voltage according to Table 1.

Table 1: Battery Voltage Settings

R_{VBATT} Range	V_{BATT_REG}
30kΩ to 35kΩ	8.4V
70kΩ to 75kΩ	8.6V
100kΩ to 105kΩ	8.7V
130kΩ to 135kΩ	8.8V

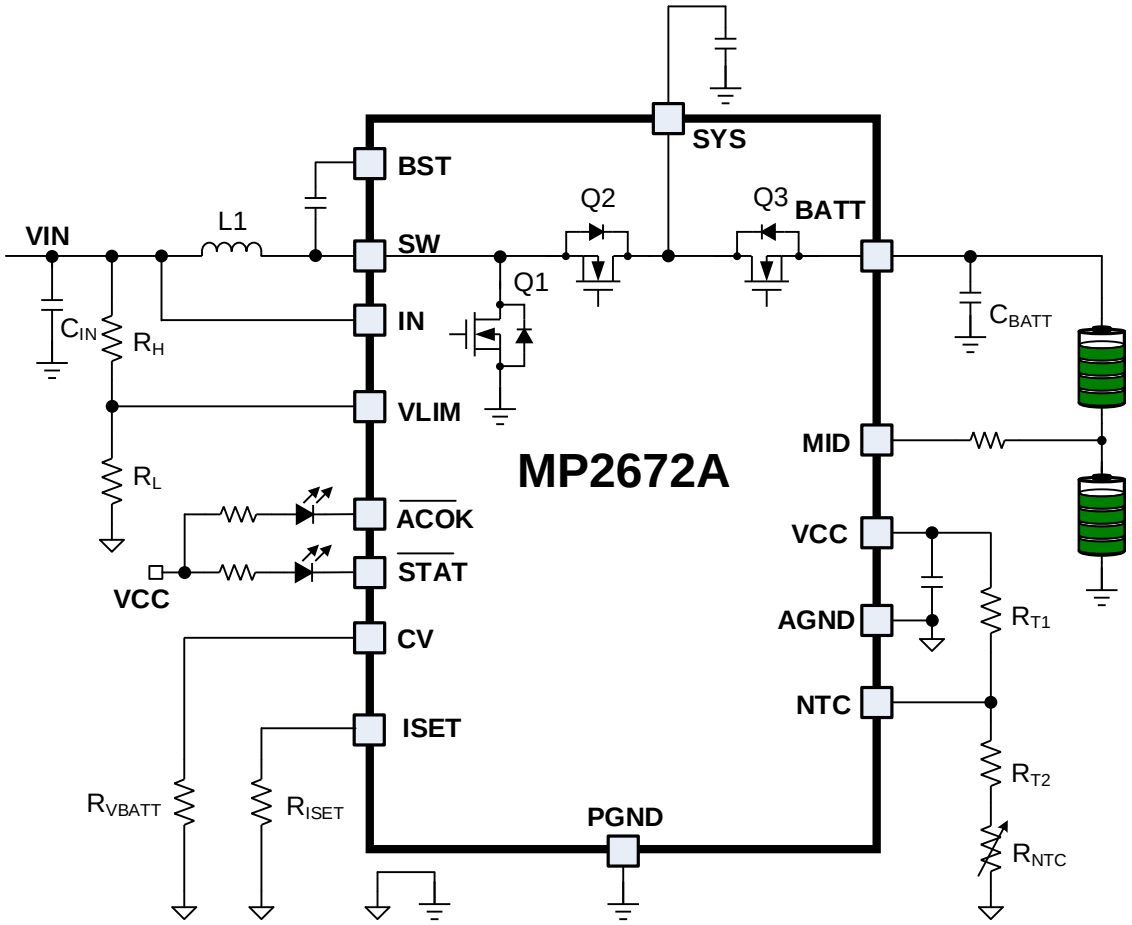


Figure 1: Typical Application in Standalone Mode

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TYPICAL APPLICATIONS *(continued)*

Host-Control Mode

Connect the CV pin to VCC. Set the battery-full voltage according to the I²C register (see Figure 2).

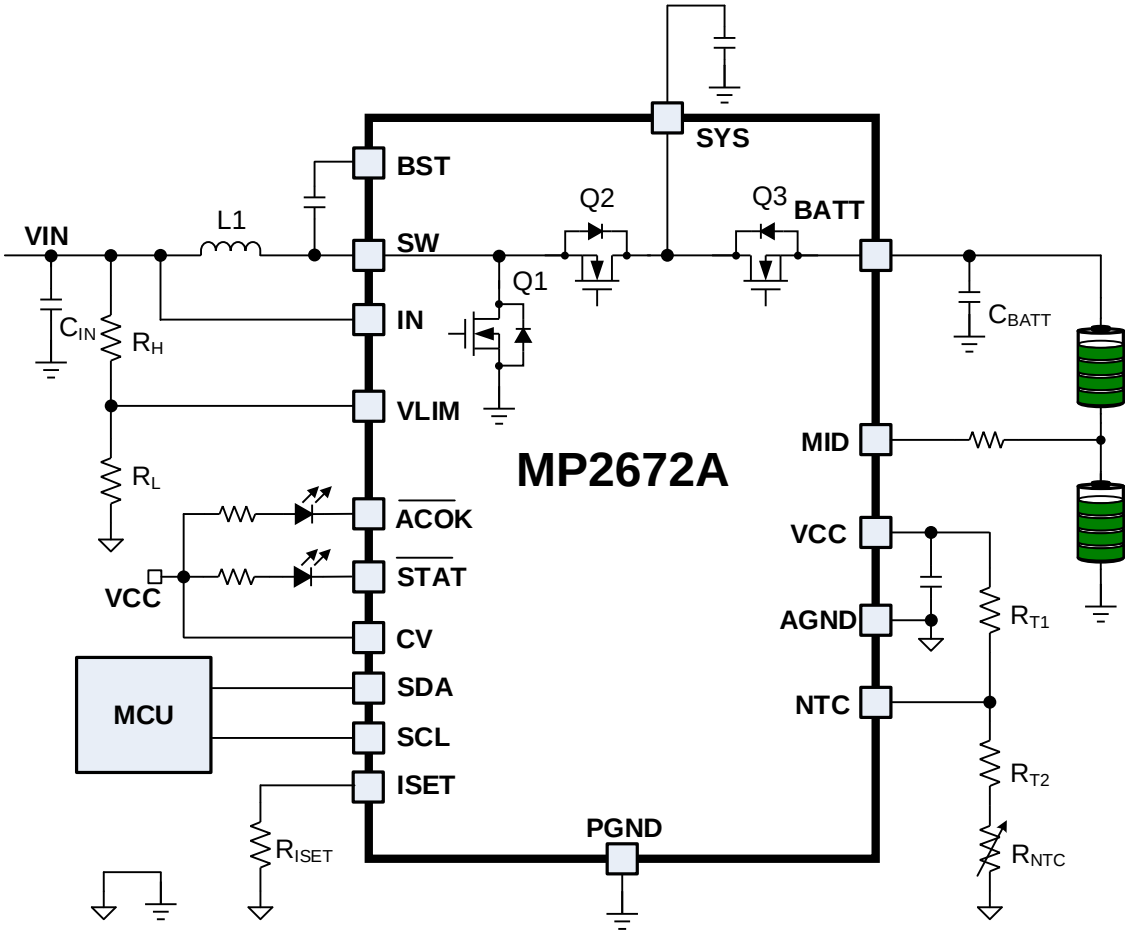


Figure 2: Typical Application in Host Control Mode

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ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MP2672AGD-xxxx**	QFN-18 (2mmx3mm)	*See Below*	1
EVKT-MP2672A	Evaluation kit	N/A	N/A

*For Tape & Reel, add suffix –Z (e.g. MP2672AGD–xxxx–Z).

**"-xxxx" is the register setting option. The factory default is "-0000". This content can be viewed in the I²C Register Map section starting on page 28. For custom options, contact an MPS FAE to obtain an "-xxxx" value.

TOP MARKING

BNJ
YWW
LLLL

BNJ: Product code
Y: Year code
WW: Week code
LLLL: Lot number

EVALUATION KIT EVKT-MP2672A

EVKT-MP2672A kit contents (items below can be ordered separately):

#	Part Number	Item	Quantity
1	EV2672A-D-00A	MP2672A evaluation board	1
2	EVKT-USBI2C-02 bag	Includes one USB to I²C communication interface, one USB cable, and one ribbon cable	1
3	Online resources	Include datasheet, user guide, product brief, and GUI	1

Order directly from MonolithicPower.com or our distributors.

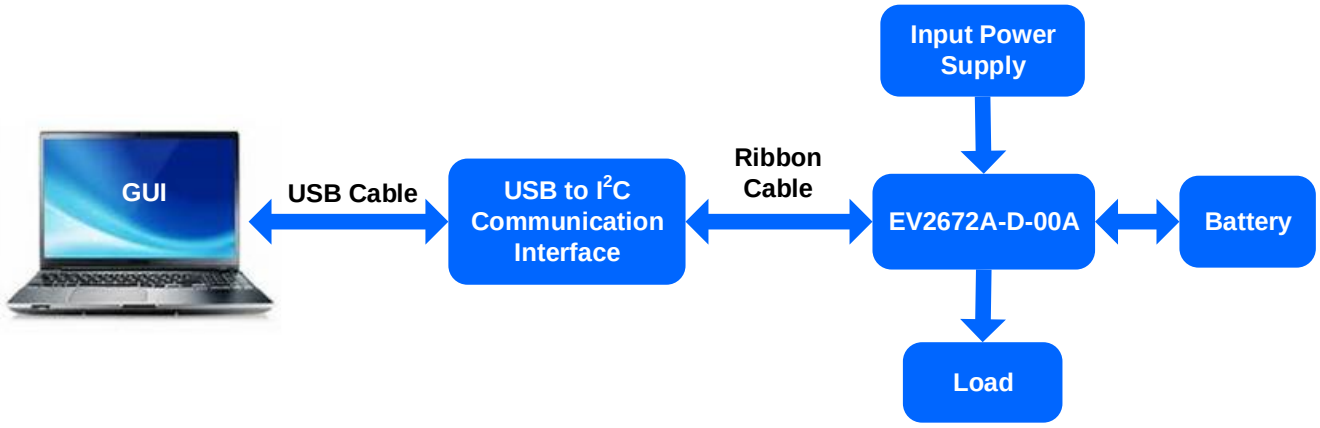
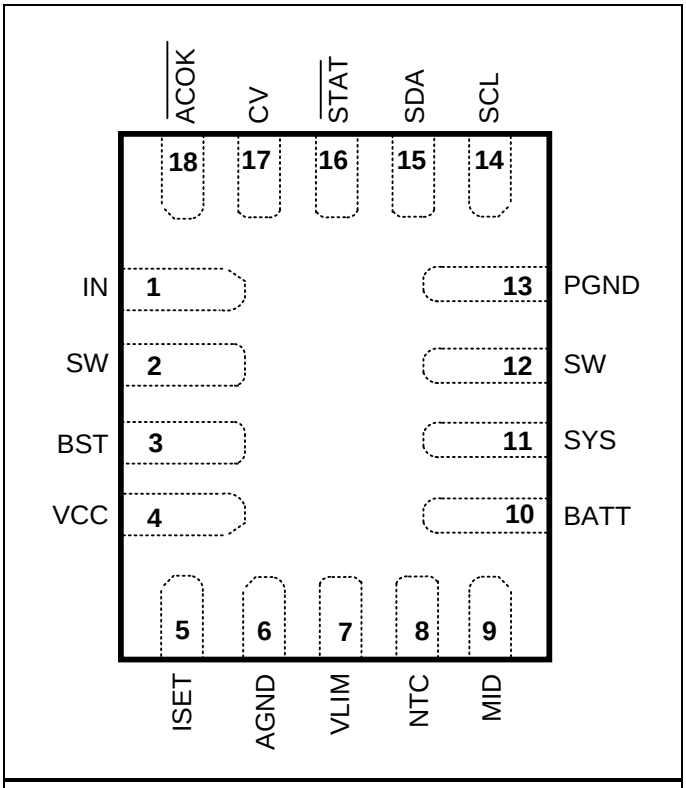


Figure 3: EVKT-MP2672A Evaluation Kit Set-Up

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PACKAGE REFERENCE



QFN-18 (2mmx3mm)

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PIN FUNCTIONS

Pin #	Name	Type (1)	Description
1	IN	P	**Input power pin.**
2, 12	SW	P	**Switching node.** The SW pin is the middle point between the MP2672A's high-side and low-side MOSFETs.
3	BST	P	**Bootstrap.** Connect a bootstrap capacitor between the BST and SW pins to provide a floating supply for the high-side FET driver.
4	VCC	P	**Internal LDO output pin.** Bypass a 1µF ceramic capacitor from this pin to AGND. It is not recommended to pull more than 20mA from this pin.
5	ISET	AI	**Charge current setting.** Connect an external resistor from this pin to AGND to configure the charge current. This also limits the maximum charge current in host-control mode.
6	AGND	P	**Analog ground.**
7	VLIM	AI	**Input voltage limit feedback pin.** Connect a resistor divider from IN to AGND to configure the minimum input voltage limit threshold.
8	NTC	AI	**Battery temperature-sense input.** Connect NTC to a negative temperature coefficient thermistor. Configure the temperature window with a voltage divider connected from VRNTC to NTC to AGND. Configurable JEITA thresholds are supported. See the Negative Temperature Coefficient (NTC) Thermistor section on page 23 for more details.
9	MID	P	**Middle point of the high-side and low-side cells.** The MID pin measures the voltage of each cell and provides a balance path for each cell. Connect MID to AGND to disable the cell balance function.
10	BATT	P	**Battery positive terminal.** Connect a capacitor from BATT to PGND, and place it as close as possible to the IC.
11	SYS	P	**System output.** Connect a capacitor from SYS to PGND, and place it as close as possible to the IC.
13	PGND	P	**Power ground.**
14	SCL	DI	**I²C interface clock pin.** This pin is only valid if the CV pin is connected to VCC.
15	SDA	DIO	**I²C interface data pin.** This pin is only valid if the CV pin is connected to VCC.
16	$\overline{\text{STAT}}$	DO	**Charging operation indicator.** This pin is an open-drain output.
17	CV	AI	**Operation mode and battery voltage control pin.** Pull CV to VCC to configure the IC to host-control mode. Connect an external resistor to AGND to configure IC to standalone mode. In standalone mode, configure the battery-full voltage via the CV pin's resistor.
18	$\overline{\text{ACOK}}$	DO	**Valid input supply indicator.** This pin is an open-drain output. It is pulled low when the input voltage exceeds the under-voltage lockout threshold (V_{IN_UVLO}) and is below the over-voltage lockout threshold (V_{IN_OVLO}).

Note:

1) AI = analog input, DI = digital input, DO = digital output, DIO = digital input and output, P = power.

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ABSOLUTE MAXIMUM RATINGS (2)

BATT.....-0.3V to +14V
SW.....-0.3V (-2V for 50ns) to +14V
SYS.....-0.3V to +14V
MID, IN.....-0.3V to +12V
BST to SW.....-0.3V to +5V
All other pins to AGND.....-0.3V to +5V
Continuous power dissipation.....(T_A = 25°C) (3)
..... 1.78W
Junction temperature .....150°C
Lead temperature (solder) .....260°C
Storage temperature.....-65°C to +150°C

ESD Ratings

Human body model (HBM) (5) 2000V
Charged device model (CDM) (6) 250V

Recommended Operating Conditions (4)

IN to PGND..... 4V to 5.75V
BATT to PGND .....Up to 9V
I_{CC}.....Up to 2A
I_{DSCHG}.....Up to 3A
I_{SYS} .....Up to 2A
Operating junction temp (T_J).... -40°C to +125°C

Thermal Resistance (7) θ_{JA} θ_{JC}

QFN-18 (2mmx3mm)	70	15	°C/W

Notes:

2) Exceeding these ratings may damage the device.
3) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can cause excessive die temperature, and the regulator may go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
4) The device is not guaranteed to function outside of its operating conditions.
5) Per ANSI/ESDA/JEDEC JS-001.
6) Per JESD22-C101.
7) Measured on JESD51-7, 4-layer PCB.

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ELECTRICAL CHARACTERISTICS

V_{IN} = 5V, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Input Power Characteristics						
Input over-voltage lockout (OVLO) threshold	V_{IN_OVLO}	V_{IN} rising	5.75	6.0	6.25	V
Input OVLO threshold hysteresis				150		mV
Input under-voltage lockout (UVLO) threshold	V_{IN_UVLO}	V_{IN} falling	3.25	3.45	3.65	V
Input UVLO threshold hysteresis				150		mV
Boost Converter						
VCC LDO output	V_{VCC}	V_{IN} = 5V, I_{VCC} = 20mA	3.5	3.6	3.7	V
Low-side N-channel MOSFET on resistance	R_{ON_Q1}			54	70	mΩ
High-side N-channel MOSFET on resistance	R_{ON_Q2}			28	40	mΩ
Peak current limit for low-side N-channel MOSFET	I_{LS_PK}	V_{IN}=5V	6	7		A
Valley current limit for high-side N-channel MOSFET	I_{HS_VL}	V_{IN}=5V	5	6		A
Operating frequency	f_{SW}	REG07H, bit[7] = 1	1100	1270	1440	kHz
System regulation minimum voltage (V_{BATT_PRE} + V_{TRACK})		REG00H, bits[3:1] = 100, V_{BATT} = 5V	6.55	6.7	6.85	V
Battery track regulation voltage	V_{TRACK}			300		mV
Battery Charger						
Pre-charge threshold	V_{BATT_PRE}	REG00H, bits[3:1] = 000	5.9	6.05	6.2	V
		REG00H, bits[3:1] = 100	6.25	6.4	6.55	
		REG00H, bits[3:1] = 111	6.6	6.75	6.9	
Pre-charge threshold hysteresis		V_{BATT} falling		250		mV
Pre-charge current	I_{PRE}	V_{BATT} = 5.9V	230	320	410	mA

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ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 5V, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Fast charge current	I_{CC}	REG01H, bits[3:0] = 0101, R_{ISET} = 6kΩ	0.9	1	1.1	A
		REG01H, bits[3:0] = 1111, R_{ISET} = 6kΩ	1.8	2	2.2	A
Termination charge current	I_{TERM}	If I_{CC} > 1.5A, as a percentage of I_{CC}	8	11	14	%
		If I_{CC} ≤ 1.5A (setting)	130	160	190	mA
Input minimum voltage regulation reference	$V_{IN_MIN_REF}$		1.18	1.2	1.22	V
Battery charge voltage regulation	$V_{BATT_REG_ACC}$	V_{BATT_REG} = 8.3V, host-control mode, REG00H, bits[7:5] = 000	-0.50		+0.50	%
		V_{BATT_REG} = 8.4V, host-control mode: REG00H, bits[7:5] = 001, standalone mode: R_{VBATT} = 30kΩ				
		V_{BATT_REG} = 8.8V, host-control mode: REG00H, bits[7:5] = 101, standalone mode: R_{VBATT} = 135kΩ				
		V_{BATT_REG} = 8.2V, host-control mode, REG00H, bits[7:5] = 111				
Recharge threshold below V_{BATT_REG}	V_{RECH}			450		mV
Battery pack over-voltage protection (OVP) threshold	V_{BATT_OVP}	As a percentage of V_{BATT_REG}	102	104	105	%
Battery pack OVP hysteresis		REG00H, bit[0] = 0		150		mV
SYS-to-BATT N-channel MOSFET on resistance	R_{ON_Q3}		22	31	40	mΩ
Battery quiescent current	I_{BATT_Q}	V_{IN} < V_{IN_UVLO}, V_{BATT} = 8.4V, system no load	19	31	42	μA
$\overline{ACOK}$, $\overline{STAT}$, pin output low voltage		Sinking 1.5mA			400	mV
$\overline{ACOK}$, $\overline{STAT}$, pin leakage current		Connected to 5V			1	μA

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ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 5V, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Termination deglitch time	t_{TERM_DGL}			180		ms
Recharge deglitch time	t_{RECH_DGL}			180		ms
Battery Temperature Monitoring (JEITA)						
NTC low temp rising threshold	V_{COLD}	As a percentage of V_{CC}	70	71	72	%
NTC low temp rising threshold hysteresis		As a percentage of V_{CC}		2.4		%
NTC cool temp rising threshold	V_{COOL}	As a percentage of V_{CC}	62	63	64	%
NTC cool temp rising threshold hysteresis		As a percentage of V_{CC}		2.2		%
NTC warm temp falling threshold	V_{WARM}	As a percentage of V_{CC}	39.4	40.4	41.4	%
NTC warm temp falling threshold hysteresis		As a percentage of V_{CC}		2.5		%
NTC hot temp falling threshold	V_{HOT}	As a percentage of V_{CC}	33.5	34.5	35.5	%
NTC hot temp falling threshold hysteresis		As a percentage of V_{CC}		2.5		%
Thermal Regulation and Protection						
Thermal shutdown temperature	T_{J_SHDN}	Rising threshold		150		°C
Thermal shutdown hysteresis		Temperature falling		20		°C
Cell Balance Function						
Internal balance FET on resistance	R_{ON_BHS}			2.1		Ω
	R_{ON_BLS}			1.3		Ω
Cell balance starting voltage threshold	V_{CELL_BAL}	I^2C-configurable, REG01H, bit[6] = 0	3.35	3.5	3.65	V
Cell voltage high-to-low cell mismatch threshold	$V_{CELL_DIFF_HTL}$	REG01H, bit[5] = 0		50	70	mV
Cell voltage high-to-low cell mismatch threshold hysteresis				52		mV
Cell voltage low-to-high cell mismatch threshold	$V_{CELL_DIFF_LTH}$	REG01H, bit[4] = 0		50	70	mV
Cell voltage low-to-high cell mismatch threshold hysteresis				58		mV
High-side cell OVP threshold	V_{HCELL_OVP}	As a percentage of the battery-full voltage	101	102.5	104	%
Low-side OVP threshold	V_{LCELL_OVP}	As a percentage of the battery-full voltage	101	102.5	104	%

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ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 5V, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
I²C Communication Interface						
Input high threshold level	V_{IH}	$V_{PULL\ UP}$ = 1.8V	1.3			V
Input low threshold level	V_{IL}	V_{PULL_UP} = 1.8V			0.4	V
Output low threshold level	V_{OL}	I_{SINK} = 5mA			0.4	V
I²C clock frequency	f_{SCL}				400	kHz
Timing Characteristics						
Clock frequency	f_{CLK}			131		kHz
Watchdog timer(8)	t_{WTD}	REG02H, bits[5:4] = 01		40		sec
Safety charge timer	t_{TMR}	I²C-configurable, REG02H, bits[2:1] = 11	16	20		hours
Pre-charge timer				1		hours

Note:

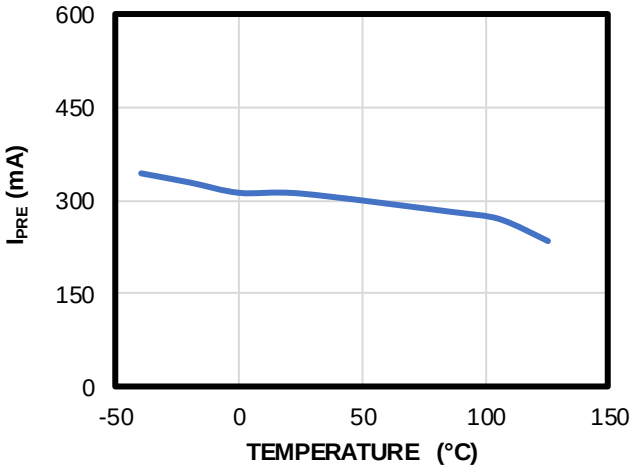
8) Guaranteed by design

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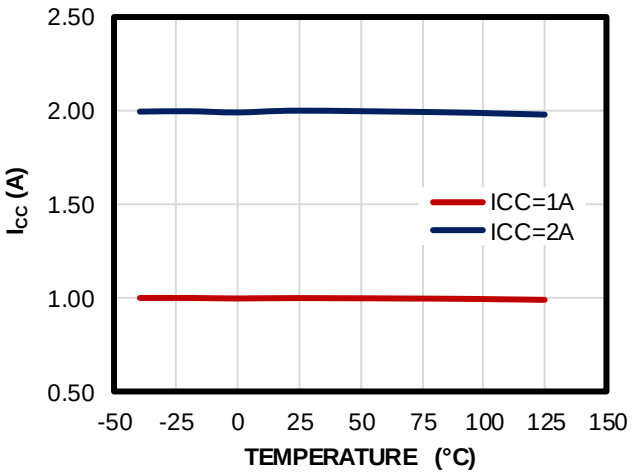
TYPICAL CHARACTERISTICS

I_{PRE} vs. Junction Temperature

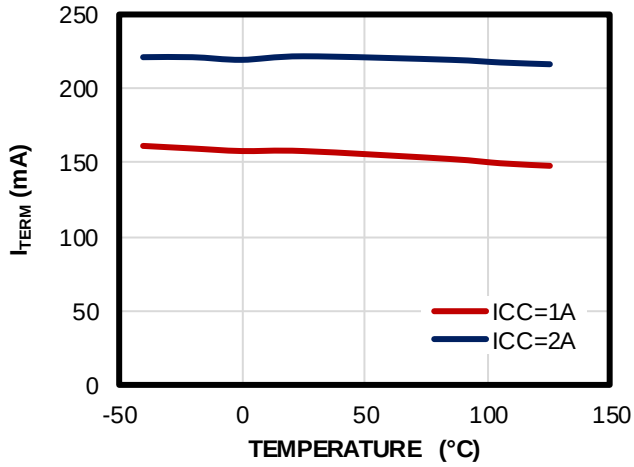
V_{BATT} = 5V



I_{CC} vs. Junction Temperature

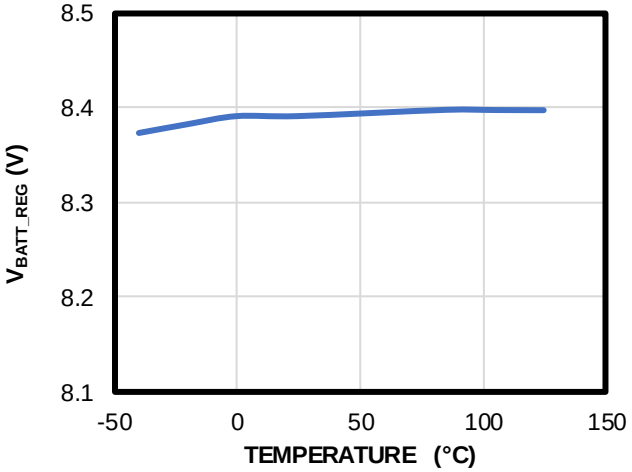


I_{TERM} vs. Junction Temperature

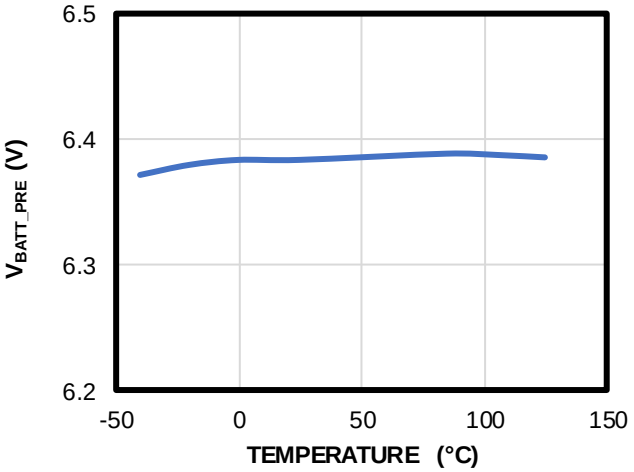


V_{BATT_REG} vs. Junction Temperature

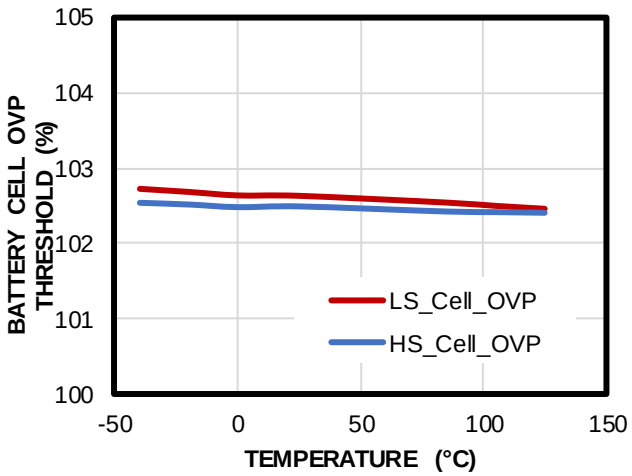
V_{BATT_REG} = 8.4V



V_{BATT_PRE} vs. Junction Temperature



Battery Cell OVP vs. Junction Temperature



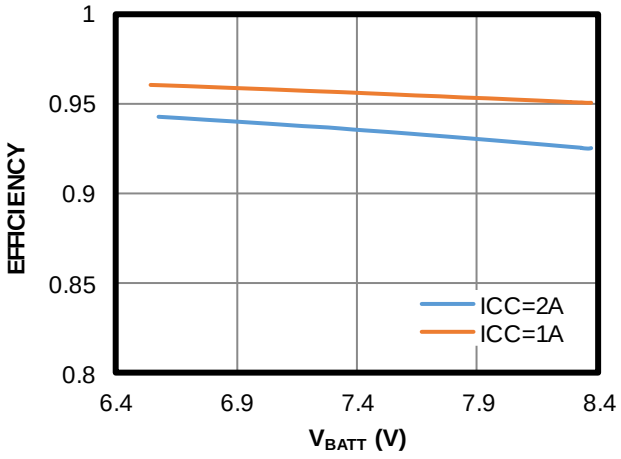
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TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 5V, T_A = 25°C, unless otherwise noted.

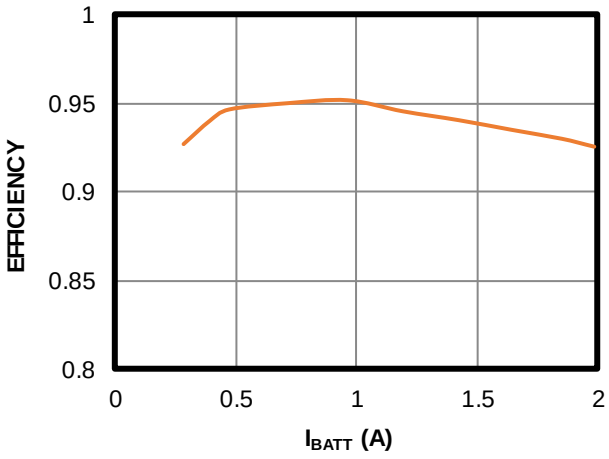
Constant Current Mode Charge Efficiency

V_{IN} = 5V, f_{SW} = 1200kHz , L = 1.5µH, (DCR = 10mΩ), I_{SYS} = 0A



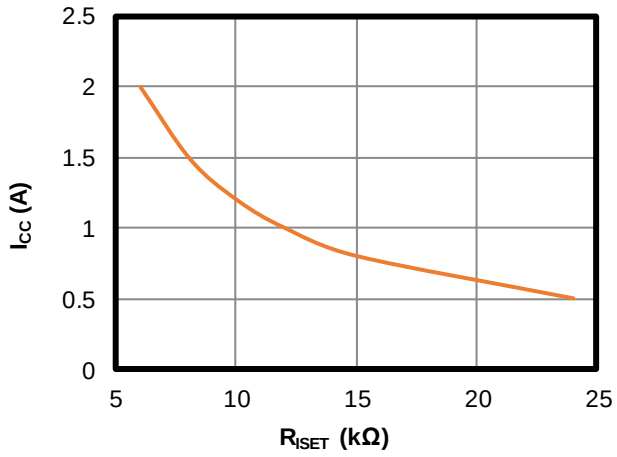
Constant Voltage Mode Charge Efficiency

V_{IN} = 5V, f_{SW} = 1200kHz, L = 1.5µH, (DCR = 10mΩ), V_{BATT} = 8.4V, I_{SYS} = 0A



Configurable Charge Current

Standalone mode



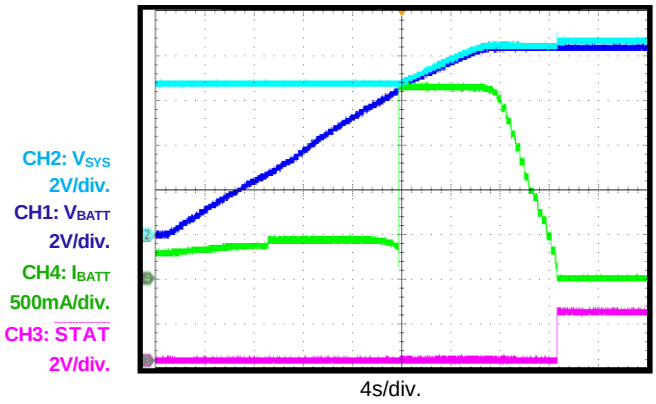
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TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{BATT_PRE} = 6.5V, I_{CC} = 2A, I_{SYS} = 0A, V_{BATT} = 0V to 8.4V, C_{IN} = 10µF, C_{SYS} = 44µF, C_{BATT} = 22µF, L = 1.5µH, f_{SW} = 1200kHz, T_A = 25°C, unless otherwise noted.

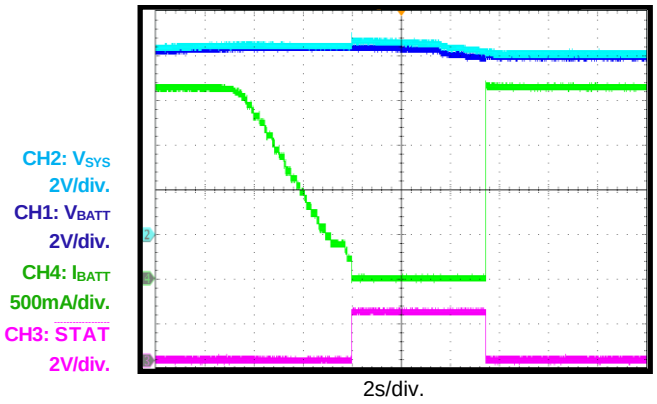
Battery Charge Curve

V_{BATT_REG} = 8.4V



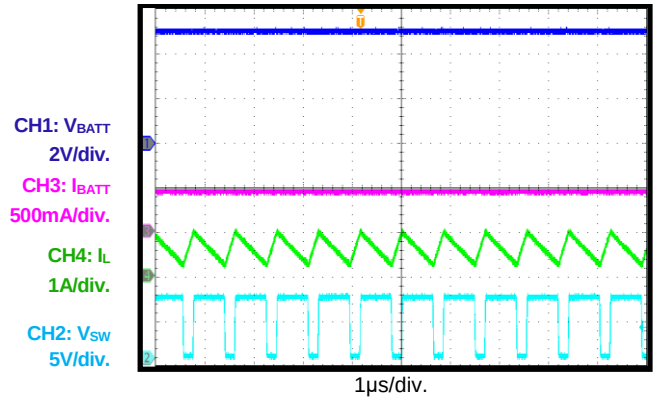
Auto-Recharge

V_{BATT_REG} = 8.4V



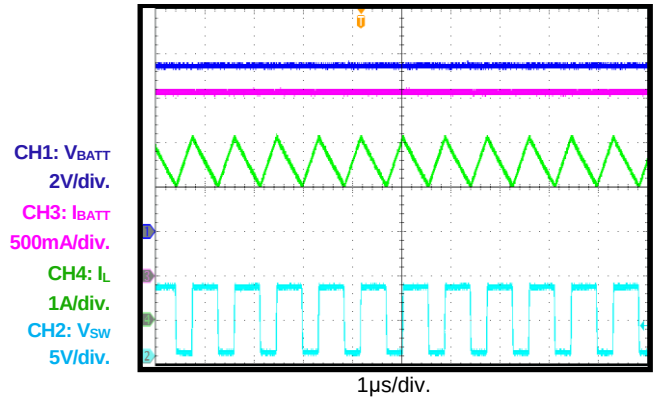
Pre-Charge Steady State

V_{BATT} = 5V



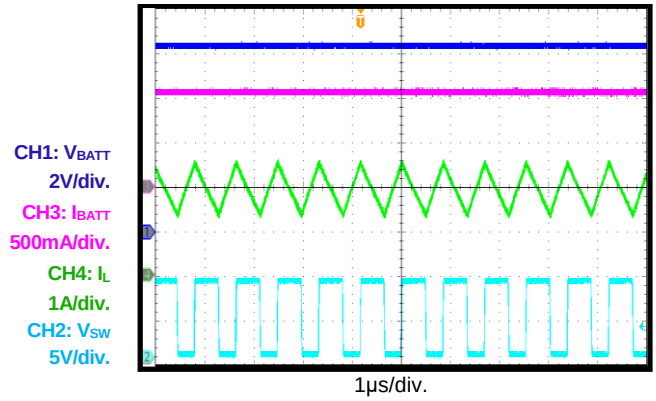
Constant Current Charge Steady State

V_{BATT} = 7.4V



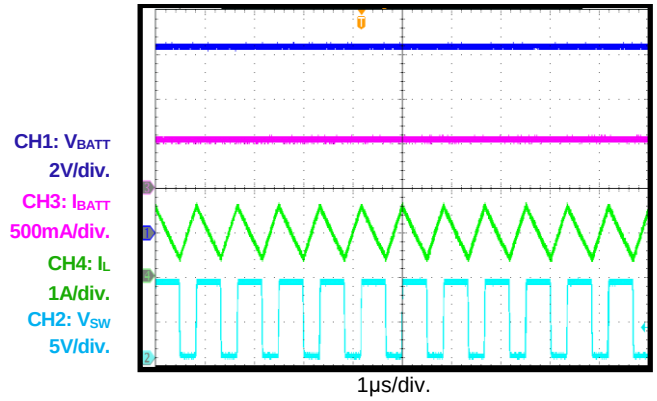
Constant Voltage Charge Steady State

V_{BATT} = 8.4V (1A)



Constant Voltage Charge Steady State

V_{BATT} = 8.4V (0.5A)



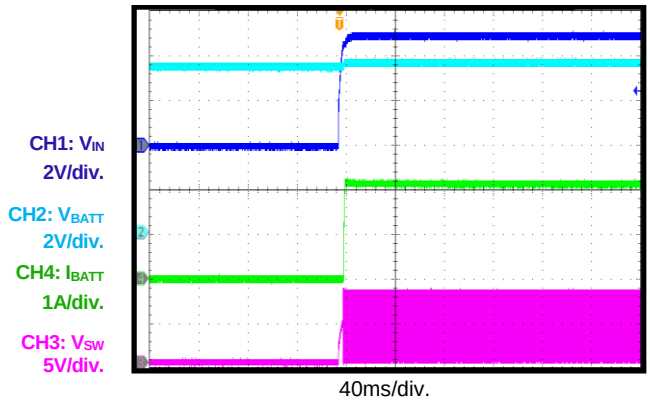
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TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{BATT_PRE} = 6.5V, I_{CC} = 2A, I_{SYS} = 0A, V_{BATT} = 0V to 8.4V, C_{IN} = 10µF, C_{SYS} = 44µF, C_{BATT} = 22µF, L = 1.5µH, f_{SW} = 1200kHz, T_A = 25°C, unless otherwise noted.

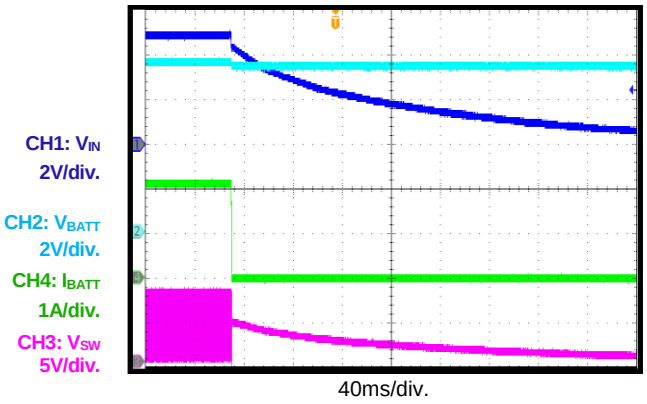
Start-Up through VIN

V_{BATT} = 7.4V



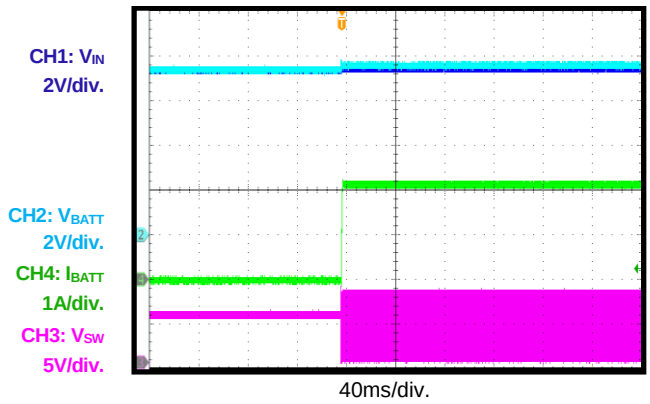
Shutdown through VIN

V_{BATT} = 7.4V



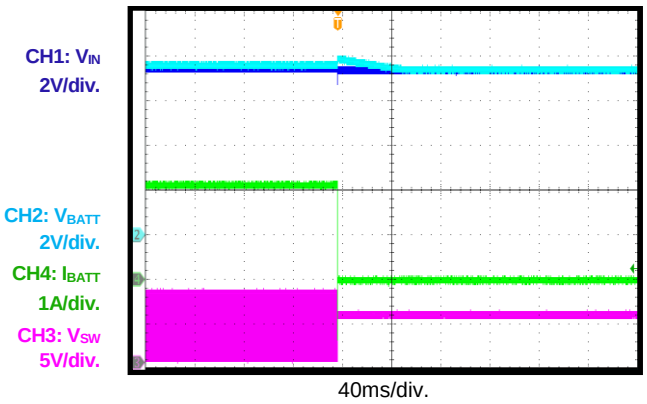
Boost Enabled

V_{BATT} = 7.4V



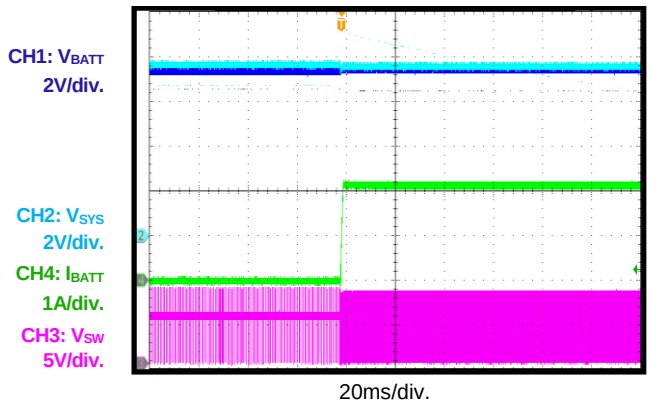
Boost Disabled

V_{BATT} = 7.4V



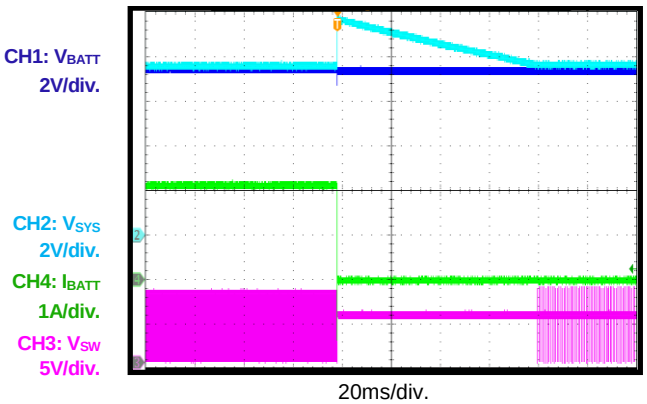
Constant Current Charge Enabled

V_{BATT} = 7.4V, MP2672A-0000



Constant Current Charge Disabled

V_{BATT} = 7.4V, MP2672A-0000



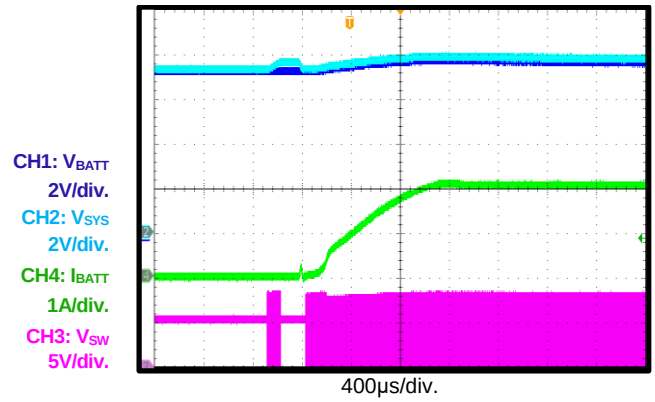
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TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{BATT} = 0V to 8.4V, C_{IN} = 10µF, C_{SYS} = 44µF, C_{BATT} = 22µF, L = 1.5µH, f_{SW} = 1200kHz, T_A = 25°C, unless otherwise noted.

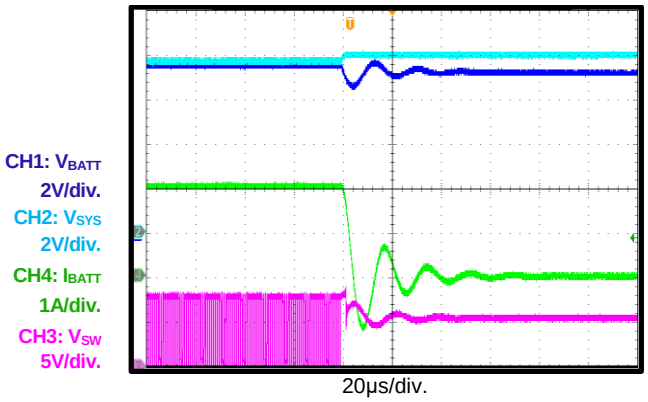
Constant Current Charge Enabled

V_{BATT} = 7.4V, MP2672A-000E



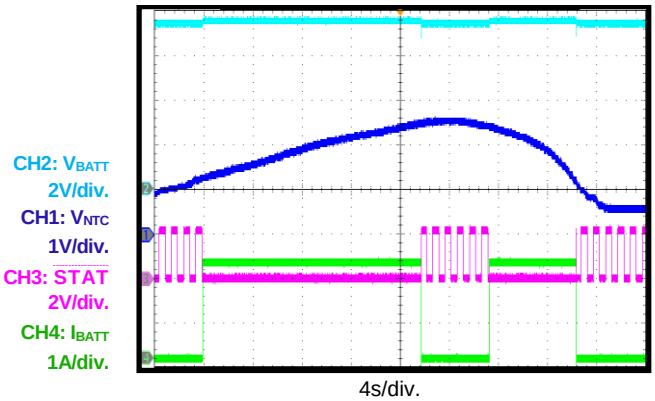
Constant Current Charge Disabled

V_{BATT} = 7.4V, MP2672A-000E



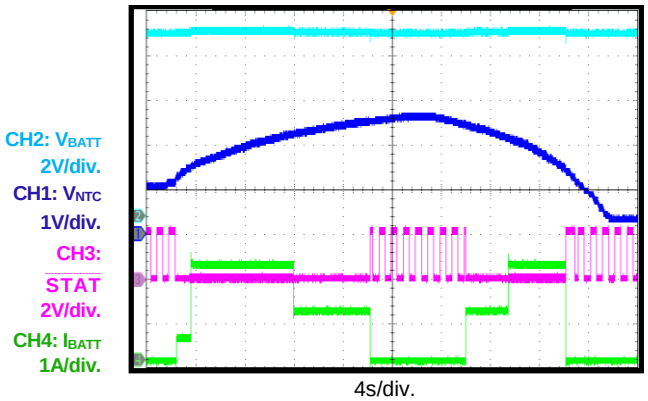
Standard NTC Protection

V_{BATT} = 7.4V, standard NTC, I_{CC} = 2A, vary V_NTC



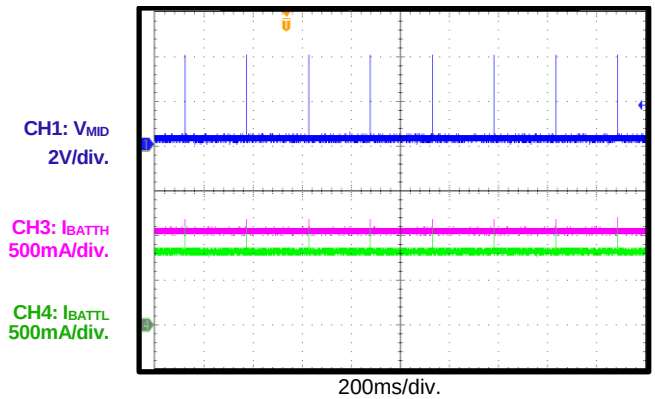
JEITA NTC Protection

V_{BATT} = 8.15V, JEITA NTC, I_{CC} = 2A, vary V_NTC



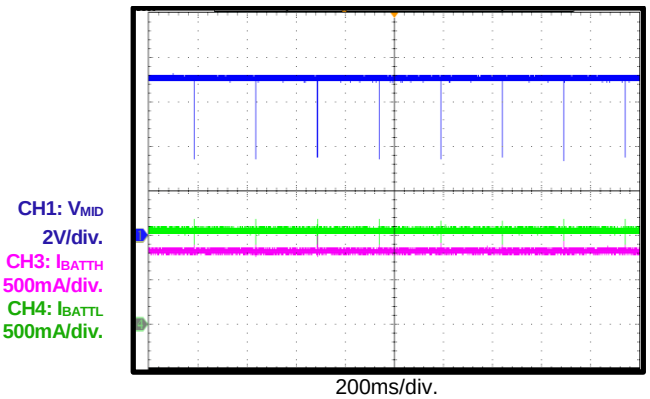
LS Cell Balance

I_{CC} = 1A, I_{SYS} = 0A, HS cell is 3.6V and LS cell is 3.8V, balance enabled, balance resistor is 17mΩ



HS Cell Balance

I_{CC} = 1A, I_{SYS} = 0A, HS cell is 3.8V and LS cell is 3.6V, balance enabled, balance resistor is 17mΩ



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FUNCTIONAL BLOCK DIAGRAM

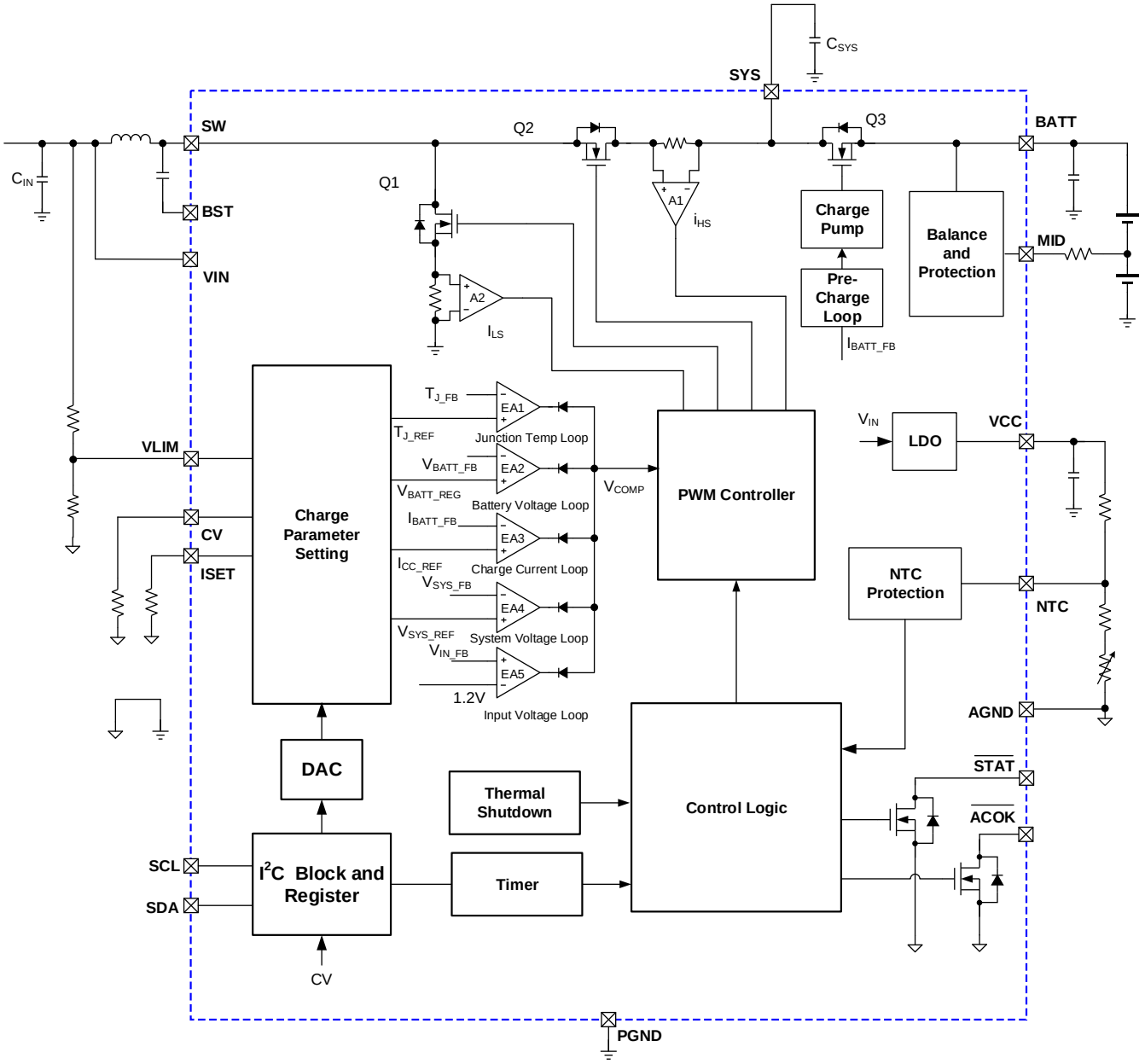


Figure 4: Functional Block Diagram

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OPERATION

The MP2672A is a highly integrated switch-mode battery charger IC that charges lithium-ion batteries with two cells in series from a 5V input power supply. This means it can be used with an adapter or USB input.

Host-Control Mode and Standalone Mode

The MP2672A can operate in either host-control mode or standalone mode. After the input starts up, the MP2672A checks the CV pin's status.

If CV is pulled up to logic high, the MP2672A works in host-control mode. If CV is connected to ground through a resistor, the MP2672A works in standalone mode.

In host-control mode, the charging parameters (V_{BATT_REG} and I_{CC}) can be configured by the I^2C registers. In standalone mode, they can be set by hardware pins.

Table 2: Host-Control Mode vs. Standalone Mode

CV Pin	Mode	V_{BATT_REG}	I_{CC}
Connected to AGND via resistor	Standalone	Set by CV resistor	Set by ISET resistor
Pulled up to VCC	Host-control	Set by I^2C register	Set by I^2C register (9)

Note:

9) The maximum charge current is limited by the ISET pin, even in host-control mode.

Internal Power Supply

The VCC LDO is powered by the input power supply, and it powers the internal circuit and MOSFET driver. When the input is absent, the VCC LDO is off. An external capacitor must be connected from the VCC pin to AGND. The VCC output is regulated to about 3.6V when V_{IN} is 5V. If V_{IN} is below 3.6V, the LDO enters low-dropout mode, and the LDO FET fully turns on. The VCC output cannot handle current loads exceeding 20mA.

Input Voltage vs. System Voltage Limitation

To prevent the MP2672A from entering open-loop operation due to the low-side MOSFET's minimum on time, the boost converter turns off if V_{SYS} drops below 110% of V_{IN}. The converter restarts, then checks the input voltage and system voltage again. The boost converter turns off again if V_{SYS} is still below 110% of V_{IN} after a 1ms soft-start time.

It is recommended to choose V_{BATT_PRE} and V_{TRACK} to ensure that the minimum output voltage of the boost converter exceeds 110% of the maximum DC input voltage.

Input Power Start-Up

When the input voltage is below the under-voltage lockout threshold (V_{IN_UVLO}), SYS is powered by the battery via Q3, which is fully turned on at this time. When input power is connected and V_{IN} exceeds V_{IN_UVLO}, Q3 stops being fully on and enters virtual diode mode. At the same time, the boost converter starts up with a soft start of the system voltage loop. When the system voltage rises to about 20mV above the battery voltage, Q3 turns off. It turns on again with a soft-start charging current after the system's voltage soft start completes.

Narrow Voltage DC (NVDC) Power Structure

The MP2672A features a narrow voltage DC (NVDC) power structure that is comprised of a frond-end boost converter and a rear-end battery FET between the SYS and BATT pins. This allows for separate control between the system and the battery. The system is given the priority to start up, even with a deeply discharged or missing battery. When input power is available and a depleted battery is connected, the system voltage is regulated to the minimum system voltage (V_{SYS_MIN}) which is set via REG00H, bits[3:1].

Figure 5 shows the system voltage control, described in detail below:

- When the battery voltage (V_{BATT}) is below V_{BATT_PRE}, the system voltage is regulated to $V_{SYS_REG_MIN}$ = V_{BATT_PRE} + V_{TRACK}. The battery FET works linearly to charge the battery with the pre-charge current.
- When V_{BATT} is above V_{BATT_PRE}, the battery FET is fully turned on, and the system voltage always exceeds V_{BATT} by the value calculated with I_{BATT} x R_{ON_Q3}. Once battery charging completes, the system output (V_{SYS}) is regulated to V_{BATT} + V_{TRACK}.

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- When charging is disabled and REG00H, bit[4] = 0, V_{SYS} is also regulated to V_{TRACK}, which is greater than the real battery voltage.

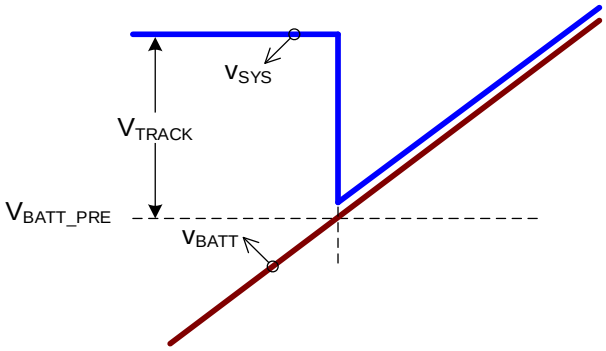


Figure 5: V_{SYS} Variation with V_{BATT}

Battery Charge Profile

The MP2672A provides three main charging phases: constant current pre-charge, constant current fast charge, and constant voltage charge (see Figure 6).

Phase 1 (Constant Current Pre-Charge): When V_{BATT} is below the pre-charge to fast charge threshold (V_{BATT_PRE}), the MP2672A regulates the system voltage to $V_{SYS_REG_MIN}$. The part applies a safe pre-charge current (I_{PRE}) to charge the deeply depleted battery until V_{BATT} reaches V_{BATT_PRE}. If V_{BATT_PRE} is not reached before the pre-charge timer (60min) expires, the charge cycle ceases, and a corresponding timeout fault signal is asserted.

Phase 2 (Constant Current Fast Charge): When V_{BATT} exceeds V_{BATT_PRE}, the MP2672A stops the pre-charge phase and enters the fast charge phase. The fast charge current can be configured via the ISET pin in standalone mode or via the I^2C register in host-control mode.

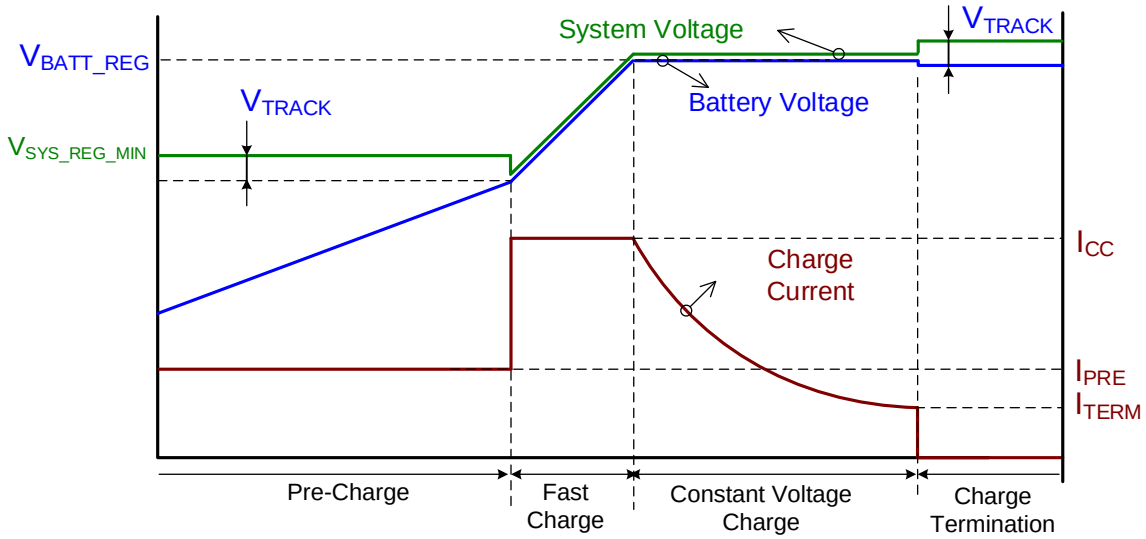
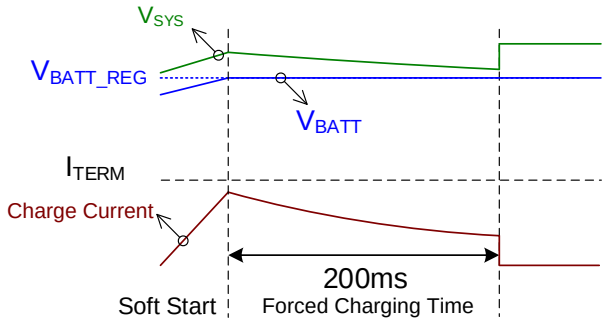


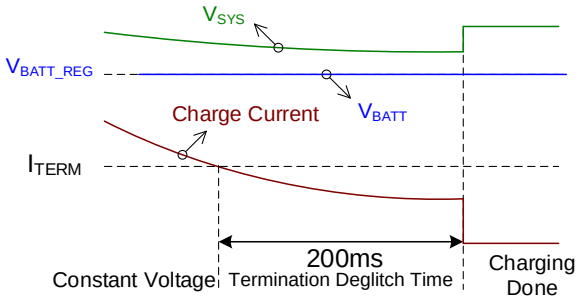
Figure 6: Battery Charge Profile

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Phase 3 (Constant Voltage Charge): When V_{BATT} reaches the battery regulation voltage (V_{BATT_REG}), the charge current begins to decrease (see Figure 7). The charge cycle is complete once the constant voltage loop is dominant, and the charge current drops below the charge termination current threshold for a 200ms deglitch time. This 200ms deglitch time is designed to start each charge cycle; after 200ms expires, the charge-full signal asserts whether the termination conditions have been met.



a) Forced Charge Time



b) Termination Deglitch Time

Figure 7: Forced Charge Time and Termination Deglitch Time

If I_{TERM} is not reached before the safety charge timer expires (see the Safety Timer section on page 22), the charging cycle stops and the corresponding timeout fault signal is asserted.

Charging termination can be manually disabled by pulling the NTC pin up to VCC. A new charging cycle starts when the following conditions are valid:

- The input power is re-plugged in
- Auto-recharge is enabled
- The charging enable bit is toggled (only for host-control mode)
- There is no thermistor fault on the NTC pin
- There is no safety timer fault
- There is no battery over-voltage condition
- Thermal shutdown is not occurring

Auto-Recharge

When the battery is fully charged and charging is terminated, the battery may be discharged by system consumption or self-discharge (see Figure 8). The MP2672A automatically starts a new charging cycle (without requiring a manual charging cycle restart) when the battery voltage drops below the recharge threshold for 200ms.

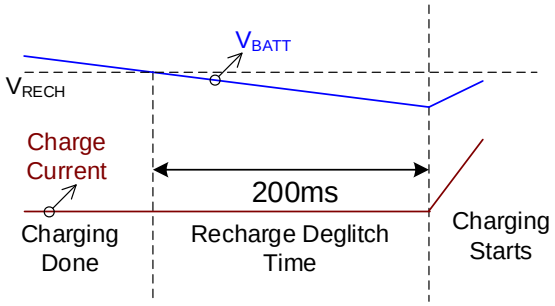


Figure 8: Recharging Profile

Charging Enabled (Default Setting)

If the battery is not expected to be charged frequently during high state of charge (SOC) conditions, the MP2672A has an one-time programmable (OTP) option (REG05H, bit[7]) to disable charging when the input power is on, and the battery voltage exceeds the recharge voltage threshold. Charging is enabled until the battery voltage falls below the recharge threshold.

Battery-Full Voltage Setting

The MP2672A has a CV pin that can configure the battery regulation voltage.

When CV is pulled up to VCC, the MP2672A operates in host-control mode. The battery regulation voltage is configured through the I^2C.

When CV is connected to AGND via a resistor, the MP2672A operates in standalone mode. The battery regulation voltage is set according to Table 3.

Table 3: V_{BATT_REG} vs. R_{VBATT} Resistor

Resistor Range	V_{BATT_REG}
30kΩ to 35kΩ	8.4V
70kΩ to 75kΩ	8.6V
100kΩ to 105kΩ	8.7V
130kΩ to 135kΩ	8.8V

Figure 9 shows the simplified diagram.

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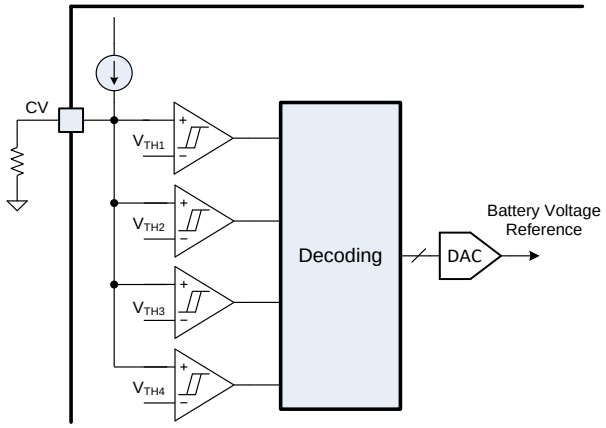


Figure 9: Simplified Diagram of the V_{BATT_REG} Setting in Standalone Mode

Charge Current Setting

In standalone mode, the charge current (I_{CC}) is set by a resistor connected to the ISET pin (R_{ISET}). Calculate I_{CC} with Equation (1):

$$I_{CC}=\frac{12k\Omega}{R_{ISET}}(A) \quad (1)$$

In host-control mode, the charge current can be configured via R_{ISET} and REG01H, bits[3:0]. R_{ISET} determines the full-scale value of the register. For example, if R_{ISET} is 6kΩ, the I^2C-configurable range is between 500mA and 2000mA, with 100mA per step. If R_{ISET} is 24kΩ, the I^2C-configurable range is between 125mA and 500mA, with 25mA per step. R_{ISET} is recommended to be between 6kΩ and 24kΩ.

Minimum Input Voltage Limit

To avoid overloading the adapter, the MP2672A implements input voltage based power management by continuously monitoring the input voltage (V_{IN}). When the minimum input voltage limit (V_{IN_MIN}) is reached, the charge current is reduced to prevent V_{IN} from dropping further. V_{IN_MIN} can be configured by a voltage divider on the VLIM pin.

The internal reference of the input voltage loop is 1.2V, and V_{IN_MIN} can be estimated with Equation (2):

$$V_{IN_MIN}=1.2\times\frac{R_H+R_L}{R_L} \quad (2)$$

Battery Supplement Mode and Virtual Diode Mode

When V_{IN_MIN} is reached, the charge current is reduced to keep V_{IN} from dropping further. However, if the charge current drops to 0A and the input source is still overloaded due to a heavy system load, the system voltage (V_{SYS}) continues dropping. If V_{SYS} falls below V_{BATT}, the MP2672A enters battery supplement mode. The battery starts to supplement the system load along with the boost converter. In supplement mode, the battery FET operates as a virtual diode.

When V_{SYS} falls 30mV below V_{BATT}, the battery FET turns on, and its source-to-drain voltage is regulated at 24mV. As the battery discharge current rises, the virtual diode loop is saturated and the battery FET fully turns on. The source-to-drain voltage is the discharge current times the on resistance of the battery FET.

Missing Battery Detection

The MP2672A is capable of detecting whether a battery is connected. The device detects a missing battery under the following conditions:

- Charging is enabled
- Auto-recharge is triggered
- Recovery from any fault

If a battery cannot be found, a 1Hz blinking on the $\overline{STAT}$ pin indicates the missing battery condition, or the BATTFLOAT_STAT bit is set 1 in host-control mode. Figure 10 shows the battery missing detection flowchart.

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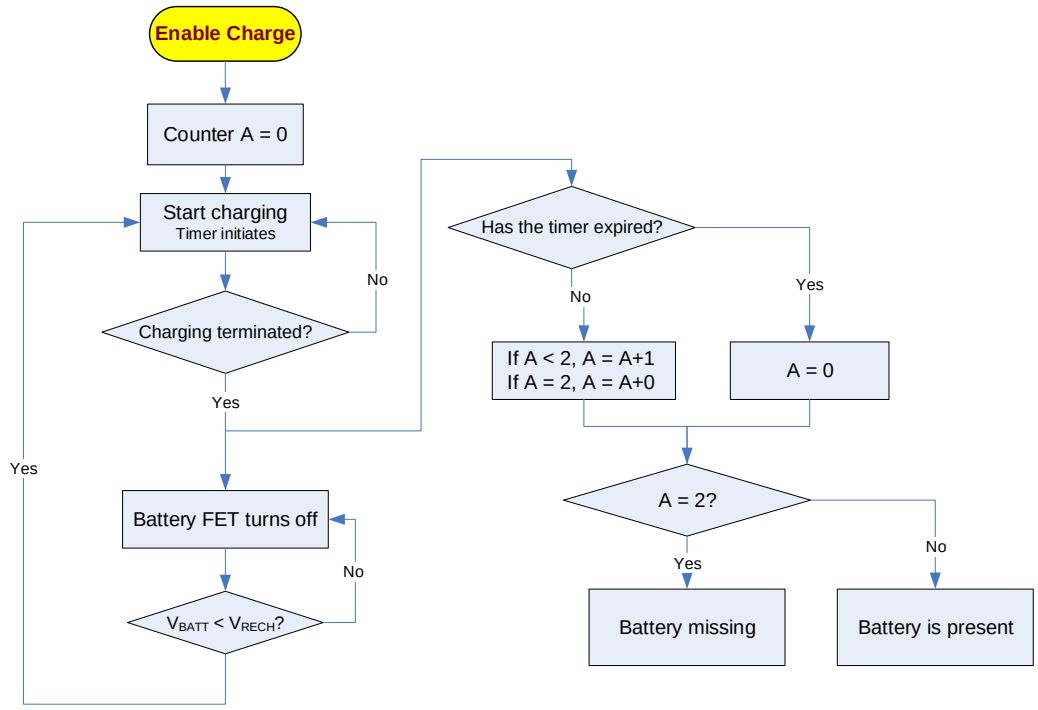


Figure 10: Missing Battery Detection Flowchart

Battery Over-Voltage Protection

The MP2672A is designed with a built-in battery over-voltage protection (OVP) threshold, which is 104% of V_{BATT_REG}. If a battery OV event occurs, the MP2672A turns off the battery FET (Q3) and stops charging. At this time, the boost converter continues operating, and the system voltage tracks the battery voltage with additional V_{TRACK}.

When the balance function is enabled (the MID pin is not pulled down to AGND), the MP2672A uses the MID pin to monitor each cell's voltage. Generally, if any one of the cell's voltages exceeds 102.5% of V_{BATT_REG} / 2, the MP2672A stops charging the battery.

Safety Timer

The MP2672A provides both a pre-charge and fast charge cycle safety timer to avoid an extended charging cycle due to abnormal battery conditions. When the battery is below V_{BATT_PRE}, the safety timer for pre-charge is 60 minutes. The fast charge cycle safety timer starts when the battery enters fast charge mode. The fast charge safety timer can be configured or disabled via the I^2C.

The safety timer is reset at the beginning of a new charging cycle. It can also be reset by writing 0 and 1 sequentially to the REG00H, bit[4]. The following actions restart the safety timer:

- Beginning a new charge cycle
- Writing REG00H, bit[4] from 0 to 1 (charge enabled)
- Writing REG02H, bits[2:1] from 00 to 01/10/11 (safety timer enabled)
- Writing REG02H bit[3] from 0 to 1 (software reset)

In the event of an NTC hot or cold fault, the charging timer is suspended. Once the NTC fault is removed, the timer continues to count from the value it was at before the NTC fault.

Watchdog Timer

When the MP2672A operates in host-control mode, a watchdog timer is provided to reset all the registers to their default values if the watchdog timer is not reset periodically. By doing this, the MP2672A's register values return to their default settings when no action occurs on the I^2C bus for a certain time. The watchdog timer duration can be configured and disabled via the I^2C.

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Negative Temperature Coefficient (NTC) Thermistor

The term thermistor refers to any thermally sensitive resistor, and a negative temperature coefficient (NTC) thermistor is generally called a thermistor. Thermistors can be used for multiple purposes, as their characteristics are different based on their manufacturing method, structure, and shape. Unless otherwise noted, the thermistor resistance values are classified at a standard temperature of 25°C. The resistance of a thermistor is solely a function of its absolute temperature.

Refer to the thermistor's datasheet for the mathematic equation that calculates the relationship between resistance and the absolute temperature of the thermistor. It can also be calculated with Equation (3):

$$R_1 = R_2 \times e^{\beta \times \left(\frac{1}{T1} - \frac{1}{T2}\right)} \quad (3)$$

Where R1 is the resistance at the absolute temperature T1, R2 is the resistance at the absolute temperature T2, and β is a constant that depends on the thermistor's material.

The MP2672A continuously monitors the battery's temperature by measuring the voltage on the NTC pins. This voltage is determined by the voltage divider. The voltage divider ratio is determined by the NTC thermistor's resistance values under different ambient battery temperatures.

The MP2672A internally sets a predetermined upper and lower bounds of the temperature range. If the voltage at the NTC pin goes out of the hot or cold threshold, the temperature is outside its safe operating limit. At this time, charging ceases until the operating temperature returns to within its safe range.

To satisfy JEITA requirements, the MP2672A monitors four temperature thresholds: the cold battery threshold (T_{NTC} < 0°C), the cool battery threshold (0°C < T_{NTC} < 10°C), the warm battery threshold (45°C < T_{NTC} < 60°C), and the hot battery threshold (T_{NTC} > 60°C).

For a given NTC thermistor, these temperatures correspond to the V_{COLD}, V_{COOL}, V_{WARM}, and V_{HOT} values. Figure 11 shows the typical JEITA operation when the battery temperature is in a different temperature window, described in detail below:

1. When V_{NTC} < V_{HOT} or V_{NTC} > V_{COLD}, charging is suspended, and all timers are suspended.
2. When V_{HOT} < V_{NTC} < V_{WARM}, the battery regulation voltage (V_{BATT_REG}) is reduced by 120mV/cell from the configurable threshold.
3. When V_{COOL} < V_{NTC} < V_{COLD}, the charging current is reduced to half of the configurable charge current.

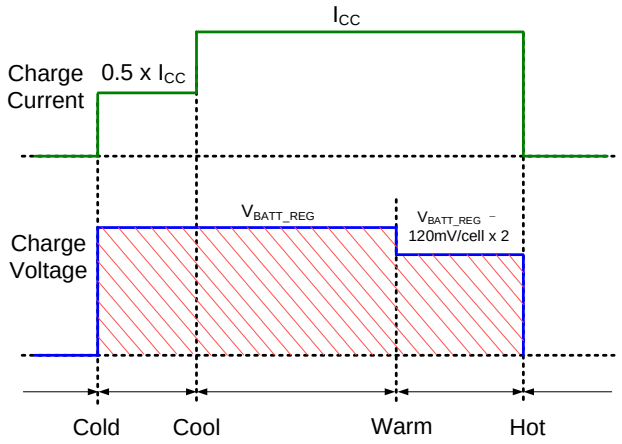


Figure 11: JEITA Compatible NTC Window

For a given thermistor, two of four temperature thresholds can be configured by changing the values of R_{T1} and R_{T2}. See the Selecting an NTC Sensor Resistor section on page 34 for more details.

Thermal Regulation and Thermal Shutdown

To guarantee safe operation, the MP2672A limits the die temperature. If the internal junction temperature reaches the preset threshold, the MP2672A starts to reduce the charge current to prevent greater power dissipation.

When V_{BATT} > V_{BATT_PRE}, the die temperature limit is always set to 120°C. When V_{BATT} < V_{BATT_PRE}, the die temperature limit can be configured to multiple values (60°C, 80°C, 100°C, or 120°C), which can be configured by the one-time programmable (OTP) register (REG05H, bits[4:3]).

If the junction temperature reaches 150°C, the boost converter enters shutdown mode.

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Indications

The MP2672A has two open-drain pins ($\overline{ACOK}$ and $\overline{STAT}$) to indicate the input power and charging status. Table 4 shows the behavior for each of these indications.

Table 4: Input Power and Charging Statuses

Charging State	$\overline{ACOK}$	$\overline{STAT}$
Charging	Low	Low
Charging complete, charging disabled	Low	Open drain
Charging suspended due to one of the following: • Battery OVP • Timer fault • NTC hot fault • NTC cold fault • Battery floating	Low	1Hz blinking
Thermal shutdown	Low	Open drain

Battery Cell Balance and Protection

The MP2672A provides battery cell balance and protection for dual-cell applications (see Figure 12). The part can sense the voltage across each cell. Generally, if these two cells have voltages that are mismatched by more than 50mV, the internal discharge path turns on to discharge the cell with the higher voltage until the two cell voltages have a difference that is below 30mV.

If battery over-voltage protection (OVP) occurs before the two cells are equalized, charging is suspended.

The MP2672A integrates the balance path and control circuit. An external power dissipation resistor is also required to limit the balance current. If the cell balance function is not used, connect MID directly to AGND.

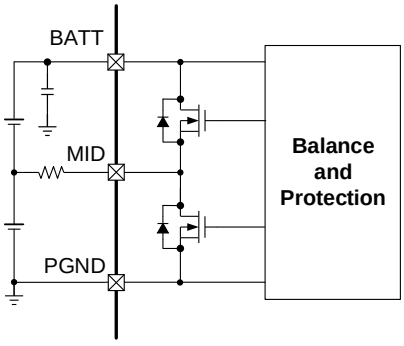


Figure 12: Battery Balance Block Diagram

Balancing Algorithm

The balance block only operates in charge mode. Balancing starts when any cell voltage exceeds the balance start point (V_{CELL_BAL}).

The voltage difference between cells should exceed V_{CELL_DIFF}. The MP2672A detects the cell voltages in the pack, then checks the voltage difference between two cells. If the differential voltage exceeds V_{CELL_DIFF}, the corresponding balance MOSFET turns on.

To measure the open-circuit voltage of the cell, balancing is frequently suspended for a short duration. Charging always operates independently of the balance algorithm if no other charging fault occurs. The cell voltage is measured for 200µs when cell balancing is suspended. Then cell balancing operates for 249.8ms each 250ms cycle (see Figure 13).

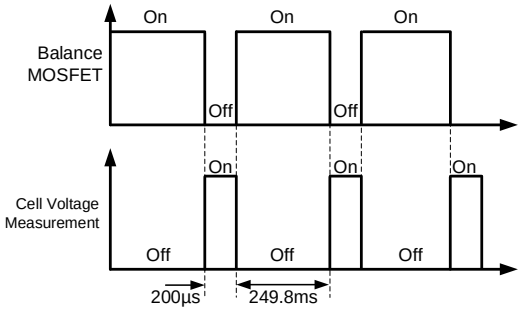


Figure 13: Battery Balance Clock

Figure 14 shows the battery balance flowchart.

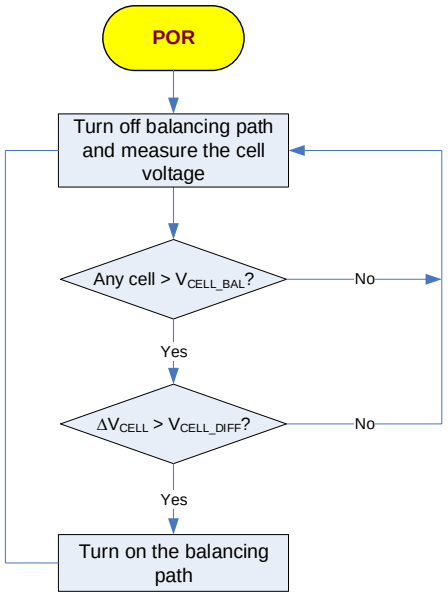


Figure 14: Battery Balance Flowchart

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For extremely unbalanced dual-cell batteries, the charger takes a few cycles to balance the battery voltages. For some applications, such as removable dual-cell batteries, a charger is required to balance two cells in one charge cycle. In this case, an external cell-balance circuit is recommended (see Figure 15).

The MP2672A also has an option to automatically disable termination if cell balancing is active. By doing this, the two cells are better matched once charging is terminated.

The cell voltage measured within the 200µs time is also delivered to the battery cell OVP block. If OVP occurs, charging is suspended (the battery FET turns off) until the measured cell voltage drops below the recovery threshold, which is set by REG00H, bit[0].

Boost Converter Suspend Mode

The MP2672A offers suspend mode to turn off the boost converter even when the input is present. In this mode, the SYS pin is powered by the battery through the internal battery FET, and the input quiescent current is optimized.

The MP2672A enters this mode by setting REG02H, bit[0] to 0. The MP2672A-000E is preset to this mode. The boost is suspended if any of the following conditions occur:

- Charging terminated
- Charging disabled
- An NTC fault has occurred
- A timer fault has occurred
- Battery over-voltage protection (OVP) has occurred

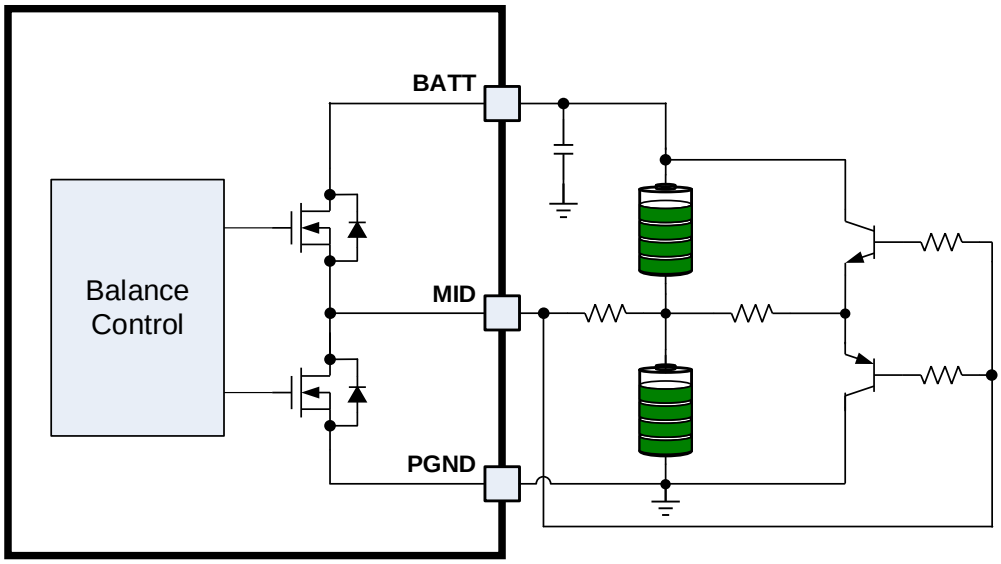


Figure 15: External Cell-Balancing Circuit

Series Interface

The IC uses two wires: a serial data (SDA) wire and serial clock (SCL) wire. All I²C master and slave devices are connected with these two wires. The master (e.g. a microcontroller or digital signal processor) generates the bus clock and initiates communication on the bus. The slave devices receive and respond to the bus commands from the master device. To communicate with a specific device, each slave device must have a unique bus address.

The I²C interface supports both standard mode (up to 100kbits), and fast mode (up to 400kbits). The SDA and SCL pins are open drains. Both the SDA and SCL are connected to the positive supply voltage via a current source or pull-up resistor. When the bus is free, both lines are pulled high.

The MP2672A's SDA is a bidirectional line, and SCL is a unidirectional line.

The data on the SDA line must be stable during the high period of the clock (see Figure 16). The high or low state of the data line can only change when the clock signal on the SCL line is low. One clock pulse is generated for each data bit transferred.

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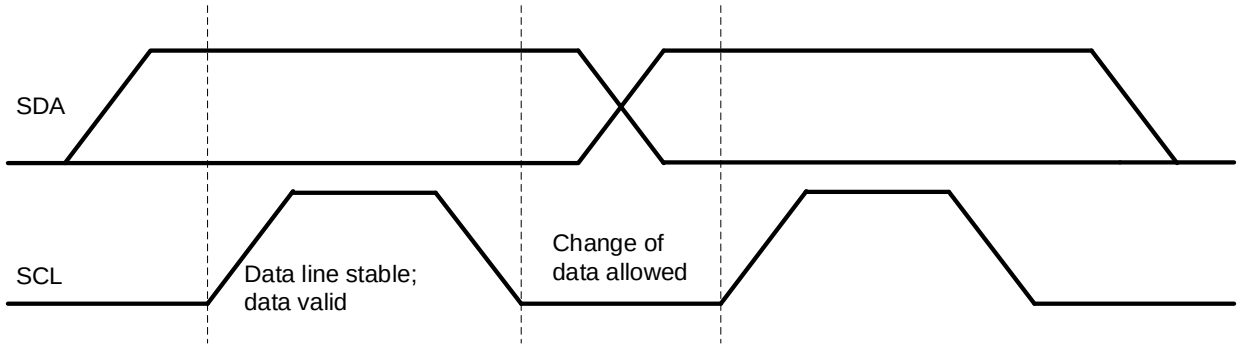


Figure 16: Bit Transfer on the I²C Bus

All transactions begin with a start (S) command and can be terminated by a stop (P) command. A start condition is defined as a high-to-low transition on the SDA line while SCL is high. A stop condition is defined as a low-to-high transition on the SDA line when the SCL is high (see Figure 17). Start and stop conditions are always generated by the master. The bus is considered busy after a start condition, and free after a stop condition.

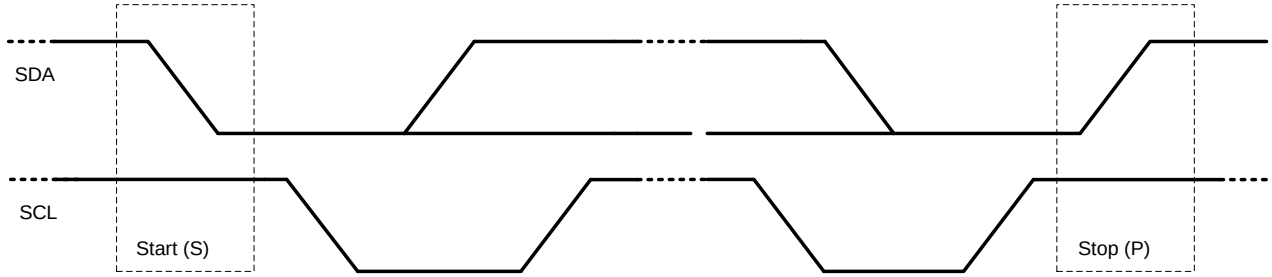


Figure 17: Start and Stop Conditions

Data on the I²C bus is transferred in 8-bit packets (bytes) (see Figure 18). Each byte must be followed by an acknowledge bit (ACK). Data is transferred with the most significant bit (MSB) first.

An acknowledgement occurs after every byte. The acknowledge bit allows the receiver to signal to the transmitter that the byte was successfully received and another byte may be sent. All clock pulses, including the 9th acknowledge clock pulse, are generated by the master.

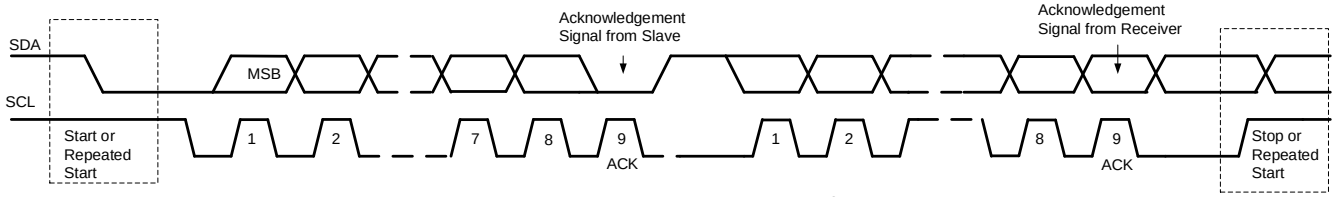


Figure 18: Data Transfer on the I²C Bus

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The transmitter releases the SDA line during the acknowledge clock pulse so the receiver can pull the SDA line low. If it remains high during the 9th clock pulse, this is called a not acknowledge (NACK) signal. The master can then generate either a stop condition to abort the transfer, or a repeated start (S) to start a new transfer.

After the start condition is received, a slave address is sent. This address is 7 bits long followed by an 8th data direction bit (R/W). A 0 indicates a transmission (write) and a 1 indicates a request for data (read). Figure 19 shows the complete data transfer.

If the register address is not defined, the charger IC sends back a NACK signal and returns to the idle state.

The MP2672A operates as a slave device with the address 4BH. The MP2672A supports single-byte R/W (see Figure 20 and Figure 21).

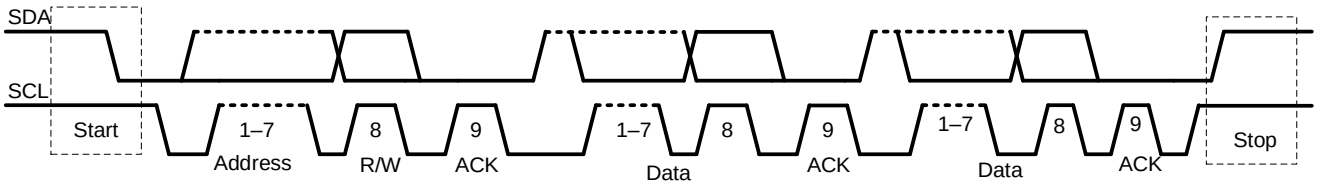


Figure 19: Complete Data Transfer

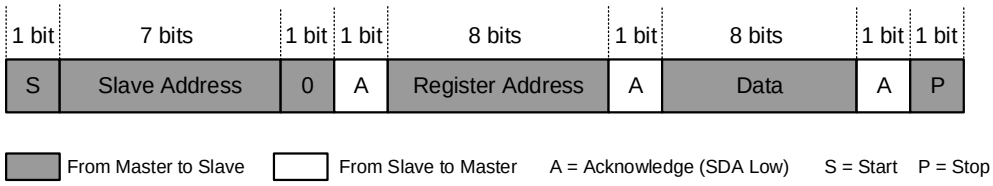


Figure 20: I²C Single Write

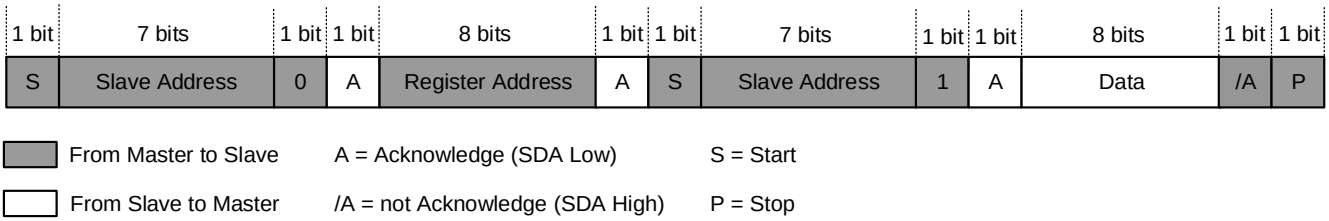


Figure 21: I²C Single Read

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I²C REGISTER MAP

IC Address 4BH

Register Name	Address	R/W	Description	Default
REG00H	0x00	R/W	Battery regulation voltage, charge configuration, and SYS voltage setting register.	0011 1000
REG01H	0x01	R/W	Cell balance setting and charge current setting register.	1000 1111
REG02H	0x02	R/W	Timer setting register.	1001 0101
REG03H	0x03	R	Status register.	0000 0000
REG04H	0x04	R	Fault register.	0000 0000

REG 00H (Default: 0011 1000)

Bit	Name	POR	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
7	V_{BATT_REG}[2]	0	Y	Y	R/W	000: 8.3V 001: 8.4V 010: 8.5V 011: 8.6V 100: 8.7V 101: 8.8V 110: 8.9V 111: 8.2V	These bits set the battery regulation voltage. They are set to 001 by default. They are OTP-configurable.
6	V_{BATT_REG}[1]	0	Y	Y	R/W		
5	V_{BATT_REG}[0]	1	Y	Y	R/W		
4	CHG_CONFIG	1	Y	Y	R/W	0: Charging disabled 1: Charging enabled	This bit is set to 1 by default.
3	V_{BATT_PRE}[2]	1	Y	N	R/W	0.4V	These bits set the system minimum voltage offset. It has a 6.0V offset, ranges between 6.0V and 6.7V, and is set to 6.4V by default. This threshold is also used as the pre-charge battery voltage threshold. It is OTP-configurable.
2	V_{BATT_PRE}[1]	0	Y	N	R/W	0.2V	
1	V_{BATT_PRE}[0]	0	Y	N	R/W	0.1V	
0	CELL_OVP_HYS	0	Y	N	R/W	0: 80mV 1: 0mV	The bit sets the cell over-voltage protection (OVP) hysteresis.

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REG 01H (Default: 1000 1111)

Bit	Name	POR	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
7	NTC_TYPE	1	Y	Y	R/W	0: Standard 1: JEITA	This bit is set to 0 by default. It is OTP-configurable.
6	V_{CELL_BAL}	0	Y	Y	R/W	0: 3.5V 1: 3.7V	This bit sets the cell-balance start point. It is set to 0 by default, and is OTP-configurable.
5	BALANCE_ THRESHOLD_ H2L	0	Y	Y	R/W	0: 50mV 1: 70mV	This bit sets the cell-balance threshold. It is set to 0 by default, and is OTP-configurable.
4	BALANCE_ THRESHOLD_ L2H	0	Y	Y	R/W	0: 50mV 1: 70mV	This bit sets the cell-balance threshold. It is set to 0 by default, and is OTP-configurable.
3	I_{CC}[2]	1	Y	Y	R/W	800mA	These bits set the fast charge current setting. If R_{ISET} is 6kΩ: These bits have a 500mA offset, a 500mA to 2000mA range, and are set to 1111 by default. If R_{ISET} is 24kΩ: These bits have a 125mA offset, a 125mA to 500mA range, are set to 1111 by default, and are OTP-configurable.
2	I_{CC}[2]	1	Y	Y	R/W	400mA	
1	I_{CC}[1]	1	Y	Y	R/W	200mA	
0	I_{CC}[0]	1	Y	Y	R/W	100mA	

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REG 02H (Default: 1001 0101)

Bit	Name	POR	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
7	f_{SW}	1	Y	Y	R/W	0: 600kHz 1: 1200kHz	This bit is set to 1 by default. It is OTP-configurable.
6	I^2C_WD_TIMER_RESET	0	Y	N	R/W	0: Normal 1: Reset	This bit is set to 0 by default.
5	WD_TIMER [1]	0	Y	N	R/W	00: Disable timer 01: 40s 10: 80s 11: 160s	These bits set the I^2C watchdog timer limit. They are set to 01 by default, and are OTP-configurable.
4	WD_TIMER [0]	1	Y	N	R/W		
3	REGISTER_RESET	0	Y	N	R/W	0: Keep current setting 1: Reset	This bit is set to 0 by default. After a reset, this bit returns to 0 automatically.
2	CHG_TMR[1]	1	Y	Y	R/W	00: Disable charge timer 01: 8 hours 10: 20 hours 11: 12 hours	These bits are set to 10 by default.
1	CHG_TMR[0]	0	Y	Y	R/W		
0	EN_SUSP	1	Y	Y	R/W	0: Enable suspended mode (disable the boost) 1: Disable suspended mode (enable the boost)	This bit is set to 1 by default.

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REG 03H (Default: 0000 0000)

Bit	Name	POR	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
7	RESERVED	N/A	N/A	N/A	R	Reserved.	Reserved.
6	RESERVED	N/A	N/A	N/A	R	Reserved.	Reserved.
5	CHG_STAT[1]	0	N/A	N/A	R	00: Not charging 01: Pre-charge 10: Constant current or constant voltage charge 11: Charging complete	These bits are set to 00 by default.
4	CHG_STAT[0]	0	N/A	N/A	R		
3	PPM_STAT	0	N/A	N/A	R	0: Not in PPM 1: in VIN PPM	This bit is set to 0 by default.
2	BATTFLOAT_STAT	0	N/A	N/A	R	0: Battery present 1: Battery missing	This bit is set to 0 by default.
1	THERM_STAT	0	N/A	N/A	R	0: Normal 1: Thermal regulation	This bit is set to 0 by default.
0	VSYS_STAT	0	N/A	N/A	R	0: Not in V_{SYSMIN} regulation 1: In V_{SYSMIN} regulation	This bit is set to 0 by default.

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REG 04H (Default: 0000 0000)

Bit	Name	POR	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
7	WD_FAULT	0	N/A	N/A	R	0: Normal operation 1: The watchdog timer has expired	This bit is set to 0 by default.
6	INPUT_FAULT	0	N/A	N/A	R	0: Normal operation 1: Input OVP has occurred	This bit is set to 0 by default.
5	THERMSD_ FAULT	0	N/A	N/A	R	0: Normal operation 1: Thermal shutdown	This bit is set to 0 by default.
4	TIMER_FAULT	0	N/A	N/A	R	0: Normal operation 1: The safety timer has expired	This bit is set to 0 by default.
3	BAT_FAULT	0	N/A	N/A	R	0: Normal operation 1: Battery OVP has occurred	This bit is set to 0 by default.
2	NTC_FAULT[2]	0	N/A	N/A	R	000: Normal operation 001: An NTC cold fault has occurred 010: An NTC cool fault has occurred 011: An NTC warm fault has occurred 100: An NTC hot fault has occurred	These bits are set to 000 by default.
1	NTC_FAULT[1]	0	N/A	N/A	R		
0	NTC_FAULT[0]	0	N/A	N/A	R		

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REG 05H (Default: 1110 0000) (10)

Bit	Name	POR	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
7	RCHG	1	N/A	N/A	N/A	0: No charging after input start-up when $V_{BATT} > V_{RECH}$ 1: Automatic charging after input start-up when $V_{BATT} > V_{RECH}$	This bit is set to 1 by default.
6	RESERVED	1	N/A	N/A	N/A	Reserved.	Reserved.
5	BALANCE_EOC_EN	1	N/A	N/A	N/A	0: Do not suspend termination when cell balancing is active 1: Suspend termination when cell balancing is active	This bit is set to 1 by default.
4	T_{J_REG}[1]	0	N/A	N/A	N/A	00: 120°C 01: 100°C 10: 80°C 11: 60°C	This bit is set to 00 by default.
3	T_{J_REG}[0]	0	N/A	N/A	N/A		
2	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.
1	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.
0	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.

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REG 06H (Default: 0000 0011) (10)

Bit	Name	POR	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
7	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.
6	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.
5	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.
4	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.
3	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.
2	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.
1	RESERVED	1	N/A	N/A	N/A	Reserved.	Reserved.
0	NVDC_MODE_EN	1	N/A	N/A	N/A	When charging is suspended: 0: Disable DC/DC switching 1: Enable DC/DC switching	This bit is set to 1 by default.

Note:

10) This register is for OTP only. It is not accessible.

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OTP MAP

#	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]
00H	V_{BATT_REG}: 8.2V-8.9V			N/A	V_{BATT_PRE}: 6.0V to 6.7V			N/A
01H	NTC Type	V_{CELL_BAL}	$V_{CELL_DIFF_HL}$	$V_{CELL_DIFF_LH}$	I_{CC}: 500mA to 2000mA/100mA step (R_{ISET} = 6kΩ)			
02H	FSW	N/A	WATCHDOG		N/A	N/A	N/A	N/A
05H (10)	RCHG	N/A	BALANCE_ EOC_EN	T_{J_REG}: 60°C, 80°C, 100°C , or 120°C		N/A	N/A	N/A
06H (10)	N/A	N/A	N/A	N/A		N/A	N/A	NVDC Mode_EN

Note:

10) This register is for OTP only. It is not accessible.

OTP DEFAULT

OTP Items	Default
V_{BATT_REG}	8.4V
V_{BATT_PRE}	6.4V
NTC Type	JEITA
V_{CELL_BAL}	3.5V
Balance Threshold H2L	50mV
Balance Threshold L2H	50mV
I_{CC}	2000mA
SW FREQ	1200kHz
WATCHDOG	40s
RCHG	New charge cycle starts after start-up when $V_{BATT} > V_{RECH}$
BALANCE_EOC_EN	Enabled (if the two cells are not balanced, EOC is not asserted, even all conditions are met)
Thermal Regulation Threshold	120°C
NVDC Mode_EN	Enable DC/DC switching when charging is suspended

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APPLICATION INFORMATION

Setting the Charge Current in Standalone Mode

In standalone mode, the MP2672A's charge current (I_{CC}) can be set by an external resistor (R_{ISET}). Estimate I_{CC} with Equation (4):

$$I_{CC}=\frac{12k\Omega}{R_{ISET}}(A) \quad (4)$$

The charge current can be configured up to 2.0A. Table 5 shows the expected R_{ISET} value for typical charge currents.

Table 5: Charge Current Setting Table

R_{ISET} (kΩ)	I_{CC} (A)
24	0.5
12	1.0
6	2.0

Setting the Minimum Input Voltage Limit

In charge mode, connect a voltage divider from IN to AGND, then tap it to VLIM to configure the minimum input voltage. Calculate the minimum input voltage with Equation (5):

$$V_{IN_MIN}=1.2V\times\frac{R_H+R_L}{R_L} \quad (5)$$

Where 1.2V is the reference of the minimum input voltage loop. With a given R_L, R_H can be estimated with Equation (6):

$$R_H=R_L\times\frac{V_{IN_MIN}-1.2V}{1.2V} \quad (6)$$

For example, if a 4.675V minimum input voltage limit is expected, R_L = 10kΩ and R_H = 28.7kΩ.

Selecting an NTC Sensor Resistor

Figure 22 shows an internal voltage divider reference circuit that limits the high and low temperature thresholds for V_{HOT} and V_{COLD}, respectively.

For a given NTC thermistor, select the appropriate R_{T1} and R_{T2} values to set the NTC window. Calculate R_{T1} and R_{T2} using Equation (7) and Equation (8), respectively:

$$R_{T1}=\frac{(1-V_{COLD})(1-V_{HOT})(R_L-R_H)}{(1-V_{HOT})\times V_{COLD}-(1-V_{COLD})\times V_{HOT}} \quad (7)$$

$$R_{T2}=\frac{V_{COLD}\times R_{T1}}{1-V_{COLD}}-R_L \quad (8)$$

Where V_{HOT} is the high temperature threshold, V_{COLD} is the low temperature threshold, R_H is the value of the NTC resistor at high temperatures within the required temperature operation range, and R_L is the value of the NTC resistor at low temperatures.

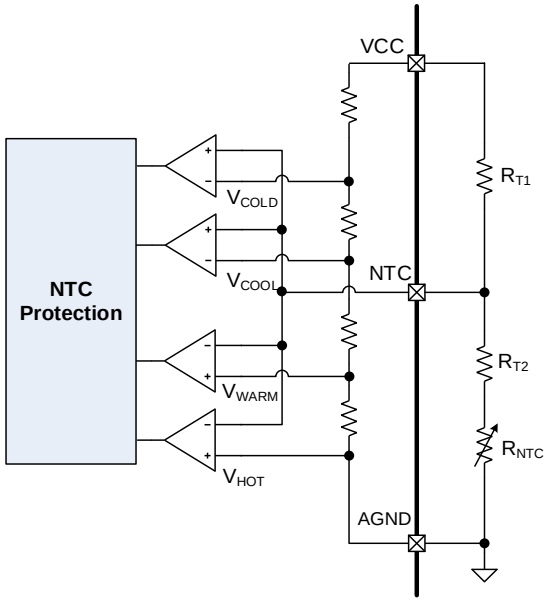


Figure 22: NTC Protection Block

R_{T1} and R_{T2} allow the high temperature limit and low temperature limit to be configured independently. With this feature, the MP2672A can use most types of NTC resistors with different temperature operation range requirements.

The R_{T1} and R_{T2} values depend on the type of the NTC resistor. For example, the 103AT thermistor has the following electrical characteristics:

- At 0°C, R_{NTC_COLD} = 27.28kΩ
- At 60°C, R_{NTC_HOT} = 3.02kΩ

Based on Equations (7) and Equation (8), as well as the V_{HOT} and V_{COLD} values from the electrical characteristics mentioned above, R_{T1} = 12.62kΩ, and R_{T2} = 3.63kΩ.

Apply the spreadsheet for R_{T1} and R_{T2} calculation if required.

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Selecting the Inductor

Inductor selection is a tradeoff between cost, size, and efficiency. A lower-value inductor results in lower DCR for components of a similar size, but results in higher current ripple, magnetic hysteretic losses, and output capacitances. The inductor ripple current should not exceed 30% of the maximum input current under the worst-case conditions.

Choose an inductor that does not saturate under the worst-case load conditions. The inductor's saturation current should be greater than the peak current limit of the low-side MOSFET.

When the MP2672A works in charge mode, estimate the required inductance with Equation (9):

$$L=\frac{V_{IN}\times(V_{SYS}-V_{IN})}{V_{SYS}\times f_{SW}\times\Delta I_{L_MAX}} \quad (9)$$

Where V_{SYS} is the system's minimum regulation voltage, f_{SW} is the switching frequency, and ΔI_{L_MAX} is the peak-to-peak inductor ripple current, calculated with Equation (10):

$$\Delta I_{L_MAX}=2\times\left(I_{L_PK}-I_{IN(MAX)}\right) \quad (10)$$

Where I_{L_PK} is the expected inductor peak current, and $I_{IN(MAX)}$ is maximum input current, estimated with Equation (11):

$$I_{IN(MAX)}=\frac{V_{SYS}\times I_{SYS(MAX)}}{V_{IN}\times\eta} \quad (11)$$

Where $I_{SYS(MAX)}$ is the maximum boost output current, and Ƞ is the boost efficiency.

With an 8.4V battery voltage, 2A maximum charge current, 8.7V system voltage, typical input voltage (V_{IN} = 5V), 1.2MHz switching frequency, 90% efficiency, and expected 4.5A inductor peak current, the inductance is calculated to be about 1.5µH.

A 1.5µH inductor with >5A saturation current is recommended for applications with a 1.2MHz switching frequency. A 2.5µH inductor with >5A saturation current is recommended for applications with a 600kHz switching frequency.

Selecting the Input Capacitor

C_{IN} is the boost converter's input capacitor in charge mode. Calculate C_{IN} with Equation (12):

$$C_{IN}=\frac{1-V_{IN}/V_{SYS}}{8\times f_{SW}^{2}\times L\times\Delta V_{IN}/V_{IN}} \quad (12)$$

Where ΔV_{IN} / V_{IN} can be estimated with Equation (13):

$$\frac{\Delta V_{IN}}{V_{IN}}=\frac{1-V_{IN}/V_{SYS}}{8\times C_{IN}\times f_{SW}^{2}\times L} \quad (13)$$

Assume the maximum input voltage ripple is 1%. When V_{SYS} is 9.2V, V_{IN} is 5V, L is 1µH, and f_{SW} is 1200kHz, then C_{IN} is calculated to be 4.7µF.

Place one >4.7µF ceramic capacitor with X5R or X7R dielectrics at the IN terminal.

Selecting the System Capacitor

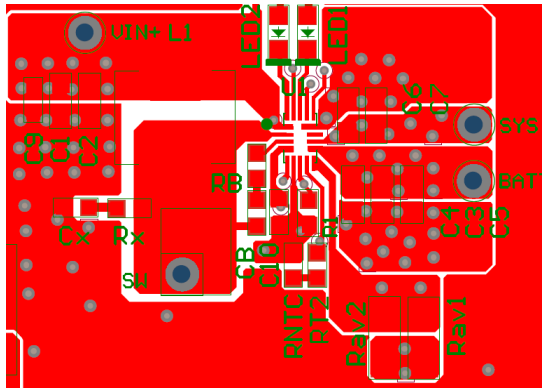
In charge mode, C_{SYS} is the output capacitor of the boost converter. C_{SYS} keeps the V_{SYS} ripple small (<0.5%) and ensures feedback loop stability. Select the system capacitor based on the ripple current. For the best results, X5R or X7R dielectric ceramic capacitors are recommended for their low ESR and small temperature coefficients. For most applications, two 22µF capacitors and one 1µF capacitor are sufficient. Place these capacitors as close as possible to the IC.

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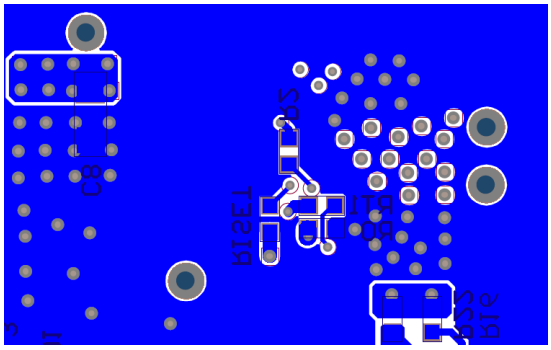
PCB Layout Guidelines

Efficient PCB layout is critical for meeting specified noise, efficiency, and stability requirements. For the best results, refer to Figure 23 and follow the guidelines below:

1. Place the output capacitor as close to SYS and PGND as possible.
2. Place the local power input capacitors as close as possible to the IN and PGND pins.
3. Minimize the length of the high-side switching node (SW, inductor) trace that carries the high current.
4. Keep the switching node short, and route it away from all control signals, especially the feedback network.
5. Route the power stages adjacent to their grounds.



Top Layer



Bottom Layer

Figure 23: Recommended PCB Layout

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TYPICAL APPLICATION CIRCUITS

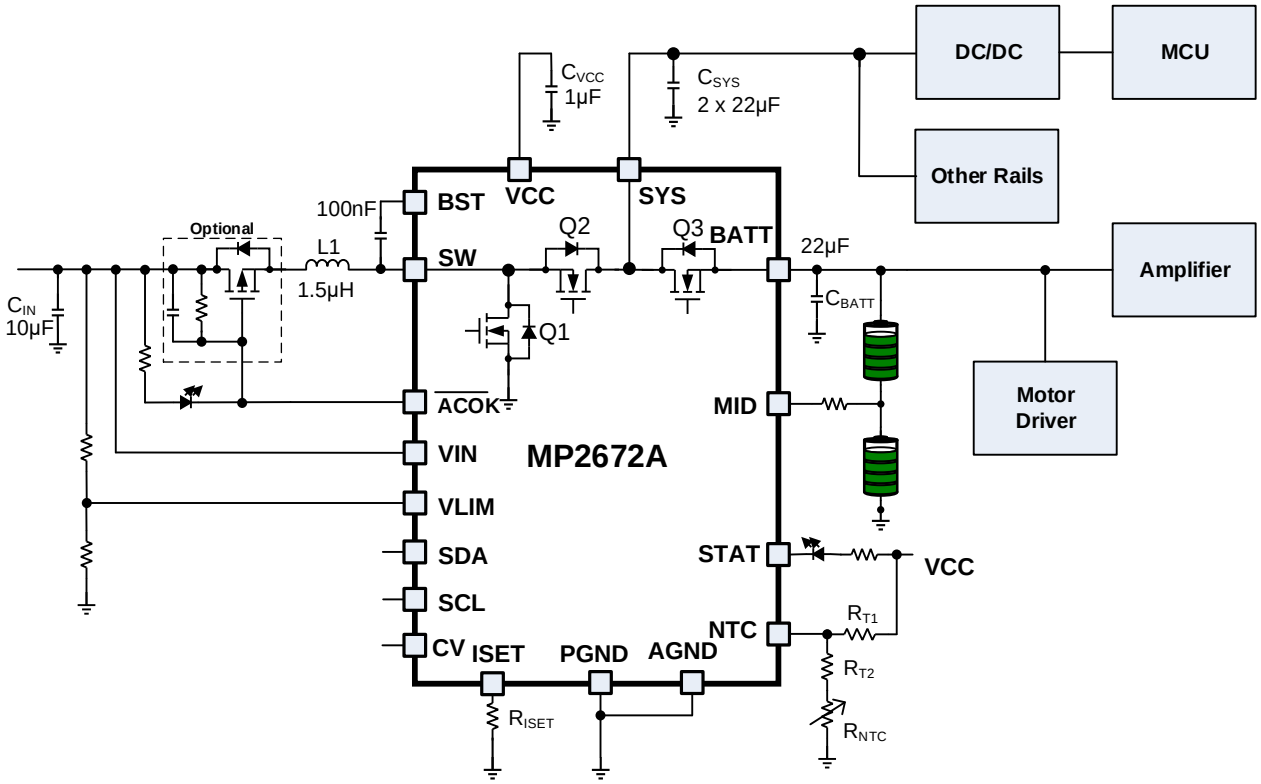


Figure 24: MP2672A-0000 Application Reference Circuit for NVDC Applications

Table 6: Key BOM from Figure 24

Qty	Ref	Value	Description	Package	Manufacturer
1	C_{IN}	10µF	Ceramic capacitor, 16V, X5R or X7R	0805	Any
2	C_{SYS}	22µF	Ceramic capacitor, 16V, X5R or X7R	0805	Any
1	C_{BATT}	22µF	Ceramic capacitor, 16V, X5R or X7R	1206	Any
1	C_{VCC}	1µF	Ceramic capacitor, 10V, X5R or X7R	0603	Any
1	C_{BST}	100nF	Ceramic capacitor, 25V, X5R or X7R	0603	Any
1	L1	1.5µH	Inductor, 1.5µH, saturation current >8A, low DCR	SMD	Any

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TYPICAL APPLICATION CIRCUITS *(continued)*

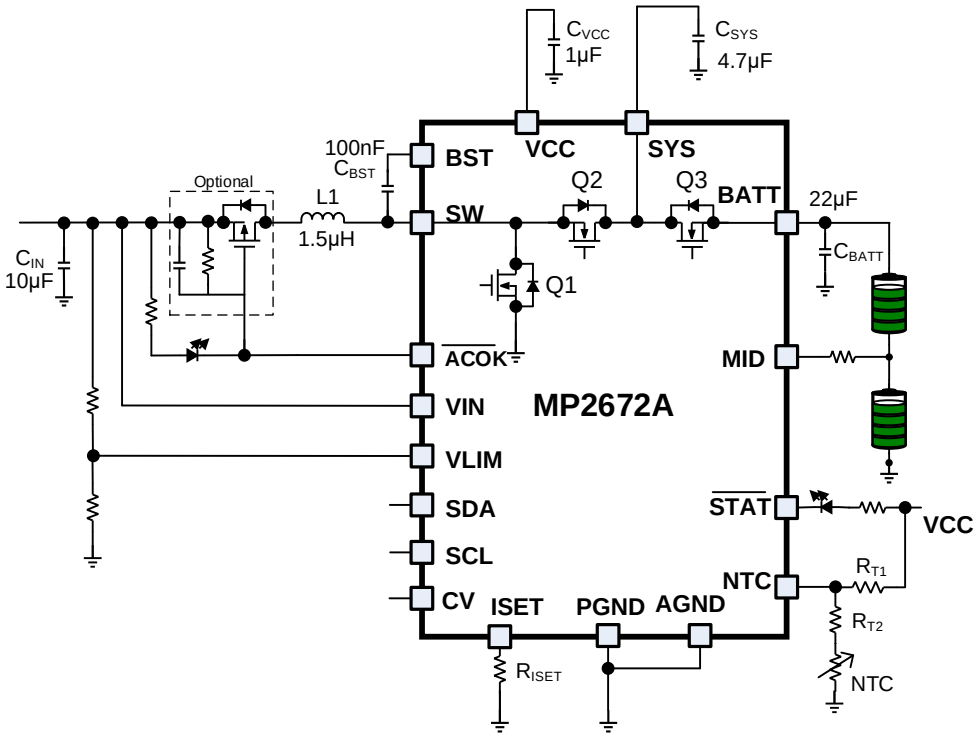


Figure 25: MP2672A-000E Application Reference Circuit for Charge Only Applications

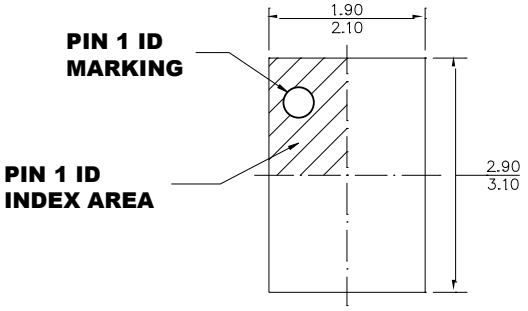
Table 7: Key BOM from Figure 25

Qty	Ref	Value	Description	Package	Manufacturer
1	C_{IN}	10µF	Ceramic capacitor, 16V, X5R or X7R	0805	Any
1	C_{SYS}	4.7µF	Ceramic capacitor, 16V, X5R or X7R	0805	Any
1	C_{BATT}	22µF	Ceramic capacitor, 16V, X5R or X7R	1206	Any
1	C_{VCC}	1µF	Ceramic capacitor, 10V, X5R or X7R	0603	Any
1	C_{BST}	100nF	Ceramic capacitor, 25V, X5R or X7R	0603	Any
1	L1	1.5µH	Inductor; 1.5µH, saturation current >8A, low DCR	SMD	Any

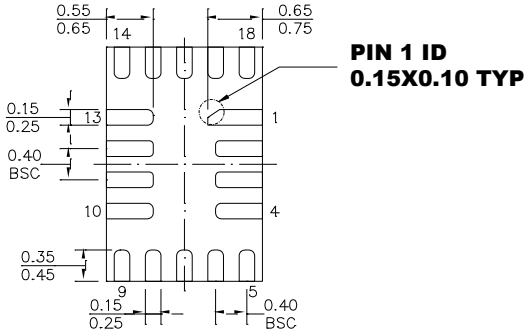
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PACKAGE INFORMATION

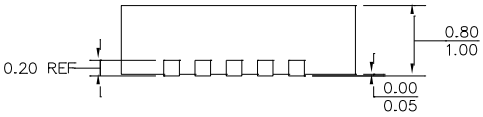
QFN-18 (2mmx3mm)



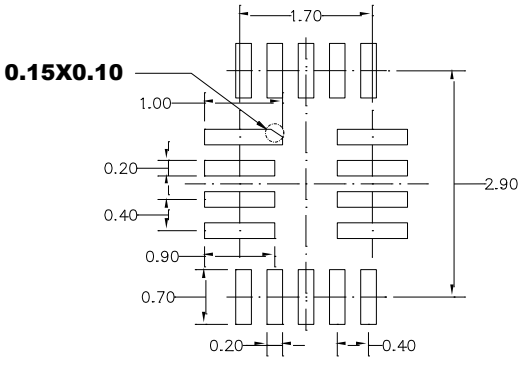
TOP VIEW



BOTTOM VIEW



SIDE VIEW



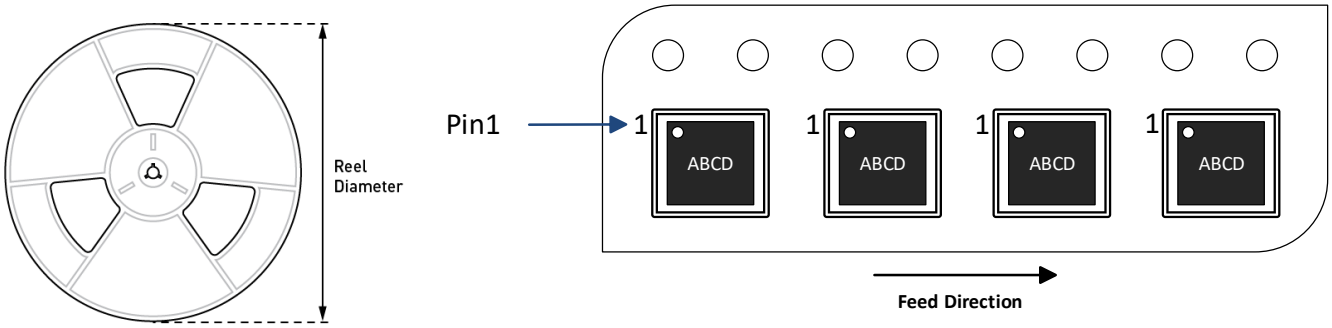
RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

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CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP2672AGD-xxxx–Z	QFN-18 (2mmx3mm)	5000	N/A	N/A	13in	12mm	8mm

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Revision History

Revision #	Revision Date	Description	Pages Updated
1.0	11/10/2020	Initial Release	-

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