MP2759

36V Switching Charger with Power Path Management for 1-Cell to 6-Cell Batteries

DESCRIPTION

The MP2759 is a highly integrated switching charger designed for applications with 1-cell to 6-cell series Li-ion or Li-polymer battery packs. The device supports several battery chemistry types with different battery regulation voltages.

The device operates from a maximum 36V DC input voltage and hold-off up to 45V. When an input power supply is present, the MP2759 charges the battery with four phases: trickle charge, pre-charge, constant current (CC) charge, and constant voltage (CV) charge.

The MP2759 offers input current limiting and a minimum input voltage limit function. If the input current reaches the input current limit, or the input voltage drops to the minimum input voltage limit, the MP2759 automatically reduces the charge current to limit the input power.

To guarantee safe operation, the MP2759 includes robust protection features such as battery over-voltage protection, battery temperature sensing and protection, thermal shutdown, and a charging safety timer.

The MP2759 is available in a small QFN-19 (3mmx3mm) package.

FEATURES

- Up to 36V Operating Input Voltage
- 45V Max Sustainable Voltage when Not Switching
- Up to 3A Charge Current
- 1 Cell to 6 Cells in Series with 3.6V, 4.0V, 4.1V, 4.15V, 4.2V, 4.35V, or 4.4V Battery Regulation Voltage for Each Cell
- Input Current Limit Regulation
- Input Minimum Voltage Regulation
- Support OR Selection Power Path Management
- 0.5% Battery Regulation Voltage Accuracy
- Integrated Reverse Blocking FET
- Internal Loop Compensation
- Charge Operation Indicator
- Input Status Indicator
- Battery Over-Voltage Protection
- Charging Safety Timer
- Battery Thermal Monitoring and Protection with JEITA Profile
- Available in a QFN-19 (3mmx3mm) Package
- Safety-Related Certification
  - IEC 62368-1 CB Certification

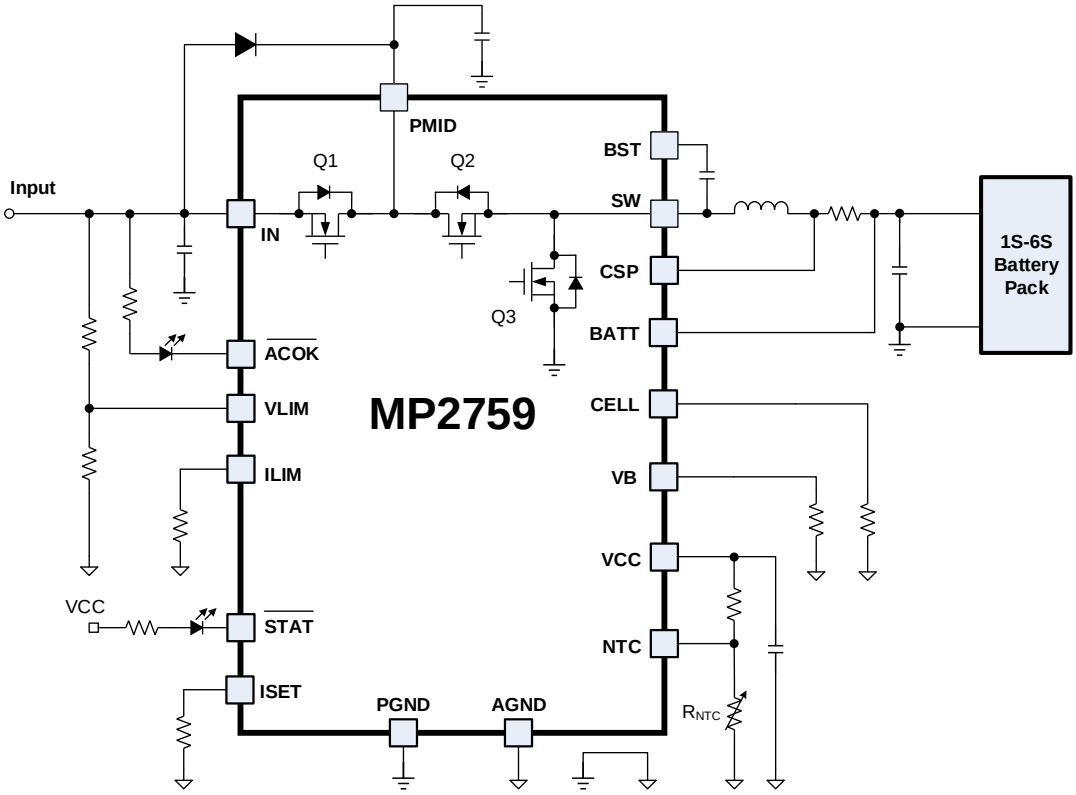
APPLICATIONS

- Industrial Medical Equipment
- Power Tools
- Robot and Portable Vacuum Cleaners
- Wireless Speakers

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TYPICAL APPLICATION



CELL Pin Connection	Number of Battery Cells
AGND	1-cell series
30kΩ to 40kΩ	2-cell series
60kΩ to 70kΩ	3-cell series
100kΩ to 110kΩ	4-cell series
160kΩ to 170kΩ	5-cell series
Pull up to VCC	6-cell series

VB Pin Connection	Battery Regulation Voltage
AGND	3.6V
30kΩ to 40kΩ	4.0V
60kΩ to 70kΩ	4.15V or 4.1V (OTP-configurable)
100kΩ to 110kΩ	4.2V
160kΩ to 170kΩ	4.35V
Pull up to VCC	4.4V

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ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MP2759GQ-xxxx**	QFN-19 (3mmx3mm)	*See Below*	1
EV2759-Q-00A	Evaluation Kit	N/A	

* For Tape & Reel, add suffix –Z (e.g. MP2759GQ-xxxx–Z).

**"-xxxx" is the register setting option. The factory default is "-0000." This content can be viewed in the OTP register map. Contact an MPS FAE to obtain an "-xxxx" value.

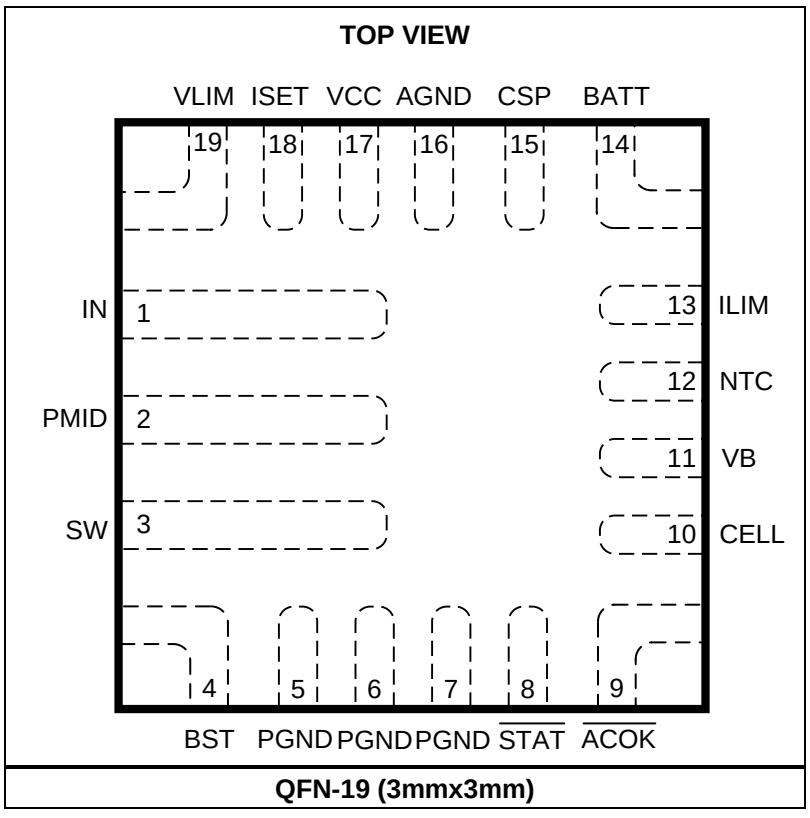
TOP MARKING

BMEY

LLLL

BME: Product code of MP2759GQ
Y: Year code
LLLL: Lot number

PACKAGE REFERENCE



QFN-19 (3mmx3mm)

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PIN FUNCTIONS

Pin #	Name	Type	Description
1	IN	Power	**Power input.** Connect a 1µF capacitor from IN to PGND. See Application Section for capacitor and voltage clamping recommendation.
2	PMID	Power	**Decoupling capacitor of the power stage.** Bypass PMID with a 2.2µF ceramic capacitor from PMID to PGND. Place the capacitor as close to the IC as possible with the shortest route for both the PMID and PGND current path. A 2A/40V Schottky diode must be placed between the IN pin and PMID pin.
3	SW	Power	**Switching node.** Connect SW to the inductor.
4	BST	Power	**Bootstrap pin.** Connect a 100nF bootstrap capacitor between the BST and SW pins to form a floating supply to drive the high-side MOSFET (HS-FET) above the supply voltage.
5, 6, 7	PGND	Power	**Power ground.**
8	$\overline{\text{STAT}}$	O	**Status indication.** This pin indicates the charging operation status and fault status with an open-drain output (see Table 3 on page 15).
9	$\overline{\text{ACOK}}$	O	**Input voltage valid indication.** This pin is an open-drain output, active low.
10	CELL	I	**Battery cell number selection.**
11	VB	I	**Battery regulation voltage setting.**
12	NTC	I	**Temperature-sense input.** Connect the NTC pin to a negative temperature coefficient (NTC) thermistor. A JEITA profile is supported with configurable thresholds.
13	ILIM	I	**Input current limit setting pin**. Connect a resistor from ILIM to AGND.
14	BATT	I	**Battery positive sensing pin.** Place a minimum 10µF capacitor from BATT to PGND. See Application Section for capacitor and voltage clamping recommendation.
15	CSP	I	**Battery current-sense positive input.**
16	AGND	Power	**Analog ground.**
17	VCC	I	**Internal circuit power supply.** Bypass VCC to AGND with a 1µF ceramic capacitor.
18	ISET	I	**Charging current setting pin.** Connect a resistor from ISET to AGND.
19	VLIM	I	**Input voltage limit setting pin.** Connect to a resistor divider from VLIM to IN and AGND. This pin can be pulled low to disable charging.

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ABSOLUTE MAXIMUM RATINGS (1)

IN, PMID, ACOK, BATT, CSP to PGND .....-0.3V to +45V
SW to PGND.....-0.3V (-2V for 20ns) to +45V
BST to SW……..SW to SW + 5.5V
CSP to BATT .....-0.6V to +0.6V
All other pins to AGND.....-0.3V to +5.5V
Continuous power dissipation (T_A = 25°C) (2) 2.5W
Junction temperature .....150°C
Lead temperature (solder) .....260°C
Storage temperature..... -65°C to +150°C

ESD Ratings

Human body model (HBM) (3)..... 2000V
Charge device mode (CDM) (4)……..... 750V

Recommended Operating Conditions (5)

Supply voltage (V_{IN}) .....4V to 36V
I_{IN}.....Up to 3A
I_{CHG}.....Up to 3A
V_{BATT}.....Up to 26.4V
Operating junction temp (T_J).... -40°C to +125°C

Thermal Resistance (6) θ_{JA} θ_{JC}

QFN-19 (3mmx3mm)..... 50 ..... 12.. °C/W.

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can cause excessive die temperature, and the regulator may go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) Per ANSI/ESDA/JEDEC JS-001.
4) Per JESD22-C101.
5) The device is not guaranteed to function outside of its operating conditions.
6) Measured on JESD51-7, 4-layer PCB.

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ELECTRICAL CHARACTERISTICS

V_{IN} = 24V, 4-cell, V_{BATT} = 3.7V/cell, R_{SNS} = 20mΩ, T_A = -40°C to +125°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Input Power Characteristics						
IN under-voltage lockout (UVLO) threshold	V_{IN_UVLO}	V_{IN} falling	3.3	3.6	3.9	V
IN UVLO threshold hysteresis		V_{IN} rising		360		mV
IN vs. BATT headroom	V_{HDRM}	V_{IN} rising	1.5	2	2.4	V
IN vs. BATT headroom hysteresis		V_{IN} falling		400		mV
IN over-voltage lockout (OVLO) threshold	V_{IN_OVLO}	V_{IN} rising	35	36	37	V
IN OVLO threshold hysteresis		V_{IN} falling		1		V
DC/DC Converter						
Input shutdown current	I_{IN_SHDN}	V_{IN} = 32V, VLIM = AGND			600	μA
Input quiescent current	I_{IN_Q}	V_{IN} = 32V, charging is enabled, 4-cell, charging terminated		1		mA
BATT leakage current in shutdown mode	I_{BATT_SHDN}	V_{BATT} = 24V, V_{IN} = PGND		5.5	10	μA
VCC LDO output voltage	V_{VCC}	V_{IN} = 24V	4.8	5	5.2	V
VCC LDO output current limit	I_{VCC}		30			mA
Blocking FET on resistance	R_{ON_Q1}	T_A = 25°C		38	43	mΩ
HS-FET on resistance	R_{ON_Q2}	T_A = 25°C		38	43	mΩ
LS-FET on resistance	R_{ON_Q3}	T_A = 25°C		55	63	mΩ
Peak current limit for HS-FET	I_{HS_PK}	Constant current charge mode, T_A = 25°C	4.5	5.5	6.5	A
		Trickle charge or pre-charge, T_A = 25°C		3.2		
Switching frequency	f_{SW}	f_{SW} = 700kHz		690		kHz
		f_{SW} = 450kHz		440		
Battery Charger						
Trickle charge to pre-charge threshold	V_{BATT_TC}		1.9	2.0	2.1	V/cell
Trickle charge current	I_{TC}	T_A = -20°C to +85°C	70	100	130	mA
Pre-charge to fast charge threshold	V_{BATT_PRE}	VB = 4.0V, 4.1V, 4.15V, 4.2V, 4.35V, or 4.4V	2.9	3	3.1	V/cell
		VB = 3.6V	2.3	2.5	2.7	V/cell
Pre-charge current	I_{PRE}	I_{PRE} = 10% of I_{CC}, T_A = -20°C to +85°C	7	10	13	%
		I_{PRE} = 20% of I_{CC}, T_A = -20°C to +85°C	16	20	24	
Minimum pre-charge current	I_{PRE_MIN}	T_A = -20°C to +85°C	70	100	130	mA
Fast charge current	I_{CC}	R_{ISET} = 96kΩ	0.9	1	1.1	A
		R_{ISET} = 48kΩ	1.8	2	2.2	

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ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 24V, 4-cell, V_{BATT} = 3.7V/cell, R_{SNS} = 20mΩ, T_A = -40°C to +125°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Battery charge voltage regulation	V_{BATT_REG}	VB set to 4.2V, CELL set to 1S, T_A = 25°C	4.18	4.20	4.22	V
		VB set to 4.2V, CELL set to 2S, T_A = 25°C	8.36	8.40	8.44	
		VB set to 4.2V, CELL set to 3S, T_A = 25°C	12.54	12.60	12.66	
		VB set to 4.2V, CELL set to 4S, T_A = 25°C	16.72	16.80	16.88	
		VB set to 4.2V, CELL set to 5S, T_A = 25°C	20.90	21.00	21.11	
		VB set to 4.2V, CELL set to 6S, T_A = 25°C	25.07	25.20	25.33	
		VB set to 3.6V, CELL set to 3S, T_A = 25°C	10.75	10.80	10.85	
		VB set to 4.0V, CELL set to 3S, T_A = 25°C	11.94	12.00	12.06	
		VB set to 4.1V, CELL set to 3S, T_A = 25°C	12.24	12.30	12.36	
		VB set to 4.15V, CELL set to 3S, T_A = 25°C	12.39	12.45	12.51	
		VB set to 4.35V, CELL set to 3S, T_A = 25°C	12.98	13.05	13.12	
		VB set to 4.4V, CELL set to 3S, T_A = 25°C	13.13	13.20	13.27	
Battery charge termination current	I_{TERM}	I_{TERM} = 10% of I_{CC}, T_A = -20°C to +85°C	7	10	13	%
		I_{TERM} = 20% of I_{CC}, T_A = -20°C to +85°C	16	20	24	
Minimum termination current	I_{TERM_MIN}	T_A = -20°C to +85°C	60	100	145	mA
Charge termination deglitch time	t_{TERM_DGL}			100		ms
Auto-recharge battery voltage threshold	V_{RECH}	Below V_{BATT_REG}	150	200	250	mV/cell
Battery over-voltage protection threshold	V_{BATT_OVP}	Compared with V_{BATT_REG}, rising	110	150	190	mV/cell
Battery over-voltage protection threshold hysteresis		Compared with V_{BATT_OVP}, falling		125		mV/cell
Input Voltage and Input Current Regulation						
Input current limit	I_{IN_LIM}	R_{ILIM} = 80kΩ	0.9	1	1.1	A
		R_{ILIM} = 40kΩ	1.8	2	2.2	
Minimum input voltage regulation reference	$V_{IN_MIN_REF}$		1.18	1.2	1.22	V

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ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 24V, 4-cell, V_{BATT} = 3.7V/cell, R_{SNS} = 20mΩ, T_A = -40°C to +125°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Thermal Protection						
Thermal shutdown rising threshold (7)	T_{J_SHDN}	T_J rising		150		°C
Thermal shutdown hysteresis (7)				20		°C
Battery Temperature Monitoring and Protection						
NTC cold temp rising threshold	V_{COLD}	V_{COLD} = 74% of V_{VCC}	73	74	75	%
		V_{COLD} = 70% of V_{VCC}	69	70	71	
NTC cold temp rising threshold hysteresis		As a percentage of V_{VCC}		1.4		
NTC cool temp rising threshold	V_{COOL}	V_{COOL} = 65% of V_{VCC}	64	65	66	
		V_{COOL} = 60% of V_{VCC}	59	60	61	
NTC cool temp rising threshold hysteresis		As a percentage of V_{VCC}		1.4		
NTC warm temp falling threshold	V_{WARM}	V_{WARM} = 32.5% of V_{VCC}	31.5	32.5	33.5	
		V_{WARM} = 29% of V_{VCC}	28	29	30	
NTC warm temp falling threshold hysteresis		As a percentage of V_{VCC}		1.4		
NTC hot temp falling threshold	V_{HOT}	V_{HOT} = 23% of V_{VCC}	22	23	24	
		V_{HOT} = 25.9% of V_{VCC}	24.9	25.9	26.9	
NTC hot temp falling threshold hysteresis		As a percentage of V_{VCC}		1.4		
Logic I/O Pin Characteristics						
$\overline{\text{STAT}}$ pin output voltage		I_{SINK} = 5mA			0.4	V
$\overline{\text{ACOK}}$ pin output voltage		I_{SINK} = 2mA			0.4	V
VLIM pin off voltage	V_{VLIM_OFF}	VLIM falling	0.6	0.8	1.0	V
VLIM pin off hysteresis				40		mV
Timing Characteristic						
Charge safety timer	t_{TMR}	t_{TMR} = 20hrs	18	20	22	hours

Notes:

7) Guaranteed by design.

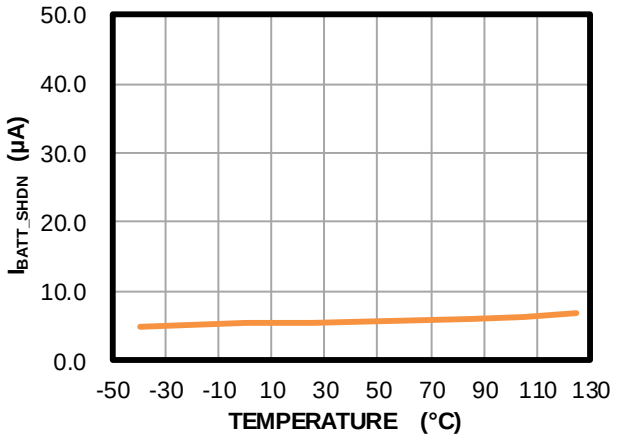
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TYPICAL PERFORMANCE CHARACTERISTICS

L = 10µH/35mΩ, C_{BATT} = 10µF, R_{SNS} = 20mΩ, unless otherwise noted.

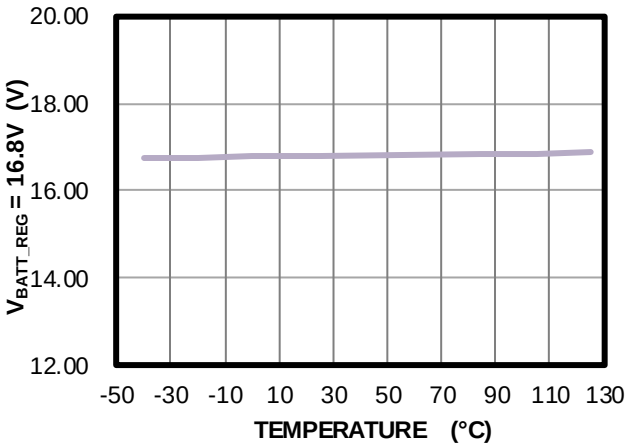
Battery Leakage Current in Shutdown Mode vs. Temperature

BATT = 24V



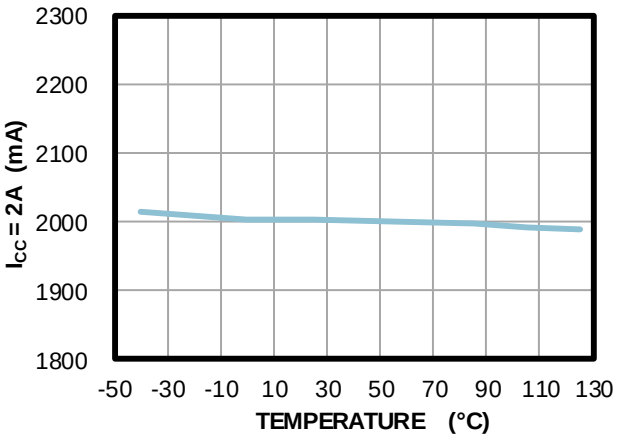
Battery Charge Voltage Regulation vs. Temperature

V_{BATT_REG} = 16.8V



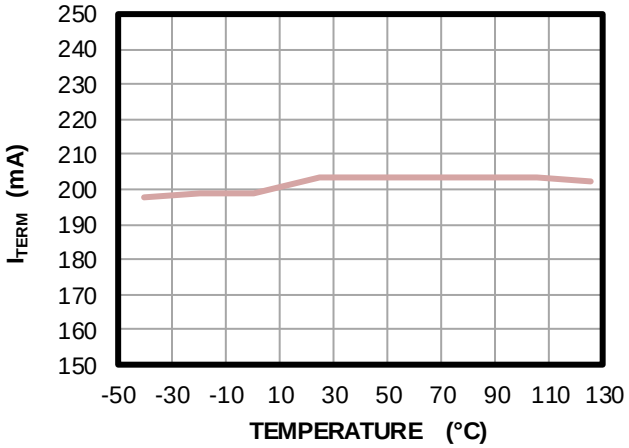
Charge Current vs. Temperature

I_{CC} = 2A



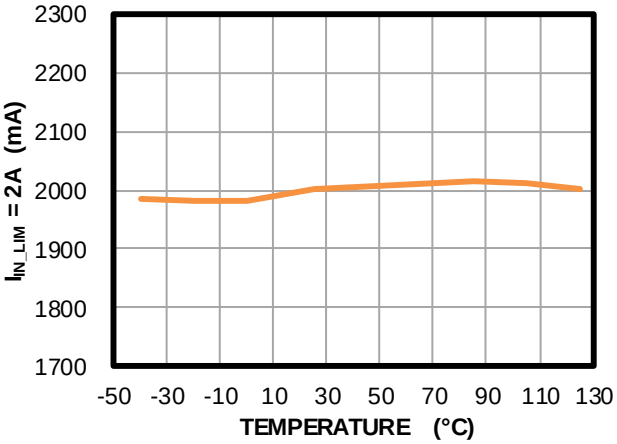
Termination Current vs. Temperature

I_{CC} = 2A

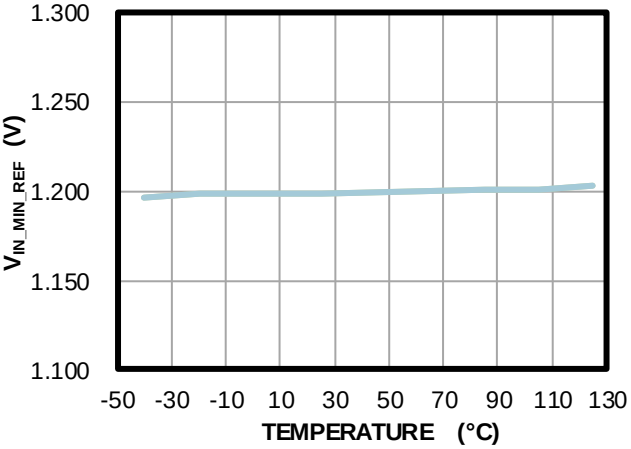


Input Current Limit vs. Temperature

I_{IN_LIM} = 2A



Minimum Input Voltage Reference vs. Temperature



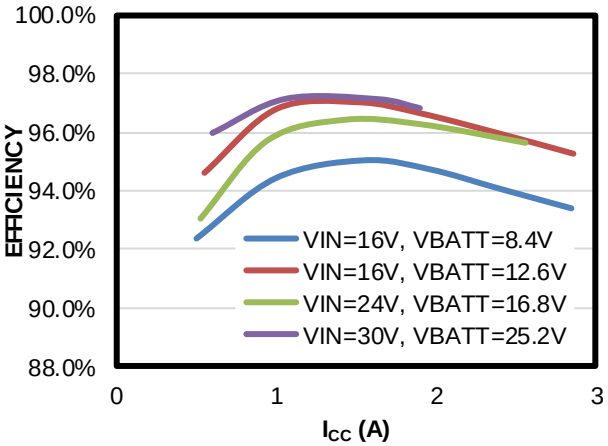
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TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

L = 10µH/35mΩ, C_{BATT} = 10µF, R_{SNS} = 20mΩ, T_A = 25°C, unless otherwise noted.

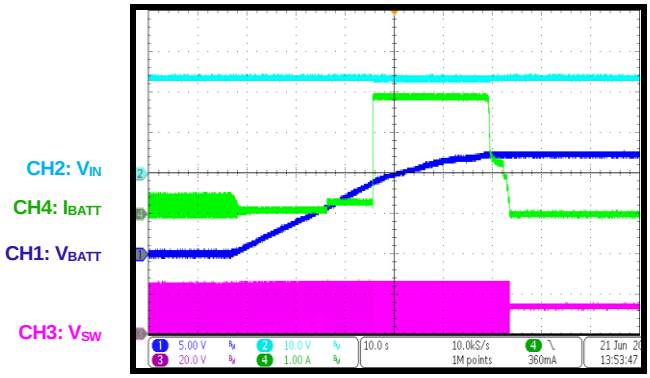
Efficiency vs. Charge Current

f_{SW} = 700kHz



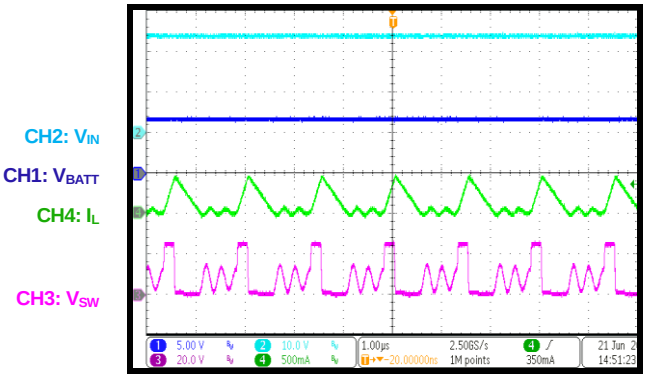
Battery Charge Curve

V_{IN} = 24V, 3-cell, V_{BATT_REG} = 4.2V, I_{CC} = 3A, I_{IN_LIM} = 2A



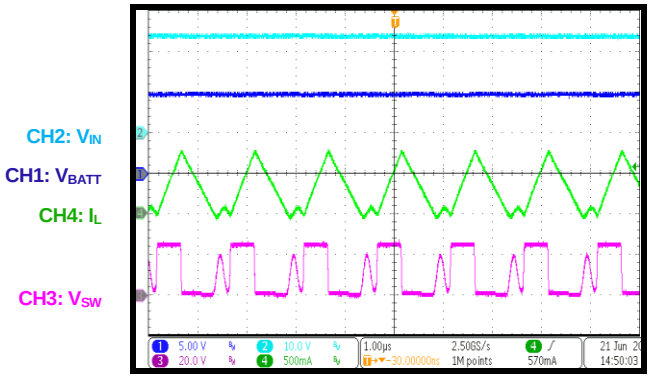
Trickle Charge Steady State

V_{IN} = 24V, 4-cell, V_{BATT} = 7V, I_{CC} = 3A, I_{IN_LIM} = 2A



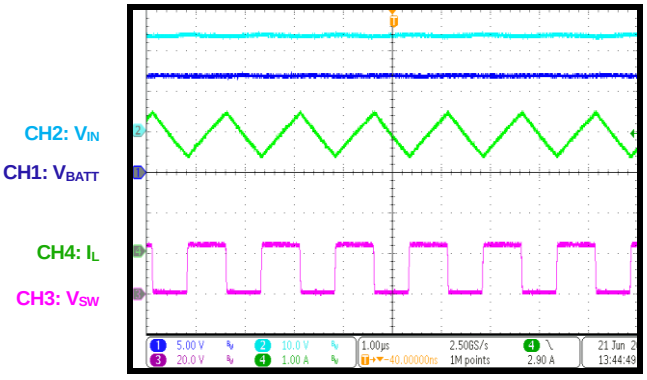
Pre-Charge Steady State

V_{IN} = 24V, 4-cell, V_{BATT} = 10V, I_{CC} = 3A, I_{IN_LIM} = 2A



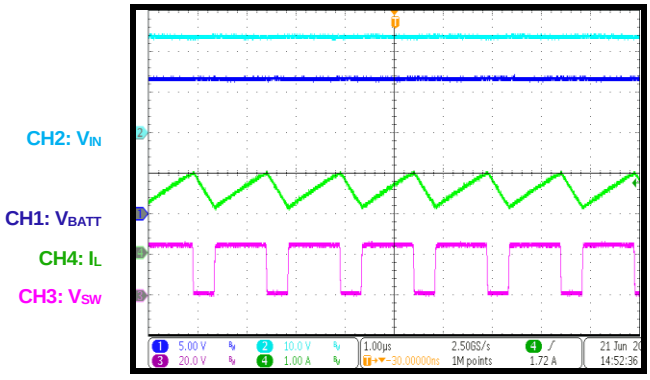
Constant Current Charge Steady State

V_{IN} = 24V, 4-cell, V_{BATT} = 12V, I_{CC} = 3A, I_{IN_LIM} = 2A



Constant Voltage Charge Steady State

V_{IN} = 24V, 4-cell, V_{BATT} = 16.8V, I_{CC} = 3A, I_{IN_LIM} = 2A



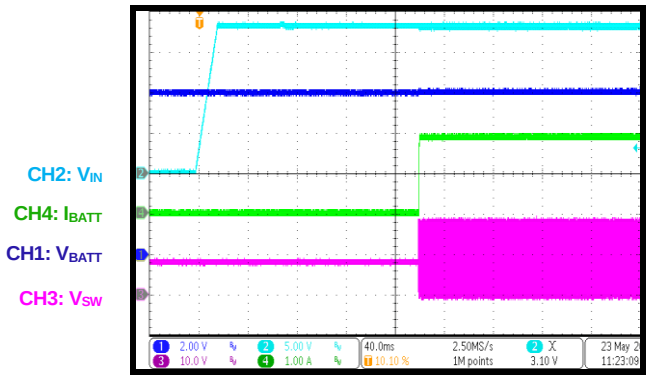
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TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

L = 10µH/35mΩ, C_{BATT} = 10µF, R_{SNS} = 20mΩ, T_A = 25°C, unless otherwise noted.

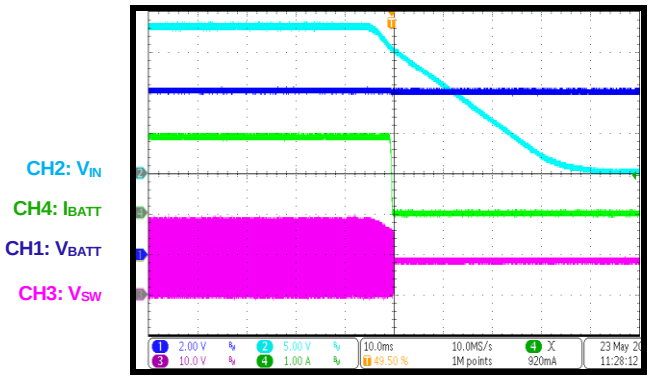
Start-Up, Constant Current Charge Mode

V_{IN} = 18V, 2-cell, V_{BATT} = 8V, I_{CC} = 2A, I_{IN_LIM} = 2A



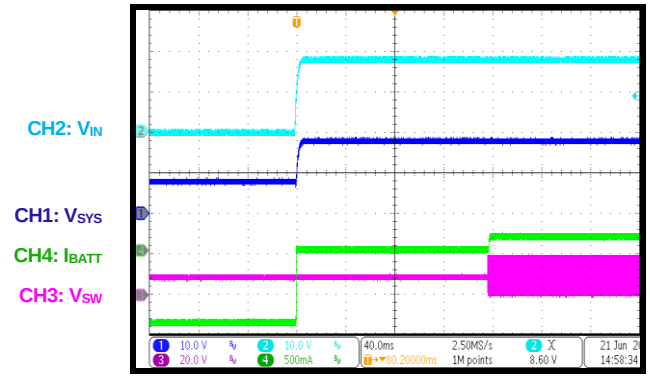
Shutdown, Constant Current Charge Mode

V_{IN} = 18V, 2-cell, V_{BATT} = 8V, I_{CC} = 2A, I_{IN_LIM} = 2A



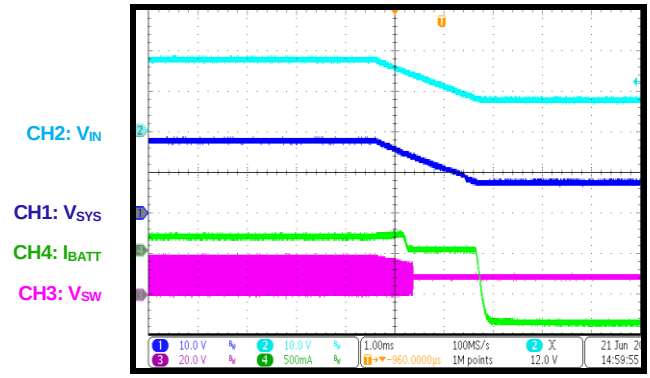
Start-Up, Power Path Operation

V_{IN} = 18V, 2-cell, V_{BATT} = 8V, I_{CC} = 2A, I_{IN_LIM} = 1A, I_{SYS} = 0.9A



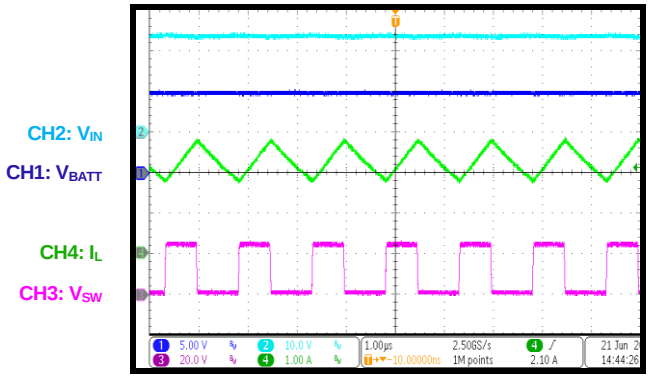
Shutdown, Power Path Operation

V_{IN} = 18V, 2-cell, V_{BATT} = 8V, I_{CC} = 2A, I_{IN_LIM} = 1A, I_{SYS} = 0.9A



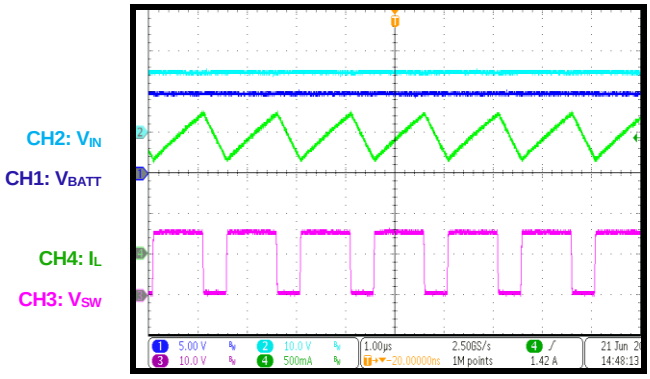
Input Current Limit Loop Control

V_{IN} = 24V, 3-cell, V_{BATT} = 10V, I_{CC} = 3A, I_{IN_LIM} = 1A



Input Voltage Limit Loop Control

V_{IN} = 24V/1A, 3-cell, V_{BATT} = 10V, I_{CC} = 3A, I_{IN_LIM} = 2A, V_{IN_LIM} = 15V



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FUNCTIONAL BLOCK DIAGRAM

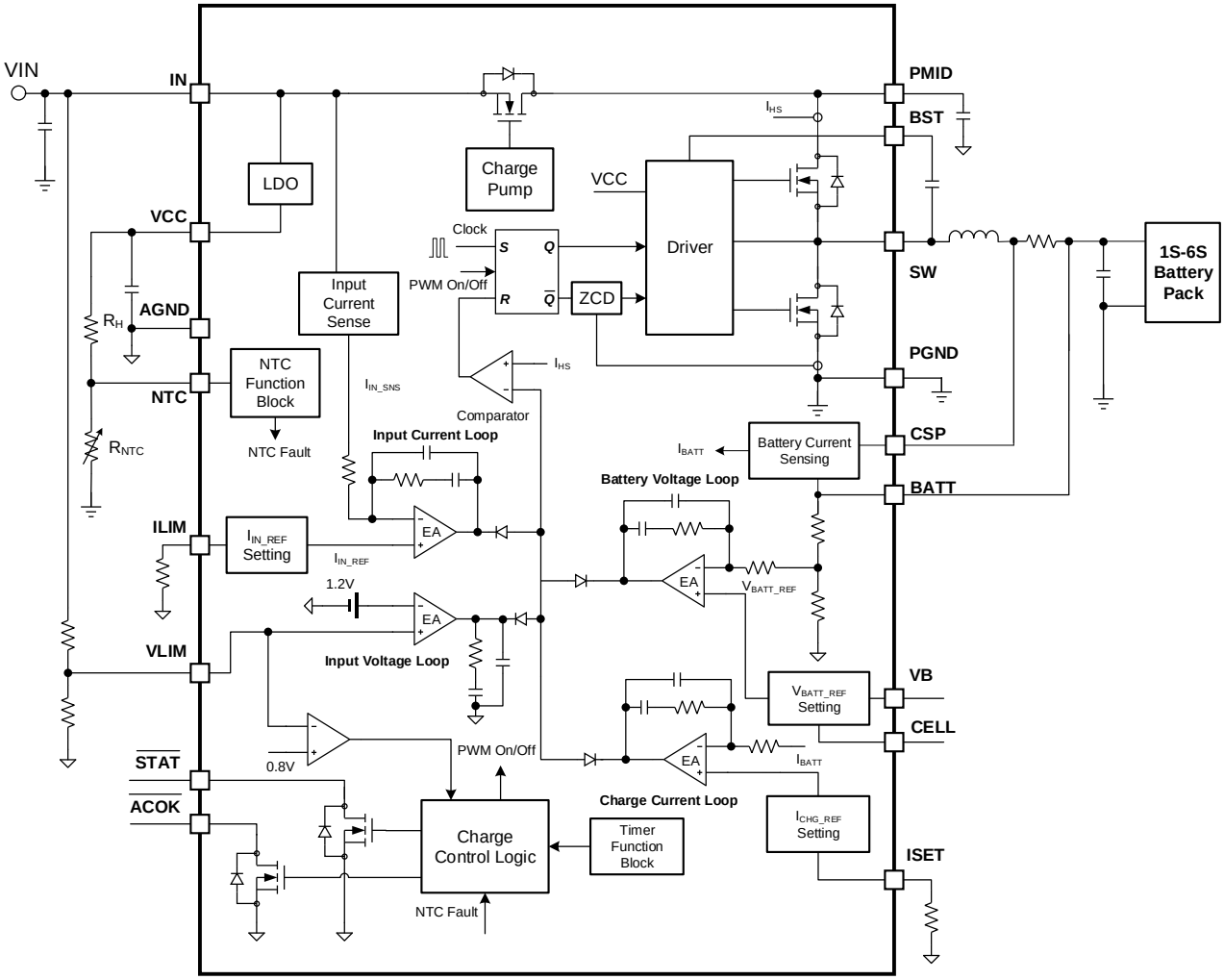


Figure 1: Functional Block Diagram

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OPERATION

Introduction

The MP2759 is a highly integrated switching charger designed for applications with 1-cell to 6-cell series Li-ion or Li-polymer batteries. The device manages battery charging with various series cell number selections and charge regulation voltages.

Power Supply

The VCC pin is powered by the IN pin. VCC generates a regulated 5V output with a minimum 30mA current limit. The VCC voltage (V_{VCC}) powers the internal bias circuit and power MOSFET driver. It can also be used for external resistor logic pull up, or LED driver bias. When the input source is absent and only a battery is present, VCC has no output.

The IC exits sleep mode and is ready to start the charging process once V_{VCC} exceeds the internal under-voltage lockout (UVLO) threshold.

Input Valid Indication

The IC checks the voltage of the input source (V_{IN}) before start-up. The input source has to meet the following conditions:

- $V_{IN} > V_{IN_UVLO}$
- $V_{IN} > V_{BATT} + V_{HDRM}$

The $\overline{ACOK}$ pin pulls low after V_{IN} meets the requirements above, which indicates that the input power source is ready. After a 170ms delay, the DC/DC converter is enabled.

Charge Cycle

The IC checks the battery voltage to provide four charging phases: trickle charge, pre-charge, constant current (CC) charge, and constant voltage (CV) charge (see Figure 2). These phases are described below:

Phase 1 (trickle charge): If the battery voltage is below V_{BATT_TC} (2V/cell), the IC charges the battery with a trickle charge current of 100mA.

Phase 2 (pre-charge): When the battery voltage exceeds V_{BATT_TC} (2V/cell) but is below V_{BATT_PRE} (3V/cell) (2.5V/cell for a 3.6V battery regulation setting), the IC charges the battery with 10% of the fast charge setting current (I_{CC}), and the minimum pre-charge current is clamped to 100mA.

Phase 3 (constant current fast charge): When the battery voltage exceeds V_{BATT_PRE} (3V/cell) (2.5V/cell for 3.6V battery regulation setting), the IC enters the constant current fast charge phase. The charge current (I_{CC}) can be set by the ISET pin resistor.

Phase 4 (constant voltage charge): When the battery voltage reaches the charge regulation voltage (V_{BATT_REG}), the charge current begins to decrease. When the charge current drops to the battery termination threshold (I_{TERM}), the charge cycle is considered complete after a deglitch time (t_{TERM_DGL}). If the charge current does not reach I_{TERM} before the charging safety timer expires, then the charge cycle ends and the corresponding timeout fault signal is asserted.

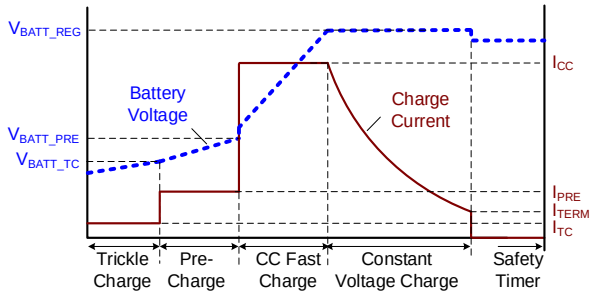


Figure 2: Typical Charge Profile

Charge Termination

The termination current threshold (I_{TERM}) is 10% of the fast charge setting current (I_{CC}), and the minimum termination threshold is clamped to 100mA.

Charging is terminated when all of the following conditions are met:

- The charge current is below the termination threshold for the deglitch time (t_{TERM_DGL}, typically 100ms).
- The IC operates in constant voltage charge mode.
- The IC is not in input current or input voltage loop operation.

Auto-Recharge

Once the battery charging cycle completes, the charger remains off. During this time, the external load may consume battery power, or the battery may self-discharge.

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A new charge cycle automatically begins if the battery voltage falls below the auto-recharge threshold and input power is present. The charging safety timer resets when the auto-recharge cycle begins.

Input Voltage and Input Current Limit

The MP2759 has input current and input voltage limiting to avoid overloading the input power supply.

The VLIM pin's voltage is the feedback input for the input voltage regulation loop. When the VLIM pin voltage falls to 1.2V, the charge current is reduced to prevent the input source from being further overloaded.

The input voltage can be regulated by a resistor divider connected from the IN pin to AGND. The regulated input voltage can be calculated with Equation (1):

$$V_{IN_MIN_REF} = V_{IN_MIN} \times \frac{R_1}{R_1 + R_2} (V) \quad (1)$$

Where $V_{IN_MIN_REF}$ is the internal voltage reference (about 1.2V), V_{IN_MIN} is the desired regulation voltage, and R1 and R2 are the resistor dividers.

When the VLIM pin's voltage is pulled below 0.8V, the charger is disabled.

The input current limit (I_{IN_LIM}) can be set by the ILIM pin with a resistor (R_{ILIM}) connected to AGND. If Q1's input current reaches the preset limit, the charge current is reduced to keep the input current under regulation.

The input current limit can be estimated with Equation (2).

$$I_{IN_LIM}(A) = \frac{80(k\Omega)}{R_{ILIM}(k\Omega)} (A) \quad (2)$$

Cell Selection

The MP2759 can be configured to charge 1-cell to 6-cell series battery packs. The number of cells can be configured via the CELL pin (see Table 1).

Table 1: CELL Pin Selection

CELL Pin Connection	Battery Cell Number
AGND	1-Cell Series
30kΩ to 40kΩ	2-Cell Series
60kΩ to 70kΩ	3-Cell Series
100kΩ to 110kΩ	4-Cell Series
160kΩ to 170kΩ	5-Cell Series
Pull up to VCC	6-Cell Series

With different series cell number selections, the trickle charge to pre-charge threshold (V_{BATT_TC}), the pre-charge to fast charge threshold (V_{BATT_PRE}), the battery charge voltage regulation (V_{BATT_REG}), and the recharge threshold (V_{RECH}) all scale with the cell number to properly manage the charging phases.

Battery Regulation Voltage

The MP2759 supports several battery charge regulation voltages, which can be configured via the VB pin (see Table 2).

Table 2: Battery Regulation Voltage Selection

VB Pin Connection	Battery Regulation Voltage
AGND	3.6V
30kΩ to 40kΩ	4.0V
60kΩ to 70kΩ	4.15V/cell or 4.1V/cell (set via the OTP, bit[5])
100kΩ to 110kΩ	4.2V
160kΩ to 170kΩ	4.35V
Pull up to VCC	4.4V

Charge Current Setting

The MP2759 senses the external sense resistor to regulate the charge current. Generally, a 20mΩ sensing resistor is recommended. With a 20mΩ sensing resistor, the charge current can be set by the resistor placed between the ISET and AGND pins (R_{ISET}). I_{CC} can be calculated with Equation (3):

$$I_{CC}(A) = \frac{96(k\Omega)}{R_{ISET}(k\Omega)} (A) \quad (3)$$

The maximum charge current can be set at up to 3A, and is related to the PCB's thermal dissipation condition and the input voltage. With a lower input voltage, the IC's switching loss is

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smaller, and the maximum deliverable current can be higher. The charge current should be set according to the thermal performance for each application.

JEITA-Based Thermistor Qualification

The MP2759 monitors the battery temperature by measuring the voltage ratio between the NTC pin's voltage and the VCC pin's voltage. The IC has four voltage ratio thresholds: hot, warm, cool, and cold.

To initiate a charge cycle, the voltage on the NTC pin must be within the V_{HOT} to V_{COLD} range. If the NTC pin voltage exceeds V_{HOT} or falls below V_{COLD}, the IC suspends charging and waits for the NTC voltage to return to within its normal range.

If the NTC voltage is within the cool temperature range (V_{COLD} to V_{COOL}), the charge current is reduced to 50% of the set value.

If the NTC voltage in within the warm temperature range (V_{WARM} to V_{HOT}), the charge regulation voltage is reduced by 100mV/cell of the set value.

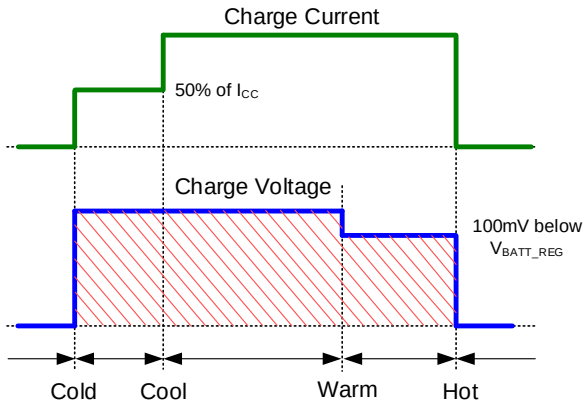


Figure 3: JEITA Protection

The recommend thermistor is 103AT with β = 3435. It is also recommended to have a pull-up resistor equal to the 25°C thermistor resistance.

Battery Over-Voltage Protection (OVP)

The MP2759 has battery over-voltage protection (OVP). If the battery voltage exceeds the battery over-voltage threshold (V_{BATT_OVP}), charging is disabled, the switcher stops, and the fault status is reported on the $\overline{STAT}$ pin.

Charging Safety Timer

The IC provides a safety timer to prevent extended charging cycles due to abnormal battery conditions. If the charging timer finishes before charging completes, charging is terminated.

The safety timer resets at the beginning of a new charge cycle. The safety timer restarts if any of the following actions occur:

- Input voltage removal and re-insertion
- A new charge cycle starts
- The VLIM pin is pulled below 0.8V, then released

Operation Indication

The IC has $\overline{ACOK}$ and $\overline{STAT}$ pins to indicate the power source and operation status. The statuses of the $\overline{ACOK}$ and $\overline{STAT}$ pins change based on different input power sources and operating conditions (see Table 3).

Table 3: Operation Indications

IN	Charging State	$\overline{ACOK}$	$\overline{STAT}$
Absent	NA	Hi-Z	Hi-Z
Present	In charging	Low	Low
Present	Charging complete, charging disabled	Low	Hi-Z
Present	NTC fault, safety timer expires, battery OVP	Low	Blinking at 2Hz

One-Time Programmable (OTP)

The MP2759 has a one-time programmable (OTP) memory function to configure the default value of several parameters. See the OTP Map section on page 16 for details on the configurable parameters.

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OTP MAP

Bit #	Symbol	Default	Description
10	JEITA_EN	0	0: JEITA enabled 1: JEITA disabled
9	VCOLD	0	Cold rising threshold as percentage of V_{NTC}/V_{VCC}. 0: 74% (0°C) 1: 70% (5°C)
8	VCOOL	0	Cool rising threshold as percentage of V_{NTC}/V_{VCC}. 0: 65% (10°C) 1: 60% (15°C)
7	VWARM	0	Warm falling threshold as Percentage of V_{NTC}/V_{VCC}. 0: 32.5% (45°C) 1: 29% (50°C)
6	VHOT	0	Hot falling threshold as percentage of V_{NTC}/V_{VCC}. 0: 23% (60°C) 1: 25.9% (55°C)
5	VREG_4P1	1	The bit sets the battery regulation voltage when the VB pin's resistor is between 60kΩ and 70kΩ. 0: 4.1V/cell 1: 4.15V/cell
4	ITERM	0	This bit sets the termination current. 0: 10% of I_{CC} 1: 20% of I_{CC}
3	IPRE	0	This bit sets the pre-charge current. 0: 10% of I_{CC} 1: 20% of I_{CC}
2	FSW	0	This bit selects the switching frequency. 0: 700kHz 1: 450kHz
1	TTMR	0	This bit sets the charging safety timer. 0: 20hrs 1: 10hrs
0	EN_TMR	0	This bit enables the safety timer. 0: Enabled 1: Disabled

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APPLICATION INFORMATION

COMPONENT SELECTION

Selecting the Inductor

Choose an inductor that does not saturate under the worst-case load condition. Estimate the required inductance with Equation (4):

$$L = \frac{V_{IN} - V_{BATT}}{\Delta I_{L_MAX}} \times \frac{V_{BATT}}{V_{IN} \times f_{SW}} \quad (4)$$

Where V_{IN} is the input voltage, V_{BATT} is the battery voltage, f_{SW} is the switching frequency, and ΔI_{L_MAX} is the maximum peak-to-peak inductor current, which is usually designed at 30% to 40% of the CC charge current.

It is recommended to use a 10µH inductor with a 5A saturation current for most applications.

Selecting the PMID Capacitor (C_{PMID})

The PMID pin capacitor (C_{PMID}) serves as the buck regulator's decoupling capacitor. A ceramic 2.2µF/50V capacitor with X5R or X7R dielectrics and 1206 size is recommended.

Do not put additional capacitance on the PMID pin. Connect a 2A/40V Schottky diode in an SMA package from IN to PMID.

Selecting the IN Capacitor

For applications where the input is ≤20V, it is recommended to make the input capacitor (C_{IN}) a 1µF/50V ceramic capacitor in a 0805 or 1206 package.

For applications where the input is >20V, (especially for those with input hot insertion conditions), add a ≥47µF electrolytic capacitor on the IN pin.

If a high-voltage adapter is plugged in during input hot insertion, the cable's parasitic inductance (together with the IN/PMID node capacitance) can generate an inrush current and voltage spike. An electrolytic capacitor and a TVS diode can help dampen or clamp the voltage spike.

The ESR of the electrolytic capacitor can effectively damp the inrush oscillation magnitude. A 47µF/50V electrolytic capacitor is recommended (see Table 4).

The hot insertion must be tested and verified for real applications. In case of a higher input voltage application (e.g. 28V), it is recommended to place a TVS diode across IN pin and GND pin. It is recommended to use one of the following diodes:

- 1SMA33A from Sunmate in an SMA package
- SMAJ33AQ from Diode in an SMA package

Selecting the BATT Capacitor

The MP2759 requires a ≥10µF capacitor to stabilize the loop on the BATT node. However, the battery capacitor (C_{BATT}) is generally effective only during hot plug insertion or short-circuit conditions.

When the battery is plugged in, there can be an overshoot on the BATT pin due to the oscillation caused by C_{BATT} and battery cable parasitic inductance. For 5-cell or 6-cell applications, this overshoot may harm the BATT pin. A 47µF/50V electrolytic capacitor can damp the overshoot with its ESR. Otherwise, use a TVS diode to clamp the BATT node spike. The recommended TVS diodes are listed above.

If the BATT node can be shorted to ground, C_{BATT} and the cable inductance can induce a negative voltage spike on the BATT pin, and may harm the IC. An electrolytic capacitor can help dampen the spike, or a unidirectional TVS diode can clamp the spike (see Table 4).

Protecting the PMID Pin

When a high-voltage battery is plugged in, there is a current path that flows from the main inductor, high-side MOSFET body diode, then charges up the PMID pin capacitor. An LC resonant circuit may induce a voltage spike on the PMID pin. With a high voltage battery, the PMID voltage can rise to a dangerous level, so the PMID pin must be protected.

For 5-cell or 6-cell applications, the PMID pin overshoot of battery insertion should be tested and verified in real application. A TVS diode can be added on PMID node to clamp the overshoot. The recommended TVS diodes are listed above. If the PMID pin has a TVS diode, the IN pin does not require a TVS diode (see Table 4).

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Table 4: Components Selection Guide

Pin	Condition	Recommendations
IN	≤20V input	1µF/50V ceramic capacitor for adapter applications. Add a ≥47µF capacitance for solar applications.
	>20V input	Add a 47µF/50V electrolytic capacitor. A TVS diode is required if the IN voltage exceeds the pin's maximum voltage rating during a VIN hot insertion test.
BATT	1-cell to 4-cell	10µF/50V ceramic capacitor.
	5-cell or 6-cell	Add a TVS diode or ≥47µF electrolytic capacitor.
PMID	-	Add a 2.2µF/50V ceramic capacitor (1206 size preferred). Connect a 2A/40V Schottky diode from IN to PMID. A TVS diode is required if the PMID voltage exceeds the pin's maximum voltage rating during a VBATT hot insertion test.

Setting the VLIM Pin

The VLIM pin is capable of multiple functions, described below.

Minimum Input Voltage Limiting

A resistive voltage divider connected from the IN pin to VLIM pin sets the minimum input voltage limit (V_{IN_MIN}).

The maximum V_{IN_MIN} regulation voltage should be set below the power supply's minimum DC output voltage, including the IR voltage drop from the DC input current and the series resistance on the PCB, connector, and cable.

The minimum V_{IN_MIN} regulation voltage should be set above $V_{BATT_REG} + V_{HDRM}$.

Disable Minimum Input Voltage Limiting

If input voltage limiting is not required, the VLIM pin can be tied to the VCC pin.

Enable Control

Pull the VLIM pin down below 0.8V to disable the charger and reset the safety timer. Figure 4 shows a recommended application circuit for this function.

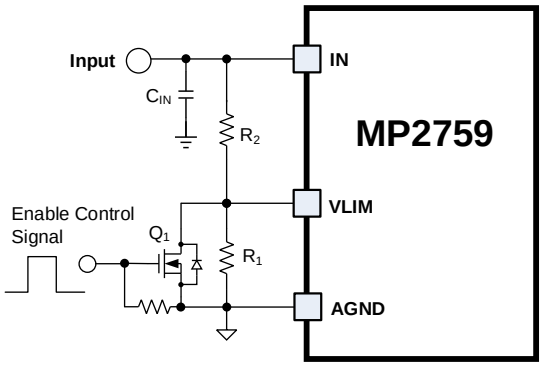


Figure 4: Enable Control

In this application, it is recommended to set R1 to 10kΩ.

Direct Enable Control

If input voltage limiting is not used, the VLIM pin can be directly driven by the host to enable/disable charging. It is recommended to use a 100kΩ resistor to pull the VLIM pin up to VCC. The logic high level should be above 1.3V, and the logic low level should be below 0.4V.

Power Path Operation

With an external P-channel battery MOSFET, the MP2759 supports power path management (see Figure 5). The battery FET gate can be driven by the IN pin signal. When an input source is not present, the battery FET connects the battery to the system. When an input is present, the battery FET turns off, and the system power is supplied by the input source through Q1.

The input current limit function helps power path operation because it prevents the input source from becoming overloaded. If the total input current in Q1 reaches the preset input current limit, the charging current is reduced, which keeps the input current limit within regulation.

For applications where the battery regulation voltage is below 15V, the battery FET gate can be directly driven by the IN node. If the input source is greater than 15V, use a Zener diode circuit to protect the battery FET gate from an over-voltage condition (see Figure 5).

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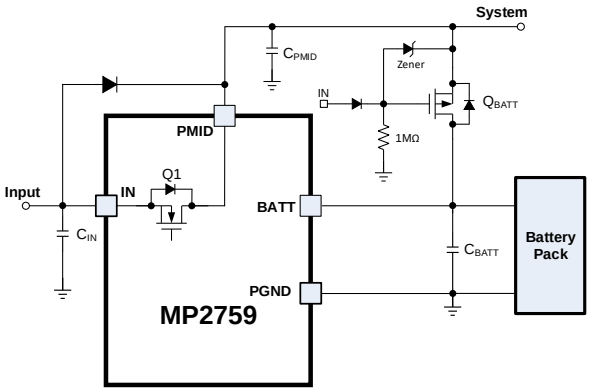


Figure 5: Power Path Management

Setting NTC Function

A JEITA profile is supported for battery temperature management. The NTC thermistor should be connected between the NTC pin and ground, and a pull-up resistor (R_H) should be placed between the VCC and NTC pins. It is recommended that the pull-up resistor value be equal to the 25°C thermistor resistance.

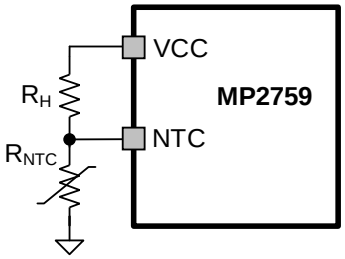


Figure 6: Thermistor Connection

The preset hot, warm, cool, and cold voltage thresholds are defined for a β = 3435 thermistor. A 103AT-2 thermistor with a 10kΩ pull-up resistor is recommended.

Selecting the Current-Sense Resistor

The MP2759 senses the current-sense resistor voltage drop to get the feedback information of the battery charge current. The default configuration is a 20mΩ resistor, and the data in this datasheet is derived from that resistor value.

Note that the soldering tin for the resistor has a resistance of about 1mΩ to 2mΩ, which can introduce some current regulation error. This error can be easily compensated for by fine-tuning the ISET pin resistor.

For smaller power applications, the current-sense resistor can be scaled up to improve regulation accuracy. The charge current scales inversely to the sensing resistor, such as the fast charge current (I_{CC}), pre-charge current (I_{PRE}), trickle charge curent (I_{TC}), and termination current (I_{TERM}).

PCB Layout Guidelines

PCB layout is important to meet specified noise, efficiency and stability requirements. For the best results, refer to Figure 7 and follow the guidelines below:

1. Place the PMID capacitor as close as possible to the PMID and PGND pins using a short copper plane connection.
2. Place the PMID capacitor on the same layer as the IC.
3. Minimize the high-frequency current path loop between the PMID capacitor and the buck converter power MOSFETs (PMID pin to capacitor, PGND to capacitor) (see Figure 7).
4. If possible, choose the PMID capacitor to have a 1206 or 1210 dimension, and route the SW traces beneath the PMID capacitor.
5. Minimize the copper area of the inductor's input terminal trace to reduce electrical and magnetic field radiation, but ensure that the trace is still wide enough to carry the charging current.
6. Connect the AGND pin to the ground of the battery capacitor, such as C_{BATT} or the PCB ground.
7. Connect the IC's power pin to as many copper planes as possible to conduct heat away from the IC.
8. Ensure that the number and physical size of the vias is sufficient for a current path.

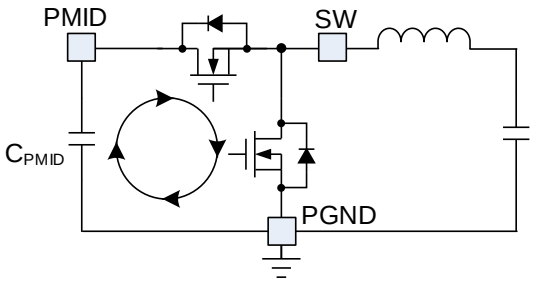


Figure 7: High-Frequency Current Path

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TYPICAL APPLICATION CIRCUIT

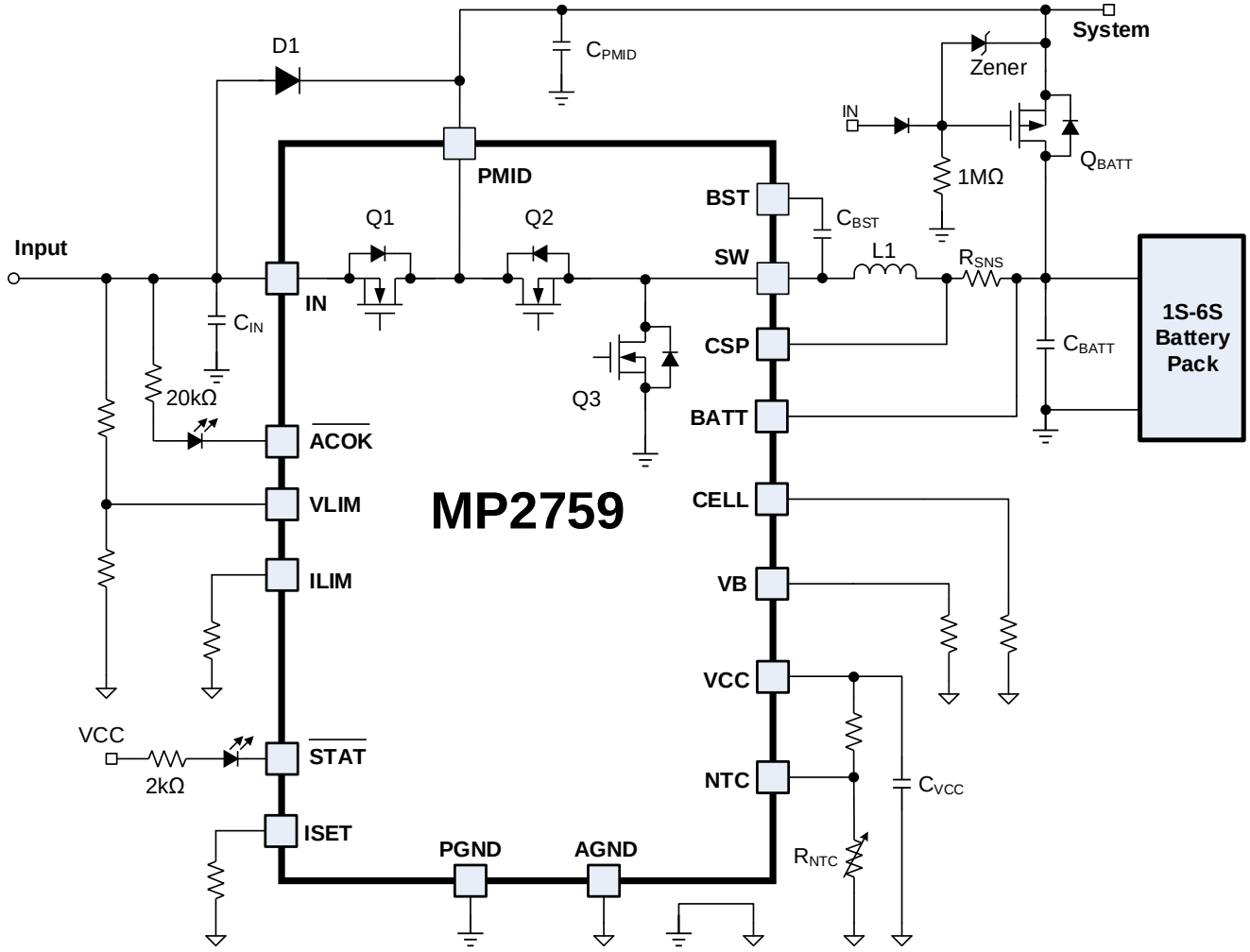


Figure 8: OR Selection Power Path Typical Application Circuit

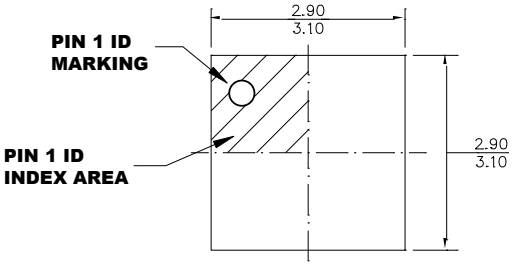
Table 5: Key BOM for Figure 8

Qty	Ref	Value	Description	Package	Manufacturer
1	C_{IN}	1µF	Ceramic capacitor, 50V, X5R or X7R	0805	Any
1	C_{BATT}	10µF	Ceramic capacitor, 50V, X5R or X7R	1206	Any
1	C_{PMID}	2.2µF	Ceramic capacitor, 50V, X5R or X7R	1206	Any
1	C_{VCC}	1µF	Ceramic capacitor, 16V, X5R or X7R	0603	Any
1	C_{BST}	100nF	Ceramic capacitor, 16V, X5R or X7R	0603	Any
1	L1	10µH	Inductor, I_{SAT} > 4A	SMD	Any
1	D1	B240	Schottky diode, 2A/40V	SMA	Any

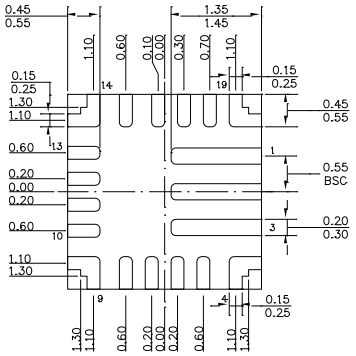
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PACKAGE INFORMATION

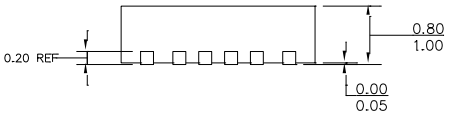
QFN-19 (3mmx3mm)



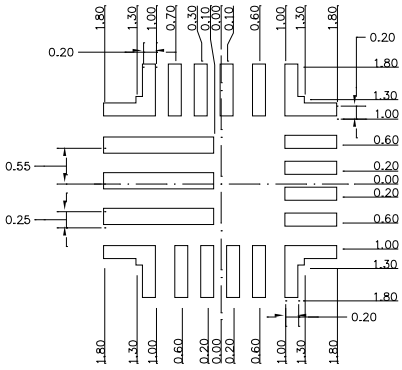
TOP VIEW



BOTTOM VIEW



SIDE VIEW



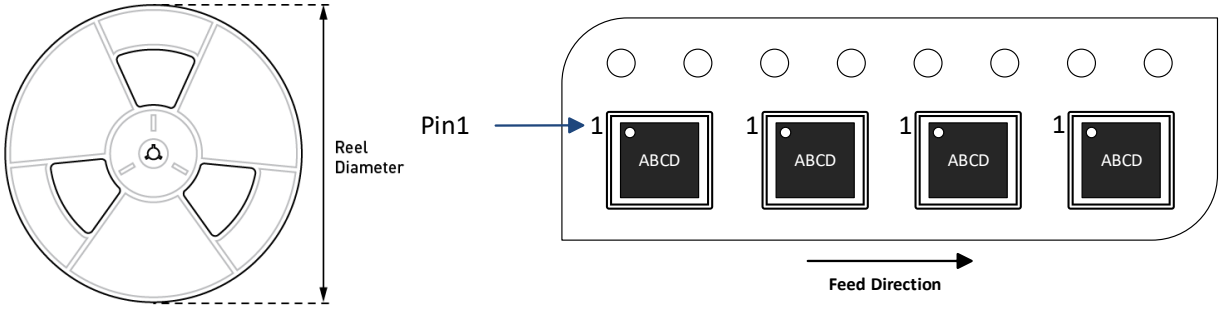
RECOMMENDED LAND PATTERN

NOTE:

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3) JEDEC REFERENCE IS MO-220.
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CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP2759GQ-xxxx–Z	QFN-19 (3mmx3mm)	5000	N/A	13in	12mm	8mm

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Revision History

Revision #	Revision Date	Description	Pages Updated
1.0	11/30/2020	Initial Release	-

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