MP3378

24 V, 4-Channel WLED Controller Plus High-Efficiency Buck Converter

The Future of Analog IC Technology

DESCRIPTION

The MP3378 is a one-chip solution designed for monitor applications. It includes a step-up controller with 4 current channels for backlighting and a high-efficiency buck converter for internal bus voltage or standby power.

The 4-string WLED controller drives an external MOSFET to boost up the output voltage from the input supply. It regulates the current in each LED string to the programmed value set by an external current-setting resistor. It supports both analog and PWM dimming independently to meet the special dimming mode request. In addition, rich protection modes are integrated including OCP, OTP, UVP, OVP, LED short/open protection, and inductor/diode short protection.

The high-efficiency buck converter operates in current mode with a built in MOSFET and synchronous rectifier. It offers a very compact solution to achieve excellent load and line regulation. Full protection features include OCP and thermal shutdown.

The MP3378 is available in SOIC28 and TSSOP28EP package.

FEATURES

WLED Controller:

- 4-String, Max 350 mA/String WLED Controller
- Up to 24 V Input Voltage Range
- 2.5% Current Matching Accuracy
- Programmable Switching Frequency
- PWM and Analog Dimming Mode
- Open and Short LED Protection
- Programmable Over-Voltage Protection
- Recoverable Thermal Shutdown Protection
- Over-Current Protection
- Over-Temperature Protection
- Inductor/Diode Short Protection

Buck Converter:

- 144 mΩ/58 mΩ Low Rds(on) Internal Power MOSFETs
- Low Quiescent Current
- Fixed 235 kHz Switching Frequency
- Frequency Sync from 250 kHz to 2 MHz External Clock
- AAM Power-Save Mode
- Internal Soft Start
- OCP and Hiccup
- Over-Temperature Protection
- Output Adjustable from 0.8 V

APPLICATIONS

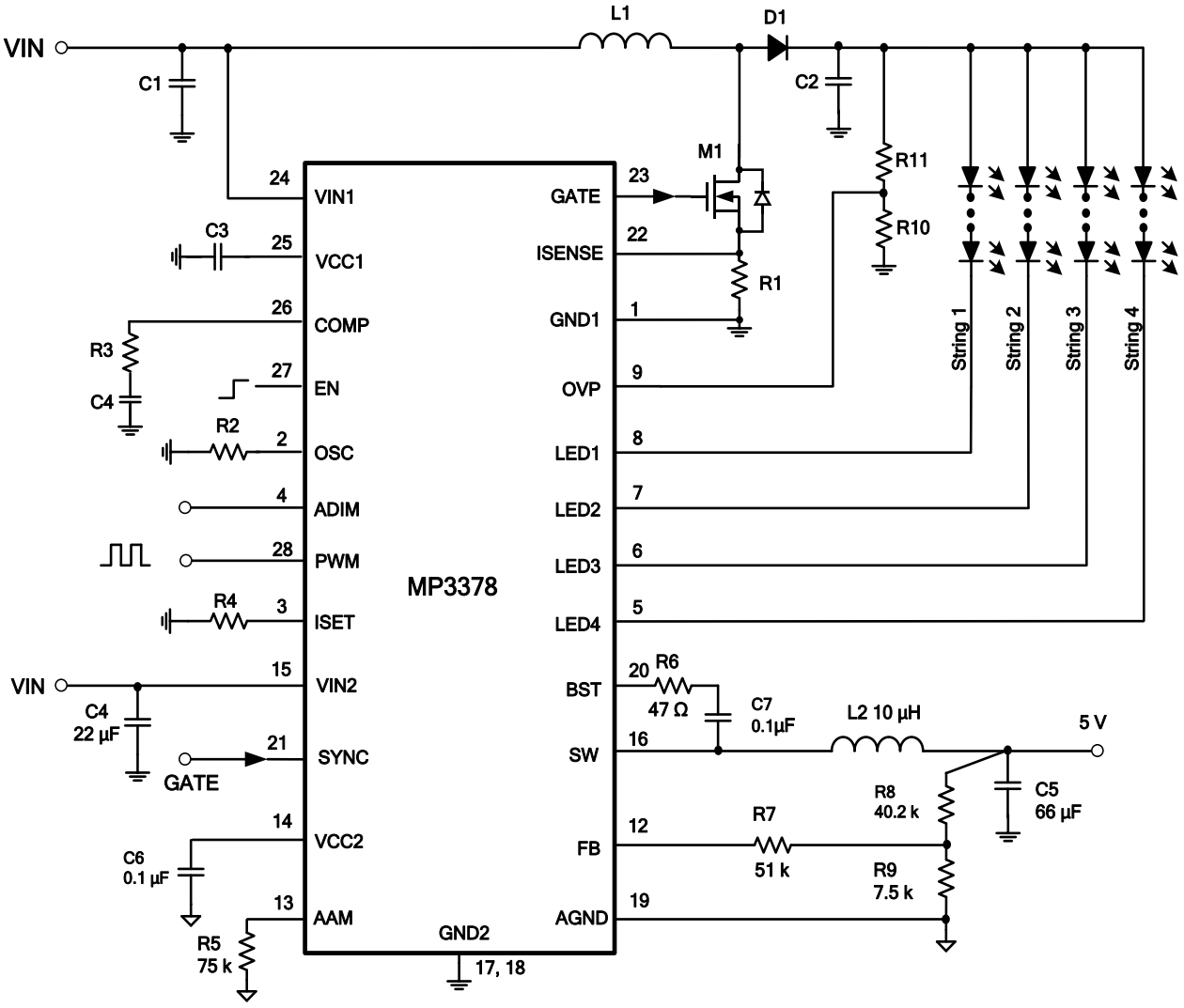
- Desktop LCD Flat Panel Displays
- Flat Panel Video Displays
- 2D/3D LCD TVs and Monitors

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TYPICAL APPLICATION



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ORDERING INFORMATION

Part Number	Package	Top Marking
MP3378GY	SOIC-28	*See Below*
MP3378GF	TSSOP-28 EP	*See Below*

* For Tape & Reel, add suffix –Z (e.g. MP3378GY–Z);
* For Tape & Reel, add suffix –Z (e.g. MP3378GF–Z);

TOP MARKING (MP3378GY)

MPSYYWW
MP3378
LLLLLLLLL

MPS: MPS prefix
YY: Year code
WW: Week code
MP3378: Product code of MP3378GY
LLLLLLLLL: Lot number

TOP MARKING (MP3378GF)

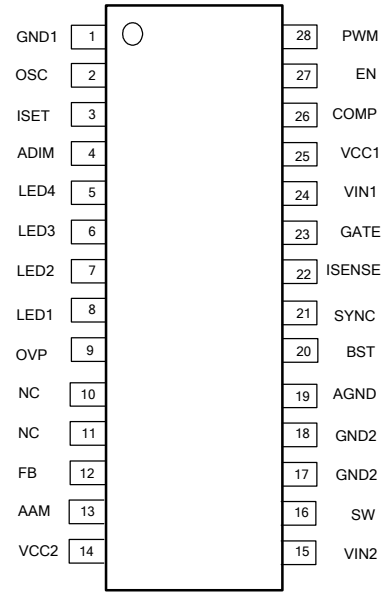
MPSYYWW
MP3378
LLLLLLLLL

MPS: MPS prefix
YY: Year code
WW: Week code
MP3378: Product code of MP3378GF
LLLLLLLLL: Lot number

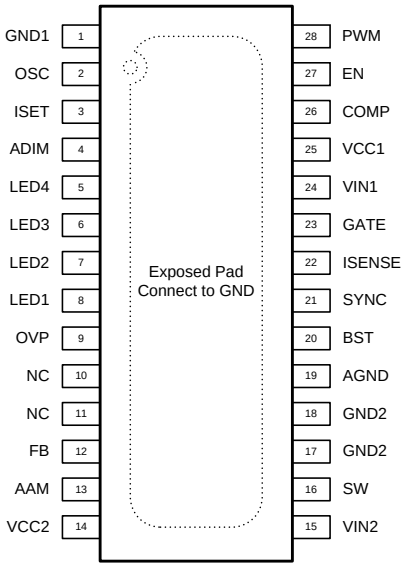
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PACKAGE REFERENCE

TOP VIEW



SOIC28



TSSOP28EP

ABSOLUTE MAXIMUM RATINGS (1)

WLED Driver

V_{IN1} ..... -0.3 V to + 28 V
V_{LED1} to V_{LED4} ..... -1 V to + 55 V
V_{GATE}, V_{CC1}, V_{ISENSE} ..... -0.3 V to + 6.5 V
All other pins..... –0.3 V to VCC1

Buck Converter

V_{IN2}, V_{SW} ..... –0.3 V to 28 V
V_{BST} ..... V_{SW} + 6 V
All other pins..... –0.3 V to 6 V
Continuous power dissipation (T_A = 25°C) **(2)**
SOIC-28 .....2 W
TSSOP-28 EP .....3.9 W
Junction temperature .....150°C
Lead temperature .....260°C

Recommended Operating Conditions (3)

Supply voltage (V_{IN1}, V_{IN2}) ..... 5 V to 24 V
Operating junction temp. (T_J). .. -40°C to +125°C

Thermal Resistance (4) θ_{JA} θ_{JC}

SOIC-28	62.5	30 °C/W
TSSOP-28 EP	32	6 °C/W

NOTES:

1) Exceeding these ratings may damage the device. The voltage is measured with a 20 MHz bandwidth limited oscilloscope.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

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ELECTRICAL CHARACTERISTICS (5)

V_{IN1} = V_{IN2} = 12 V, V_{EN} = 5 V, T_A = 25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
WLED controller section						
Supply current (quiescent)	I_{Q1}	V_{IN1} = 12 V, V_{EN} = 5 V, no load without switching, buck disabled	1.2	1.35	1.5	mA
Supply current (shutdown)	I_{ST}	V_{EN} = 0 V, V_{IN} = 12 V, buck disabled			1	μA
LDO output voltage	V_{CC1}	V_{EN} = 5 V, 7 V < V_{IN1} < 28 V, 0 < I_{VCC1} < 10 mA	5.4	6	6.6	V
VCC1 UVLO threshold	V_{CC1_UVLO}	Rising edge	3.6	4	4.4	V
VCC1 UVLO hysteresis				200		mV
EN high voltage	V_{EN_HIGH}	V_{EN} rising	1.8			V
EN low voltage	V_{EN_LOW}	V_{EN} falling			0.6	V
STEP-UP CONVERTER						
Gate driver impedance (sourcing)		V_{CC1} = 6 V, V_{GATE} = 6 V		4.1	7	Ω
Gate driver impedance (sinking)		V_{CC1} = 6 V, I_{GATE} = 10 mA		3	5	Ω
Switching frequency	f_{SW1}	R_{OSC} = 115 kΩ	470	530	590	kHz
		R_{OSC} = 374 kΩ	150	180	210	kHz
OSC voltage	V_{OSC}		1.20	1.23	1.26	V
Maximum duty cycle	D_{MAX1}			93		%
Cycle-by-cycle ISENSE current limit		Max duty cycle	145	180	230	mV
COMP source current limit	$I_{COMP\ SOLI}$	1 V < COMP < 1.9 V		70		μA
COMP sink current limit	$I_{COMP\ SILI}$	1 V < COMP < 1.9 V		17		μA
COMP transconductance	G_{COMP}	ΔI_{COMP} = ±10 μA		440		μA/V
CURRENT DIMMING						
PWM input low threshold	V_{PWM_LO}	V_{PWM} falling			0.75	V
PWM input high threshold	V_{PWM_HI}	V_{PWM} rising	1.25			V
Analog dimming input low threshold			0.38	0.41	0.44	V
Analog dimming input high threshold			1.44	1.49	1.54	V
LED CURRENT REGULATION						
ISET voltage	V_{ISET}		1.20	1.225	1.25	V
LEDX average current	I_{LED}	R_{ISET} = 30.5 kΩ	31.4	32	34.2	mA
Current matching (5)		I_{LED} = 32 mA			2.5	%
VCC max current limit	I_{CC1}_Limit		50	75	100	mA
LED FET resistance	R_LED	I_{LED} = 10 mA		1.7		Ω

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ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN1} = V_{IN2} = 12 V, V_{EN} = 5 V, T_A = 25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
LEDX regulation voltage	V_{LEDX}	I_{LED} = 330 mA		800		mV
		I_{LED} = 60 mA		260		mV
PROTECTION						
OVP (over-voltage protection) threshold	V_{OVP_OV}	Rising edge	1.20	1.23	1.26	V
OVP (over-voltage protection) threshold HYS	V_{OVP_HYS}	HYS		65		mV
OVP UVLO threshold	V_{OVP_UV}	Step-up converter fails	20	57	100	mV
LEDX UVLO threshold	V_{LEDX_UV}		120	190	260	mV
LEDX over-voltage threshold	V_{LEDX_OV}		5.8	6.3	6.8	V
LED short fault cycles	T_LED_OV			4096		
Latch-off current limit	V_{LMT}		600	660	720	mV
Thermal protection threshold	T_{ST}			150		°C
Thermal protection hysteresis				25		°C
Buck converter section						
Supply current (quiescent)	I_{Q2}	V_{FB} = 1 V, AAM = 0.5 V, WLED controller disabled	150	200	250	μA
VIN2 under-voltage lockout threshold	V_{IN2_UVLO}	Rising edge	3.7	3.9	4.1	V
VIN2 under-voltage lockout threshold-hysteresis			550	650	750	mV
VCC2 regulator	V_{CC2}		4.65	4.9	5.15	V
VCC2 load regulation		ICC2 = 5 mA	0	1	3	%
HS switch on resistance	HS_{RDS-ON}	V_{BST-SW} = 5 V		144		mΩ
LS switch on resistance	LS_{RDS-ON}	V_{CC2} = 5 V		58		mΩ
Current limit	I_{LIMIT}	Duty cycle = 40%	4.8	6	7.2	A
Oscillator frequency	f_{SW2}	V_{FB} = 750 mV	190	235	280	kHz
Foldback frequency	f_{FB}	V_{FB} = 200 mV		0.5		f_{SW2}
Maximum duty cycle	D_{MAX2}	V_{FB} = 750 mV	90	95		%
Minimum on time [5]	T_{ON_MIN}			90		ns
Sync frequency range	f_{SYNC}		0.25		2	MHz
Feedback voltage	V_{FB}	T_A = 25ºC	779	791	803	mV
Feedback current	I_{FB}	V_{FB} = 820 mV		10	50	nA
Soft-start period	T_{SS}	10% to 90%	0.8	1.5	2.2	ms
AAM source current	I_{AAM}		5.6	6.2	6.8	uA

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ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN1} = V_{IN2} = 12 V, V_{EN} = 5 V, T_A = 25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
SYNC high threshold	V_{SYNC_HI}		1.8			V
SYNC low threshold	V_{SYNC_LO}				0.6	V
Thermal shutdown				150		˚C
Thermal hysteresis				20		˚C

NOTE:

5) Matching is defined as the difference between the maximum to minimum current divided by 2 times the average currents.

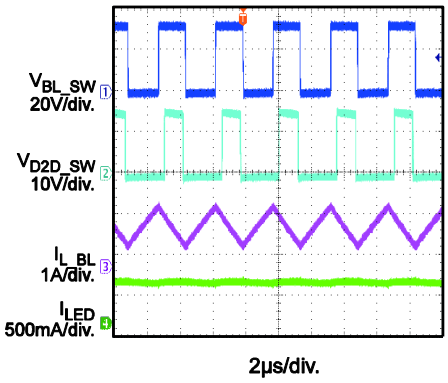
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TYPICAL PERFORMANCE CHARACTERISTICS

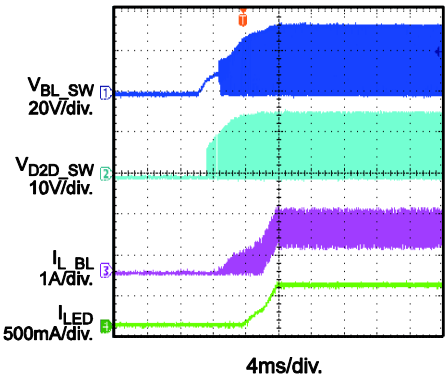
WLED Controller Section:

V_{IN} = 16 V, 10 LEDs in series, 4 strings parallel, 120 mA/string, T_A = 25°C, unless otherwise noted.

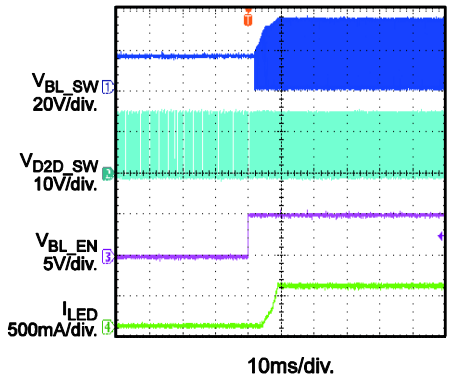
Steady State



VIN Power On

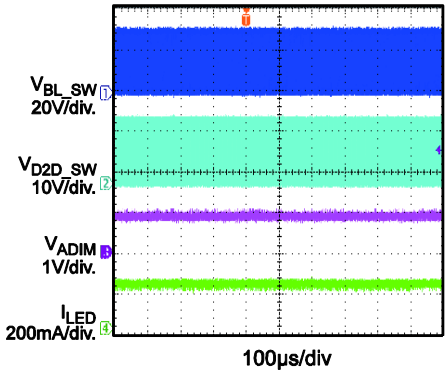


EN Power On



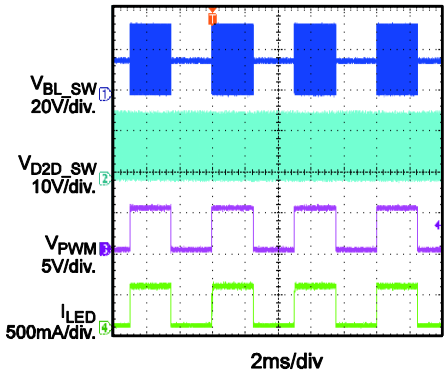
Analog Dimming

V_{ADIM}=0.9V

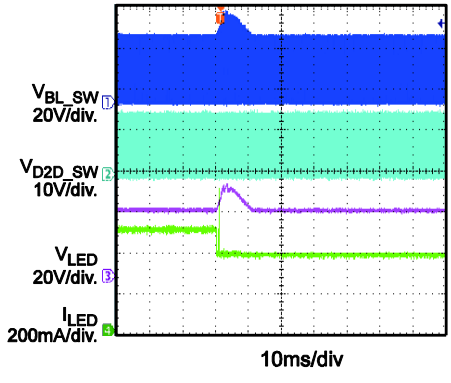


PWM Dimming

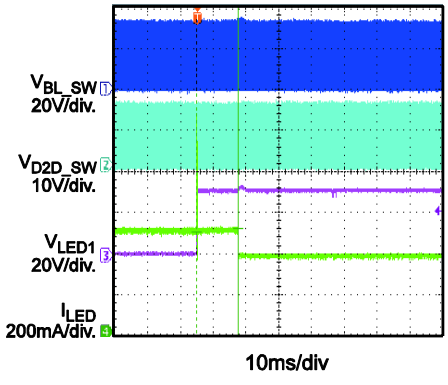
F_{PWM}=200Hz, D_{PWM}=50%



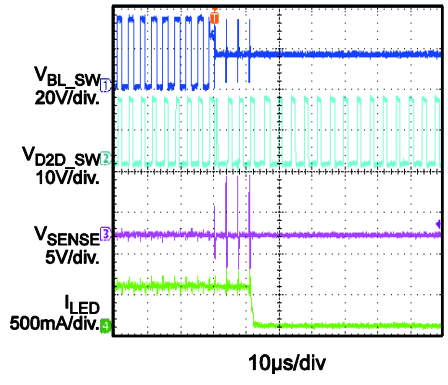
Open One String



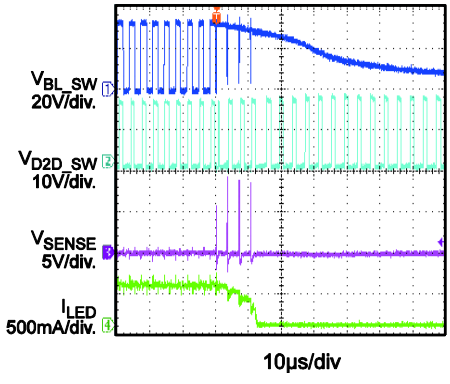
Short One String



Short Inductor



Short Diode



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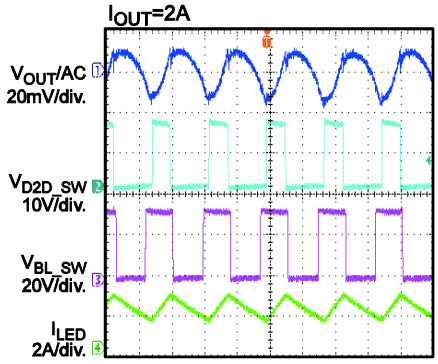
TYPICAL PERFORMANCE CHARACTERISTICS

Buck Converter Section:

V_{IN} = 16 V, V_{OUT} = 5 V, L2 = 10 µH, T_A = 25°C, unless otherwise noted.

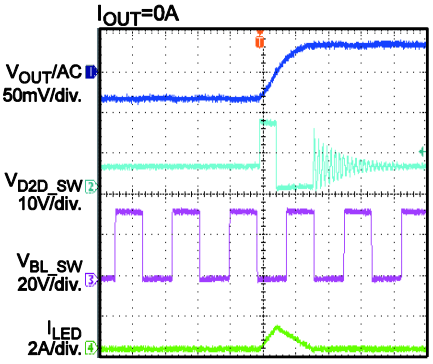
Output Ripple

I_{OUT}=2A



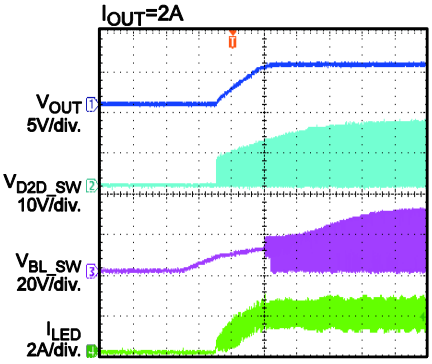
Output Ripple

I_{OUT}=0A



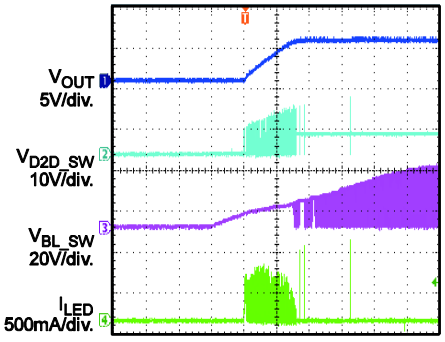
Power Up

I_{OUT}=2A



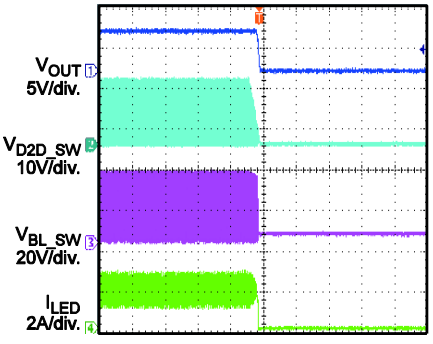
Power Up

I_{OUT}=0A



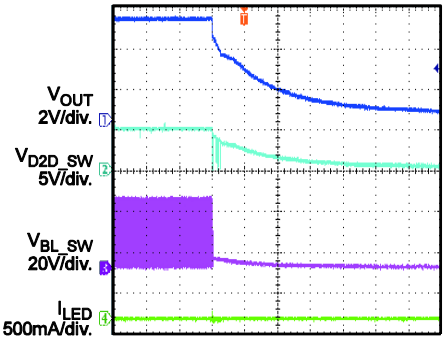
Power Off

I_{OUT}=2A



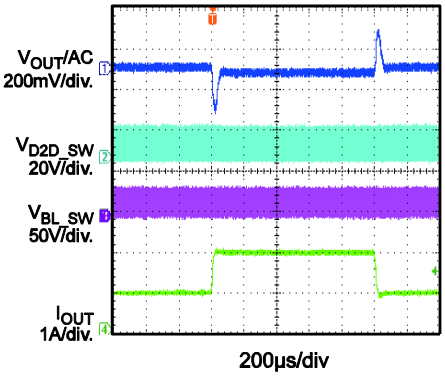
Power Off

I_{OUT}=0A



Transient Response

I_{OUT}=1A to 2A



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PIN FUNCTIONS

Pin #	Name	Description
1	GND1	**Ground for WLED controller**.
2	OSC	**Switching frequency set**. Connect a resistor between OSC and GND to set the step-up converter switching frequency. The voltage at OSC is regulated to 1.23 V. The clock frequency is proportional to the current sourced from OSC.
3	ISET	**LED current set.** Tie a current-setting resistor from ISET to ground to program the current in each LED string. ISET voltage is regulated to 1.225 V. The LED current is proportional to the current through the ISET resistor.
4	ADIM	**Input for analog brightness control.** The LED current amplitude is determined by ADMIN. The input signal can be either a PWM signal or a DC voltage signal. An internal RC filter (10 MΩ resistor and 100 pF capacitor) is integrated to ADMIN. If a PWM signal is applied to ADMIN, a >20 kHz frequency is recommended. This obtains a better PWM signal filtering performance and ensures the amplitude voltage is higher than 1.5 V and the low-level voltage is less than 0.4 V. For a DC signal input, please apply a DC input signal range from 0.41 V to 1.49 V to set linearly the LED current from minimum to full scale. If ADMIN is floated, pull internally to GND.
5	LED4	**LED string 4 current input**. LED4 is the open-drain output of an internal dimming control switch. Connect the LED string 4 cathode to LED4.
6	LED3	**LED string 3 current input.** LED3 is the open-drain output of an internal dimming control switch. Connect the LED string 3 cathode to LED3.
7	LED2	**LED string 2 current input.** LED2 is the open-drain output of an internal dimming control switch. Connect the LED string 2 cathode to LED2.
8	LED1	**LED string 1 current input**. LED1 is the open-drain output of an internal dimming control switch. Connect the LED string 1 cathode to LED1.
9	OVP	**Over-voltage protection input.** Connect a resistor divider from the output to OVP to program the OVP threshold.
10,11	NC	**No connection.**
12	FB	**Buck converter feedback**. An external resistor divider from the output to AGND (tapped to FB) sets the output voltage. To prevent current-limit runaway during a short-circuit fault condition, the frequency foldback comparator lowers the oscillator frequency when the FB voltage is below 400 mV.
13	AAM	**AAM mode setting for buck converter**. Connect a resistor from AAM to ground to set the AAM voltage and force the buck converter into non-synchronous mode when the load is small. Driving AAM high (=VCC2) forces the buck converter into CCM.

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PIN FUNCTIONS *(continued)*

Pin #	Name	Description
14	VCC2	**Bias supply for buck converter.** Decouple with a 0.1 µF-0.22 µF capacitor. The capacitance should be no more than 0.22 µF.
15	VIN2	**Supply voltage input for buck converter.** A ceramic capacitor is needed to decouple the input rail. Use a wide PCB trace to make the connection.
16	SW	**Switch output for buck converter.** Use a wide PCB trace to make the connection.
17,18	GND2	**Ground for buck converter**.
19	AGND	**Analog ground for buck converter.**
20	BST	**Bootstrap for buck converter**. A capacitor and a 47 Ω resistor connected between SW and BST are required to form a floating supply across the high-side switch driver.
21	SYNC	**Synchronization for buck converter.** Apply a clock signal with a frequency higher than 250 KHz; the frequency of the buck converter can be synchronized by the external clock. The internal clock's rising edge is synchronized to the external clock's falling edge.
22	ISENSE	**Current sense input for WLED controller.** During normal operation, ISENSE senses the voltage across the external inductor current-sensing resistor (R_{SENSE}) for peak-current–mode control. Also, it limits the inductor current during every switching cycle.
23	GATE	**Power switch gate output for WLED controller.** GATE drives the external power N-channel MOSFET.
24	VIN1	**Supply input for WLED controller.**
25	VCC1	**The internal 6 V linear regulator output for WLED controller**. VCC1 provides a power supply for the external MOSFET switch gate driver and the internal control circuitry. Bypass VCC1 to GND with a ceramic capacitor.
26	COMP	**Error amplifier output of WLED controller.** Connect a capacitor and resistor in series to stabilize the boost converter loop.
27	EN	**Enable input for WLED controller.**
28	PWM	**Input signal for PWM brightness control.** If PWM is floated, pull internally to GND.

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FUNCTIONAL BLOCK DIAGRAM

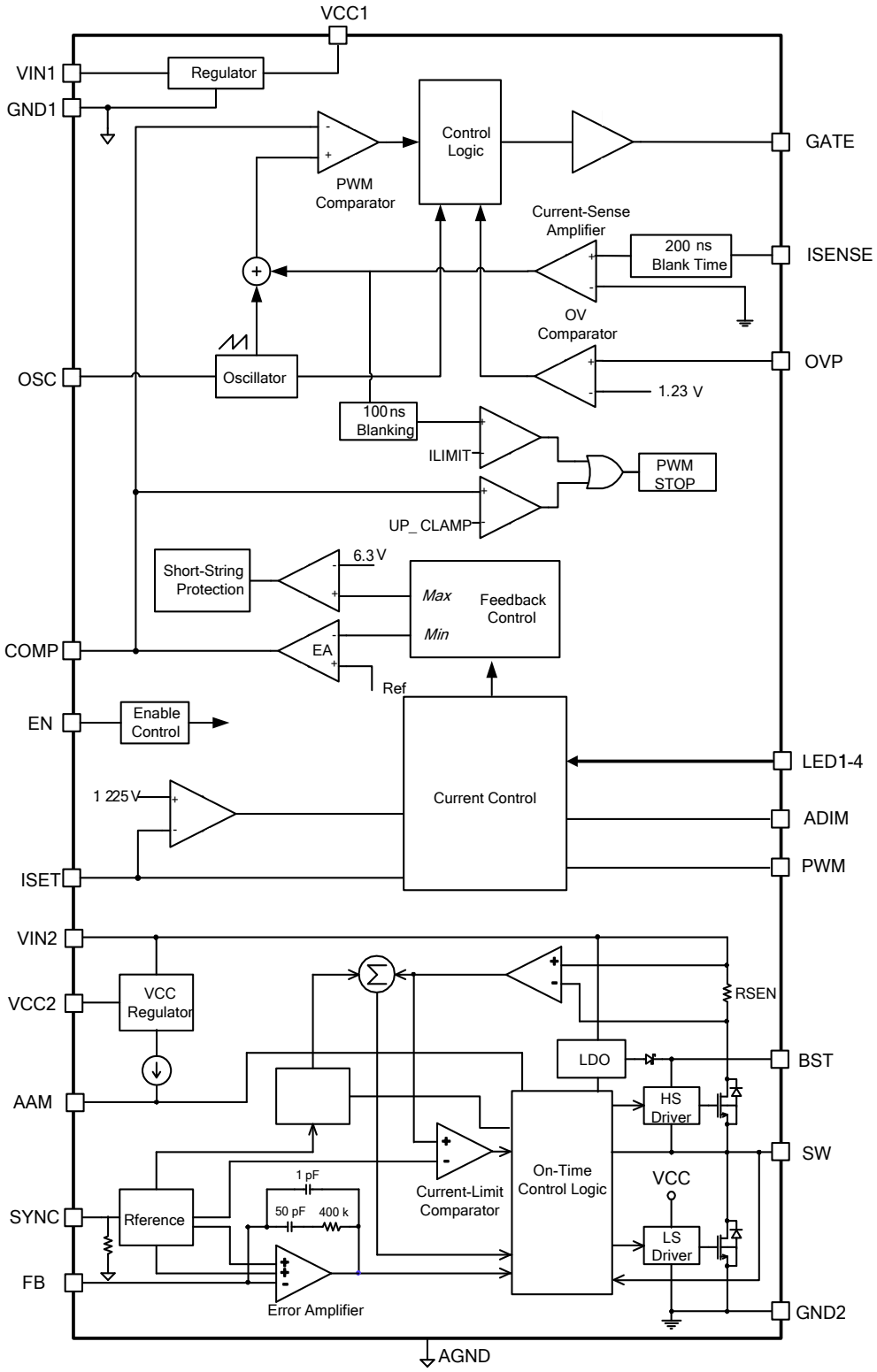


Figure 1—Functional block diagram

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OPERATION

WLED CONTROLLER SECTION:

The WLED controller employs a programmable constant frequency, peak-current–mode, step-up converter with 4 channel regulated current sources to drive an array of up to 4 strings of white LEDs.

Internal 6 V Regulator

When VIN1 is greater than 6.5 V, VCC1 outputs a 6 V power supply to the external MOSFET switch gate driver and the internal control circuitry. The VCC1 voltage drops to 0 V when the WLED controller shuts down.

System Start-Up

When enabled, the WLED controller checks the topology connection first. The WLED controller monitors the over-voltage protection (OVP) pin to see if the Schottky diode is connected or if the boost output is shorted to GND. An OVP voltage of less than 57 mV disables the WLED controller . Once all the protection tests pass, the WLED controller starts boosting the step-up converter with an internal soft-start.

It is recommended that the enable signal occurs after the establishment of the input voltage and PWM dimming signal during the start-up sequence to avoid large inrush current.

Step-Up Converter

The converter operating frequency is programmable by an external resistor on OSC. 300 kHz to 500 kHz is recommended as an operating frequency. This optimizes efficiency and the size of external components.

At the beginning of each switching cycle, the internal clock turns on the external MOSFET (In normal operation, the minimum turn-on time is 200 ns.) A stabilizing ramp added to the output of the current sense amplifier prevents sub-harmonic oscillations for duty cycles greater than 50 percent. This result is fed into the PWM comparator. When this voltage reaches the output voltage of the error amplifier (V_{COMP}) the external MOSFET turns off.

The output voltage of the internal error amplifier is an amplified signal of the difference between the reference voltage and the feedback voltage. The converter chooses automatically the lowest active LEDX voltage to provide a bus voltage high enough to power all the LED arrays.

If the feedback voltage drops below the reference, the output of the error amplifier increases. This results in more current flowing through the MOSFET, thus increasing the power delivered to the output. This forms a closed loop that regulates the output voltage.

Under light-load operation (especially in the case of $V_{OUT1} \approx V_{IN1}$), the converter runs in pulse-skipping mode where the MOSFET turns on for a minimum on-time of approximately 200 ns, and then the converter discharges the power to the output for the remaining period. The external MOSFET remains off until the output voltage needs to be boosted again.

Dimming Control

The MP3378 allows two dimming methods: PWM and analog dimming mode.

For PWM dimming, apply a PWM signal to PWM. The LED current is chopped by this PWM signal, and the average LED current is equal to I_{SET}*$D_{DIM;}$ where D_{DIM} is the duty cycle of PWM dimming signal, and I_{SET} is the LED current amplitude.

For analog dimming, either a PWM signal or DC signal can be applied to ADIM.

When a PWM signal is applied to ADIM, the signal is filtered by the internal RC filter. The LED current amplitude is equal to I_{SET} * $D_{DIM;}$ where D_{DIM} is the duty cycle of the PWM dimming signal, and I_{SET} is the LED current amplitude. A PWM signal of 20 kHz or higher is recommended to achieve better filtering performance. When a DC signal is applied to ADIM, the voltage range (0.41 V to 1.49 V) sets directly the LED current linearly from minimum to full scale.

Open-String Protection

Open-string protection is achieved through the OVP pin and LEDX pins (1 to 4). If one or more strings are open, the respective LEDX pins are pulled to ground, and the WLED controller keeps charging the output voltage until it reaches the over-voltage protection

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(OVP) threshold. If the OVP point has been triggered for >4 µs, the WLED controller stops switching and marks off the strings that have an LEDX voltage lower than 190 mV. Once marked off, the remaining LED strings force the output voltage back into tight regulation. The string with the largest voltage drop determines the output regulation. If all strings are open, the WLED controller shuts down until the WLED controller re-sets.

Short-String Protection

The WLED controller monitors the LEDX voltages to determine if a short-string fault has occurred. If one or more strings are shorted, the respective LEDX pins tolerate high-voltage stress. If an LEDX pin voltage is higher than 6.3 V, this condition triggers the detection of a short string. When a short-string fault (LEDX over-voltage fault) remains for 4096 switching clocks, the fault string is marked off and disabled. Once a string is marked off, it disconnects from the output voltage loop. The marked LED strings shut off completely until the boost part re-starts. In order to prevent mis-triggering short LED protection when opening an LED string or sharp ADIM, the short LED protection function is disabled when the Vledxs of all the used LED channels are higher than 1.5 V.

Inductor/Diode Short Protection

To prevent damage to the WLED controller and external MOSFET when the external inductor/diode is shorted, the protection mode operates in the following ways:

1. When the inductor/diode is shorted, the output cannot maintain enough energy to load the LED, causing the output voltage to drop. Thus, the COMP (the error amplifier output) voltage tends to rise until it is clamped high. If it lasts longer than 512 switching cycles, the WLED controller turns off and latches.
2. However, in some cases the COMP voltage cannot be clamped high when the inductor/diode is shorted, so the WLED controller provides the protection mode by detecting the current flowing through the power MOSFET. In this mode, when the current sense voltage across the sense resistor (connected between MOSFET and GND) hits V_{LMT} limit value and lasts for 4 switching cycles, the WLED controller turns off and latches.

Thermal Shutdown Protection

To prevent the WLED controller from operating at exceedingly high temperatures, thermal shutdown detects the die temperature. When the die temperature exceeds the upper threshold (150°C), the WLED controller shuts down. The controller resumes normal operation when the die temperature drops below the lower threshold. Typically, the hysteresis value is 25°C.

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Buck Converter Section:

The step-down, switch-mode converter has built in internal power MOSFETs and offers a very compact solution. It operates in a fixed frequency, peak-current-control mode to regulate the output voltage. A PWM cycle is initiated by the internal clock. The integrated high-side power MOSFET is turned on and remains on until its current reaches the value set by the COMP_BUCK voltage. (COMP_BUCK is one of the buck's internal control voltages; it is not the COMP pin.) When the power switch is off, it remains off until the next clock cycle starts. If the current in the power MOSFET does not reach the COMP_BUCK set current value within 95 percent of one PWM period, the power MOSFET is forced off.

Internal Regulator

Most of the internal circuitries are powered from the 5 V internal regulator. This regulator takes the VIN2 input and operates in the full VIN2 range. When VIN2 is greater than 5.0 V, the output of the regulator is in full regulation. When VIN2 is lower than 5.0 V, the output decreases; a 0.1 uF ceramic capacitor for decoupling is required.

Error Amplifier

The error amplifier compares the FB voltage with the internal 0.8 V reference (REF) and outputs a COMP_BUCK voltage, which is used to control the power MOSFET current. The optimized internal compensation network minimizes the external component count and simplifies the control loop design.

AAM Operation

MP3378 has advanced asynchronous modulation (AAM) power-save mode for light load. Connect a resistor from AAM to GND to set the AAM voltage. Under a heavy-load condition, the V_{COMP_BUCK} is higher than V_{AAM}. When the clock goes high, the high-side power MOSFET turns on and remains on until $V_{ILsense}$ reaches the value set by the COMP_BUCK voltage. The internal clock re-sets every time V_{COMP_BUCK} is higher than V_{AAM}.

Under a light-load condition, the value of V_{COMP_BUCK} is low. When V_{COMP_BUCK} is less than V_{AAM} and V_{FB} is less than V_{REF}, V_{COMP_BUCK} ramps up until it exceeds V_{AAM}. During this time, the internal clock is blocked. This causes the device to skip pulses for pulse frequency modulation (PFM) mode, achieving the light-load power save (see Figure 2).

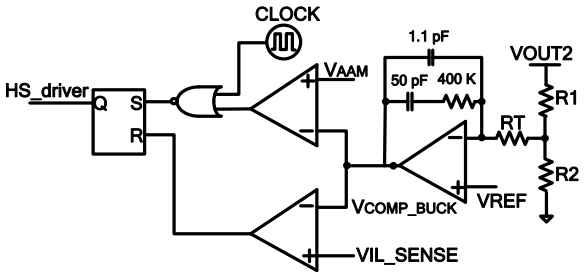


Figure 2—Simplified AAM control logic

SYNC Control

The buck converter can be synchronized through SYNC to an external clock range from 250 kHz to 2 MHz. The internal clock's rising edge is synchronized to the external clock's falling edge. The synchronized logic high voltage should be higher than 1.8 V. The synchronized logic low voltage should be lower than 0.6 V. The frequency of the external clock should be higher than the frequency of the internal clock. Otherwise the internal clock may pulse high and turn on the high-side MOSFET again.

Under-Voltage Lockout (UVLO)

Under-voltage lockout (UVLO) protects the buck converter from operating at an insufficient supply voltage by monitoring the output voltage of the internal regulator (VCC2). The UVLO rising threshold is about 3.9 V while its falling threshold is a consistent 3.25 V.

Internal Soft Start (SS)

Soft start is implemented to prevent the converter output voltage from overshooting during start up. When the chip starts up, the internal circuitry generates a soft-start voltage (SS) ramping up from 0 V. The soft-start period lasts until the voltage on the soft-start capacitor exceeds the reference voltage of 0.8 V. At this point, the reference voltage takes over. The soft-start time is set internally at around 1.5 ms.

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Over-Current Protection (OCP) and Hiccup

The cycle-by-cycle over-current limit is implemented when the inductor current peak value exceeds the set current-limit threshold. Meanwhile, the output voltage starts to drop until FB is below the under-voltage (UV) threshold (50 percent below the reference, typically). Once a UV is triggered, the buck converter enters hiccup mode to re-start the part periodically. This protection mode is useful when the output is dead shorted to ground. The average short-circuit current is reduced greatly to alleviate thermal issues and protect the regulator. The buck converter exits hiccup mode once the over-current condition is removed.

Thermal Shutdown

Thermal shutdown prevents the chip from operating at exceedingly high temperatures. When the die temperature is higher than 150°C, it shuts down the buck converter. When the temperature is lower than its lower threshold (130°C, typically) the buck converter is enabled again.

Floating Driver and Bootstrap Charging

The floating power MOSFET driver is powered by an external bootstrap capacitor. This floating driver has its own UVLO protection. The UVLO's rising threshold is 2.2 V with a hysteresis of 150 mV. The bootstrap capacitor voltage is regulated internally by VIN2 through DB, R6, C7, L2, and C5 (see Figure 3). If VIN2-VSW is more than 5 V, U1 regulates MB to maintain a 5 V BST voltage across C7.

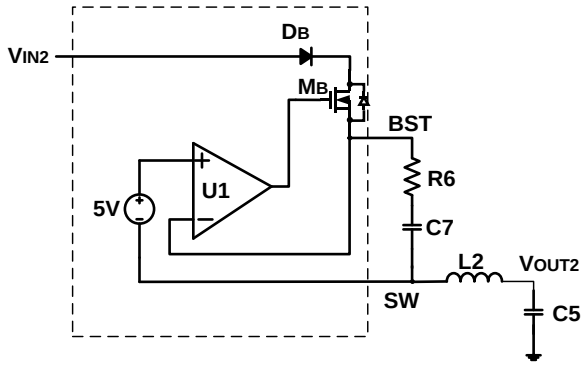


Figure 3—Internal bootstrap charging circuit start-up and shutdown

If VIN2 is higher than its appropriate thresholds, the buck converter starts up. The reference block starts first, generating stable reference voltage and currents and then the internal regulator is enabled. The regulator provides a stable supply for the remaining circuitries.

Two events can shut down the buck converter: VIN2 UVLO and thermal shutdown. During the shutdown procedure, the signaling path is blocked first to avoid any fault triggering. The COMP voltage and the internal supply rail are then pulled down. The floating driver is not subject to this shutdown command.

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APPLICATION INFORMATION

WLED CONTROLLER SECTION:

Selecting the Switching Frequency

The switching frequency of the step-up converter is recommended from 300 kHz to 500 kHz for most applications. An oscillator resistor on OSC sets the internal oscillator frequency for the step-up converter according to Equation (1):

$$F_{SW1}(KHz) = \frac{67320}{Rosc(K\Omega)} \quad (1)$$

For R_{OSC} = 224 kΩ, the switching frequency is set to 300 kHz.

Setting the LED Current

Each LED string current is set through the current-setting resistor on ISET. See Equation (2):

$$ILED(mA) = \frac{795 \times 1.23}{R_{SET}(K\Omega)} \quad (2)$$

For R_{SET} = 8.06 kΩ, the LED current is set to 120 mA. Please do NOT leave ISET open.

Selecting the Input Capacitor

The input capacitor reduces the surge current drawn from the input supply and the switching noise from the device. The input capacitor impedance at the switching frequency should be less than the input source impedance to prevent the high-frequency switching current from passing through to the input. Use ceramic capacitors with X5R or X7R dielectrics for their low ESR and small temperature coefficients. For most applications, use a 4.7 µF ceramic capacitor in parallel with a 220 µF electrolytic capacitor.

Selecting the Inductor and Current-Sensing Resistor

A larger value inductor results in less ripple current and lower peak inductor current, reducing stress on the N-channel MOSFET. However, the larger value inductor has a larger physical size, a higher series resistance, and a lower saturation current.

Choose an inductor that does not saturate under the worst-case load conditions. Select the minimum inductor value to ensure that the boost converter works in continuous conduction mode (CCM) with high efficiency and good EMI performance.

Calculate the required inductance value using Equation (3):

$$L1 \geq \frac{\eta \times V_{OUT1} \times D \times (1-D)^2}{2 \times f_{SW1} \times I_{LOAD1}}$$

$$D = 1 - \frac{V_{IN1}}{V_{OUT1}} \quad (3)$$

Where V_{IN1} and V_{OUT1} are the input and output voltages, f_{SW1} is the switching frequency, I_{LOAD1} is the LED load current, and η is the efficiency.

Usually the switching current is used for peak-current-mode control. In order to avoid hitting the current limit, the voltage across the sensing resistor (R_{SENSE}) must be less than 80% of the worst-case current-limit voltage (V_{SENSE}). See Equation (4):

$$R_{SENSE} = \frac{0.8 \times V_{SENSE}}{I_{L1(PEAK)}}$$

$$I_{L1(PEAK)} = \frac{V_{OUT1} \times I_{LOAD1}}{\eta V_{IN1}} + \frac{V_{IN1} \times (V_{OUT1} - V_{IN1})}{2 \times L1 \times F_{SW1} \times V_{OUT1}} \quad (4)$$

Where $I_{L1(PEAK)}$ is the peak value of the inductor current. V_{SENSE} is shown in Figure 4.

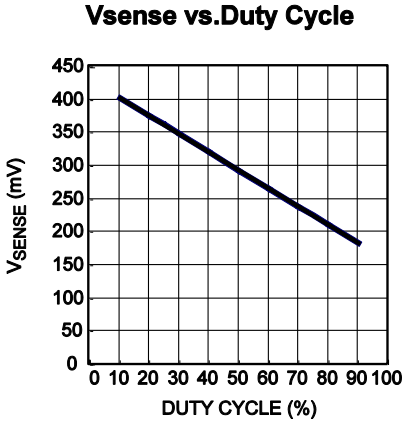


Figure 4—V_{SENSE} vs. duty cycle

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Selecting the Power MOSFET

The critical parameters for the selection of a MOSFET are as follows:

1. Maximum drain-to-source voltage, $V_{DS(MAX)}$
2. Maximum current, $I_{D(MAX)}$
3. On-resistance, $R_{DS(ON)}$
4. Gate-source charge (Q_{GS}) and gate-drain charge (Q_{GD})
5. Total gate charge, Q_G

Ideally, the off-state voltage across the MOSFET is equal to the output voltage. Considering the voltage spike when it turns off, $V_{DS(MAX)}$ should be greater than 1.5 times the output voltage.

The maximum current through the power MOSFET occurs at the minimum input voltage and the maximum output power. The maximum RMS current through the MOSFET is given by Equation (5):

$$I_{RMS(MAX)} = I_{IN1(MAX)} \times \sqrt{D_{MAX}}$$, where:

$$D_{MAX} \approx \frac{V_{OUT1} - V_{IN1(MIN)}}{V_{OUT1}} \quad (5)$$

The current rating of the MOSFET should be greater than 1.5 x I_{RMS}.

The on resistance of the MOSFET determines the conduction loss, which is given by Equation (6):

$$P_{cond} = I_{RMS}{}^2 \times R_{DS(on)} \times k \quad (6)$$

Where k is the temperature coefficient of the MOSFET.

The switching loss is related to Q_{GD} and Q_{GS1}, which determine the commutation time. Q_{GS1} is the charge between the threshold voltage and the plateau voltage when a driver charges the gate (see the chart of V_{GS} vs. Q_G of the MOSFET datasheet). Q_{GD} is the charge during the plateau voltage. These two parameters are needed to estimate turn-on and turn-off losses. See Equation (7):

$$P_{SW} = \frac{Q_{GS1} \times R_G}{V_{DR} - V_{TH}} \times V_{DS} \times I_{IN1} \times f_{SW1} + \frac{Q_{GD} \times R_G}{V_{DR} - V_{PLT}} \times V_{DS} \times I_{IN1} \times f_{SW1} \quad (7)$$

Where V_{TH} is the threshold voltage, V_{PLT} is the plateau voltage, R_G is the gate resistance, and V_{DS} is the drain-source voltage. Please note that calculating the switching loss is the most *difficult* part in the loss estimation. Equation (7) provides a simplified equation. For more accurate estimates, the equation becomes much more complex.The total gate charge (Q_G) is used to calculate the gate drive loss. See Equation (8)

$$P_{DR} = Q_G \times V_{DR} \times f_{SW1} \quad (8)$$

Where V_{DR} is the drive voltage.

Selecting the Output Capacitor

The output capacitor keeps the output voltage ripple small and ensures feedback loop stability. The output capacitor impedance must be low at the switching frequency. Ceramic capacitors with X7R dielectrics are recommended for their low ESR characteristics. For most applications, a 4.7 µF ceramic capacitor in parallel with a 22 µF electrolytic capacitor will suffice.

Setting the Over-Voltage Protection

Open-string protection detects the voltage on OVP. In some cases, an LED string failure results in the feedback voltage equaling zero. The part then keeps boosting the output voltage higher and higher. If the output voltage reaches the programmed OVP threshold, the protection is triggered.

To ensure the chip functions properly, select resistor values for the OVP resistor divider to provide an appropriate set voltage. The recommended OVP point is about 1.1 to 1.2 times higher than the output voltage for normal operation. See Equation (9):

$$V_{OVP} = 1.23 \times (1 + \frac{R_{HIGH}}{R_{LOW}}) \quad (9)$$

Selecting Dimming Control Mode

Two different dimming methods are provided:

1. Direct PWM Dimming

An external PWM dimming signal is employed to achieve PWM dimming control. Apply a PWM dimming signal (in the range of 100 Hz to 20 kHz) to PWM. The minimum recommended amplitude of the PWM signal is 1.5 V, and the low-level amplitude should be less than 0.4 V (see Table 1).

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Table 1—The range of PWM dimming duty

f_{PWM}(Hz)	D_{min}	D_{max}
100 < f ≤ 200	0.30%	100%
200 < f ≤ 500	0.75%	100%
500 < f ≤ 1 k	1.50%	100%
1 k < f ≤ 2 k	3.00%	100%
2 k < f ≤ 5 k	7.50%	100%
5 k < f ≤ 10 k	15.00%	100%
10 k < f ≤ 20 k	30.00%	100%

2. Analog Dimming

For analog dimming, apply a PWM signal or a DC voltage signal to ADIM. An internal RC filter (10 MΩ resistor and 100 pF capacitor) is integrated into ADMIN. If a PWM signal is applied to ADMIN, a >20 kHz frequency is recommended to achieve improved PWM signal filtering performance and ensure the amplitude voltage is higher than 1.5 V, and the low-level voltage is less than 0.4 V. For DC signal input, please apply a DC input signal range from 0.41 V to 1.49 V to set linearly the LED current from minimum to full scale.

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Buck Converter Section:

Setting the Output Voltage

The external resistor divider is used to set the output voltage. Also, the feedback resistor (R1) sets the feedback loop bandwidth with the internal compensation capacitor. When R1 is fixed, R2 is then given by Equation (10):

$$R2 = \frac{R1}{\frac{V_{OUT2}}{0.8V} - 1} \quad (10)$$

A T-type network is highly recommended (see Figure 5).

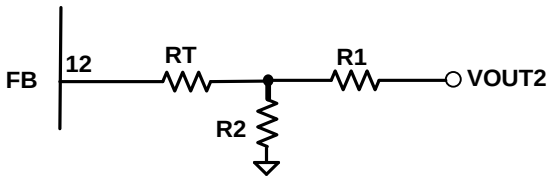


Figure 5—T-type network

Table 2 lists the recommended T-type resistor values for a common 5 V output voltage.

Table 2—Resistor selection for common 5 V output voltage

V_{OUT2} (V)	R1 (kΩ)	R2 (kΩ)	RT (kΩ)	L2 (µH)	Co (µF)
5	40.2	7.5	51	10	66

Selecting the Inductor

A 4.7 µH to 10 µH inductor with a DC current rating at least 25 percent higher than the maximum load current is recommended for most applications. For highest efficiency, the inductor DC resistance should be less than 15 mΩ. For most designs, the inductance value can be derived from Equation (11):

$$L2 = \frac{V_{OUT2} \times (V_{IN2} - V_{OUT2})}{V_{IN2} \times \Delta I_{L2} \times F_{OSC}} \quad (11)$$

Where ΔI_{L2} is the inductor ripple current.

Choose the inductor current to be approximately 30 percent of the maximum load current. The maximum inductor peak current is calculated using Equation (12):

$$I_{L2(MAX)} = I_{LOAD2} + \frac{\Delta I_{L2}}{2} \quad (12)$$

Under light-load conditions (below 100 mA), a larger inductance is recommended for improved efficiency.

Setting the AAM Voltage

The AAM voltage is used to set the transition point from AAM to CCM. It should be chosen to provide the best combination of efficiency, stability, ripple, and transient.

If the AAM voltage is set low, stability and ripple improves, but efficiency during AAM mode and transient degrades. Likewise, if the AAM voltage is set high, then the efficiency during AAM and transient improves, but stability and ripple degrade. Calculate the optimal balance point of AAM voltage for good efficiency, stability, ripple, and transient.

Adjust the AAM threshold by connecting a resistor from AAM to ground. An internal 6.2 µA current source charges the external resistor (see Figure 6).

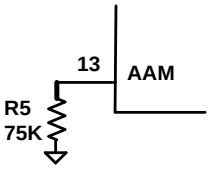


Figure 6—AAM network

Generally, R5 is then given by Equation (13):

$$V_{AAM} = R5 \times 6.2\mu A \quad (13)$$

To optimize AAM, see Figure 7.

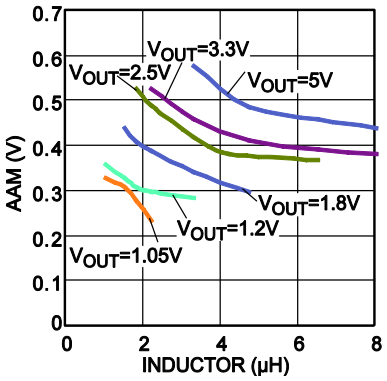


Figure 7—AAM selection for common output voltages (V_{IN2} = 4.5 V - 24 V)

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Selecting the Input Capacitor

The input current to the step-down converter is discontinuous, therefore a capacitor is required to supply the AC current to the step-down converter while maintaining the DC input voltage. Use low ESR capacitors for the best performance. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients. For most applications, a 22 µF capacitor is sufficient.

Since the input capacitor (C4) absorbs the input switching current, it requires an adequate ripple-current rating. The RMS current in the input capacitor can be estimated with Equation (14):

$$I_{C4} = I_{LOAD2} \times \sqrt{\frac{V_{OUT2}}{V_{IN2}} \times \left(1 - \frac{V_{OUT2}}{V_{IN2}}\right)} \quad (14)$$

The worse-case condition occurs at $V_{IN2} = 2V_{OUT2}$. See Equation (15):

$$I_{C4} = \frac{I_{LOAD2}}{2} \quad (15)$$

For simplification, choose an input capacitor with a RMS current rating greater than half of the maximum load current.

The input capacitor can be electrolytic, tantalum, or ceramic. When electrolytic or tantalum capacitors are used, a small high-quality ceramic capacitor (i.e. 0.1 µF) should be placed as close to the IC as possible. When using ceramic capacitors, make sure that they have enough capacitance to provide sufficient charge in order to prevent excessive voltage ripple at the input. The input voltage ripple caused by capacitance can be estimated with Equation (16):

$$\Delta V_{IN2} = \frac{I_{LOAD2}}{F_{SW2} \times C4} \times \frac{V_{OUT2}}{V_{IN2}} \times \left(1 - \frac{V_{OUT2}}{V_{IN2}}\right) \quad (16)$$

Selecting the Output Capacitor

The output capacitor (C5) is required to maintain the DC output voltage. Ceramic, tantalum, or low ESR electrolytic capacitors are recommended. Low ESR capacitors are preferred to keep the output voltage ripple low. The output voltage ripple can be estimated with Equation (17):

$$\Delta V_{OUT2} = \frac{V_{OUT2}}{F_{SW2} \times L2} \times \left(1 - \frac{V_{OUT2}}{V_{IN2}}\right) \times \left(R_{ESR} + \frac{1}{8 \times F_{SW2} \times C5}\right) \quad (17)$$

Where L2 is the inductor value and R_{ESR} is the equivalent series resistance (ESR) value of the output capacitor.

When using ceramic capacitors, the impedance at the switching frequency is dominated by the capacitance. The output voltage ripple is caused mainly by the capacitance. For simplification, the output voltage ripple can be estimated with Equation (18):

$$\Delta V_{OUT2} = \frac{V_{OUT2}}{8 \times F_{SW2}^{\ 2} \times L2 \times C5} \times \left(1 - \frac{V_{OUT2}}{V_{IN2}}\right) \quad (18)$$

When using tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be approximated with Equation (19):

$$\Delta V_{OUT2} = \frac{V_{OUT2}}{F_{SW2} \times L2} \times \left(1 - \frac{V_{OUT2}}{V_{IN2}}\right) \times R_{ESR} \quad (19)$$

The characteristics of the output capacitor affect the stability of the regulation system.

External Bootstrap Diode (BST)

An external bootstrap diode may enhance the efficiency of the regulator, the applicable conditions for an external BST diode are:

- V_{OUT2} is 5 V or 3.3 V, and
- the duty cycle is high: $D = \frac{V_{OUT2}}{V_{IN2}} > 65\%$

In these cases, an external BST diode is recommended from VCC2 to BST (see Figure 8). The recommended external BST diode is IN4148, and the BST capacitor is 0.1 µF –1µF.

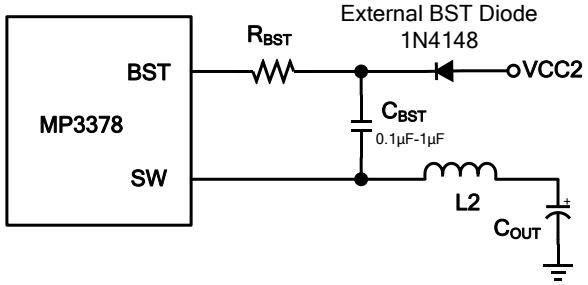


Figure 8—Add optional external bootstrap diode to enhance efficiency

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PCB Layout Guidelines

Efficient PCB layout is critical to reduce EMI noise. For best results, refer to Figure 9 (boost driver layout) and Figure 10 (buck converter layout) and follow the guidelines below:

Boost Driver Layout (see Figure 9)

1) Make the loop from the external MOSFET (M1), through the output diode (D1) and the output capacitors (C2, C3) as small and short as possible as they carry a high-frequency pulse current.
2) Separate the power ground and signal ground and then connect PGND and GND together as all logic signals refer to the signal ground. This reduces the noise affection.

Buck Converter Layout (see Figure 10)

1) Keep the connection of the input ground and GND2 (PGND) as short and wide as possible.
2) Keep the connection of the input capacitors (C16, C16A, and C17) and VIN2 as short and wide as possible.
3) Ensure all feedback connections are short and direct. Place the feedback resistors and compensation components as close to the chip as possible.
4) Route SW away from sensitive analog areas such as FB.
5) Connect a resistor (R23) to AGND as SYN is sensitive to noise. Otherwise SCP may fail, and the buck converter may be damaged.
6) Connect GND1 and GND2 together by a single point.

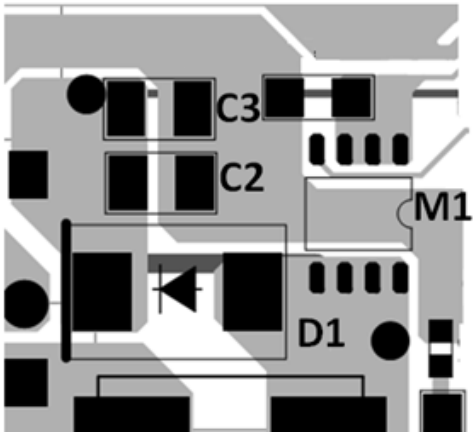


Figure 9—Recommended boost driver layout

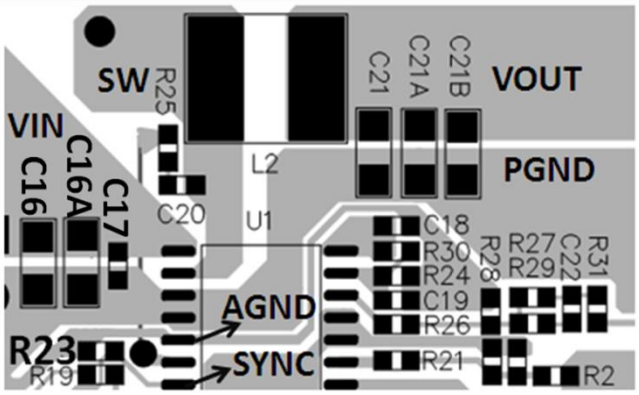


Figure 10—Recommneded buck converter layout

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TYPICAL APPLICATION CIRCUITS

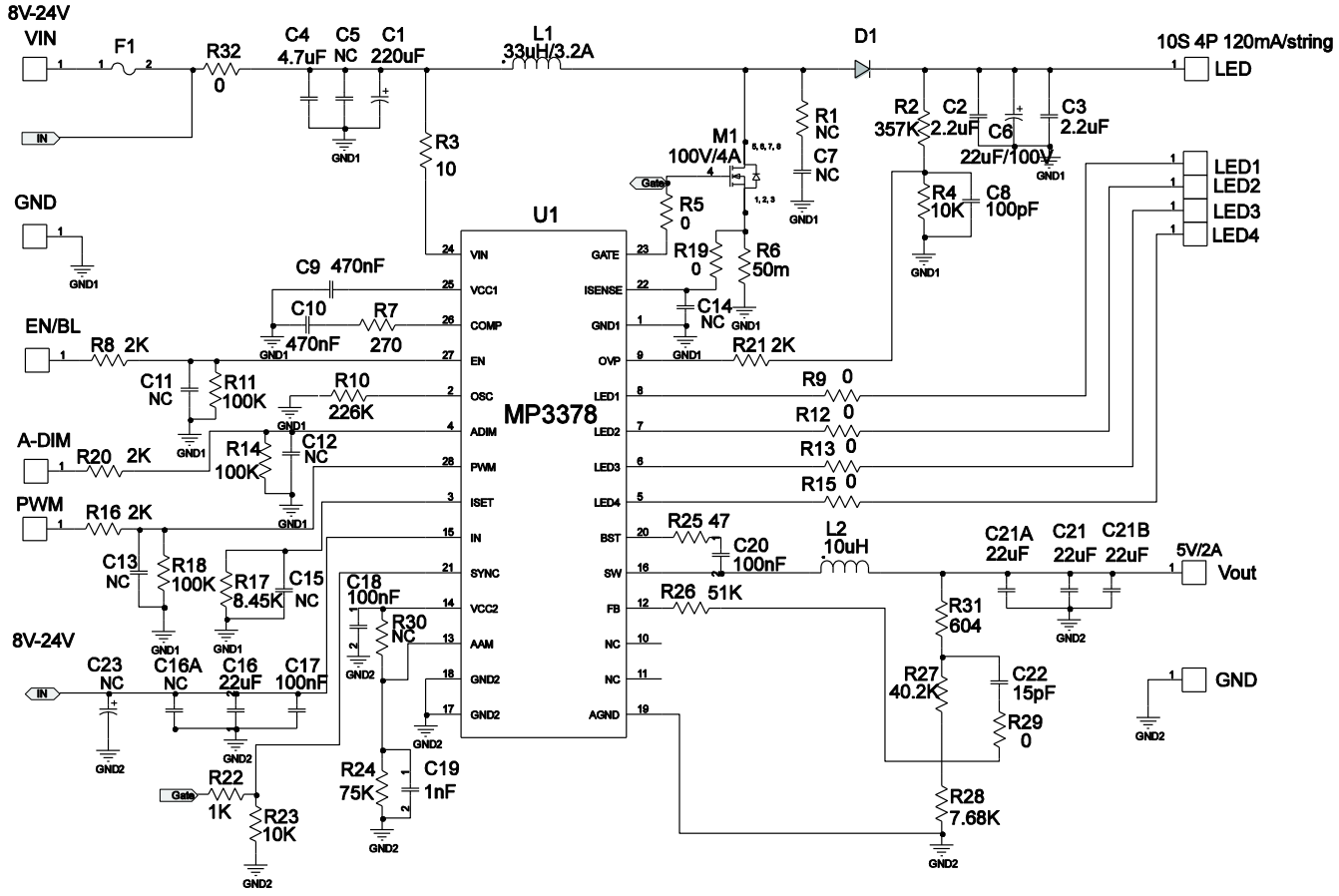
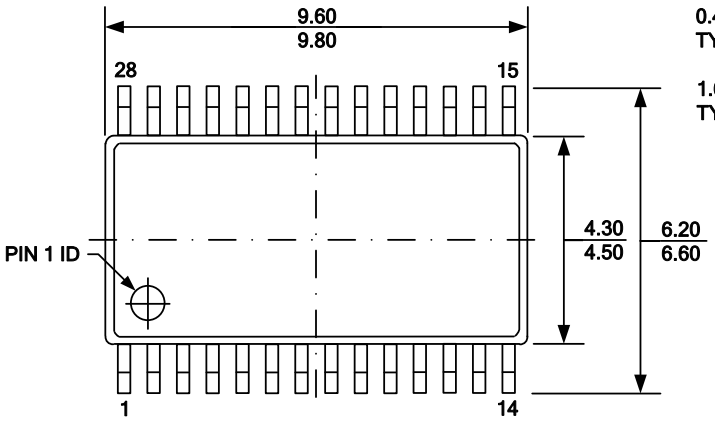


Figure 11—4 string, 10 LED in series, 120 mA/string plus 5 V output application

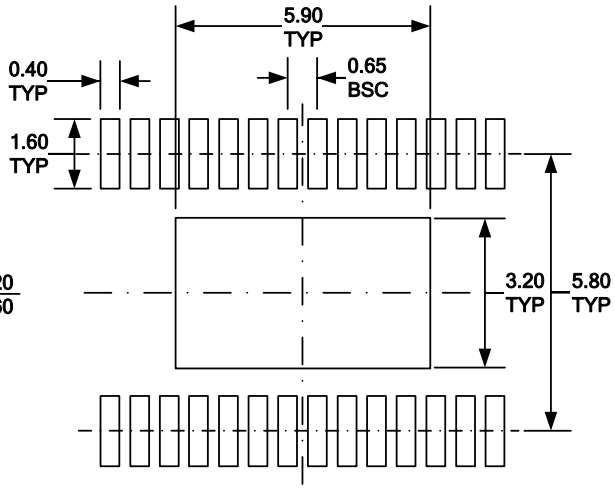
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PACKAGE INFORMATION

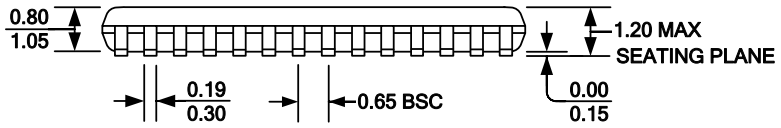
TSSOP-28 EP



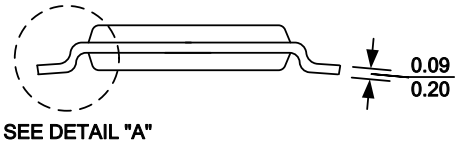
TOP VIEW



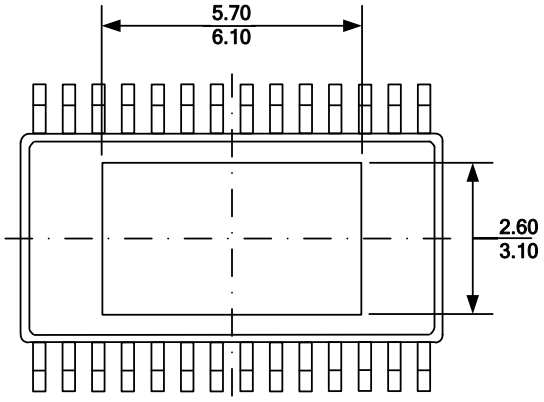
RECOMMENDED LAND PATTERN



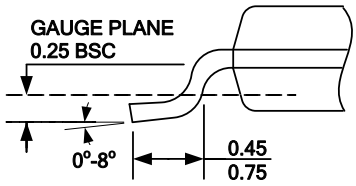
FRONT VIEW



SIDE VIEW



BOTTOM VIEW



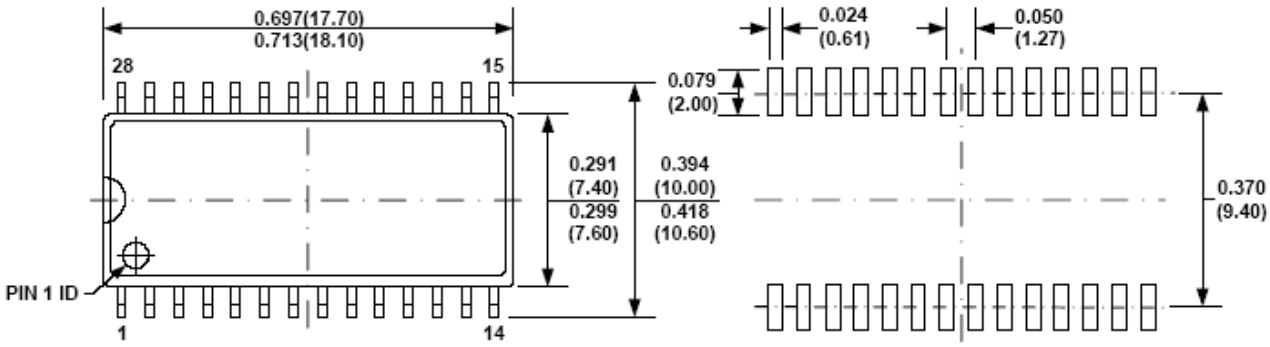
DETAIL "A"

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
5) DRAWING CONFORMS TO JEDEC MO-153, VARIATION AET.
6) DRAWING IS NOT TO SCALE.

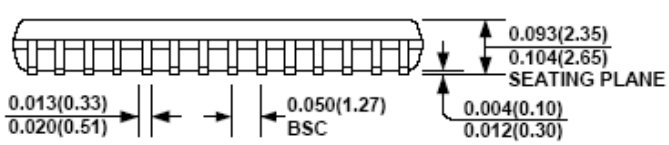
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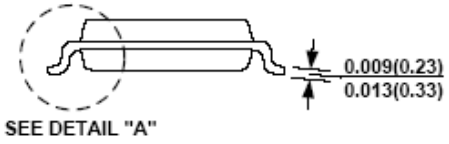


TOP VIEW

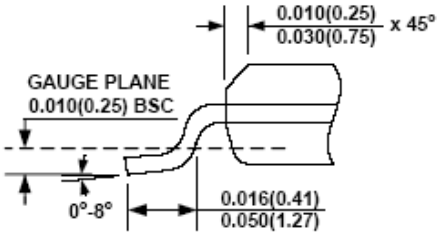
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW



DETAIL "A"

NOTE:

1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
5) DRAWING CONFORMS TO JEDEC MS-013, VARIATION AE.
6) DRAWING IS NOT TO SCALE.

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