The Future of Analog IC Technology

MP4031

TRIAC and Analog Dimmable, Primary-Side–Controlled Offline LED Controller with Active PFC

DESCRIPTION

The MP4031 is a TRIAC and analog dimmable, primary-side–controlled, offline LED lighting controller with active PFC. It can output an accurate LED current for an isolated lighting application with a single-stage converter. The proprietary real-current–control method can accurately control the LED current using primary-side information. It can significantly simplify LED lighting system design by eliminating secondary-side feedback components and the optocoupler.

The MP4031 implements power-factor correction and works in boundary-conduction mode to reduce MOSFET switching losses.

The MP4031 has an integrated charging circuit at the supply pin for fast start-up without a perceptible delay.

The proprietary dimming control expands the TRIAC-based dimming range.

The special current sense structure can implement analog dimming.

The MP4031 has multiple protections that greatly enhance system reliability and safety, including over-voltage protection, overload protection, supply-pin under-voltage lockout, and over-temperature protection.

All fault protections feature auto-restart.

The MP4031 is available in an 8-pin SOIC package.

FEATURES

- Primary-Side-Control without Secondary-Side Feedback
- Internal Charging Circuit at the Supply Pin for Fast Start-Up
- Accurate Line Regulation
- High Power Factor
- Operates in Boundary Conduction Mode
- Flicker-Free, Phase-Controlled TRIAC Dimming with Expanded Dimming Range.
- Analog-Dimming Compatible
- Cycle-by-Cycle Current Limit
- Over-Voltage Protection
- Over-Load Protection
- Over-Temperature Protection
- Available in an 8-Pin SOIC Package

APPLICATIONS

- Solid-State Lighting, including:
  - Industrial and Commercial Lighting
  - Residential Lighting

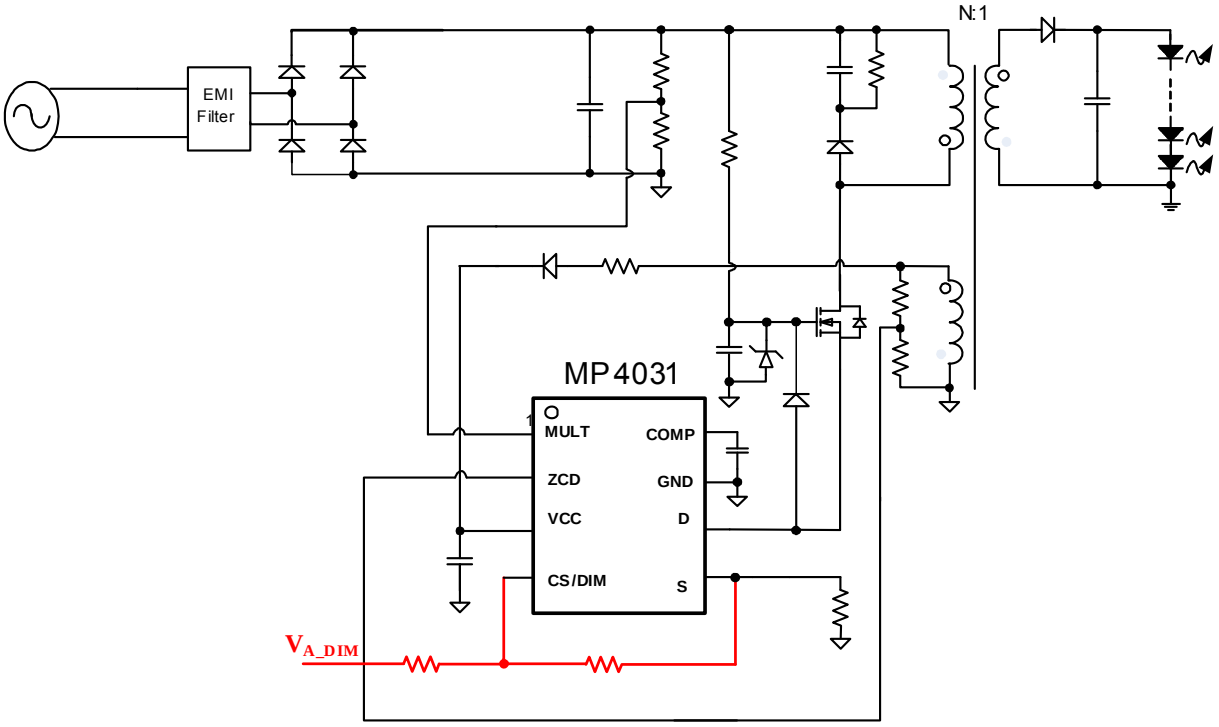
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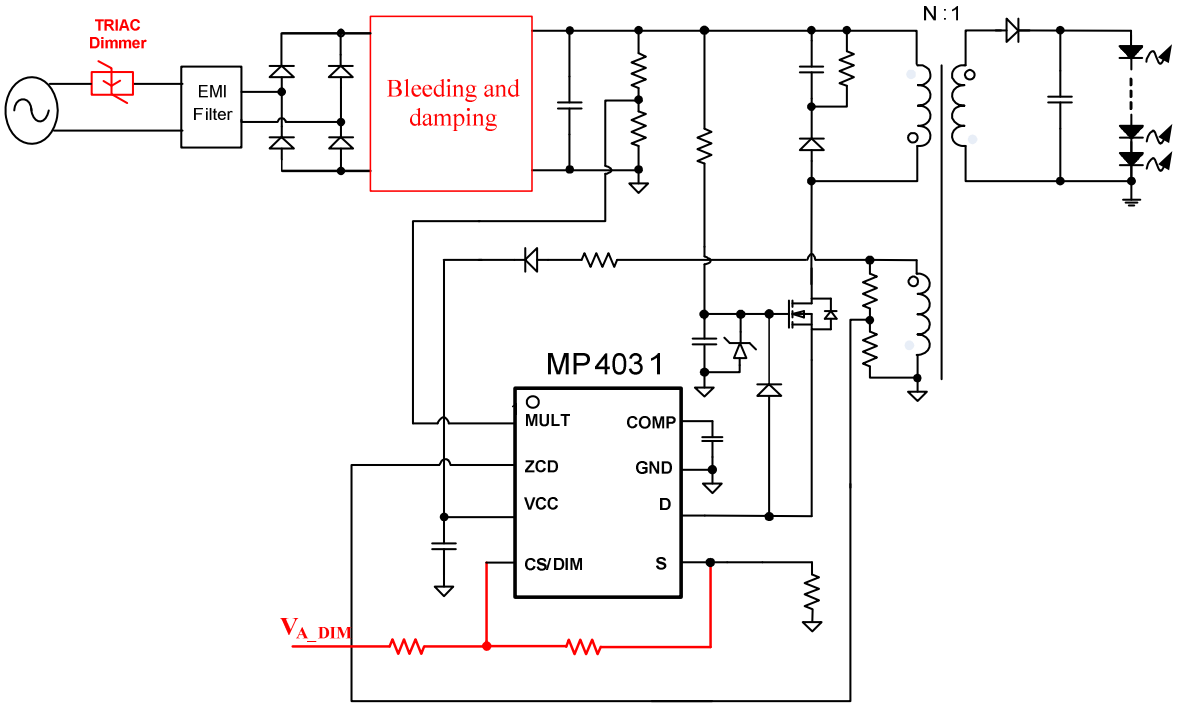
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TYPICAL APPLICATION

Analog Dimming Application



Analog with Triac Dimming Application



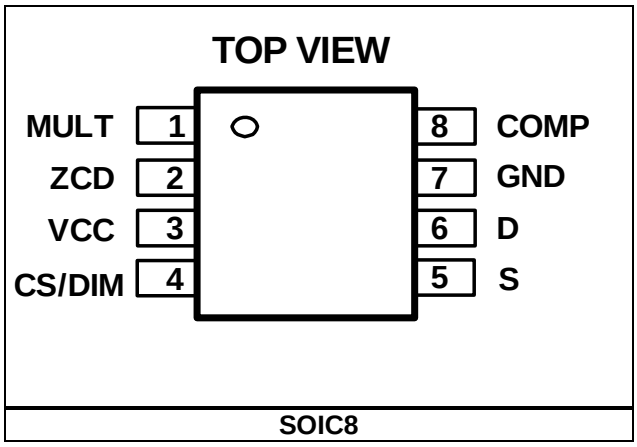
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ORDERING INFORMATION

Part Number*	Package	Top Marking
MP4031GS	SOIC8	MP4031

* For Tape & Reel, add suffix –Z (e.g. MP4031GS–Z);

PACKAGE REFERENCE



ABSOLUTE MAXIMUM RATINGS (1)

Input Voltage VCC ..... -0.3V to +30V
Low-Side MOSFET Drain Voltage -0.7V to +30V
ZCD Pin Voltage ..... -8V to +7V
Other Analog Inputs and Outputs..... -0.3V to 7V
ZCD Pin Current ..... -5mA to +5mA
Continuous Power Dissipation (T_A = +25°C) (2)
SOIC8..... 1.3W
Junction Temperature ..... 150°C
Lead Temperature ..... 260°C
Storage Temperature..... -65°C to +150°C

Recommended Operating Conditions (3)

Supply Voltage VCC ..... 11V to 27V
Operating Junction Temp (T_J). . -40°C to +125°C

Thermal Resistance (4) θ_{JA} θ_{JC}

SOIC8 ..... 96 ..... 45 ... °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J(MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D(MAX)=(T_J(MAX)-T_A)/ θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operation conditions.
4) Measured on JESD51-7 4-layer board.

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ELECTRICAL CHARACTERISTICS

T_A = +25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Supply Voltage						
Operating Range	V_{CC}	After turn on	10		27	V
VCC Upper Level: Internal Charging Circuit Stops and IC Turns On	V_{CCH}		9.5	10	10.5	V
VCC Lower Level: Internal Charging Circuit Trigger	V_{CCL}	Vcc falling, No fault	8.55	9	9.45	V
VCC Re-charge/IC Turn-Off Level in Fault Condition	V_{CCEN}	Vcc falling, Fault occurs	6.45	7	7.55	V
Supply Current						
VCC Charging Current from D	$I_{D\ charge}$	VD=16V, VCC=5V	12.5	15	17.5	mA
Quiescent Current	I_q	No switching, VCC=15V		800	1000	µA
Quiescent Current at Fault	I_{q_fault}	Fault condition, IC latch, VCC=15V	180	220	300	µA
Operating Current	I_{cc}	f_s =70kHz, VCC=15V		1	2	mA
Multiplier						
Linear Operation Range	V_{MULT}	V_{COMP} from 1.9V to 4.9V	0		3	V
Gain	$K^{(5)}$	V_{COMP}=2V, V_{MULT}=0.5V	0.84	1.06	1.26	1/V
		V_{COMP}=2V, V_{MULT}=1.5V	0.9	1.08	1.23	1/V
		V_{COMP}=2V, V_{MULT}=3V	0.93	1.1	1.25	1/V
TRIAC Dimming Off Detection Threshold	V_{MUL_off}		0.13	0.15	0.17	V
TRIAC Dimming On Detection Threshold	V_{MUL_on}		0.32	0.35	0.38	V
TRIAC Dimming Off Line-Cycle Blanking Ratio	D_{off_LEB}			25%		
Error Amplifier						
Reference Voltage	V_{REF}		0.386	0.4	0.414	V
Transconductance	G_{EA}	Guaranteed by design		250		µA/V
COMP Lower Clamp Voltage	V_{COMPL}		1.85	1.9	1.95	V
Max. Source Current	I_{COMP+}			57		µA
Max. Sink Current without Dimmer	I_{COMP-}			-300		µA
Sink Current at TRIAC Dimming Off	I_{sink_dim}		60	70	80	µA
Over-Load Detect Threshold	V_{COMP_OLP}		4.85	5	5.15	V

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ELECTRICAL CHARACTERISTICS *(continued)*

T_A = +25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Current Sense Comparator						
Leading-Edge Blanking Time	τ_{LEB}		360	450	540	ns
Current Sense Upper Clamp Voltage	$V_{S\ clamp\ H}$		2.2	2.3	2.4	V
Current Sense Lower Clamp Voltage	$V_{S\ clamp\ L}$		0.12	0.15	0.18	V
Zero-Current Detector						
Zero-Current–Detect Threshold	$V_{ZCD\ T}$	Falling Edge	0.32	0.35	0.37	V
Zero-Current–Detect Hysteresis	$V_{ZCD\ Hy}$		520	550	580	mV
Zero-Current–Detect LEB	$V_{ZCD\ LEB}$	Starts at Gate Turn Off	1.8	2.5	3.1	µs
Over-Voltage Threshold	$V_{ZCD\ OVP}$		5.2	5.5	5.8	V
OVP Detect LEB	$\tau_{OVP\ LEB}$	Starts at Gate Turn Off	1.5	2	2.5	µs
Minimum Off Time	$\tau_{off\ min}$		4.2	5.6	7	µs
Starter						
Start-Timer Period	τ_{start}		90	115	140	µs
Internal Main MOSFET						
Breakdown Voltage	$BV_{DSS\ main}$	$V_{GS=0}$	30			V
Drain-Source On-Resistor	$R_{DS(on)_main}$	I_D=100mA	200	250	300	mΩ

Notes:

5) The multiplier output is given by: $Vs=K \cdot V_{MULT} \cdot (V_{COMP}-1.5)$

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PIN FUNCTIONS

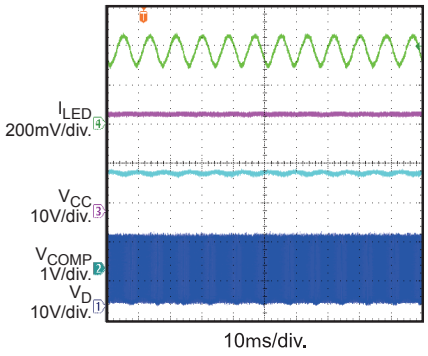
Pin #	Name	Pin Function
1	MULT	Internal Multiplier Input. Connect to the tap of resistor divider from the rectified voltage of the AC line. The half-wave sinusoid signal to this pin provides a reference signal for the internal current control loop. The MULT pin also detects the TRIAC dimming phase.
2	ZCD	Zero-Current Detection. A negative going edge triggers the internal MOSFET's turn-on signal. Connect to the tap of a resistor divider from the auxiliary winding to GND. ZCD can also detect over-voltage and over-current conditions. Over-voltage occurs if V_{ZCD} exceeds the over-voltage-protection (OVP) threshold after a 2μs blanking time when the internal MOSFET turns off.
3	VCC	Supply Voltage. Supplies power for both the control signal and the internal MOSFET's gate driver. Connect to an external bulk capacitor—typically 22μF with a 100pF ceramic capacitor to reduce noise.
4	CS/DIM	Current Sense and Analog dimming. An internal comparator compares the Current Sense voltage to the internal sinusoidal current reference to determine when the MOSFET turns off. If the voltage exceeds the current-limit threshold of 2.3V after the leading edge blanking time and during the turn-on interval, the gate signal turns off. In Triac dimming, this pin is connected directly to S Pin for current sense, and in Analog dimming, the Analog dimming signal is added through this pin as the typical application shows.
5	S	Internal Low-Side Main MOSFET Source. Connect a resistor from this pin to GND to sense the internal MOSFET current.
6	D	Internal Low-Side Main MOSFET Drain. This pin internally connects to VCC via a diode and a JFET to form an internal charging circuit for VCC. Connect to the source of the high-side MOSFET.
7	GND	Ground. Current return of the control signal and the gate drive signal.
8	COMP	Loop Compensation. Connects to a compensation network to stabilize the LED driver and accurately control the LED driver current. The COMP pin can also monitor for overload conditions: if the COMP voltage rises above 5V, the overload protection triggers.

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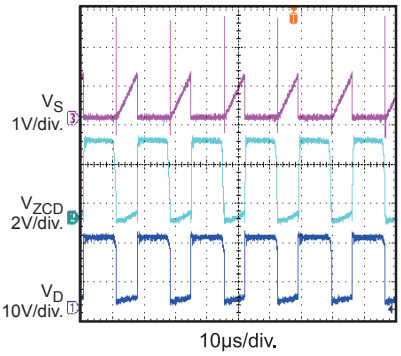
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} =120VAC, 7 LEDs in series, I_O=350mA, V_O=22V, Lm=1.6mH, N_P:N_S:N_{AUX} =82:16:19, TRIAC dimmable.

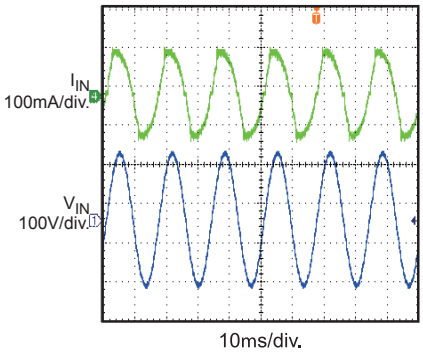
Steady State



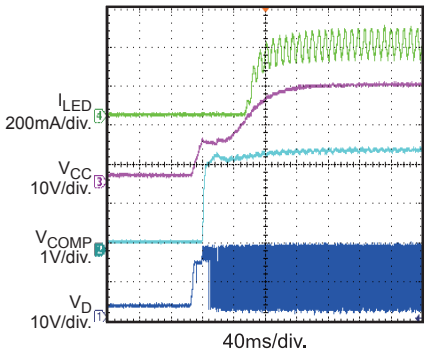
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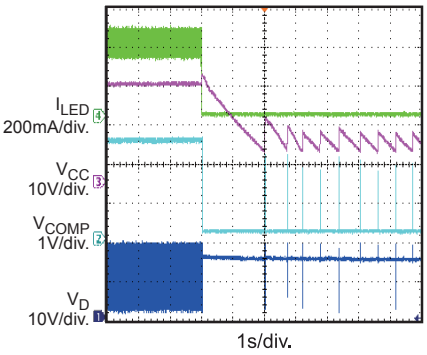
Steady State



V_{IN} Start Up

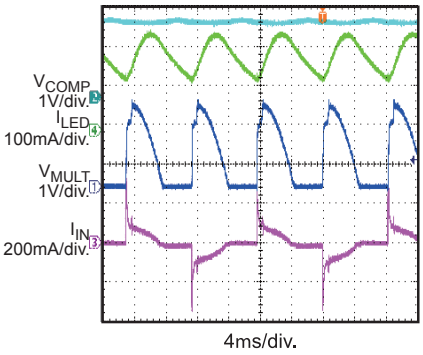


OVP, LED Load Open when working



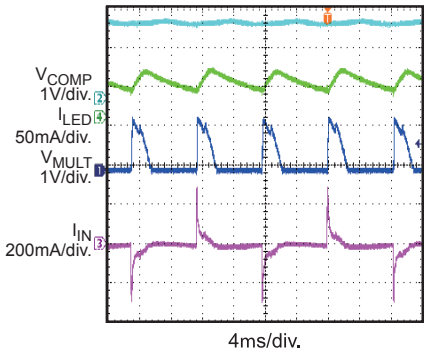
Triac Dimming

D = 60%



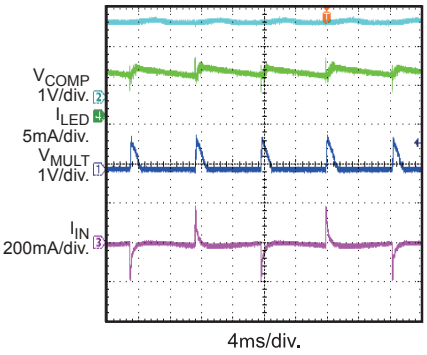
Triac Dimming

D = 40%



Triac Dimming

D = 20%

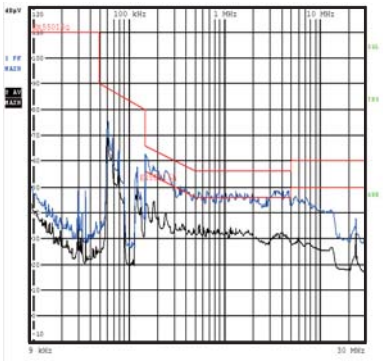


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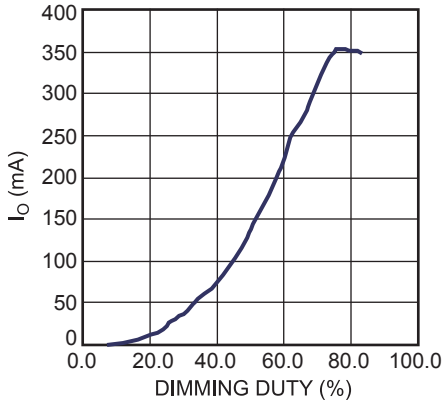
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Conducted EMI



Triac Dimming Curve



Performance Data

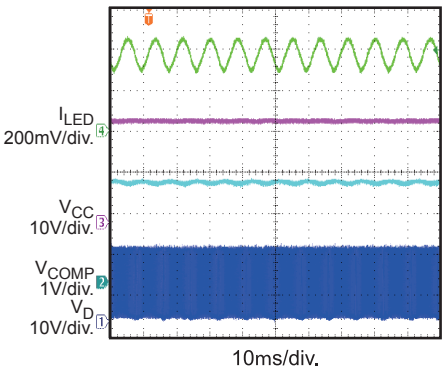
Vin (VAC)	108V	120V	132V
Pin (W)	9.58W	9.54W	9.47W
PF	0.993	0.99	0.982
THD	7.00%	9.50%	11.60%
Io (A)	0.36A	0.364A	0.364A
Vo (V)	21.62V	21.65V	21.64V
Efficiency	81.20%	82.60%	83.10%

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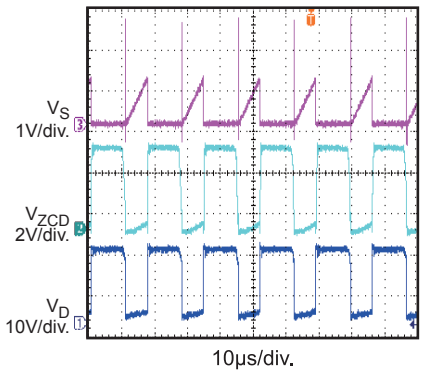
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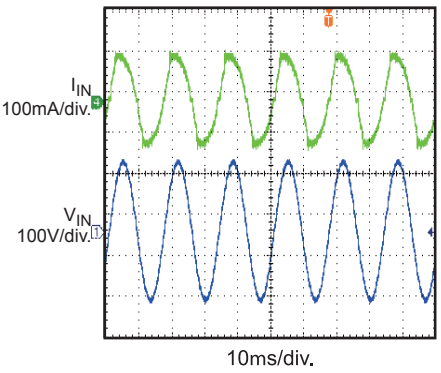
Steady State



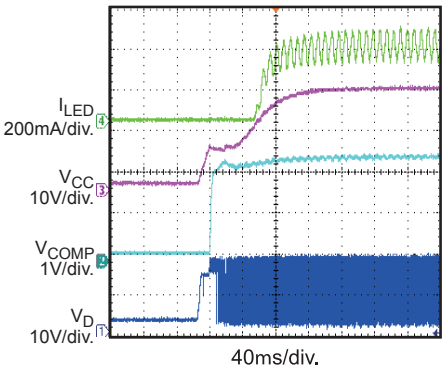
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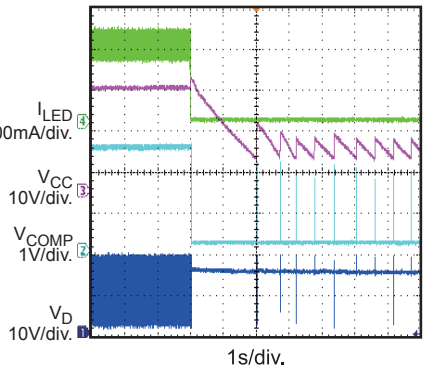
Steady State



V_{IN} Start Up

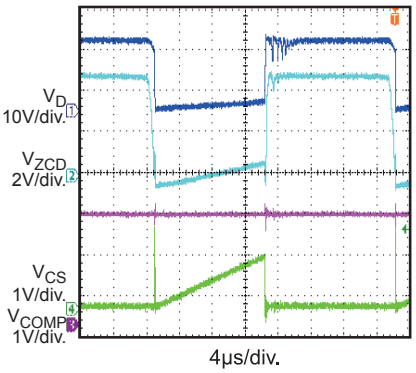


OVP, LED Load Open when working



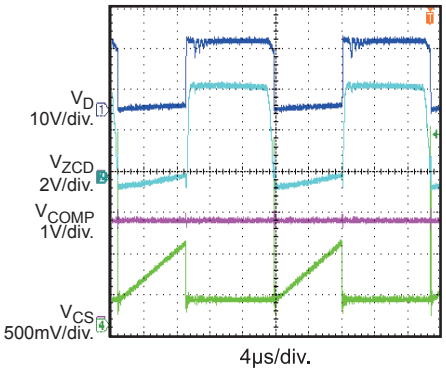
Analog Dimming

V_{A_DIM} = 0V



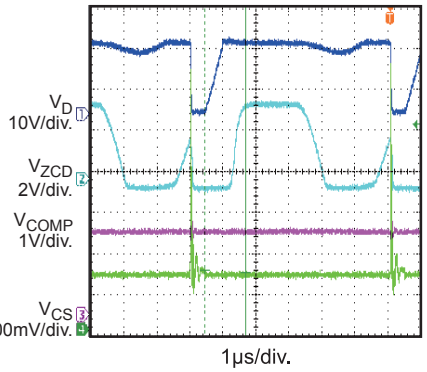
Analog Dimming

V_{A_DIM} = 4.7V



Analog Dimming

V_{A_DIM} = 10V

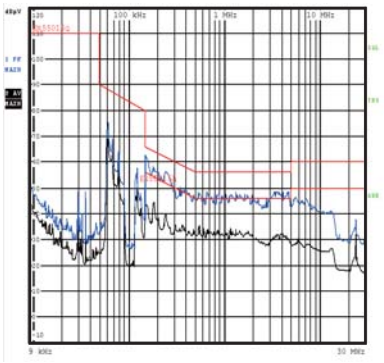


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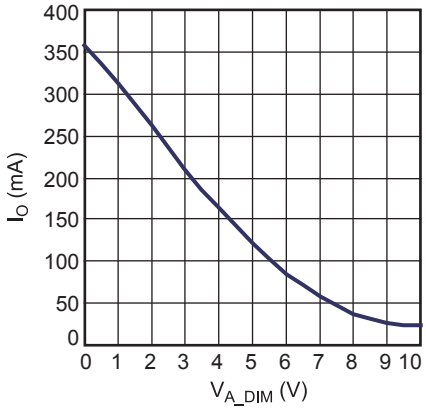
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Conducted EMI



Analog Dimming Curve



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FUNCTIONAL BLOCK DIAGRAM

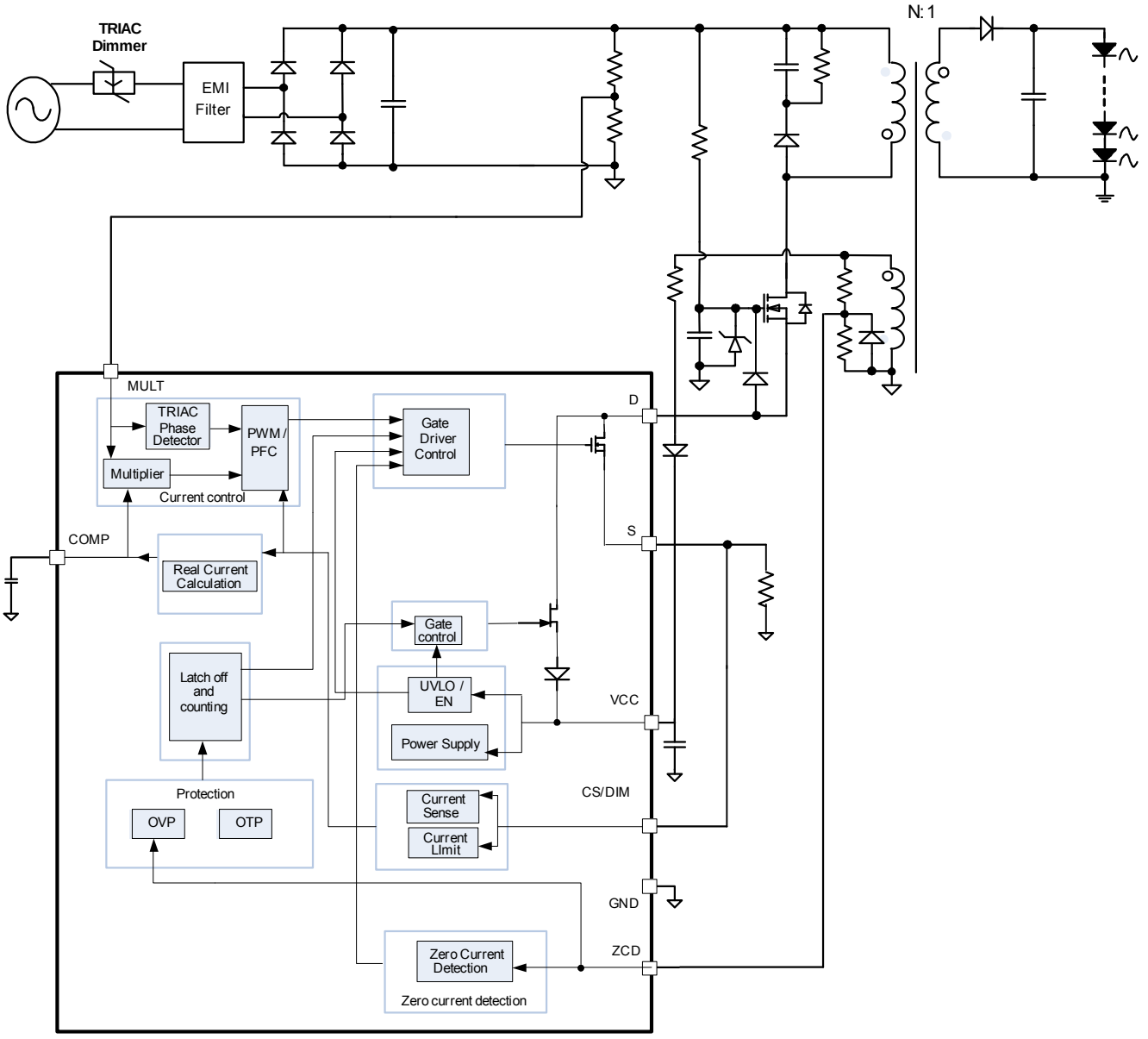


Figure 1: Functional Block Diagram

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OPERATION

The MP4031 is a TRIAC and analog dimmable, primary-side–controlled, offline LED controller designed for high-performance LED lighting. The MP4031 can accurately control the LED current using the real-current–control method based on primary-side information. It can also achieve a high power factor to eliminate noise pollution on the AC line. The integrated VCC charging circuit can achieve fast start-up without any perceptible delay. The MP4031 is suitable for TRIAC-based dimming with an extended dimming range. And the special current sense structure can implement analog dimming.

Boundary-Conduction Mode

During the external MOSFET ON time (τ_{ON}), the rectified input voltage applied across the primary-side inductor (L_m) increases the primary current increases linearly from zero to the peak value (I_{pk}). When the external MOSFET turns off, the energy stored in the inductor forces the secondary-side diode to turn on, and the inductor current decreases linearly from the peak value to zero. When the current decreases to zero, the parasitic resonance caused by the inductor and the combined parasitic capacitances decreases the MOSFET drain-source voltage that is also reflected on the auxiliary winding (see Figure 2). The zero-current detector generates the external MOSFET turn-on signal when the ZCD voltage falls below 0.35V after a blanking time and ensures the MOSFET turns on at a relatively low voltage (see Figure 3).

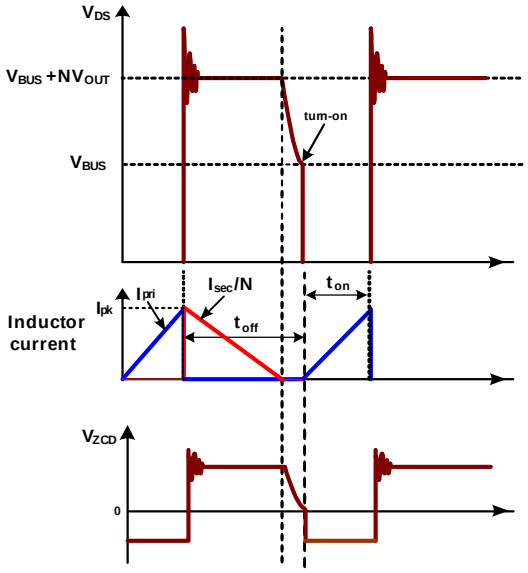


Figure 2: Boundary-Conduction Mode

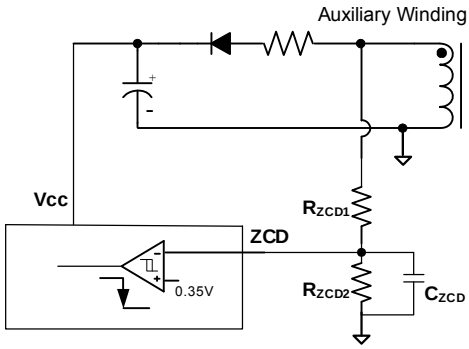


Figure 3: Zero-Current Detector

As a result, there are virtually no primary-switch turn-on losses and no secondary-diode reverse-recovery losses. This ensures high efficiency and low EMI noise.

Real-Current Control

The proprietary real-current–control method allows the MP4031 to control the secondary-side LED current based on primary-side information. The output LED mean current can be calculated approximately as:

$$I_o \approx \frac{N \cdot V_{FB}}{2 \cdot R_s}$$

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Where:

- N is the turn ratio of the primary side to the secondary side,
- V_{FB} is the feedback reference voltage (typically 0.4), and
- R_s is the sense resistor between the MOSFET source and GND.

Power-Factor Correction

The MULT pin connects to the tap of a resistor divider from the rectified instantaneous line voltage. The multiplier output also has a sinusoidal shape. This signal provides the reference for the current comparator against the primary-side–inductor current, which shapes the primary-peak current into a sinusoid with the same phase as the input line voltage. This achieves a high power factor.

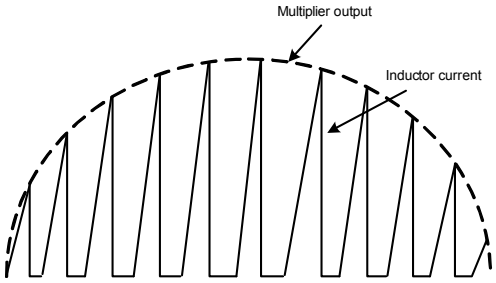


Figure 4: Power-Factor Correction

The multiplier's maximum output voltage to the current comparator is clamped to 2.3V to limit the cycle-by-cycle current. The multiplier's minimum output voltage is clamped to 0.1 to ensure a turn-on signal during the TRIAC dimming OFF interval, which pulls down the rectifier input voltage and accurately detects the dimming phase.

VCC Timing Sequence

Initially, VCC charges through the internal charging circuit from the AC line. When VCC reaches 10V, the internal charging circuit stops charging, the control logic initializes and the internal main MOSFET begins to switch. Then the auxiliary winding takes over the power supply. However, the initial auxiliary-winding positive voltage may not be large enough to charge VCC, causing VCC to drop. Instead, if the VCC voltage drops below the 9V threshold, the internal charging circuit triggers and charges VCC to 10V again. This cycle repeats until the auxiliary winding voltage is high enough to power VCC.

If any fault occurs during this time, the switching and the internal charging circuit will stop and latch, and VCC drops. When VCC decreases to 7V, the internal charging circuit re-charges for auto-restart.

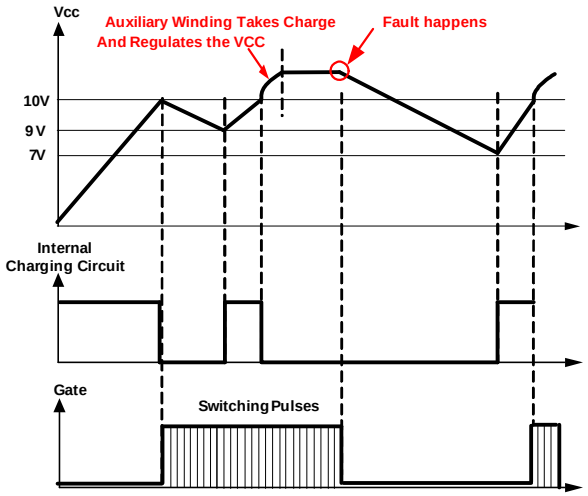


Figure 5: VCC Timing Sequence

Auto Start

The MP4031 includes an auto starter that starts timing when the MOSFET turns off. If ZCD fails to send a turn-on signal after 122μs, the starter will automatically sends a turn-on signal to avoid unnecessary IC shutdowns if ZCD fails.

Minimum OFF Time

The MP4031 operates with a variable switching frequency; the frequency changes with the instantaneous input-line voltage. To limit the maximum frequency and get good EMI performance, the MP4031 employs an internal minimum OFF-time limiter of 5μs, as shown in Figure 6.

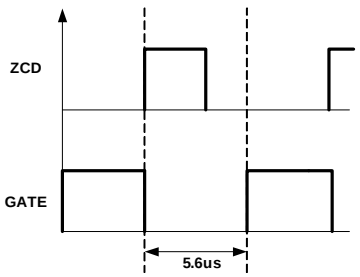


Figure 6: Minimum OFF time

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Leading-Edge Blanking

In order to avoid premature switching-pulse termination due to the parasitic capacitances discharging when the MOSFET turns on, an internal leading-edge blanking (LEB) unit between the S pin and the current-comparator input blocks the path from the S pin to the current comparator input during the blanking time. Figure 7 shows the leading-edge blanking.

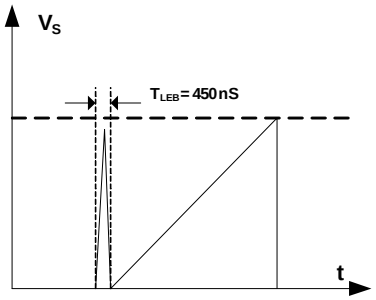


Figure 7: Leading-Edge Blanking

Output Over-Voltage Protection (OVP)

Output over-voltage protection (OVP) prevents component damage from over-voltage conditions. The auxiliary winding voltage's positive plateau is proportional to the output voltage, and the OVP monitors this auxiliary winding voltage instead of directly monitoring the output voltage as shown in Figure 8. Once the ZCD pin voltage exceeds 5.5V, the OVP signal triggers and latches, the gate driver turns off, and the IC functions in quiescent mode. When the VCC voltage drops below the UVLO threshold, the IC shuts down and the system restarts. The output OVP set point can be calculated as:

$$V_{out_ovp} \cdot \frac{N_{aux}}{N_{sec}} \cdot \frac{R_{ZCD2}}{R_{ZCD1} + R_{ZCD2}} = 5.5$$

Where:

$V_{out\text{-}ovp}$ is the output OVP threshold,

N_{aux} is the number of auxiliary winding turns, and

N_{sec} is the number of secondary winding turns

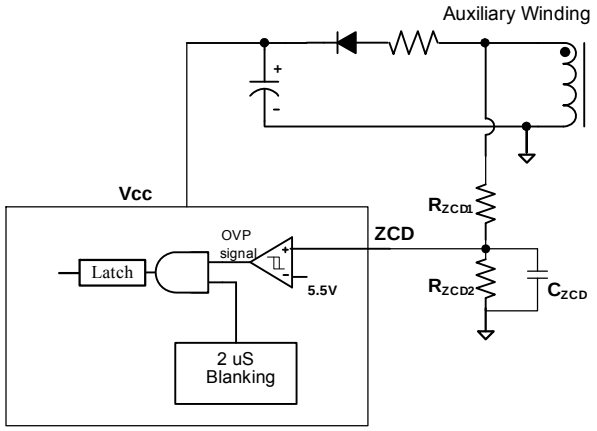


Figure 8: OVP Sampling Circuit

To avoid switch-on spikes mis-triggering OVP, OVP sampling has a τ_{OVPS} blanking period of around 2μs, as shown in Figure 9.

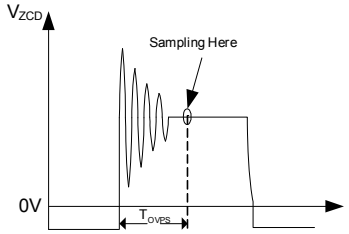


Figure 9: ZCD Voltage and OVP Sampling

Overload Protection (OLP)

In the event of an output overload, the COMP voltage rises. When the voltage reaches 5V, the IC will shut down and restart until VCC drops below UVLO.

Thermal Shutdown

To prevent internal temperatures from exceeding 150°C and causing lethal thermal damage, the MP4031 shuts down the switching cycle and latched until VCC dropping below UVLO and restarts again.

TRIAC-Based Dimming Control

The MP4031 can be used in TRIAC-based dimming application with the CS pin connected directly to the S pin. The TRIAC dimmer usually consists of a bi-directional SCR with an adjustable turn-on phase. Figure 10 shows the leading-edge TRIAC dimmer waveforms.

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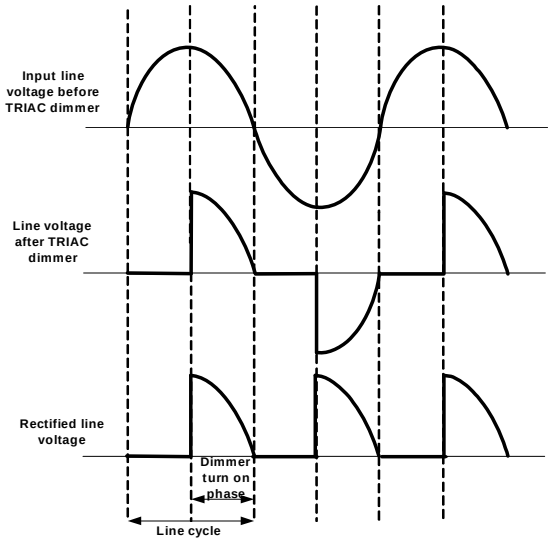


Figure 10: TRIAC Dimmer Waveforms

The MP4031 detects the dimming turn-on cycle through the MULT pin, which is fed into the control loop to adjust the internal reference voltage. When the MULT voltage exceeds 0.35V, the device treats this signal as a dimmer turn-on signal. When the MULT voltage falls below 0.15V, the system treats this as a dimmer turn-off signal. The MP4031 has a 25% line-cycle–detection blanking time with each line cycle, The real phase detector output adds this time, as shown in Figure 11. That means if the turn-on cycle exceeds 75% of the line cycle, the output remains at the same maximum current. It improves the line regulation during the maximum TRIAC turn-on cycle or without a dimmer.

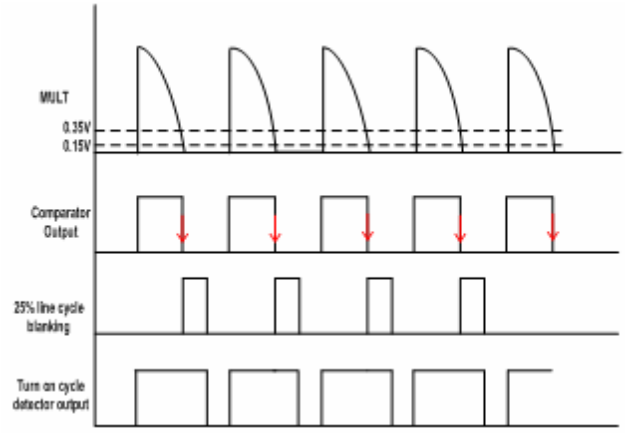


Figure 11: Dimming Turn-On Cycle Detector

If the turn-on cycle decreases to less than 75% of the line cycle, the internal reference voltage decreases as the dimming turn-on phase decreasing, and the output current decreases accordingly to implement dimming. As the dimming turn-on cycle decreases, the COMP voltage also decreases. Once the COMP voltage reaches to 1.9V, it is clamped so that the output current decreases slowly to maintain the TRIAC holding current and avoid random flicker. Figure 12 shows the relationship between the dimming turn-on phase and output current.

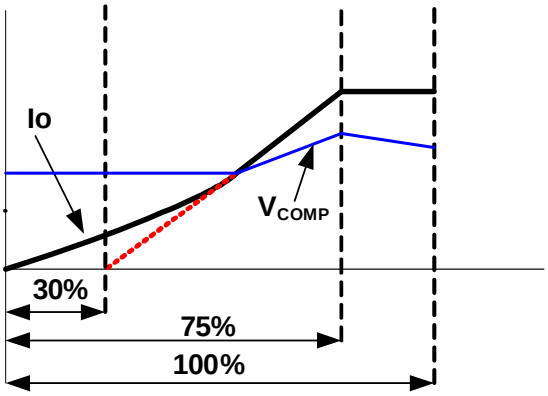


Figure 12: Dimming Curve

Analog Dimming

The MP4031 is also available for analog dimming. With injecting an analog signal to the CS/DIM pin. Figure 13 shows a typical application circuit for analog dimming.

The analog dimming signal is usually on the second side, so there will be isolation circuit (opto-coupler is used) to transfer the dimming signal from second side to the primary side. Opto-coupler can only transfer PWM signal for high accuracy, so there will be interface circuit to change the analog dimming signal into PWM signal as Figure 13 shows. The interface circuit is also used to change the logic of the second analog dimming signal, so that the output current will be direct proportion to the second analog dimming signal.

Then a 0V to 10V analog signal V_{A_DIM} is got on the primary side after these two steps. So the voltage at CS/DIM pin ($V_{CS/DIM}$) is determined by the voltage at S pin (Ip*Rs) and V_{A_DIM}. The output LED mean current (Io) can be calculated

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approximately as:

$$I_o = \frac{N \cdot V_{FB}}{2} \cdot \frac{I_p}{\frac{R_1}{R_1 + R_2} \cdot V_{A_DIM} + \frac{R_2}{R_1 + R_2} \cdot R_s \cdot I_p}$$

As the equation shows, the output current Io decreases from max value to min, when V_{A_DIM} increasing from 0V to 10V.

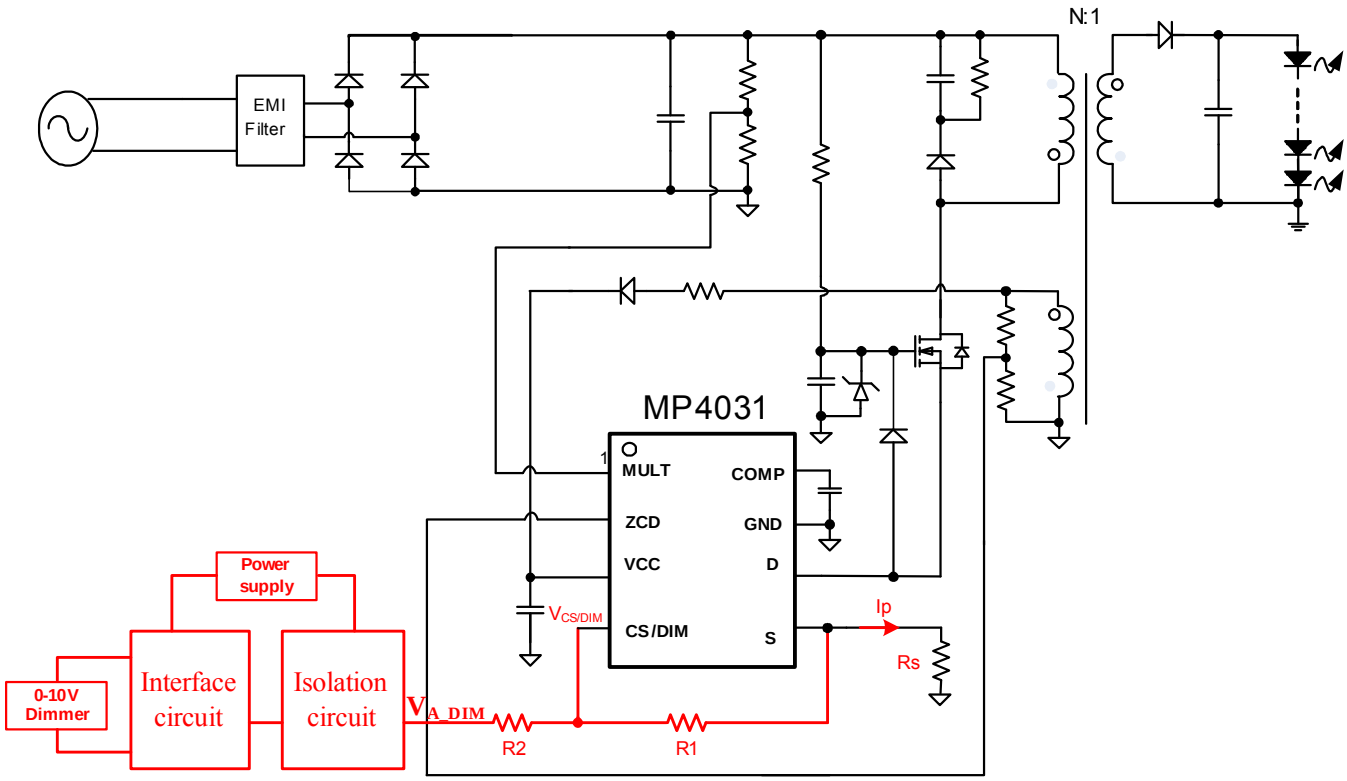


Figure 13: Typical Application Circuit for Analog Dimming

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RIPPLE SUPPRESSOR

(Innovative Proprietary)

For dimming LED lighting application, a single stage PFC converter needs large output capacitor to reduce the ripple whose frequency is double of the Grid. And in deep dimming situation, the LED would shimmer caused by the dimming on duty which is not all the same in every line cycle. What's more, the Grid has noise or inrush which would bring out shimmer even flicker. Figure 14 shows a ripple suppressor, which can shrink the LED current ripple obviously.

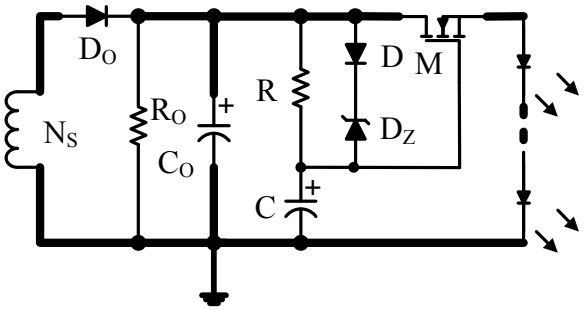


Figure14: Ripple Suppressor

Principle:

Shown in Figure 14, Resister R, capacitor C, and MOSFET M compose the ripple suppressor. Through the RC filter, C gets the mean value of the output voltage V_{Co} to drive the MOSFET M. M works in variable resistance area. C's voltage V_C is steady makes the LEDs voltage is steady, so the LEDs current will be smooth. MOSFET M holds the ripple voltage v_{Co} of the output.

Diode D and Zener diode D_Z are used to restrain the overshoot at start-up. In the start-up process, through D and D_Z, C is charged up quickly to turn on M, so the LED current can be built quickly. When V_C rising up to about the steady value, D and D_Z turn off, and C combines R as the filter to get the mean voltage drop of V_{Co}.

The most important parameter of MOSFET M is the threshold voltage V_{th} which decides the power loss of the ripple suppressor. Lower V_{th} is better if the MOSFET can work in variable resistance area. The BV of the MOSFET can be selected as double as V_{Co} and the Continues Drain current level can be selected as decuple as the LEDs' current at least.

About the RC filter, it can be selected by $\tau_{RC} \geq 50 / f_{LineCycle}$. Diode D can select 1N4148, and the Zener voltage of D_Z is as small as possible when guarantee $V_D + V_{DZ} > 0.5 \cdot V_{Co_PP}$.

Optional Protection Circuit

In large output voltage or large LEDs current application, MOSFET M may be destroyed by over-voltage or over-current when LED+ shorted to LED- at working.

Gate-Source(GS) Over-voltage Protection:

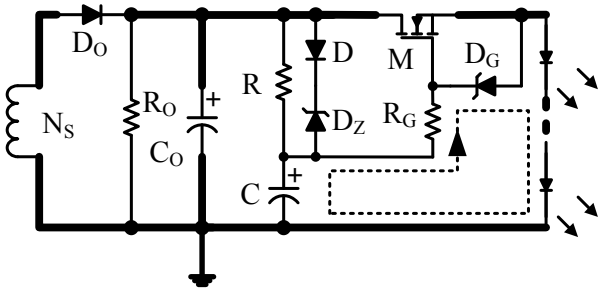


Figure 15: Gate-Source OVP Circuit

Figure 15 shows GS over-voltage protection circuit. Zener diode D_G and resistor R_G are used to protect MOSFET M from GS over-voltage damaged. When LED+ shorted to LED- at normal operation, the voltage drop on capacitor C is high, and the voltage drop on Gate-Source is the same as capacitor C. The Zener diode D_G limits the voltage V_{GS} and R_G limits the charging current to protect D_G. R_G also can limit the current of D_Z at the moment when LED+ shorted to LED-. V_{DG} should bigger than V_{th}.

Drain-Source Over-voltage and Over-current Protection

As Figure 16 shows, NPN transistor T, resistor R_C and R_E are set up to protect MOSFET M from over-current damaged when output short occurs at normal operation. When LED+ shorted to LED-, the voltage v_{DS} of MOSFET is equal to the v_{Co} which has a high surge caused by the parasitic parameter. Zener Dioder D_{DS} protects MOSFET from over-voltage damaged. Transistor T is used to pull down the V_{GS} of M. When M turns off, the load is opened, MP4030 detects there is an OVP happened, so the IC functions in quiescent. The

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pull down point is set by R_C and R_E:

$$R_C/R_E \cdot \frac{V_{CO}}{2} = 0.7V .$$

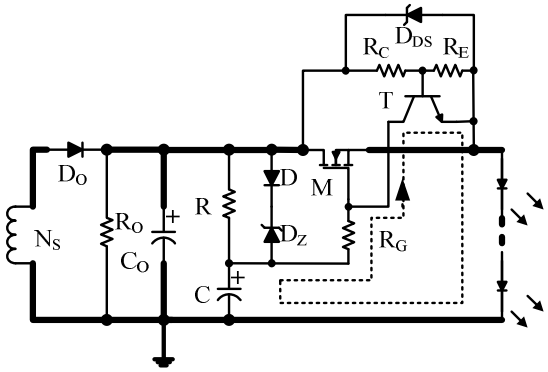


Figure 16: Drain-Source OVP and OCP Circuit

MOSFET LIST

In the Table 1, there are some recommended MOSFET for ripple suppressor.

Table 1: MOSFET LIST

Manufacture P/N	Manufacture	V_{DS}/I_D	$V_{th}(V_{DS}=V_{GS}@T_J=25°C)$	Power Stage
Si4446DY	Vishay	40V/3A	0.6-1.6V@ Id=250μA	<10W
FTD100N10A	IPS	100V/17A	1.0-2.0V@ Id=250μA	5-15W
P6015CDG	NIKO-SEM	150V/20A	0.45-1.20V@ Id=250μA	10-20W

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APPLICATION INFORMATION

Components Selection for Triac dimming application

It is the same with MP4030, please refer to AN055 for detailed information.

Components Selection for Analog dimming application

The bleeding and damping circuit are not needed in analog dimming application.

The analog dimming signal V_{A_DIM} is divided by R1 and R2, and then connected to CS/DIM pin. The selection of the current sense resistor (Rs) is the same with MP4030, it is determined by the full-load output current. A 1kΩ resistor is recommended for R1, which is much bigger than Rs, so will not influence the output current when the dimmer is not connected. R2 is determined by the V_{A_DIM}, it can be calculated by the following equation approximately:

$$\frac{R1}{R1+R2} * V_{A_DIM_MAX} = 0.8V$$

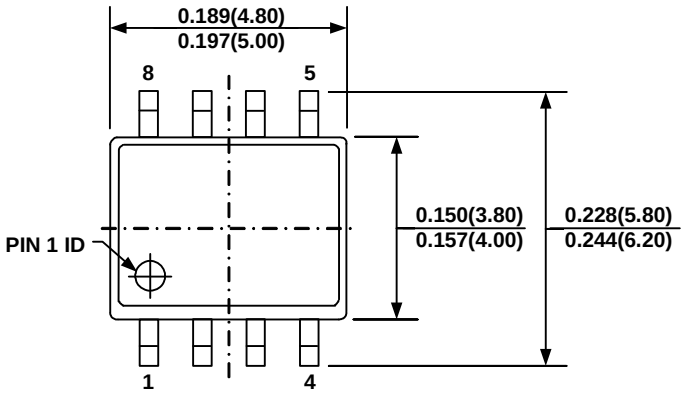
This equation can get a min R2 to make sure the output current will be at full load with max dimming signal $V_{A_DIM_MAX}$. In most application, R2 need to be increased to enlarge the dimming ratio.

And other components' selection can refer to AN055.

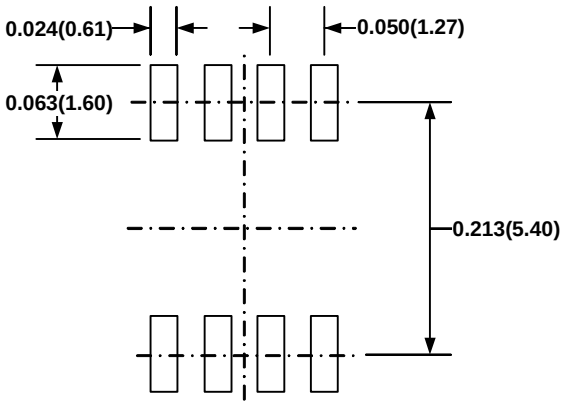
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PACKAGE INFORMATION

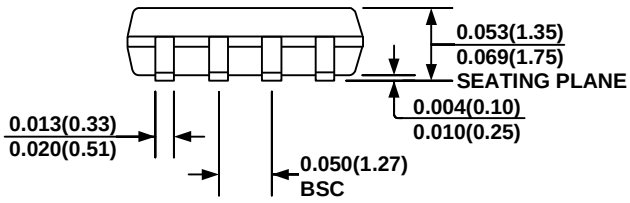
SOIC8



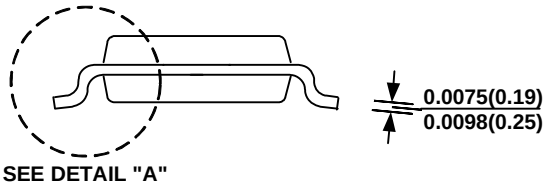
TOP VIEW



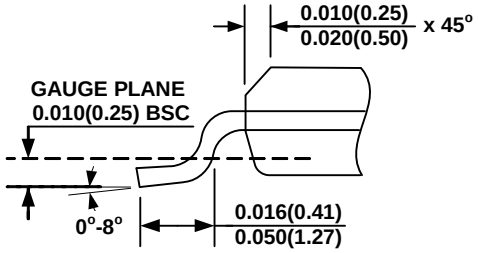
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW



DETAIL "A"

NOTE:

1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
5) DRAWING CONFORMS TO JEDEC MS-012, VARIATION AA.
6) DRAWING IS NOT TO SCALE.

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