MP4033

TRIAC Dimmable, Primary Side Control Offline LED Controller with Active PFC

The Future of Analog IC Technology

DESCRIPTION

The MP4033 is a TRIAC-dimmable primary-side–control, offline LED lighting controller with active PFC. It is also available for applications that requires analog dimming with PWM input. It outputs an accurate LED current for an isolated lighting application with a single-stage converter. The proprietary real-current–control method accurately controls the LED current using primary-side information.

The MP4033 implements power-factor correction and works in boundary-conduction mode to reduce MOSFET switching losses.

The adaptive dimmer type detection and phase-cut-based dimming control achieves good dimmer compatibility and deep dimming range.

The MP4033 has an integrated charging circuit at the supply pin for fast start-up without a perceptible delay.

With the unique control of the driver pin DIM, the MP4033 supports color temperature and brightness control for warm sunset dimming application

The MP4033 has multiple protections that greatly enhance system reliability and safety, including output over-voltage protection, output short-circuit protection, winding short circuit protection, programmable thermal fold-back (MSOP10/SOIC14), ZCD pin short circuit protection, supply-pin under-voltage lockout, and over-temperature protection.

All fault protections feature auto-restart.

The MP4033 is available in SOIC-8 / MSOP-10 / SOIC-14 package.

FEATURES

- Primary-Side-Control without Requiring a Secondary-Side Feedback Circuit
- Adaptive Dimmer Type Detection and Phase-Cut-Based Dimming Control
- Good Dimmer Compatibility and Deep Dimming Range
- Analog Dimming with PWM Input
- Fast Start-Up without Perceptible Delay
- Programmable Current Fold-back to Prolong the LED lifetime (NTC)
- Color Temperature and Brightness Control for Warm Sunset Dimming application
- Accurate Line & Load Regulation
- High Power Factor
- Operates in Boundary Conduction Mode
- Cycle-by-Cycle Current Limit
- Winding Short Circuit Protection
- Output Over-Voltage Protection
- Output Short-Circuit Protection
- ZCD Pin Short-Circuit Protection
- Over-Temperature Protection
- Available in SOIC-8/MSOP-10/SOIC-14 Package

APPLICATIONS

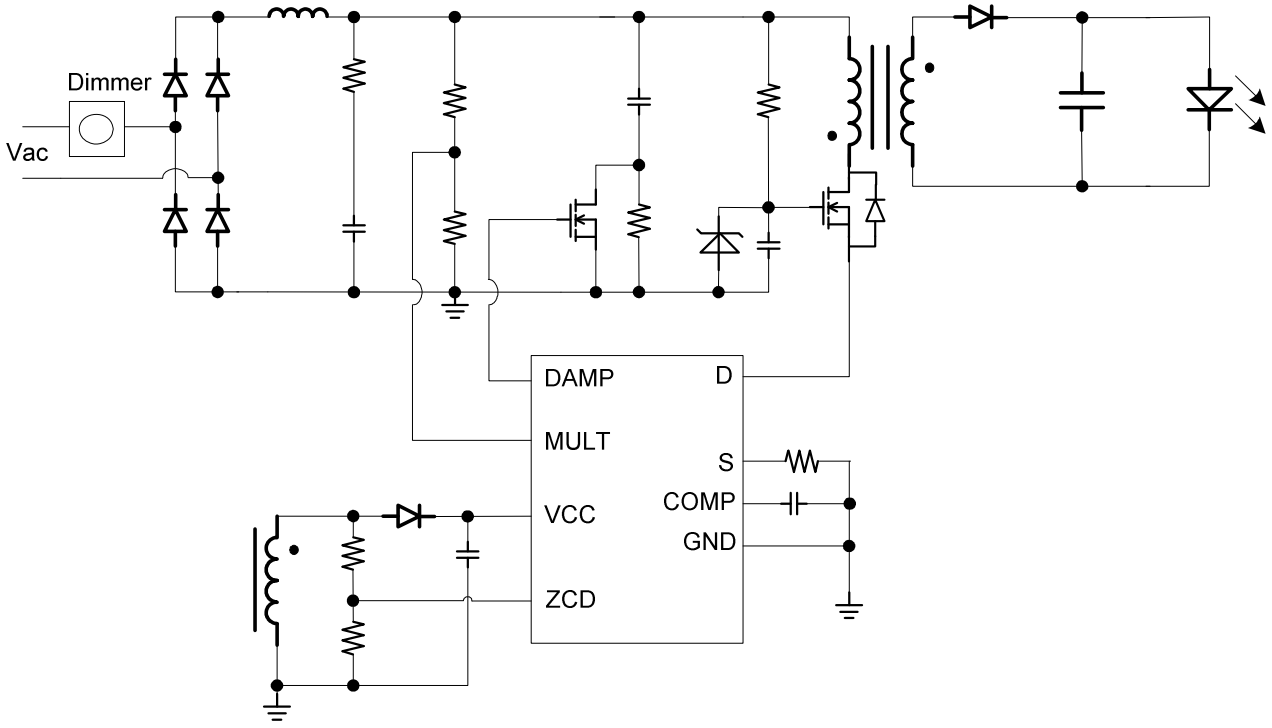
- Solid-State Lighting up to 50W
- Industrial and Commercial Lighting
- Residential Lighting

All MPS parts are lead-free and adhere to the RoHS directive. For MPS green status, please visit MPS website under Products, Quality Assurance page.

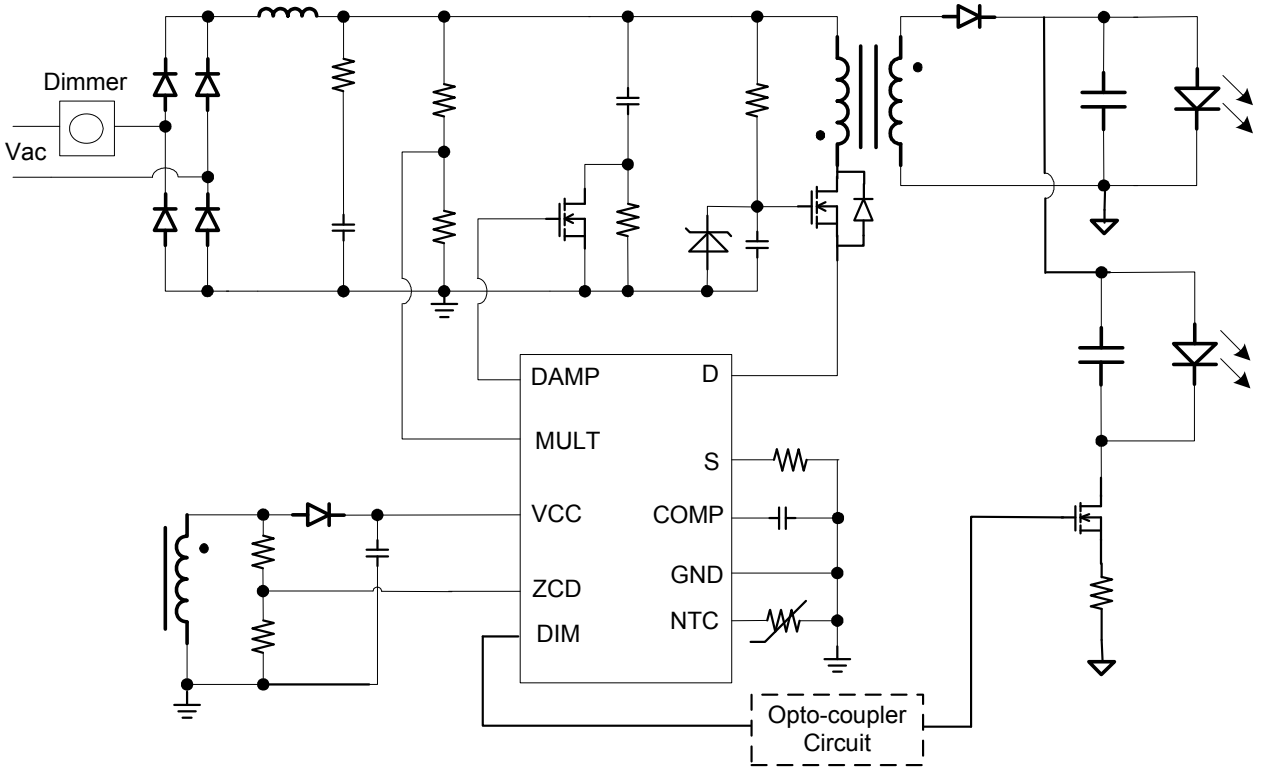
"MPS" and "The Future of Analog IC Technology" are registered trademarks of Monolithic Power Systems, Inc.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2014 MPS. All Rights Reserved.

TYPICAL APPLICATION



SOIC8



SOIC14 and MSOP10

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2014 MPS. All Rights Reserved.

ORDERING INFORMATION

Part Number	Package	Top Marking
MP4033GS*	SOIC-8	*See Below*
MP4033GK**	MSOP-10	
MP4033GSE***	SOIC-14	

* For Tape & Reel, add suffix –Z (e.g. MP4033GS–Z)
** For Tape & Reel, add suffix –Z (e.g. MP4033GK–Z)
*** For Tape & Reel, add suffix –Z (e.g. MP4033GSE–Z)

TOP MARKING (SOIC-8)

MP4033
LLLLLLLL
MPSYWW

MP4033: first six digits of the part number;
LLLLLLLL: lot number;
MPS : MPS prefix:
Y: year code;
WW: week code:

TOP MARKING (MSOP-10)

YWLLL
M4033

Y: year code;
W: week code:
LLL: lot number;
M4033: first five digits of the part number;

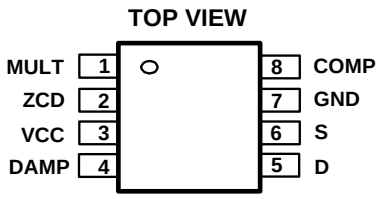
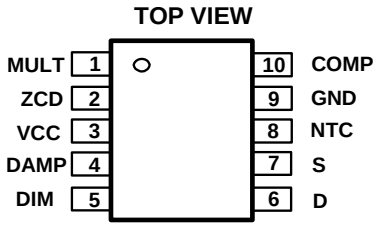
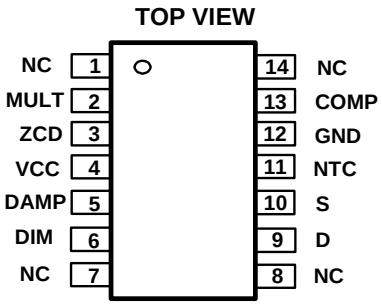
TOP MARKING (SOIC-14)

MPSYYWW
MP4033
LLLLLLLLL

MPS : MPS prefix:
YY: year code;
WW: week code:
MP4033: first six digits of the part number;
LLLLLLLLL: lot number;

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2014 MPS. All Rights Reserved.

PACKAGE REFERENCE

SOIC8	MSOP10	SOIC14
		

ABSOLUTE MAXIMUM RATINGS (1)

Input Voltage VCC ..... -0.3V to +30V
Low-Side MOSFET Drain to Source Voltage ..... -0.7V to +30V
Damp Pin Voltage ..... -0.3V to +16.5V
Other Analog Inputs and Outputs.. -0.3V to 6.5V
ZCD Pin Current ..... -5mA to +5mA
Continuous Power Dissipation (T_J = +25°C)(2)
SOIC8 ..... 1.3W
SOIC14 ..... 1.45W
MSOP10 ..... 0.83W
Junction Temperature ..... 150°C
Lead Temperature ..... 260°C
Storage Temperature ..... -65°C to +150°C

Recommended Operating Conditions (3)

Supply Voltage VCC ..... 11V to 27V
Operating Junction Temp (T_J). . -40°C to +125°C

Thermal Resistance (4)

	θ_{JA}	θ_{JC}	
SOIC8	96	45	°C/W
MSOP10	150	65	°C/W
SOIC14	86	38	°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2014 MPS. All Rights Reserved.

ELECTRICAL CHARACTERISTICS

Typical values are V_{CC} =20V, T_J = 25°C, unless otherwise noted.

Minimum and maximum values are at V_{CC} =20V, T_J = -40°C to +125°C, unless otherwise noted, guaranteed by characterization.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Supply Voltage						
Operating Range	V_{CC}	After turn on	11		27	V
VCC Upper Level: Internal Charging Circuit Stops and IC Turns On	V_{CCH}		9.5	10	10.5	V
VCC Lower Level: Internal Charging Circuit Triggers	V_{CCL}		8.55	9	9.45	V
Vcc Re-charge and IC turns off Level in Fault Condition	V_{CCEN}	Fault condition	6.55	7	7.45	V
Supply Current						
VCC Charging Current from D	$I_{D\ charge}$	VD=16V, VCC=5V	13	25	40	mA
Pull Down Current at VCC_UVLO	$I_{VCC_PULL_DOWN}$	VCC=9V, Rising	0.95	1.25	1.8	mA
Quiescent Current	I_Q	No switching, VCC=15V		800	1300	µA
Quiescent Current at Fault	I_{Q_FAULT}	Fault condition, IC latch, VCC=15V	220	340	620	µA
Operating Current	I_{CC}	f_s =70kHz, VCC=15V		1	2	mA
Multiplier						
Linear Operation Range	V_{MULT}	V_{COMP} from 1.9V to 4.9V	0		3	V
Gain	$K^{(5)}$	V_{COMP}=2V, V_{MULT}=0.5V	0.90	1.28	1.60	1/V
		V_{COMP}=2V, V_{MULT}=1.5V	0.90	1.25	1.60	1/V
		V_{COMP}=2V, V_{MULT}=3V	0.90	1.24	1.60	1/V
TRIAC Dimming Phase Off Detection Threshold	V_{MULT_OFF}		0.08	0.10	0.12	V
TRIAC Dimming Phase On Detection Threshold	V_{MULT_ON}		0.26	0.28	0.30	V
TRIAC Dimming Off Line-Cycle Blanking Ratio	D_{OFF_LEB}		28%	30%	33%	
Dimming Pull-Down Turn on Threshold	$V_{MULT\ DP\ ON\ TL}$	Trailing edge dimmer	0.43	0.45	0.47	V
	$V_{MULT\ DP\ ON\ LD}$	Leading edge dimmer	0.22	0.25	0.28	V
Dimming Pull-Down Turn off Threshold	$V_{MULT\ DP\ OFF\ TL}$	Trailing edge dimmer	0.26	0.28	0.30	V
	$V_{MULT\ DP\ OFF\ LD}$	Leading edge dimmer	0.32	0.35	0.38	V
Leading Edge Dimming Detection Low Threshold	$V_{MULT_LD_LOW}$		0.08	0.10	0.12	V
Leading Edge Dimming Detection High Threshold	$V_{MULT_LD_HIGH}$		0.26	0.28	0.30	V

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2014 MPS. All Rights Reserved.

ELECTRICAL CHARACTERISTICS *(continued)*

Typical values are V_{CC} =20V, T_J = 25°C, unless otherwise noted.

Minimum and maximum values are at V_{CC} =20V, T_J = -40°C to +125°C, unless otherwise noted, guaranteed by characterization.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Trailing Edge Dimming Detection High Threshold	$V_{MULT_TL_HIGH}$	Rising, V_{MULT_PK}≥0.58V Falling, V_{MULT_PK}≥0.50V	0.43	0.45	0.47	V
		Rising, 0.58V>V_{MULT_PK}≥0.53V Falling, 0.50V>V_{MULT_PK}≥0.45V	0.38	0.4	0.42	V
		Rising, 0.53V>V_{MULT_PK}≥0.48V Falling, 0.45V> V_{MULT_PK}≥0.40V(6)		0.35		V
		Rising, 0.48V>V_{MULT_PK}≥0.43V Falling, 0.40V>V_{MULT_PK}≥0.35V(6)		0.3		V
		Rising, 0.43V>V_{MULT_PK}≥0.38V Falling, 0.35V>V_{MULT_PK}≥0.30V(6)		0.25		V
Trailing Edge Dimming Detection High Threshold Hysteresis	$V_{MULT_TL_H_HYS}$			80		mV
Trailing Edge Dimming Detection Low Threshold	$V_{MULT_TL_LOW}$		0.08	0.10	0.12	V
Leading Edge dimmer detection Time threshold	$t_{LEADING}$	Rising	86	100	134	µs
Trailing Edge dimmer detection Time threshold	$t_{TRAILING}$	Falling	388	450	602	µs
Error Amplifier						
Reference Voltage	V_{REF}		0.400	0.414	0.428	V
Transconductance	G_{EA}	Guaranteed by design		130		µA/V
COMP Lower Clamp Voltage	V_{COMPL_LD}	Leading edge dimmer	1.83	1.88	1.94	V
	V_{COMPL_TL}	Trailing edge dimmer	1.53	1.58	1.64	V
	V_{COMPL_N}	No dimmer	1.53	1.58	1.64	V
	$V_{COMPL_NTC≤1.0V}$	NTC≤1.0V	1.44	1.49	1.55	V
Max. Source Current	I_{COMP+}			57		µA
Max. Sink Current without Dimmer	I_{COMP-}			200		µA
Sink Current at TRIAC Dimming Off	$I_{SINK_DIM_LD}$	Leading Edge Dimmer		85.50		µA
	$I_{SINK_DIM_TL}$	Trailing Edge Dimmer		155		µA

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2014 MPS. All Rights Reserved.

ELECTRICAL CHARACTERISTICS *(continued)*

Typical values are V_{CC} =20V, T_J = 25°C, unless otherwise noted.

Minimum and maximum values are at V_{CC} =20V, T_J = -40°C to +125°C, unless otherwise noted, guaranteed by characterization.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Current Sense Comparator						
Leading-Edge-Blanking Time	t_{LEB}		350	500	750	ns
Over-Current-Protection Leading-Edge-Blanking Time	t_{LEB_OCP}		260	350	550	ns
Over-Current-Protection Threshold	V_{OCP}		2.56	2. 70	2.86	V
Current Sense Upper Clamp Voltage	$V_{S\ CLAMP\ H}$		1.97	2.07	2.17	V
Current Sense Lower Clamp Voltage	$V_{S\ CLAMP\ L}$		0.01	0.035	0.09	V
Zero-Current Detector						
Zero-Current–Detect Threshold	$V_{ZCD\ T}$	Falling Edge	0.27	0.30	0.33	V
Zero-Current–Detect Hysteresis	$V_{ZCD\ HYS}$		550	590	625	mV
ZCD Pin Short Circuit Threshold	V_{ZCD_SC}		78	100	122	mV
ZCD Pin Short Circuit Blanking time	$t_{ZCD_SC_LEB}$			33		ms
Zero-Current–Detect LEB	t_{ZCD_LEB}	Starts at Gate Turn Off when $V_{MULT\ O} \geqslant 0.25V$	1.90	2.30	3.36	µs
		Starts at Gate Turn Off when $V_{MULT\ 0}$ <0.25V	0.95	1.18	1.68	µs
Over-Voltage Threshold	$V_{ZCD\ OVP}$		4.90	5.30	5.70	V
OVP Detect LEB	t_{OVP_LEB}	Starts at Gate Turn Off when $V_{MULT\ O} \geqslant 0.25V$	1.90	2.30	3.36	µs
		Starts at Gate Turn Off when $V_{MULT\ O}$ <0.25V	0.95	1.18	1.68	µs
Minimum Off Time	t_{OFF_MIN}	Normal	4	5.3	8	µs
		NTC≤1.0V		10		µs
Weak/Strong DP Mode detector current (for leading edge dimmer)	$I_{DP_DET_LD}$		140	180	220	µA
Strong DP Mode Enable Threshold (for leading edge dimmer)	$V_{EN_DP_STR_LD}$		1.13	1.18	1.23	V
Weak/Strong DP Mode Detection Time (for leading edge dimmer)	$t_{DP_DET_LD}$		150	215	320	µs
Starter						
Start Timer Period	t_{START}		100	130	165	µs

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2014 MPS. All Rights Reserved.

ELECTRICAL CHARACTERISTICS *(continued)*

Typical values are V_{CC} =20V, T_J = 25°C, unless otherwise noted.

Minimum and maximum values are at V_{CC} =20V, T_J = -40°C to +125°C, unless otherwise noted, guaranteed by characterization.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Internal Main MOSFET						
Breakdown Voltage	$BV_{DSS\ MAIN}$	$V_{GS=0}$	30			V
Drain-Source On-Resistor	$R_{DS(ON)_MAIN}$	I_D=100mA, T_J=25 °C,		250		mΩ
		I_D=100mA, T_J=25 °C, VCC= V_{CCEN} +50mV		250		mΩ
Internal OVP Pull Up MOSFET						
Breakdown Voltage	$BV_{DSS\ D\ VCC}$		30			V
Continue Drain Current	$I_{D_D\text{-}VCC}$		10	17	27	mA
Internal Dimming Pull Down Current Source						
Strong Dimming Pull Down Current for leading edge dimmer	$I_{DP_STRONG_LD}$		27	35	43	mA
Weak Dimming Pull Down Current for leading edge dimmer	$I_{DP_WEAK_LD}$		8	10	12	mA
Pull Down Current for Trailing edge dimmer	I_{DP_TL}		133	150	167	mA
Min Clamp Ratio of Pull Down Current for Trailing edge dimmer (I_Min/I_Normal)				13%		
NTC						
High Threshold Voltage	V_{H_NTC}		1.14	1.2	1.36	V
Low Threshold Voltage	V_{L_NTC}		0.70	0.80	0.90	V
Shutdown Threshold	V_{SD_NTC}		0.32	0.38	0.44	V
Shutdown Voltage Hysteresis	$V_{SD_NTC_HSY}$		80	100	120	mV
Pull Up Current Source	$I_{PULL_UP_NTC}$		42	52	62	µA
Leakage Current	$I_{LEAKAGE_NTC}$				1	µA
PWM Dimming Blanking Time	t_{PWM_LEB}			20		ms
DAMP						
Turn Off Threshold	$V_{MULT\ DAMP\ OFF}$		0.22	0.25	0.28	V
Turn On Threshold	$V_{MULT\ DAMP\ ON}$		0.32	0.35	0.38	V
Pull Down Current	$I_{DAMP\ PULL\ DOWN}$	V_{DAMP}=5V	290	370	450	µA
Pull Up Current	$I_{DAMP\ PULL\ UP}$	V_{DAMP}=0.3V	70	90	110	µA
Upper Clamp Voltage	$V_{DAMP\ CLAMP\ UP}$		13	15	16.5	V
Min Pull Up Voltage	V_{DAMP_MIN}	VCC= V_{CCEN} +50mV	5.7			V

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2014 MPS. All Rights Reserved.

ELECTRICAL CHARACTERISTICS *(continued)*

Typical values are V_{CC} =20V, T_J = 25°C, unless otherwise noted.

Minimum and maximum values are at V_{CC} =20V, T_J = -40°C to +125°C, unless otherwise noted, guaranteed by characterization.

Parameter	Symbol	Condition	Min	Typ	Max	Units
DIM						
Source Current	$I_{DIM\ SOURCE}$		2	3	4	mA
Sink Current	$I_{DIM\ SINK}$		1.5	2.8	4	mA
High Level	$V_{DIM\ HIGH}$		5.0		6.1	V
Low Level	V_{DIM_LOW}				0.3	V
Thermal Shutdown						
Thermal Shutdown Threshold(6)	T_{SD}			150		℃
Thermal Shutdown Recovery Hysteresis(6	T_{HYS}			25		℃

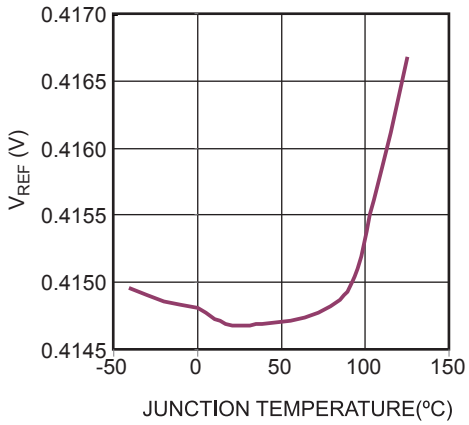
Notes:

5) The multiplier output is given by: Vs=K•VMULT• (VCOMP-1.5)
6) Guaranteed by characterization.
7) Guaranteed by design.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2014 MPS. All Rights Reserved.

TYPICAL CHARACTERISTICS

Reference Voltage vs. Junction Temperature



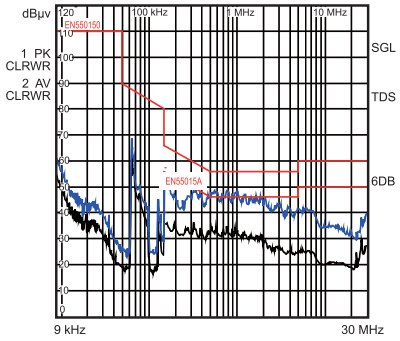
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2014 MPS. All Rights Reserved.

TYPICAL PERFORMANCE CHARACTERISTICS

Based on the EVB model: EV4033-K-00A, isolated flyback converter, 230VAC/50Hz input, 24V/420mA output, T_A=25°C, unless otherwise noted.

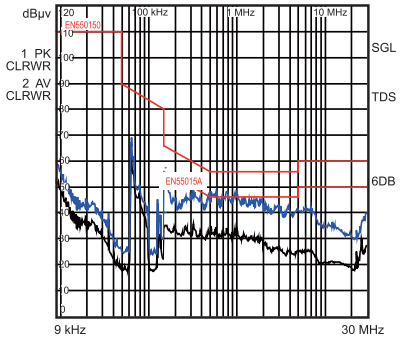
Conducted EMI L-Line

V_{IN} = 230V_{AC}/50Hz, Full Load,
RBW = 9kHz, MT = 20ms



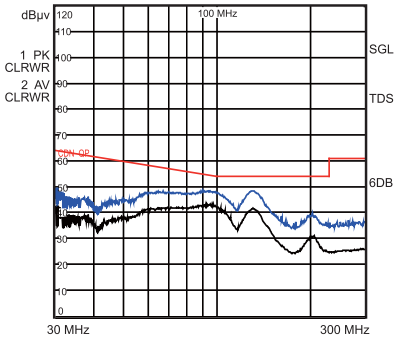
Conducted EMI N-Line

V_{IN} = 230V_{AC}/50Hz, Full Load,
RBW = 9kHz, MT = 20ms



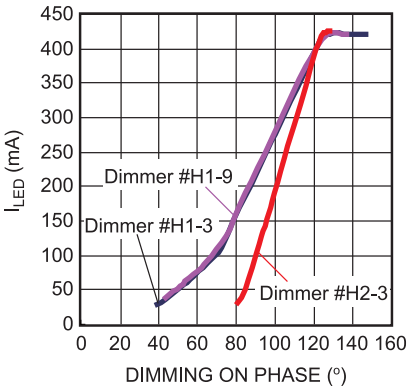
Radiated EMI

Tested by CDN,
V_{IN}=230V_{AC}/50Hz, Full Load



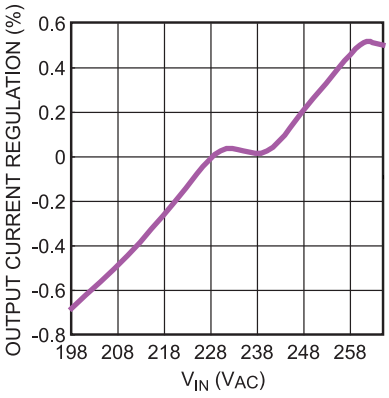
Dimming Curve

V_{IN}=120V_{AC}/60Hz, Full Load,
with Different Dimmers



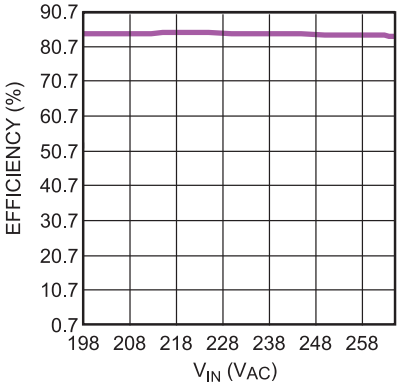
Line Regulator

Full Load



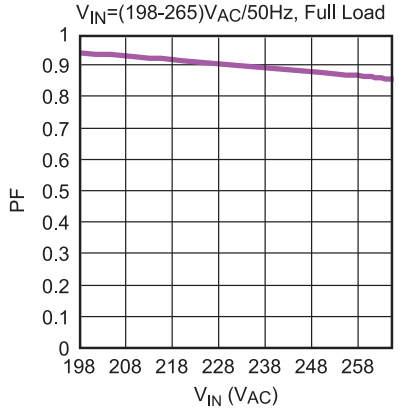
Efficiency vs. V_{IN}

V_{IN}=(198-265)V_{AC}/50Hz, Full Load



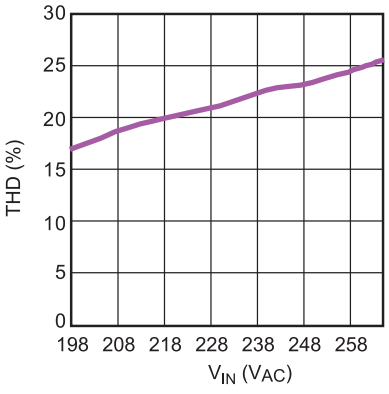
PF vs. V_{IN}

V_{IN}=(198-265)V_{AC}/50Hz, Full Load



THD vs. V_{IN}

V_{IN}=108-132V_{AC}/60Hz, Full Load

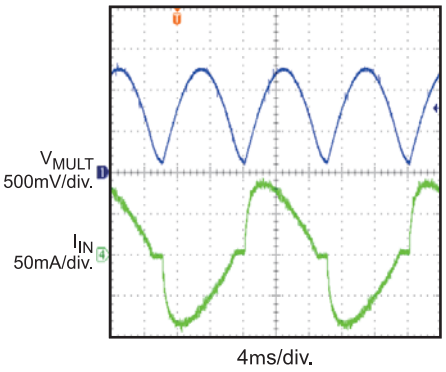


MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2014 MPS. All Rights Reserved.

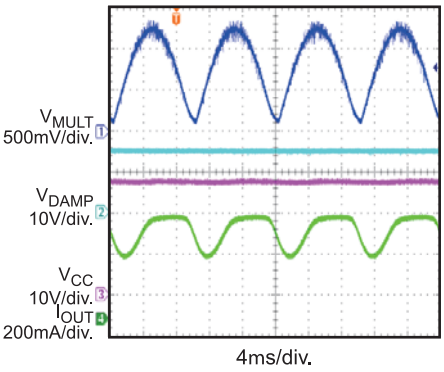
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Based on the EVB model: EV4033-K-00A, isolated flyback converter, 230VAC/50Hz input, 24V/420mA output, T_A=25°C, unless otherwise noted.

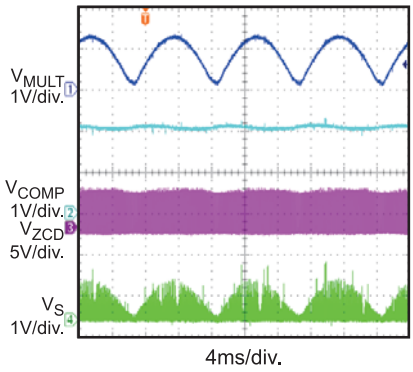
Input Voltage and Current
V_{IN}=230V_{AC}/50Hz, Full Load



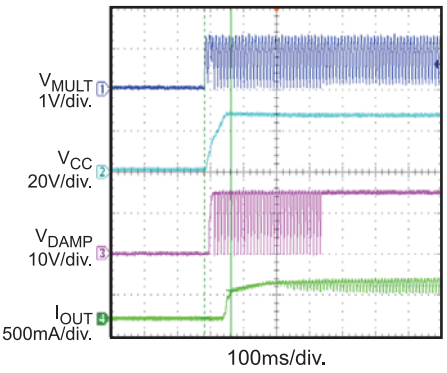
Steady State
V_{IN}=230V_{AC}/50Hz, Full Load



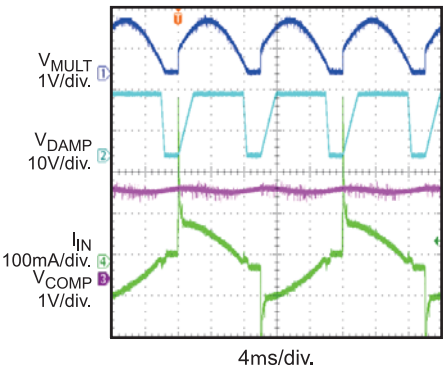
Steady State
V_{IN}=230V_{AC}/50Hz, Full Load



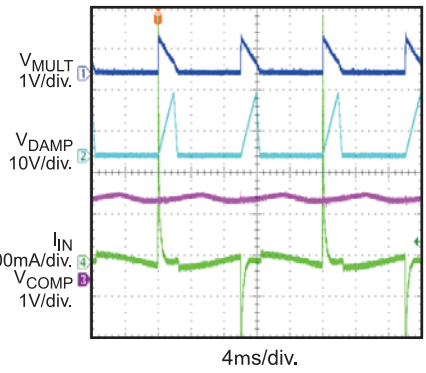
V_{IN} Start Up
V_{IN}=230V_{AC}/50Hz, Full Load



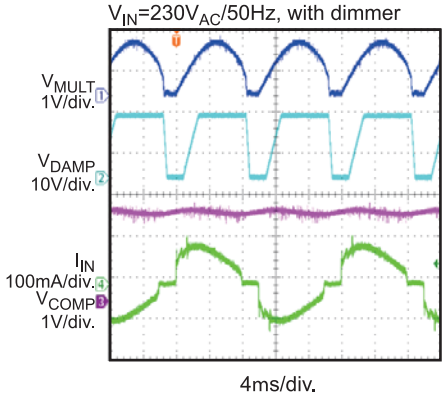
Dimming Performance
Max dimming on phase
with leading-edge dimmer
V_{IN}=230V_{AC}/50Hz, with dimmer



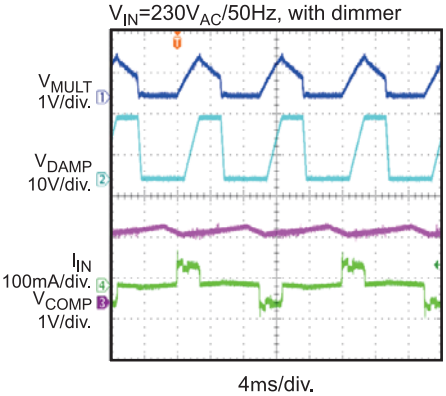
Dimming Performance
Min dimming on phase
with leading-edge dimmer
V_{IN}=230V_{AC}/50Hz, with dimmer



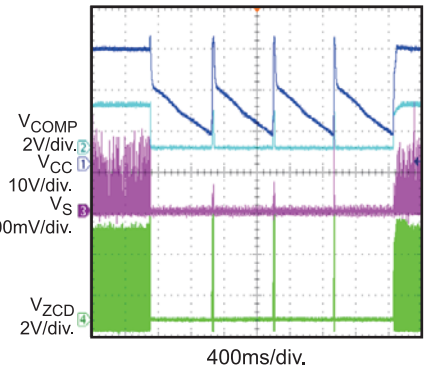
Dimming Performance
Max dimming on phase
with trailing-edge dimmer
V_{IN}=230V_{AC}/50Hz, with dimmer



Dimming Performance
Min dimming on phase
with trailing-edge dimmer
V_{IN}=230V_{AC}/50Hz, with dimmer



OVP
LED Load Open then Recovery
V_{IN}=230V_{AC}/50Hz, Full Load



MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2014 MPS. All Rights Reserved.

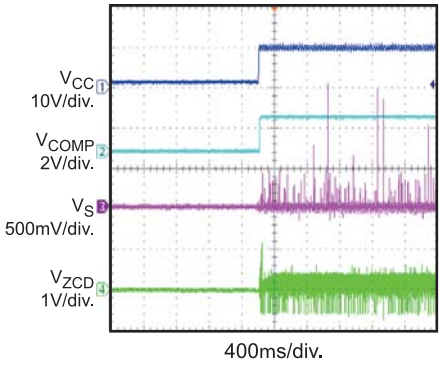
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Based on the EVB model: EV4033-K-00A, isolated flyback converter, 230VAC/50Hz input, 24V/420mA output, T_A=25°C, unless otherwise noted.

OCP

LED+ Short to LED- then start up

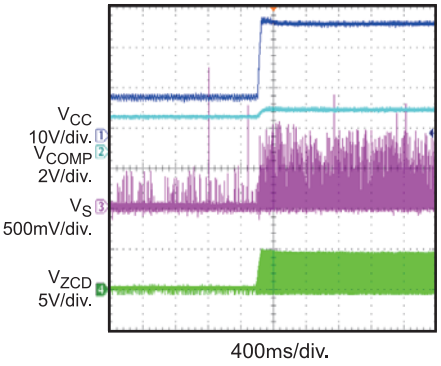
V_{IN}=230V_{AC}/50Hz, Full Load



OCP

LED+ Short to LED- then Recovery

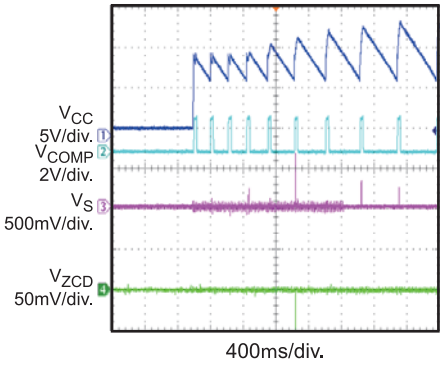
V_{IN}=230V_{AC}/50Hz, Full Load



ZCD PIN Short Protection

Short ZCD PIN then start up

V_{IN}=230V_{AC}/50Hz, Full Load



MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2014 MPS. All Rights Reserved.

PIN FUNCTIONS

Pin #			Name	Description
SOIC-8	SOIC-14	MSOP-10		
1	2	1	MULT	One of the Internal Multiplier's Input. Connect to the tap of resistor divider from the rectified voltage of the AC line. The half-wave sinusoid signal on this pin provides a reference signal for the internal current control loop. The MULT pin is also used for dimmer type detection and dimming phase detection.
2	3	2	ZCD	Zero-Current Detection. A negative going edge triggers the internal MOSFET's turn-on signal. Connect to the tap of a resistor divider from the auxiliary winding to GND. The over-voltage condition is detected in ZCD pin. Over-voltage occurs if V_{ZCD} exceeds the over-voltage-protection (OVP) threshold after a blanking time when the internal MOSFET turns off. The ZCD pin is also used to select the Strong/Weak Dimming Pull Down Current in leading edge dimming. Besides, the ZCD itself has short circuit protection to prevent the device damage when output is open and ZCD pin is short.
3	4	3	VCC	Supply Voltage. Supply power for both the control signal and the internal MOSFET's gate driver. Connect this pin to an external bulk capacitor—typically 22μF.
4	5	4	DAMP	Gate Control pin of the external Damping MOSFET.
NA	6	5	DIM	Gate driver. This is the DIM signal from internal control logic, it is used to control the color temperature and brightness for warm sunset dimming or drive an external dummy Load to enlarge the dimming depth..
5	9	6	D	Internal Low-Side main MOSFET Drain. It is connected to the source of the external high-side main MOSFET. This pin is also internally connected to VCC thro a diode and a JFET to form an internal charging circuit for VCC. There is a series-connected MOS and diode internally to pull up the D to VCC at fault condition to turn off the main switch reliably. There is an intelligent Dimming Pull Down Current Source on this pin.
6	10	7	S	Internal Low-Side main MOSFET Source. Connect a resistor from this pin to GND to sense the internal MOSFET current. An internal comparator compares the resulting voltage to the internal sinusoid shaped current reference signal to determine when the MOSFET turns off. If the voltage exceeds the upper current-clamp threshold after the leading edge blanking time during the turn-on interval, the gate signal turns off. Over-current occurs if V_s exceeds OCP Voltage during the gate-on interval after the OCP lead edge blanking time.
NA	11	8	NTC	LED temperature protection input. Connecting a NTC resistor from this pin to GND reduces the output current in high ambient temperature to protect the LED and driver. Analog dimming is accomplished with an external PWM signal through a resistor. A 1kΩ resistor is recommended.
7	12	9	GND	Ground. Current return of the control signal and power signal.
8	13	10	COMP	Loop Compensation. Connect it to a compensation network to stabilize the LED driver and accurately control the LED driver current.
	1,7,8,14		NC	

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2014 MPS. All Rights Reserved.

FUNCTION DIAGRAM

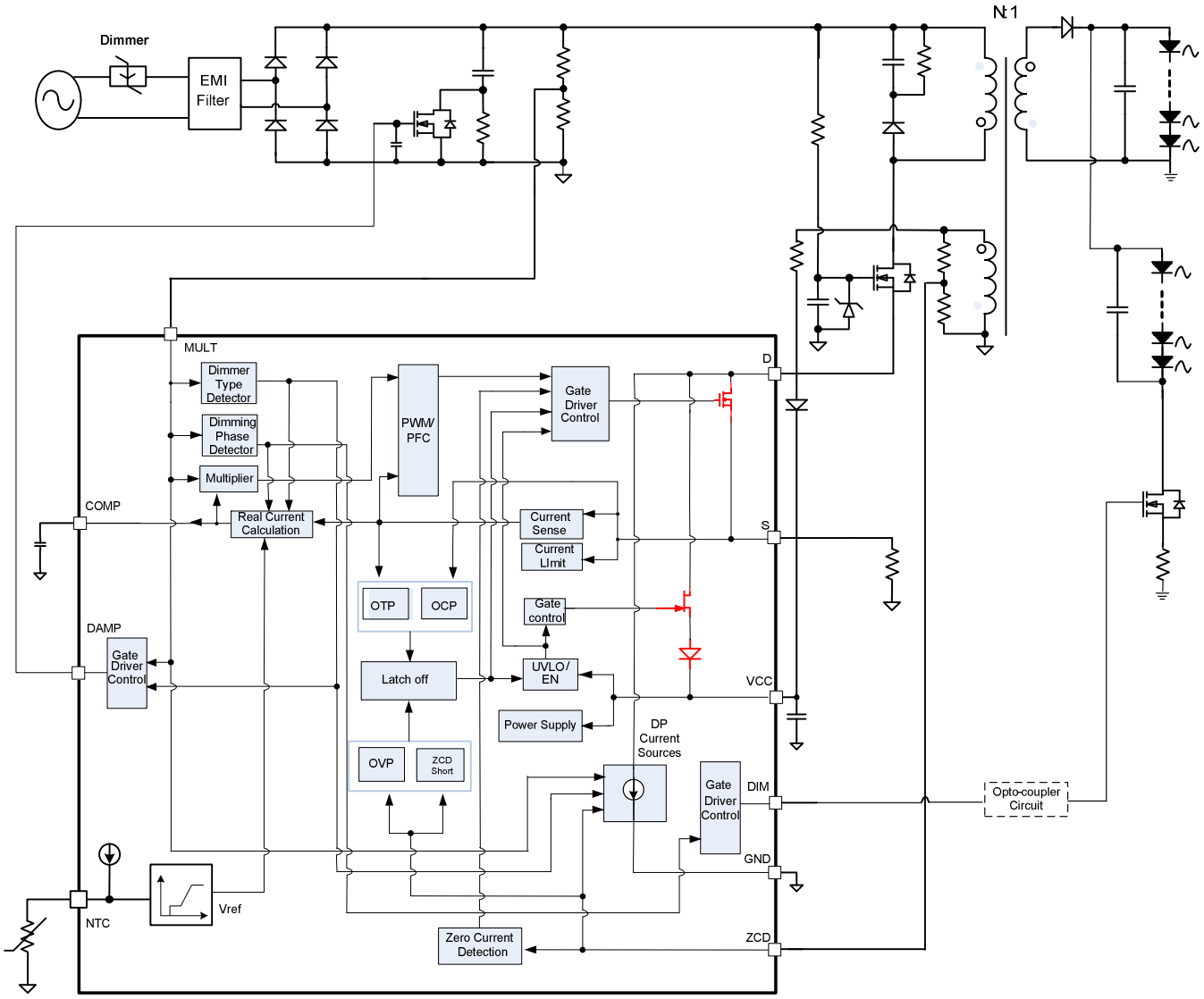


Figure 1: MP4033 Function Block Diagram

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2014 MPS. All Rights Reserved.

OPERATION

The MP4033 is a TRIAC-dimmable primary-side–control, offline LED controller designed for high-performance LED lighting. The MP4033 accurately controls the LED current using the real-current–control method based on primary-side information. The adaptive dimmer type detection and phase-cut-based dimming control bring good dimmer compatibility and deep dimming range. It also achieves a high power factor to eliminate noise pollution on the AC line. The integrated VCC charging circuit achieves fast start-up without any perceptible delay. The programmable thermal current fold back function prolongs the lifetime of the LED. With duty ratio varies with dimming cycle, the DIM pin easily supports color temperature and brightness control for warm sunset dimming application. The MP4033 is also available for analog dimming with PWM input.

Boundary-Conduction Mode

During the external MOSFET on time (T_{ON}), the rectified input voltage applied on the primary-side inductor (Lm) makes the primary current thru Lm increase linearly from zero to the peak value (I_{pk}), then the external MOSFET turns off. The energy stored in Lm forces the secondary side rectifier diode to turn on, and the inductor current decreases linearly from the peak value to zero.

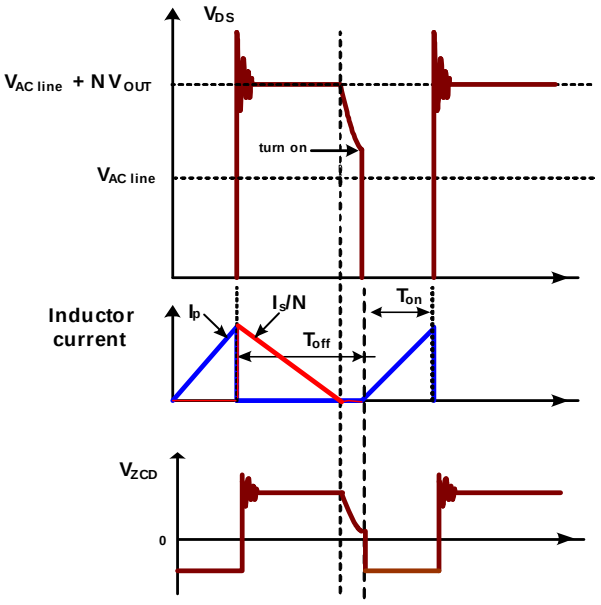


Figure 2: Boundary-Conduction Mode

When the current decreases to zero, the voltage drop on the main MOSFET drain-to-source falls and oscillates. The oscillation frequency is determined by the primary side inductor and the combined parasitic capacitances. The resonance is reflected on the auxiliary winding (see Figure 2).

The zero-current detector generates the external MOSFET turn-on signal when the ZCD voltage falls below V_{ZCD_T} after a blanking time t_{ZCD_LEB} and ensures the MOSFET turns on at a relatively low voltage (see Figure 3).

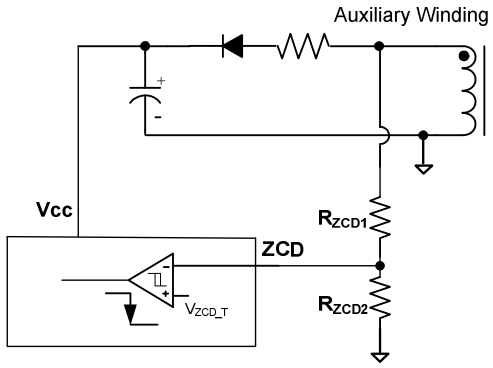


Figure 3: Zero-Current Detector

As a result, there are relatively small primary switching on losses and no secondary-diode reverse-recovery losses. This ensures high efficiency and low EMI noise.

Real-Current Control

The proprietary real-current–control method allows the MP4033 to control the secondary-side LED current based on primary-side information. The approximate output LED mean current can be calculated as:

$$I_o \approx \frac{N \cdot V_{REF}}{2 \cdot R_s}$$

Where:

- N is the turn ratio of the primary side to the secondary side,
- V_{REF} is the internal reference voltage (typically 0.414), and
- R_s is the sense resistor between the internal MOSFET source and GND.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2014 MPS. All Rights Reserved.

Power-Factor Correction

The MULT pin is connected to the tap of a resistor divider from the rectified instantaneous line voltage, driving a sinusoidal multiplier output. This signal provides the reference for the current comparator, which shapes the primary-peak current into a sinusoid and has the same phase with the input line voltage. This guarantees a high power factor.

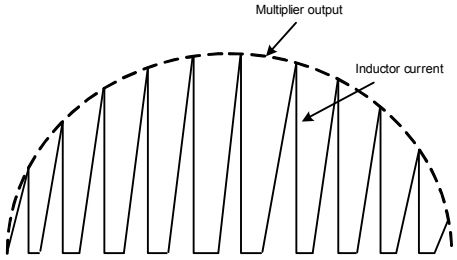


Figure 4: Power-Factor Correction

The multiplier's maximum output voltage to the current comparator is clamped to $V_{S_CLAMP_H}$ to limit the cycle-by-cycle current. The multiplier's minimum output voltage is clamped to $V_{S_CLAMP_L}$ to ensure a turn-on signal during the TRIAC dimming OFF interval, which pulls down the rectifier input voltage and accurately detects the dimming phase.

VCC Timing Sequence

The VCC timing sequence is shown in Figure5. Initially, VCC charges through the internal charging circuit from the AC line. When VCC reaches V_{CCH}, the internal charging circuit stops charging, the control logic initializes and the internal main MOSFET begins to switch. The auxiliary winding takes over the power supply. However, the initial auxiliary-winding positive voltage may not be large enough to charge VCC, causing VCC to drop. Instead, if the VCC voltage drops below V_{CCL} threshold, the internal charging circuit triggers and charges VCC to V_{CCH} again. This cycle repeats until the auxiliary winding voltage is high enough to power VCC.

If any fault occurs during this time, the switching and the internal charging circuit stop, and VCC drops. When VCC decreases below V_{CCEN}, the internal re-charge is enabled to auto-restart.

Auto Start

The MP4033 contains an auto starter that starts timing when the MOSFET turns off. If ZCD fails to send a turn-on signal after t_{START}, the starter will automatically send a turn-on signal to avoid unnecessary shutdown.

Minimum OFF Time

The MP4033 operates with a variable switching frequency; the frequency changes with the instantaneous input line voltage. In order to limit the maximum frequency and get a good EMI performance, the MP4033 employs an internal minimum off time.

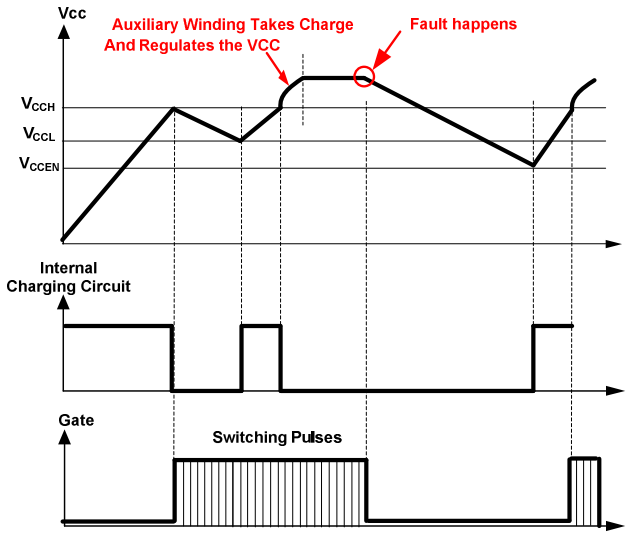


Figure 5: VCC Timing Sequence

Leading-Edge Blanking

In order to avoid premature switching-pulse termination due to the parasitic capacitances discharging when the MOSFET turns on, an internal leading-edge-blanking (LEB) time is introduced on S pin. The current comparator blocks the input path from S pin during the blanking time. Figure 6 shows the leading-edge blanking.

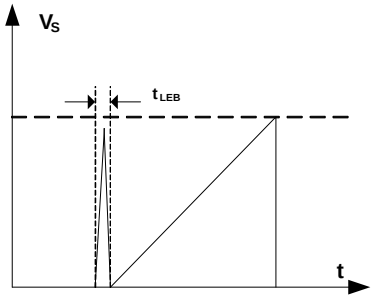


Figure 6: Leading-Edge Blanking

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2014 MPS. All Rights Reserved.

Output Over-Voltage Protection (OVP)

Output over-voltage protection (OVP) prevents the components from over-voltage damage. The auxiliary winding voltage's positive plateau is proportional to the output voltage, so the OVP block monitors this auxiliary winding voltage to apply an OVP function, as shown in Figure 7. Once the ZCD pin voltage exceeds V_{ZCD_OVP}, the OVP signal is triggered, the gate driver turns off, the IC works in its quiescent current mode. When the VCC voltage drops below the UVLO threshold, the IC shuts down and the system restarts. The output OVP set point is calculated as:

$$V_{out_ovp} \cdot \frac{N_{aux}}{N_{sec}} \cdot \frac{R_{ZCD2}}{R_{ZCD1} + R_{ZCD2}} = V_{ZCD_OVP}$$

Where:

$V_{out\text{-}ovp}$ is the output OVP threshold,

N_{aux} is the turns of auxiliary winding, and

N_{sec} is the turns of secondary winding

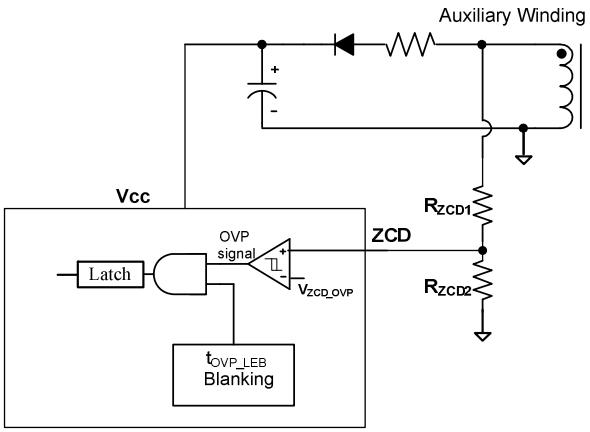


Figure 7: OVP Sampling Circuit

To avoid switch-off spikes mis-triggering OVP, OVP sampling has a t_{OVP_LEB} blanking period, as shown in Figure 8.

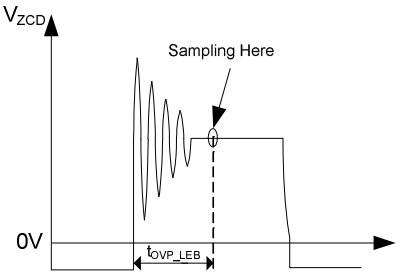


Figure 8: ZCD Voltage and OVP Sampling

Cycle by Cycle Current Limit

There is cycle by cycle current limit on the S pin, when the voltage on S pin reaches $V_{S_CLAMP_H}$ after a blanking time, the switching will be turn off to limit the peak current value.

Primary Over-Current Protection (OCP)

The S pin has an internally-integrated comparator for primary side OCP. When the gate is on, the comparator is enabled. Over-current occurs when VS exceeds V_{OCP} after a blanking time. The IC shuts down and restarts after VCC drops below UVLO. The OCP function block diagram is shown in Figure 9.

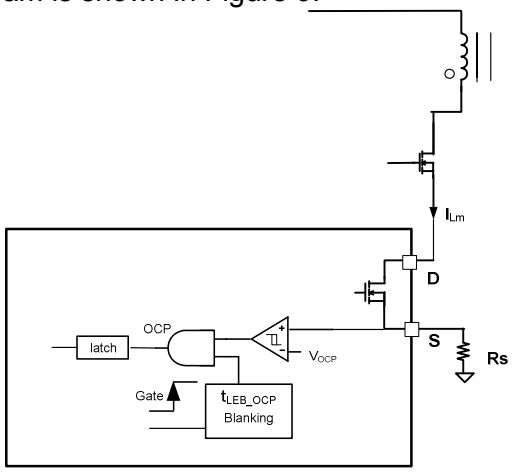


Figure 9: Over-Current Protection Circuit

LED Short Circuit Protection (SCP)

When the LED Short Circuit occurs, IC reduces the switching frequency to 7kHz. The output power at this condition is limited at a safe range.

ZCD Pin Short Circuit Protection

If ZCD pin voltage is less than V_{ZCD_SC} lasts longer than $t_{ZCD_SC_LEB}$, it is recognized as ZCD pin short circuit. The MP4033 stops the switching until VCC drops below UVLO and restarts. This prevents the components from over-voltage damage if LED load opens while ZCD pin shorts at the same time.

Thermal Shutdown

To prevent IC from thermal damage, the MP4033 latches off the switching cycle when the junction temperature is higher than 150°C. When the VCC drops below UVLO, it restarts again .

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2014 MPS. All Rights Reserved.

Adaptive Dimmer Type Detection

The MP4033 integrates adaptive dimmer type detection to accurately detect which kind of dimmer is connected at the system start-up, leading edge dimmer, trailing edge dimmer or no dimmer. The MP4033 works in different modes depending on these dimmer types to achieve the best dimmer compatibility at the highest performance.

Phase-Cut-Based Dimming Control

The MP4033 implements phase-cut-based dimming control (both for leading edge and trailing edge dimmers). For the leading edge dimmer, most of them are TRIAC-based.. The TRIAC dimmer usually consists of a bi-directional SCR and an adjustable turn on phase. Figure 10 shows the leading-edge TRIAC dimmer waveforms.

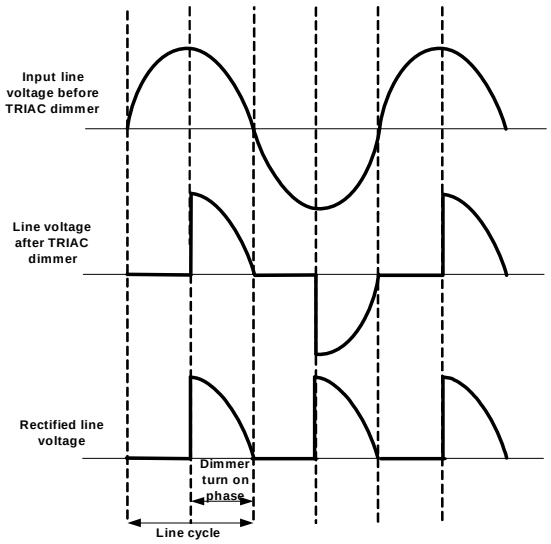


Figure 10: Leading Edge Dimmer Waveforms

For the Trailing edge dimmer, the waveforms are shown in Figure 11.

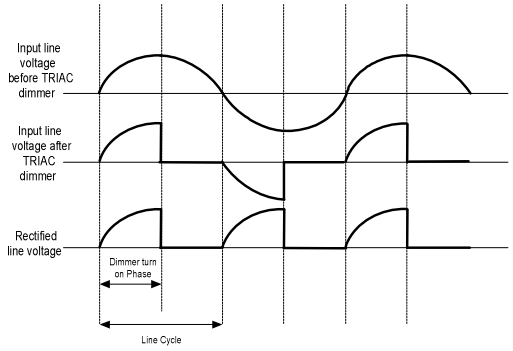


Figure 11: Trailing Edge Dimmer Waveforms

The MP4033 detects the dimming turn-on cycle through the MULT pin. Based on the turn-on cycle, the control circuitry adjusts the internal reference voltage. MULT voltage exceeding V_{MULT_ON} is recognized as a dimmer turn-on signal, MULT voltage below V_{MULT_OFF} is recognized as a dimmer turn-off signal. The MP4033 has a 30% line-cycle-detection blanking time at each line cycle, the real phase detector output added this blanking time to determine the reference voltage, if it is higher than 100%, the reference voltage is clamped to 100%. As shown in Figure**Error! Reference source not found.** 12. That means if the turn-on cycle exceeds 70% of the line cycle, the reference maintains the maximum value, which makes the maximum output current with different dimmers is almost the same with the rated output current.

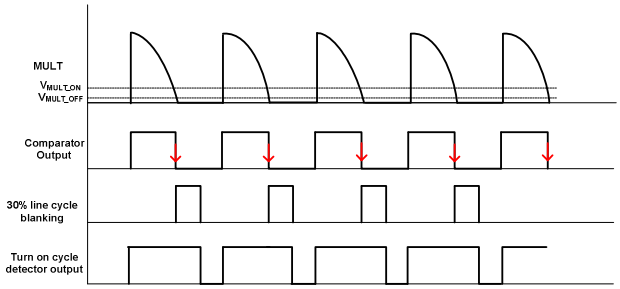


Figure12: Dimming Turn-On Cycle Detector

When the turn-on cycle decreases to less than 70% of the line cycle, the internal reference voltage decreases, lowering the output current. As the dimming turn-on cycle decreases, the COMP voltage also decreases. For leading edge dimmer, once the COMP voltage reaches V_{COMPL_LD}, it is clamped. The output current decreases slowly to maintain the TRIAC holding current and avoid random flicker. Figure **Error! Reference source not found.**13 shows the relationship between the leading edge dimming turn-on phase and output current.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2014 MPS. All Rights Reserved.

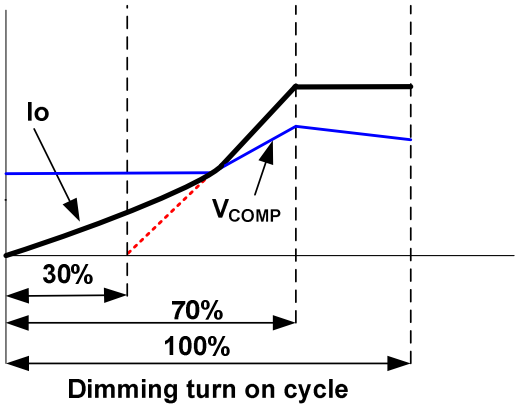


Figure 13: Leading Edge Dimming Curve

For trailing edge dimmer, there is no holding current, the COMP voltage is clamped at a lower level V_{COML_TL} to get deeper dimming depth. Figure 14 shows the relationship between the trailing edge dimming turn-on phase and output current.

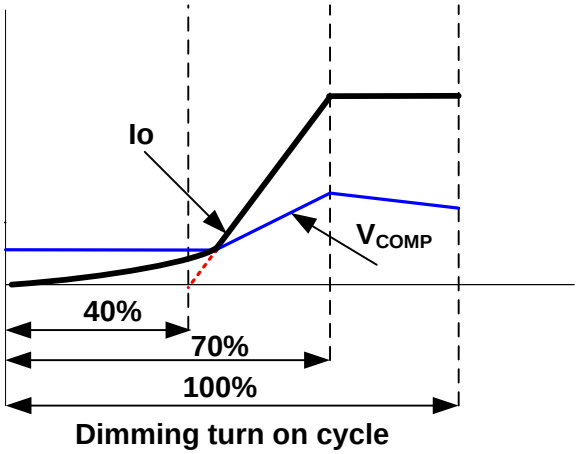


Figure 14: Trailing Edge Dimming Curve

Dimming Pull-Down Current Source

There are three kinds of dimming pull down current source in MP4033. The I_{DP_TL} current source is for trailing edge dimming, the other two (weak/strong) current sources are for leading edge dimming. The dimming pull down current is used to pull down the rectified line voltage to zero quickly to avoid any mis-detection on the MULT pin.

If the leading edge dimmer is detected, the dimming pull-down current source turns on when the MULT decreases to $V_{MULT_DP_ON_LD}$ and turns off until the MULT increases to $V_{MULT_DP_OFF_LD}$. If trailing edge dimmer is detected, the dimming pull-down current source turns on when the MULT decreases to $V_{MULT_DP_ON_TL}$ and turns off until the MULT increases to $V_{MULT_DP_OFF_TL}$.

The weak/strong dimming pull down current source is selected through different resistance on the ZCD pin. Figure 15 shows the selected logic:

If $I_{DP_DET_LD}$ *(R1+R2//R3)$\geqslant V_{EN_DP_STR_LD}$

Strong dimming pull-down current source is selected; otherwise, weak dimming pull down current source is selected.

In real application design, the weak/strong dimming pull down current selection is related to the detailed application SPEC.

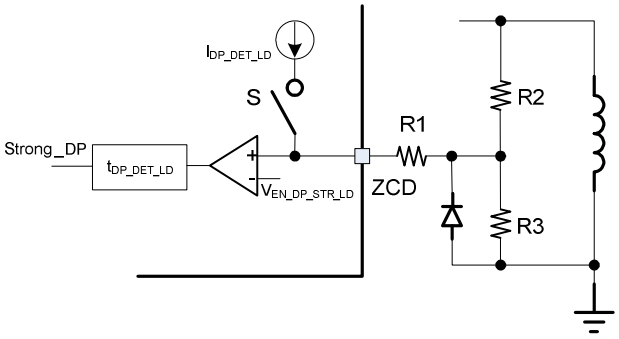


Figure 15: Weak/Strong Dimming Pull Down Current Source Selection

Damping Circuit Control

If a leading edge dimmer or trailing edge dimmer is detected, the damping circuit is enabled to limit the inrush current at the moment dimmer turns on. If no dimmer is detected, the damping circuit is disabled by pulling up the damp pin voltage so the damping resister is shorted by the damping MOSFET. The damp pin voltage begins to be pulled up if MULT voltage increases higher than $V_{MULT_DAMP_ON}$ and begins to be pulled down when MULT voltage decreases lower than $V_{MULT_DAMP_OFF}$. The maximum pull up current source is 100μA while the max pulling down current source is 400μA.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2014 MPS. All Rights Reserved.

Color Temperature and Brightness Control for Warm Sunset Dimming application

The color temperature and brightness control circuit is shown in Figure 16.

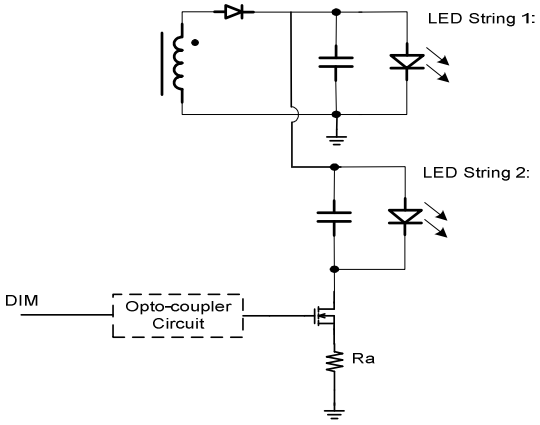


Figure 16: Color Temperature and Brightness Control Circuit

The DIM pin of MP4033 outputs a driving signal for external MOSFET. The DIM control logic is shown in Figure 17.

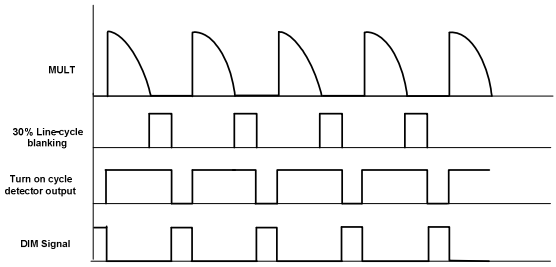


Figure 17: Dim Signal Logic

DIM turn-on signal is the compliment signal of the dimming turn-on signal. This means the longer the dimming turn-on cycle, the smaller the DIM turn-on cycle. When the dimming turn-on cycle is greater than 70%, the DIM stays low, and the output current flows only through the 1st LED string. As the dimming turn-on cycle decreases, the DIM turn-on duty cycle proportionally increases the 2nd LED string current. The total current through the 1st string and the 2nd string stays constant. This current balance achieves color temperature and brightness control. The maximum current through 2nd string is adjusted by changing the resistance of Ra.

Dimming Depth Enlargement

Driving a MOSFET to pull down a resistor from auxiliary winding to GND forms a dummy load, which to help distribute the output current. The DIM pin working timing makes the smaller dimming duty cycle is, the bigger dummy load distribution current is, the dimming depth is enlarged. The dimming depth enlargement circuit is shown in figure 18.

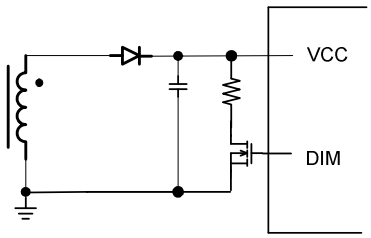


Figure 18: Dimming Depth Enlargement circuit

Programmable Thermal Fold-back (NTC)

The NTC pin is used as the LED programmable thermal fold-back. A NTC resistor is connected to this pin directly to monitor the LED temperature. The LED current changes as the voltage drops on NTC. Figure 19 shows the NTC curve.

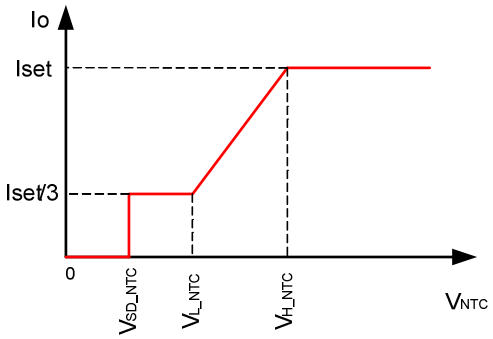


Figure 19: NTC Curve

If the voltage on the NTC pin is lower than the V_{SD_NTC}, the LED current drops to the minimum value, the minimum output current is determined by the minimum on time of the main MOSFET. (Equals to LEB time)

Analog Dimming with PWM Input

The MP4033 enables direct control of analog dimming. Applying a PWM signal (>200Hz) on NTC pin achieves analog dimming. The output current will linearly change with the PWM duty cycle from maximum to minimum. This feature dramatically reduces the BOM cost for the PWM dimming system.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2014 MPS. All Rights Reserved.

TYPICAL APPLICATION CIRCUITS

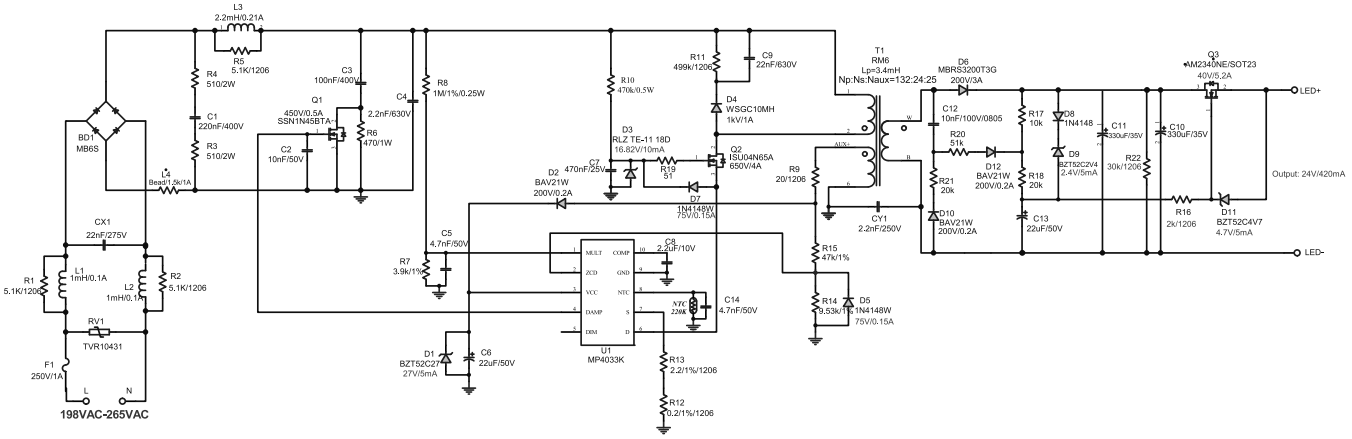


Figure 20: A19 Bulb Driver, 230VAC/50Hz Input, Isolated Flyback Converter, V_O =24V, I_O=420mA
EVB Model: EV4033-K-00A

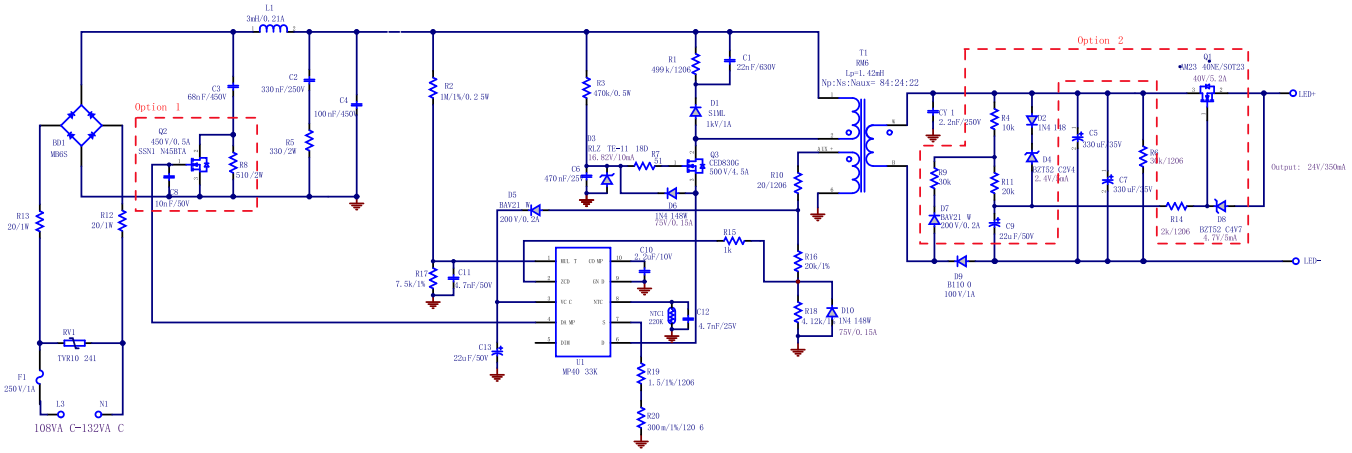
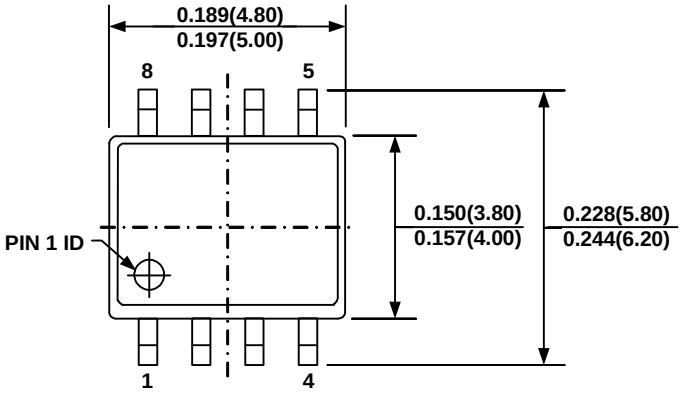


Figure 21: A19 Bulb Driver, 120VAC/60Hz Input, Isolated Flyback Converter, V_O =24V, I_O=350mA
EVB Model: EV4033-K-00B

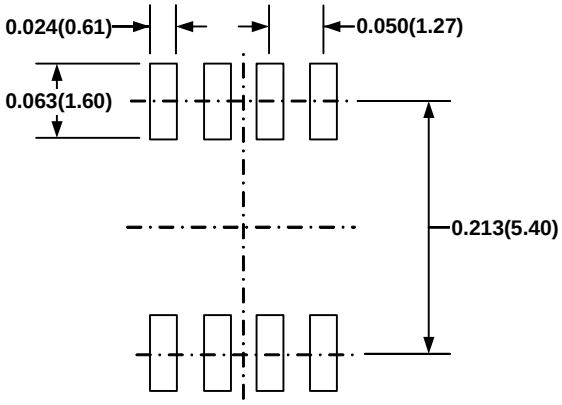
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2014 MPS. All Rights Reserved.

PACKAGE INFORMATION

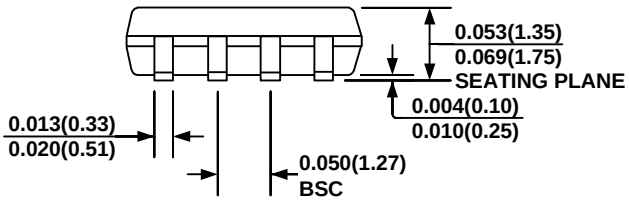
SOIC-8



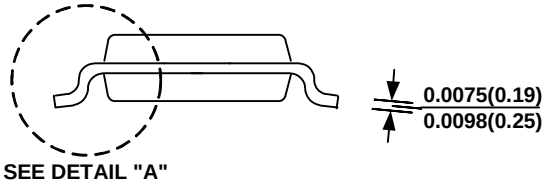
TOP VIEW



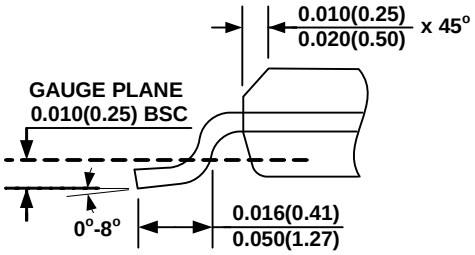
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW



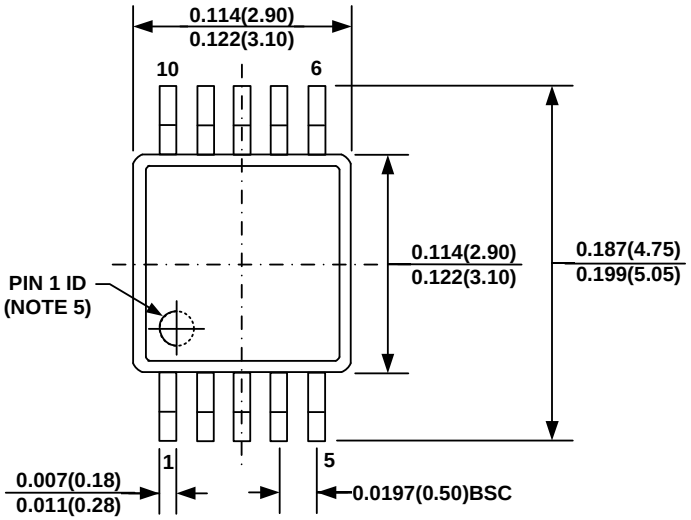
DETAIL "A"

NOTE:

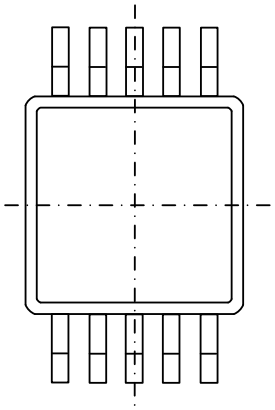
1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
5) DRAWING CONFORMS TO JEDEC MS-012, VARIATION AA.
6) DRAWING IS NOT TO SCALE.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2014 MPS. All Rights Reserved.

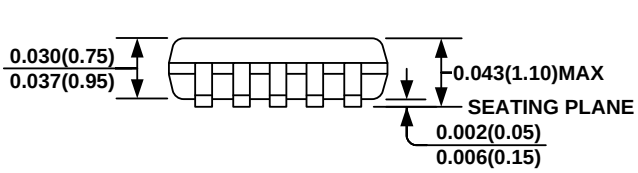
MSOP-10



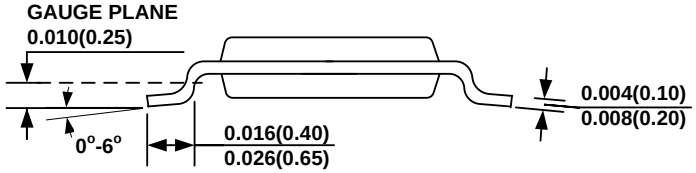
TOP VIEW



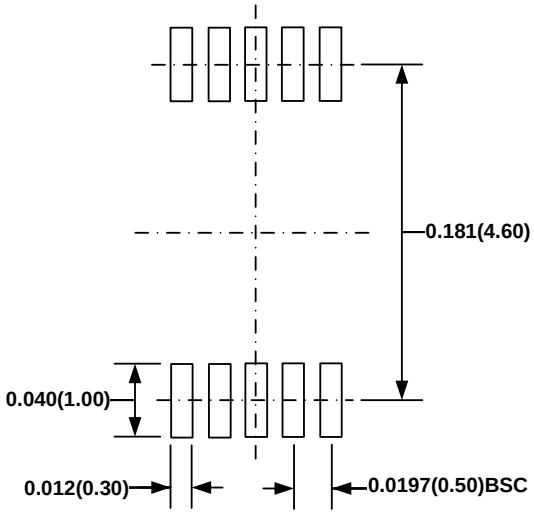
BOTTOM VIEW



FRONT VIEW



SIDE VIEW



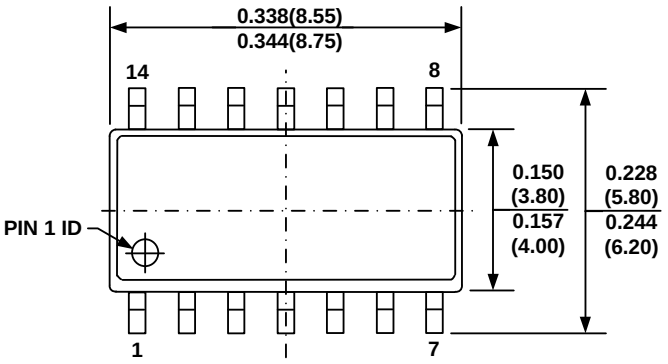
RECOMMENDED LAND PATTERN

NOTE:

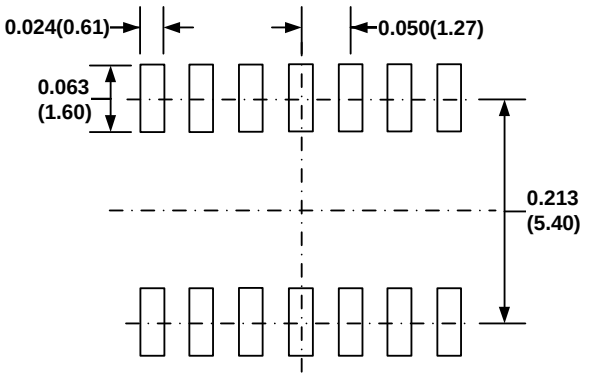
1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
5) PIN 1 IDENTIFICATION HAS THE HALF OR FULL CIRCLE OPTION.
6) DRAWING MEETS JEDEC MO-817, VARIATION BA.
7) DRAWING IS NOT TO SCALE.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2014 MPS. All Rights Reserved.

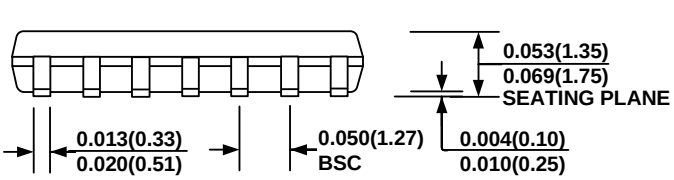
SOIC-14



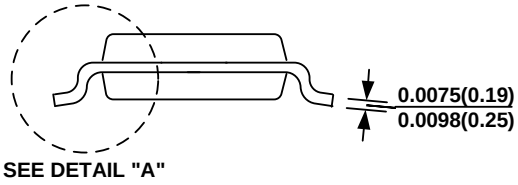
TOP VIEW



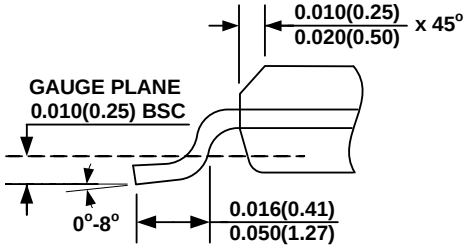
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW



DETAIL "A"

NOTE:

1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
5) DRAWING CONFORMS TO JEDEC MS-012, VARIATION AB.
6) DRAWING IS NOT TO SCALE.

NOTICE: The information in this document is subject to change without notice. Users should warrant and guarantee that third party Intellectual Property rights are not infringed upon when integrating MPS products into any application. MPS will not assume any legal responsibility for any said applications.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2014 MPS. All Rights Reserved.