MP4068

Non-Isolated,TRIAC Dimmable PFC LED Driver for 120VAC, Up to 10W LEDs

The Future of Analog IC Technology

DESCRIPTION

The MP4068 is a highly integrated TRIAC dimmable LED driver with a high power factor (PF). It regulates precisely LED current in non-isolated lighting applications. Only a single winding inductor is required to realize the solution. For low-line (120VAC) applications, the integrated 500V MOSFET ensures that the system can withstand a 500V surge test without MOV or TVS. It features MPS' proprietary hybrid operation mode, which is designed to achieve good dimming performance. The MP4068 is designed specifically for low-line input (120VAC) and TRIAC dimmable LED lighting applications, especially for low cost and small form factor applications.

The accurate output LED current is achieved by an internal averaging current feedback loop. An internal high-voltage regulator makes the MP4068 start-up quickly without a perceptible delay. The power de-rating at high temperature makes the system flicker-free when the ambient temperature is high.

The MP4068 has protection features such as VCC under-voltage lockout (UVLO), over-voltage protection (OVP), and short-circuit protection (SCP). All of these features make MP4068 an ideal solution for simple, off-line, and non-isolated TRIAC dimmable LED lighting applications.

The MP4068 is available in SOIC8-7A and SOIC-8 EP packages.

FEATURES

- Excellent TRIAC Dimming Performance
- Lowest Cost BOM
- Constant Current LED Driver
- Integrated 500V MOSFET
- Internal HV Fast Start-Up
- Single Winding Inductor
- High Power Factor(>0.7)
- Good LED Current Accuracy
- Supports Buck/Buck-Boost Topology
- LED Current Foldback at High Temperature
- Thermal Shutdown (Auto Re-Start with Hysteresis)
- VCC Under-Voltage Lockout with Hysteresis (UVLO)
- Programmable Over-Voltage Protection
- Output Short-Circuit Protection
- Available in SOIC8-7A/SOIC-8 EP Packages

APPLICATIONS

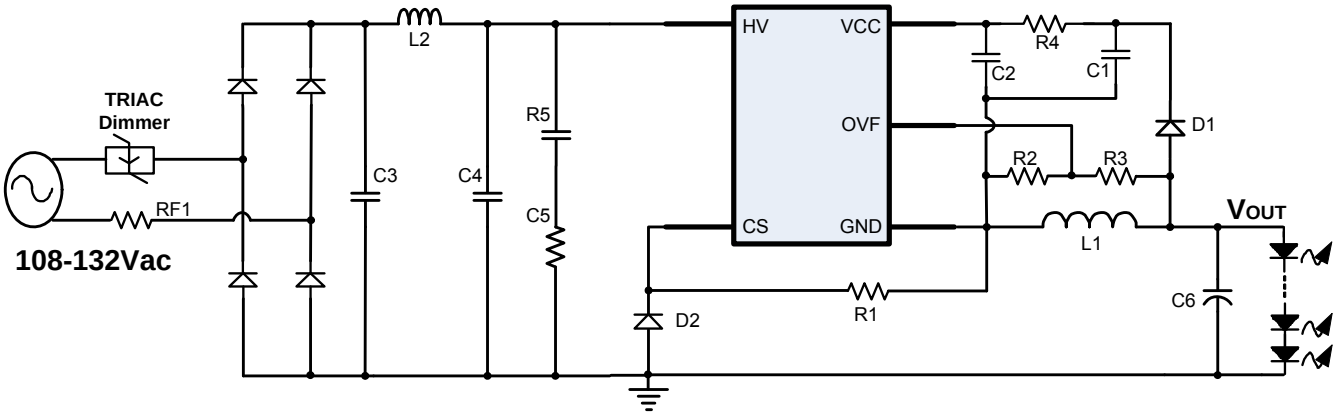
- 120VAC, Up to 10W LED Lighting
- Residential and Commercial Lighting
- TRIAC Dimmible LED Lighting, A19, GU10, PAR Lamps

All MPS parts are lead-free, halogen free, and adhere to the RoHS directive. For MPS green status, please visit MPS website under Quality Assurance.

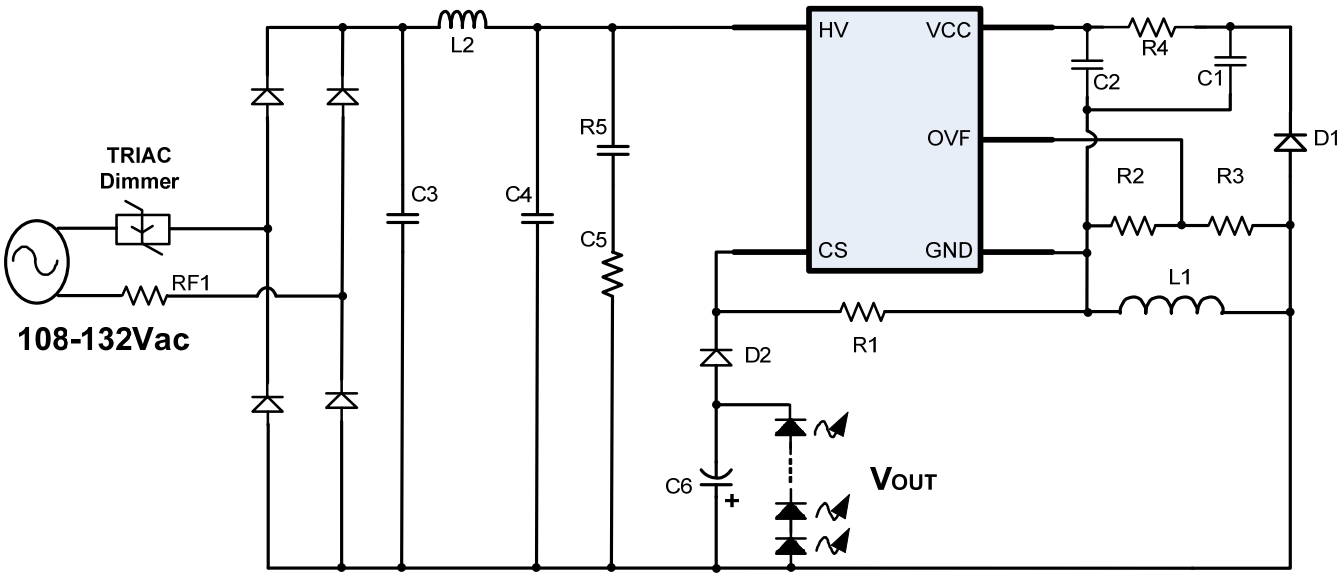
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TYPICAL APPLICATION (BUCK)



TYPICAL APPLICATION (BUCK-BOOST)



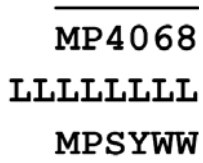
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ORDERING INFORMATION

Part Number	Package	Top Marking
MP4068GN*	SOIC-8 EP	*See Below*
MP4068GS**	SOIC8-7A	*See Below*

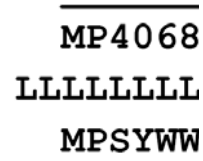
* For Tape & Reel, add suffix –Z (e.g. MP4068GN–Z)
** For Tape & Reel, add suffix –Z (e.g. MP4068GS–Z)

TOP MARKING (MP4068GN)



MP4068: product code of MP4068GN;
LLLLLLLL: lot number;
MPS: MPS prefix;
Y: year code;
WW: week code;

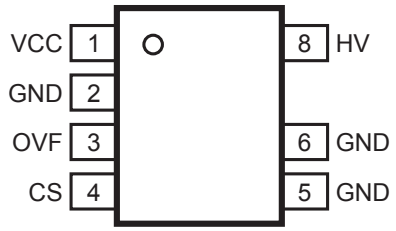
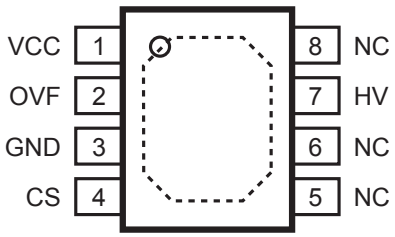
TOP MARKING (MP4068GS)



MP4068: product code of MP4068GS;
LLLLLLLL: lot number;
MPS: MPS prefix;
Y: year code;
WW: week code;

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PACKAGE REFERENCE

TOP VIEW	TOP VIEW
	
SOIC8-7A	**SOIC-8 EP**

ABSOLUTE MAXIMUM RATINGS (1)

HV to CS .....-0.3V to 500V
VCC, CS to GND .....-0.3V to6.5V
OVF to GND .....-0.7V to 6.5V
Source Current on OVF 4mA
Continuous Power Dissipation (T_A = +25°C) **(2)**
SOIC8-7A 1.6W
SOIC-8 EP 2.6W
Lead Temperature .....260°C
Storage Temperature..... -60°C to +150°C
ESD Capability Human Body Mode..... 2.0kV
CDM ESD Capability..... 2.0kV

Recommended Operating Conditions (3)

Operating VCC Range.....4.1V to 5V

Thermal Resistance (4)

	θ_{JA}	θ_{JC}	
SOIC8-7A	76	35	°C/W
SOIC-8 EP	48	10	°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

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ELECTRICAL CHARACTERISTICS

Typical values are VCC =5V, T_J = 25°C, unless otherwise noted.

Minimum and maximum values are at VCC =5V, T_J = -40°C to +125°C, unless otherwise noted, guaranteed by characterization.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Start-Up Current Source (HV)						
Internal Regulator Supply Current	$I_{REGULATOR}$	VCC=0V;V_{HV}=100V	3.8	5	6.1	mA
Leakage Current from HV	I_{HV_LKG}	VCC=5V;V_{HV}=400V		14	22	µA
Supply Voltage Management (VCC)						
VCC Upper Threshold for Internal Regulator Turn-Off	VCC_{OFF}	VCC Rising Edge	4.3	4.65	5	V
VCC Lower Threshold for Internal Regulator Turn-On	VCC_{ON}	VCC Falling Edge	4.10	4.40	4.75	V
VCC Hysteresis between Regulator On/Off	VCC_{HYS}		0.15	0.24	0.32	V
VCC Lower Threshold for IC Shutdown	VCC_{STOP}	VCC Falling Edge	3.0	3.4	3.8	V
VCC Hysteresis between Regulator Off/IC Shutdown	$VCC_{HYS-STOP}$		0.93	1.25	1.60	V
VCC Lower Threshold at which the Protection Phase Ends	VCC_{PRO}	VCC Falling Edge	1.90	2.35	2.80	V
Internal IC Consumption	I_{CC}	VCC=4.6V, fsw=63kHz, D=56%		350	400	µA
Internal IC Consumption, Latch-Off Phase	I_{CC_LATCH}	VCC=5V		18	32	µA
Internal MOSFET (HV to CS)						
Breakdown Voltage	V_{BR}		500			V
On-State Resistance	R_{ON}	I_{HV}=10mA, T_J =25°C		8.5	12	Ω
		VCC= VCC_{STOP} +50mV, I_D=10mA, T_J =25°C		8.5	12	Ω
Current Sampling Management (CS)						
Peak Current Limit at Normal Operation	V_{LIMIT}		0.40	0.46	0.52	V
Leading Edge Blanking	t_{LEB}			200		ns
Feedback Threshold to Turn On MOSFET	V_{REF}		0.186	0.195	0.204	V
Minimum Off-Time Limitation at Normal Operation	t_{OFF_MIN}		5.4	7	8.5	µs

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ELECTRICAL CHARACTERISTICS *(continued)*

Typical values are VCC =5V, T_J = 25°C, unless otherwise noted.

Minimum and maximum values are at VCC =5V, T_J = -40°C to +125°C, unless otherwise noted, guaranteed by characterization.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Maximum On-Time Limitation	t_{ON_MAX}		6.7	9	11.5	µs
Ratio of Max_on/Min_off	σ		1.09	1.29	1.5	
Protection Input (OVF)						
Threshold to Trigger OVP	V_{OVP}		1.89	2.0	2.15	V
Time Constraint on OVP Comparator	t_{OVP}			21	32	µs
Thermal Protection						
Power De-Rating Threshold (5)	T_{START}			145		°C
Thermal Shutdown Threshold (5)	T_{SD}			160		°C
Thermal Shutdown Recovery Hysteresis (5)	T_{HYS}			50		°C

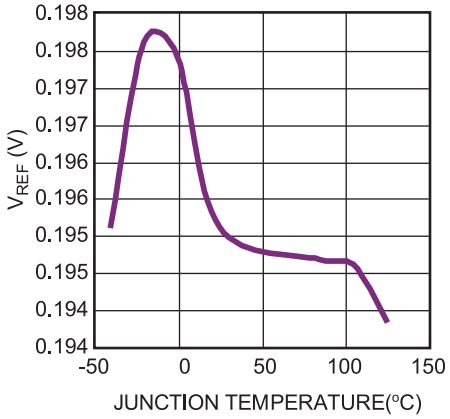
Notes:

5) Guaranteed by characterization.

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TYPICAL CHARACTERISTICS

Reference Voltage vs. Junction Temperature



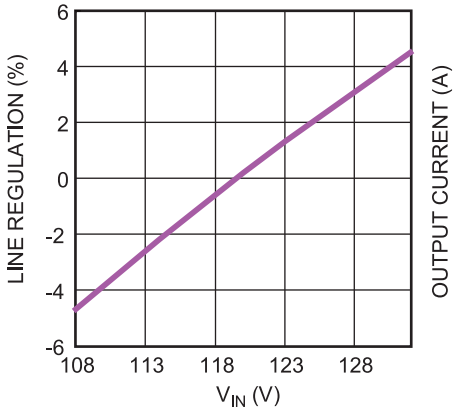
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TYPICAL PERFORMANCE CHARACTERISTICS

Performance waveforms are tested on the evaluation board of the Design Example section.
V_{IN} = 120VAC, V_{OUT} = 50V, I_{OUT}=160mA, L = 1mH, T_A = 25°C, unless otherwise noted.

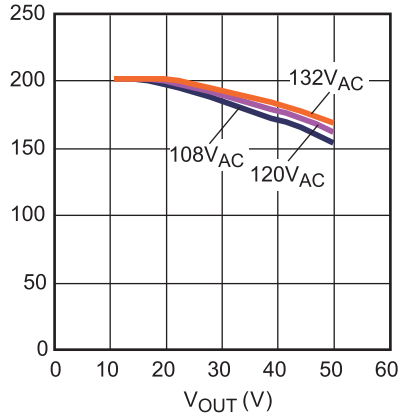
Line Regulation

V_{IN}=(108-132)V_{AC}/60Hz, Full Load



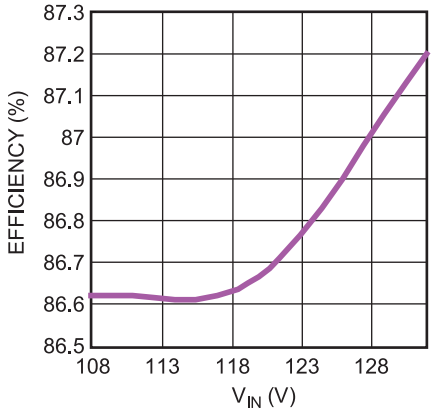
Load Regulation

V_{IN}=(108-132)V_{AC}/60Hz



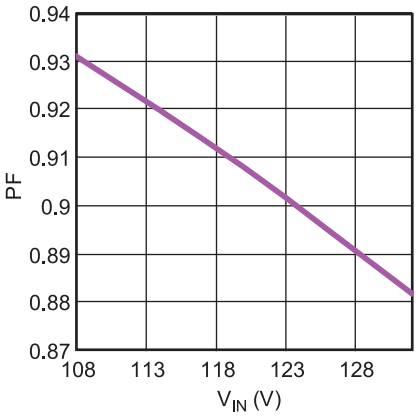
Efficiency

V_{IN}=(108-132)V_{AC}/60Hz, Full Load



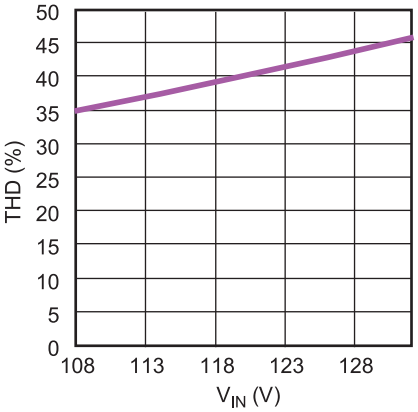
PF vs. V_{IN}

V_{IN}=(108-132)V_{AC}/60Hz, Full Load



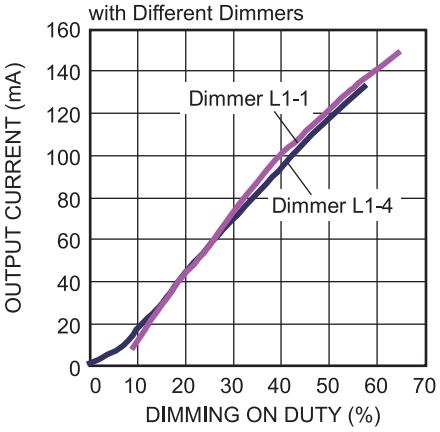
THD vs. V_{IN}

V_{IN}=(108-132)V_{AC}/60Hz, Full Load



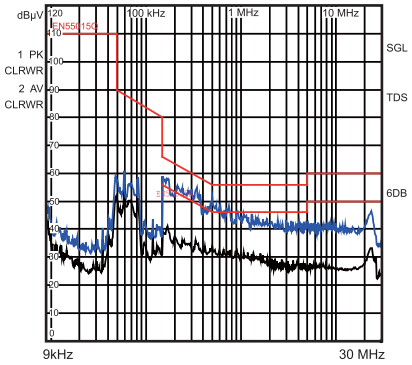
Dimming Curve

V_{IN}=120V_{AC}/60Hz, Full Load,
with Different Dimmers



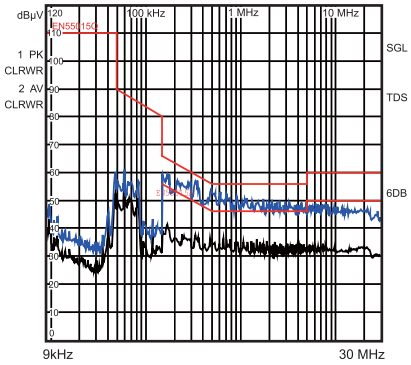
Conducted EMI, L-Line

V_{IN}=115V_{AC}, RBW=9kHz, MT=20ms



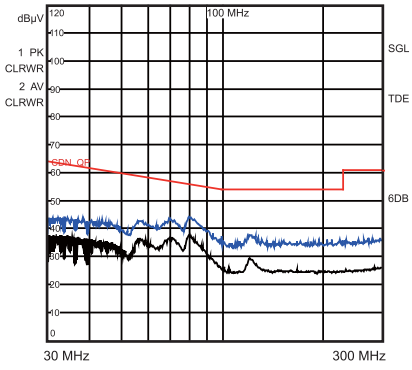
Conducted EMI, N-Line

V_{IN}=115V_{AC}, RBW=9kHz, MT=20ms



CDN Test

V_{IN}=115V_{AC}, RBW=120kHz, MT=1ms



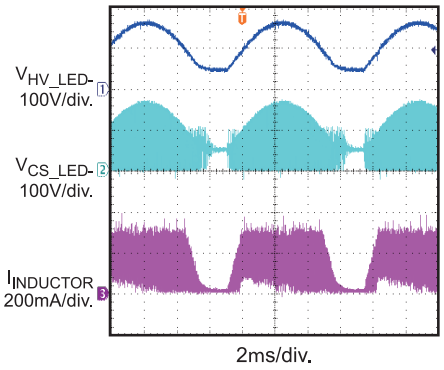
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TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board of the Design Example section.
V_{IN} = 120VAC, V_{OUT} = 50V, I_{OUT}=160mA, L = 1mH, T_A = 25°C, unless otherwise noted.

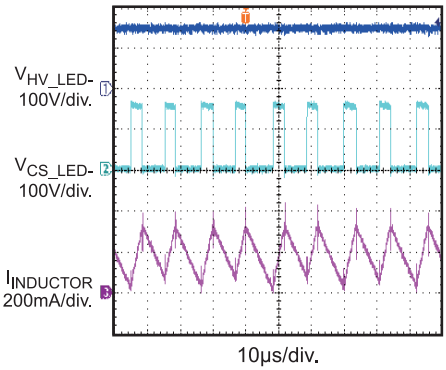
Steady State

V_{IN}=120V_{AC}/60Hz, Full Load



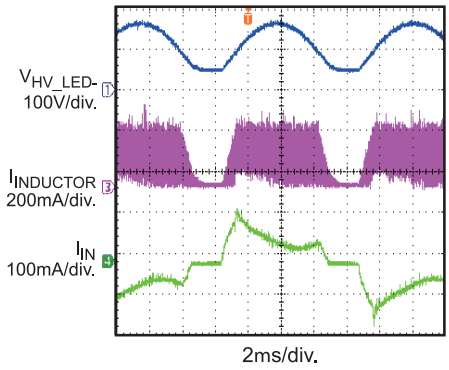
Steady State

V_{IN}=120V_{AC}/60Hz, Full Load

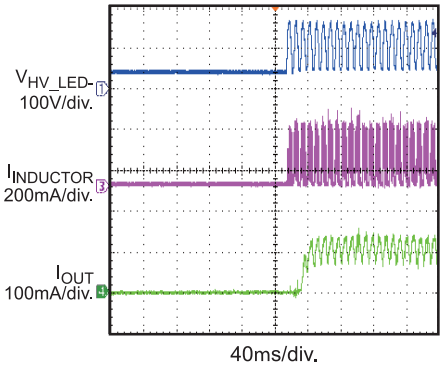


Steady State

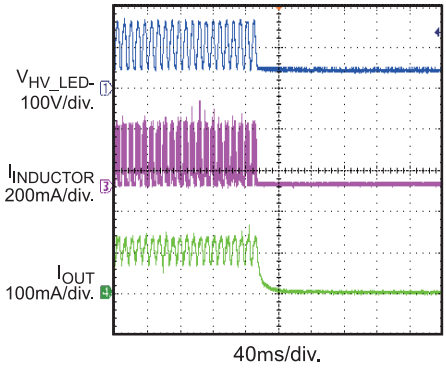
V_{IN}=120V_{AC}/60Hz, Full Load



V_{IN} Start-Up

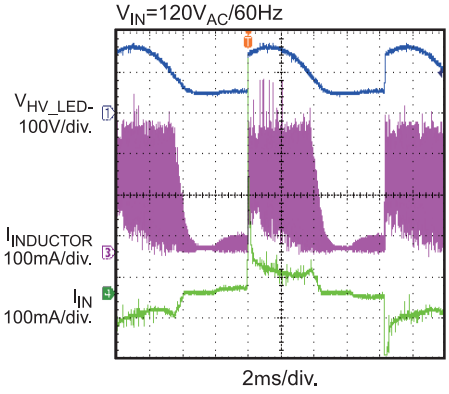


V_{IN} Shutdown



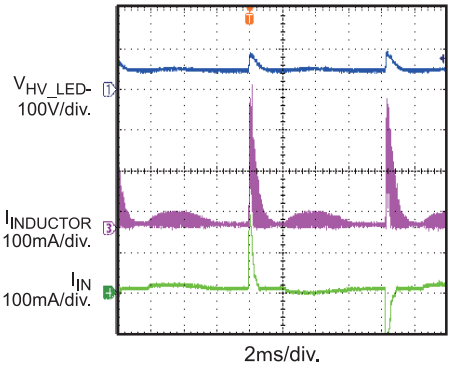
Dimming Performance

Max Dmming on Phase
with Leading-Edge Dimmer
V_{IN}=120V_{AC}/60Hz



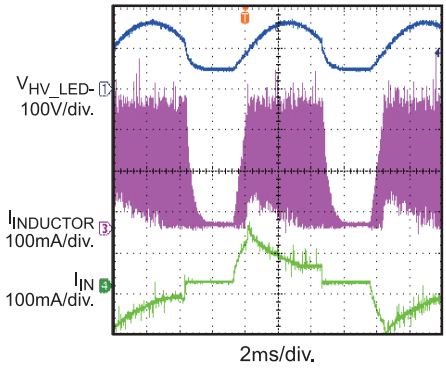
Dimming Performance

Min Dmming on Phase
with Leading-Edge Dimmer
V_{IN}=120V_{AC}/60Hz



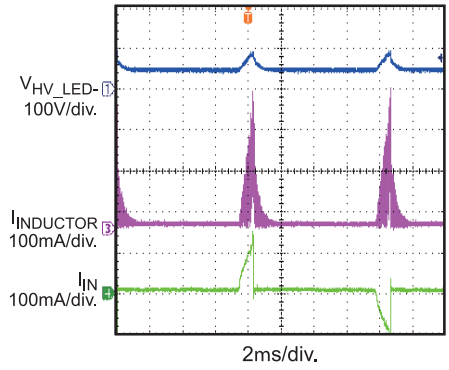
Dimming Performance

Max Dmming on Phase
with Trailing-Edge Dimmer
V_{IN}=120V_{AC}/60Hz



Dimming Performance

Min Dmming on Phase
with Trailing-Edge Dimmer
V_{IN}=120V_{AC}/60Hz



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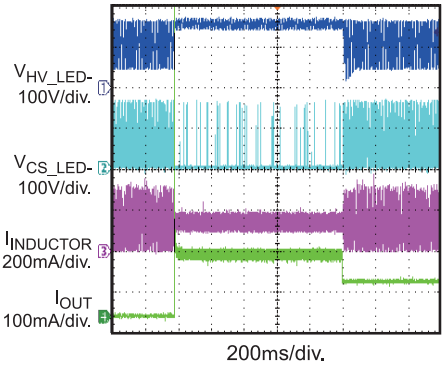
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board of the Design Example section.
V_{IN} = 120VAC, V_{OUT} = 50V, I_{OUT}=160mA, L = 1mH, T_A = 25°C, unless otherwise noted.

SCP

LED+ short to LED- and then Recovery

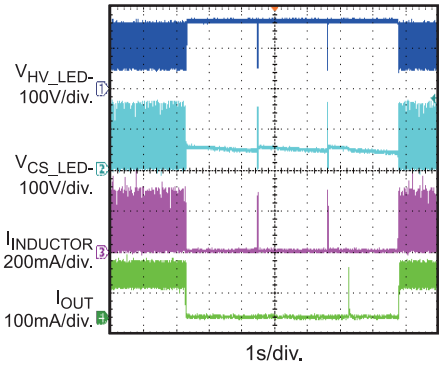
V_{IN}=120V_{AC}/60Hz, Full Load



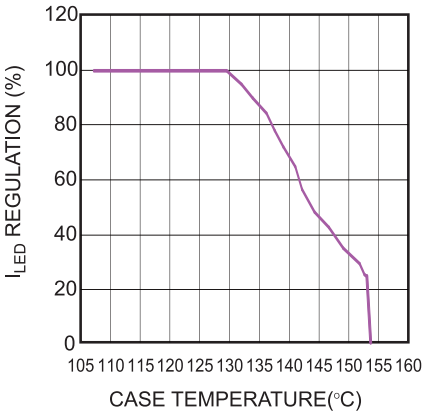
OVP

LED Load Open then Recovery

V_{IN}=120V_{AC}/60Hz, Full Load



Output Current Thermal Foldback Curve



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PIN FUNCTIONS

Pin # SOIC8-7A	Pin # SOIC-8 EP	Name	Description
1	1	VCC	**Power Supply**. Supply power for all the control circuits. Typically, connect VCC to an external 2.2uF capacitor.
2,5,6	3	GND	**Ground**. Virtual Ground of the IC.
3	2	OVF	**Output Voltage Feedback**. The over-voltage condition is detected on OVF. When the voltage on OVF exceeds the V_{OVP} (after a blanking time), the OVP is triggered, and the chip shuts down.
4	4	CS	**Current Sense of the Internal Power MOSFET**. Connect a resistor from CS to GND to sense the current through the inductor. When the voltage on CS exceeds 0.46V, the internal MOSFET is turned off. If the start-up time exceeds the maximum on time (9us), the internal MOSFET is turned off (even though the voltage on CS has not reached 0.46V).
8	7	HV	**High-Voltage Input of the Internal Power MOSFET**. HV is also the input of the internal high-voltage current source.
	5,6,8	NC	**No Connection**. Do NOT connect.

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BLOCK DIAGRAM

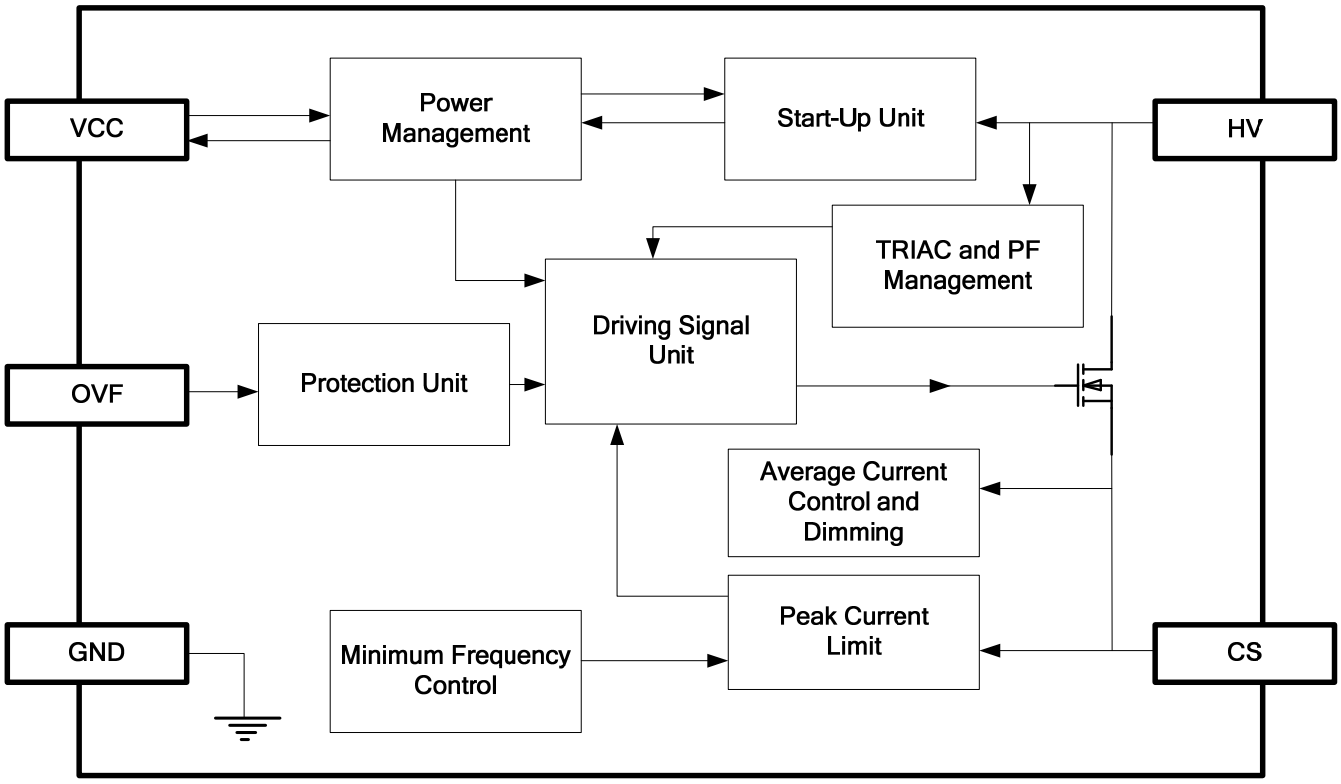


FIGURE 1. Functional Block Diagram

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OPERATION

The MP4068 is a highly integrated and cost-effective TRIAC dimmable LED driver with a high power factor (PF). Minimal external components make the MP4068 a competitive IC in low-line (120VAC) input, non-isolated applications, especially for small form factor applications. Hybrid operation mode achieves both good dimming performance and an accurate output current. The power factor is higher than 0.7 in most applications to eliminate the harmonic pollution on AC line. The integrated high-voltage regulator enables fast start-up without any perceptible delay. The power de-rating function at high temperatures protects the IC from thermal damage.

Hybrid Operation Mode

To achieve smooth TRIAC dimming performance, the MP4068 implements an MPS proprietary hybrid operation mode, in which the IC self-adjusts the internal PWM control mode between CCM and DCM during different times of the AC cycle. The hybrid operation mode actively maintains the latching current and holding current of the leading edge TRIAC, and it enables good power factor.

Also, the hybrid operation mode achieves the small dimming duty condition. The IC works in CCM during the entire dimming on time when the dimmer is set to a small dimming duty. The higher and smoother input current achieves excellent dimming performance.

Power Supply

The IC is self supplied by the internal high-voltage regulator (which is drawn from the drain). The IC starts switching and the internal high-voltage regulator turns off as soon as the voltage on VCC reaches VCC_{OFF} (4.65V, typically). When the voltage on VCC falls below VCC_{ON} (4.4V, typically), the internal high-voltage regulator turns on again to charge the external VCC capacitor. A small capacitor (several μF) is recommended. In TRIAC dimming applications, the internal high-voltage regulator works only when the dimmer is on and cannot afford enough power supply for the chip, so an external charging circuit is recommended (see Fig. 2).

When the voltage on VCC drops below VCC_{STOP} (3.4V, typically), the IC stops working, and the internal high-voltage regulator re-charges the VCC capacitor.

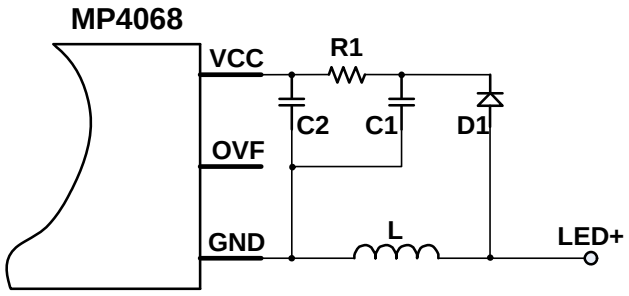


FIGURE 2. VCC Charging Circuit

When OVP occurs, the MP4068 stops working, and an 18μA internal current source discharges the VCC capacitor. After VCC drops below VCC_{PRO} (2.35V, typically), the internal high-voltage regulator re-charges the VCC capacitor again. The re-start time can be calculated by the following equation:

$$t_{restart} = C_{Vcc} \times \frac{Vcc - 2.35V}{18\mu A} + C_{Vcc} \times \frac{4.65V - 2.35V}{5mA}$$

Fig. 3 shows the typical waveform with VCC under-voltage lockout.

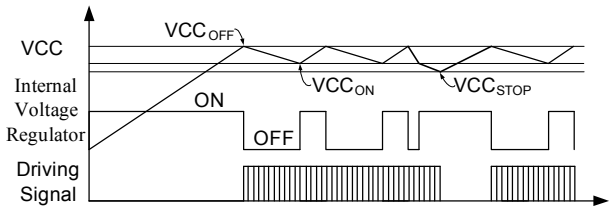


FIGURE 3. VCC Under-Voltage Lock Out (UVLO)

Constant Current Operation

The MP4068 is a highly integrated driver. The internal feedback logic responds to the internal sample and hold circuit to achieve constant output-current regulation. The voltage of the internal sampling capacitor (V_{FB}) is compared to the internal reference (0.195V). When the sampling capacitor voltage (V_{FB}) falls below the reference voltage (which indicates an insufficient output current), the integrated MOSFET is

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turned on. The on period is determined by the peak current limit. After the on period elapses, the integrated MOSFET is turned off (see Fig. 4).

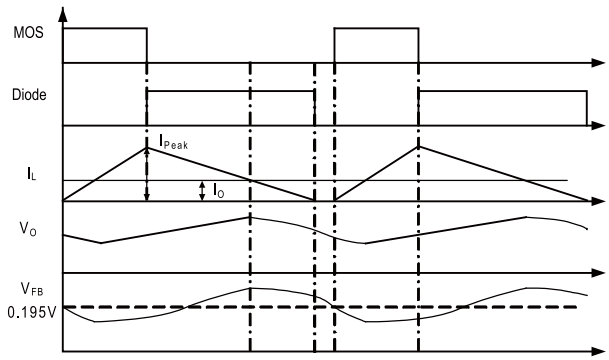


FIGURE 4. V_{FB} vs I_{OUT}

By monitoring the internal sampling capacitor voltage, the output current can be regulated. The output current is determined by the following equation:

$$I_O = \frac{0.195V}{R1}$$

The peak current can be calculated as follows:

$$I_{Peak} = \frac{0.46V}{R1}$$

Where R1 is the sense resistor.

Minimum Operating Frequency Limit

The MP4068 incorporates a minimum operating frequency (22kHz) to eliminate audible noise when the frequency is less than 20kHz.

When the operating frequency is less than 22kHz, the internal peak current regulator will decrease the peak current value to keep the operating frequency constant (about 22kHz).

Minimum Off-Time Limit

A minimum off-time limit is implemented. During normal operation, the minimum off-time limit is 7μs. During the start-up period, the minimum off-time limit is shortened gradually from 24μs to 12μs to 7μs (see Fig. 5). Each minimum off time maintains a 32 switching cycle. This soft-start function enables a safe start-up.

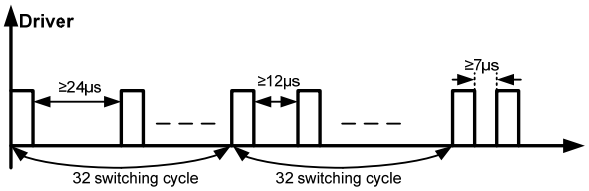


FIGURE 5. t_{minoff} at Start-Up

Thermal Protection (TSD)

To prevent the IC and system from thermal damage, the MP4068 reduces the reference to decrease the output current. This limits the temperature rising speed of the IC when the junction temperature exceeds 145°C. Typically, the output current drops to around 20% when the IC temperature rises to 160°C. Once the junction temperature exceeds 160°C, the MP4068 shuts down the switching cycle. As soon as the junction temperature drops below 110°C, the power supply resumes operation. During the thermal shutdown condition, the VCC is discharged to VCC_{PRO}, and then it is re-charged by the internal high-voltage regulator.

Over-Voltage Protection (OVP)

When the MOSFET turns off, if V_{OVF} is higher than V_{OVP}, the MP4068 stops working, and a re-start cycle begins. When OVP occurs, the chip works in hiccup mode; the MP4068 monitors the OVF voltage continuously, and the VCC voltage discharges and re-charges repeatedly. The MP4068 resumes operation once the fault disappears.

Short-Circuit Protection (SCP)

When an LED short circuit occurs, the switching off time is extended. Due to the minimum operating frequency limit, the IC reduces automatically the switching frequency and achieves close loop control. Then the output power at this condition is limited at a safe range. The MP4068 resumes working in normal operation once the short circuit is released.

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Leading Edge Blanking (LEB)

There are parasitic capacitances in the circuit which can cause a high-current spike during the turn-on period of the internal MOSFET. In order to avoid premature termination of the switching pulse, an internal leading edge blanking (LEB) unit is employed. During the blanking time, the current comparator is disabled and blocked from turning off the internal MOSFET (see Fig. 6).

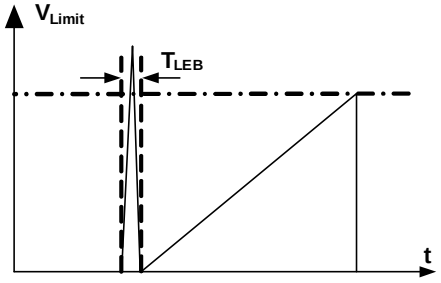


FIGURE 6. Leading Edge Blanking (LEB)

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APPLICATION INFORMATION

Component Selection

Inductor

The MP4068 has a minimum off-time limit. The inductor current ripple at CCM is determined by the inductor value and the minimum off-time limit. The current ripple is limited to 80% to get a tradeoff between the PF and dimming performance. The inductance value can be calculated as follows:

$$L = \frac{V_O \times t_{OFF_MIN}}{0.8 \times I_{peak}}$$

If the inductance value is too large, the switching frequency will be low, so the EMI performance will be good, however, the TRIAC dimming performance will be poor at this condition. If the inductance value is too small, the TRIAC dimming performance will be good, but the system may work in open loop condition, the current consistency will be bad. So a tradeoff must be made.

Freewheeling Diode

The diode should have a maximum reverse-voltage rating, which is greater than the maximum input voltage. The current rating of the diode is determined by the output current, which should be larger than 1.5 to 2 times the output current.

Slow diodes cause excessive leading edge current spikes during start-up, which is not acceptable. Long reverse-recovery time of the freewheeling diode can also affect the efficiency and the circuit operation. An ultrafast diode (t_{rr}<75ns) such as WUGC10JH or ES1G is recommended.

Over-Voltage Protection Point Set

A feedback resistor is used to detect an over-voltage condition. Fig. 7 shows the feedback resistor's connection.

The MP4068 is integrated with over-voltage protection. The maximum output voltage when over-voltage protection is triggered can be calculated with the following equation:

$$V_{O_MAX} = V_{OVP} * \frac{R2 + R3}{R2} - V_D$$

Where V_D is the freewheeling diode forward voltage drop.

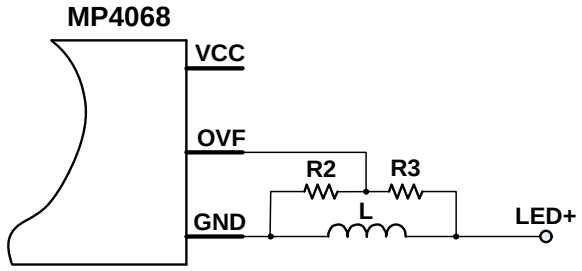


FIGURE 7. Feedback Resistor Connection

The upper feedback resistor (R3) should be larger than 100kΩ to avoid an efficiency reduction in application. A 1% tolerance type is recommended to achieve accurate protection.

Dummy Load

The dummy load is used to consume the power transferred to the output capacitor when over-voltage protection occurs. The IC works in hiccup mode without any power consumption.

Normally, a dummy load less than 1mA is recommended, which will not deteriorate the system efficiency but can guarantee normal over-voltage protection.

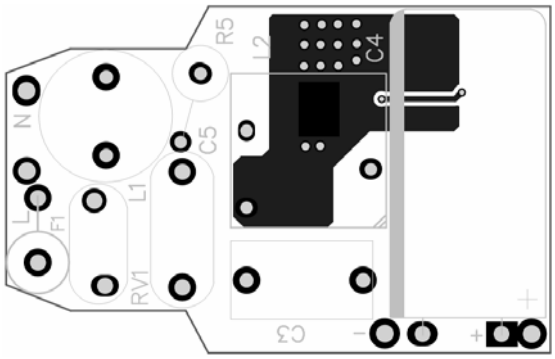
PCB Layout Guidelines

Efficient PCB layout is critical to achieve stable operation, good EMI, and good thermal performance, especially in very small sized LED applications. For best results, refer to Fig. 8 and follow the guidelines below:

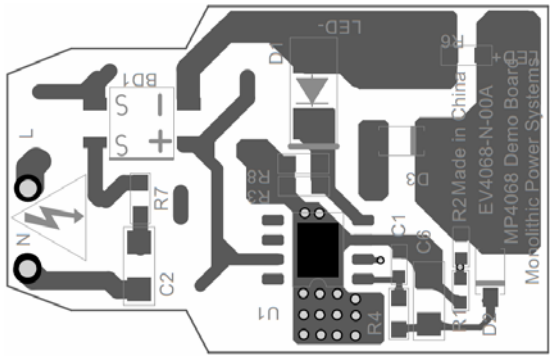
1. Keep the loop formed between the MP4068, the inductor, the freewheeling diode, and the output capacitor as small as possible for better EMI.
2. Place the AC input far away from the switching nodes to minimize the noise coupling that may bypass the input filter.
3. The VCC capacitor should be located very close to the VCC and GND.

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4. Place the feedback resistor as close to OVF as possible to minimize the feedback sampling loop in order to minimize the noise coupling route.
5. With buck topology, since CS and GND are switching nodes, the copper area connected to these pins should be small to improve EMI performance. Also, GND is used as a heat-sink; a large copper area GND can improve thermal performance, so you must make a tradeoff between EMI and thermal performance.



Top Layer



Bottom Layer

FIGURE 8. Recommended PCB Layout

Design Example

Below is a design example following the application guidelines based on the following specifications:

TABLE 1. Design Example

V_{IN}	108Vac~132Vac
V_{OUT}	50V
I_{OUT}	160mA

Fig. 9 shows the detailed application schematic. This circuit is used for the typical performance and circuit waveforms. For more device applications, please refer to the related evaluation board datasheets.

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TYPICAL APPLICATION CIRCUITS

Fig. 9 shows a typical application example of a 50V, 160mA, non-isolated buck topology power supply using the MP4068.

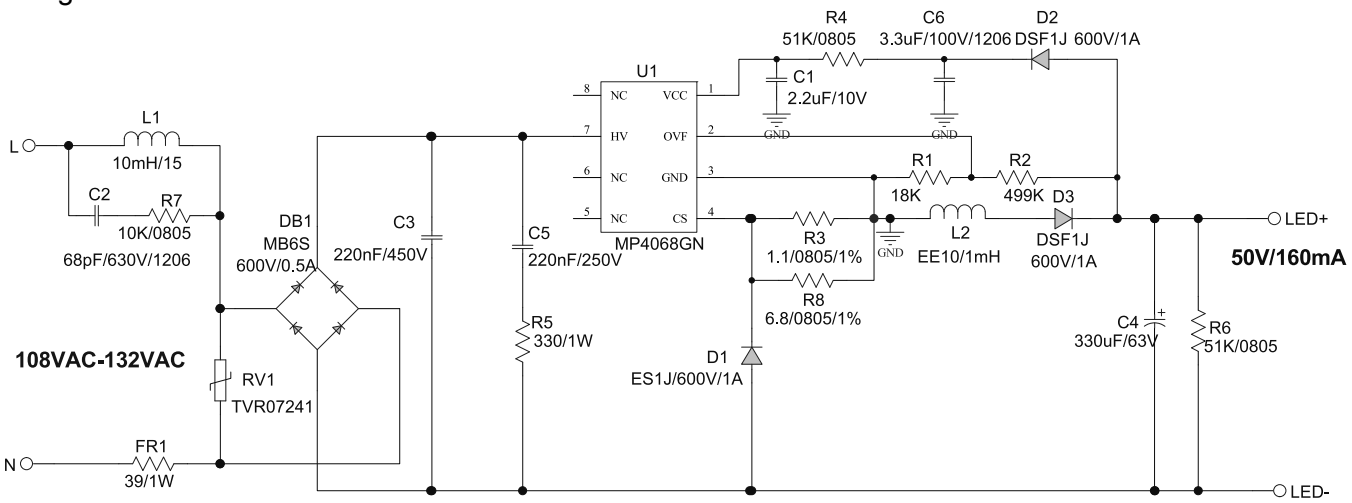
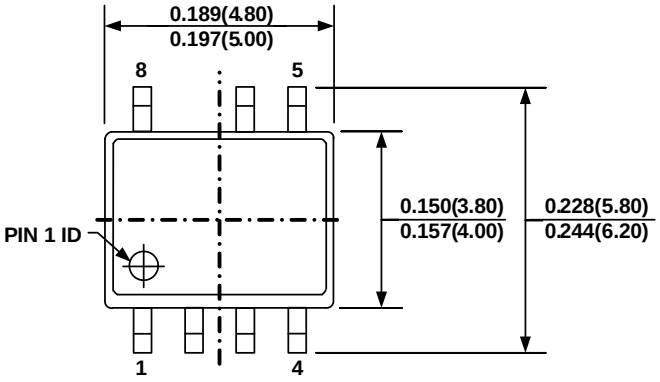


FIGURE 9. Typical Buck Converter Application

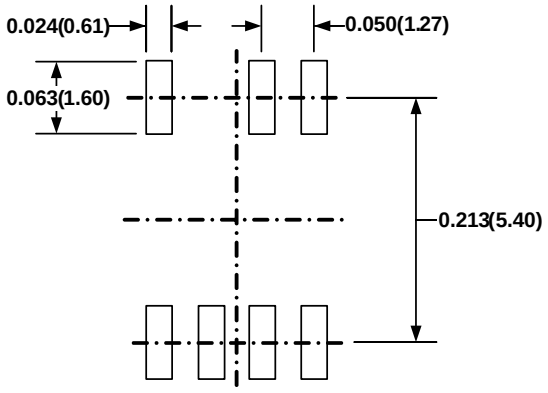
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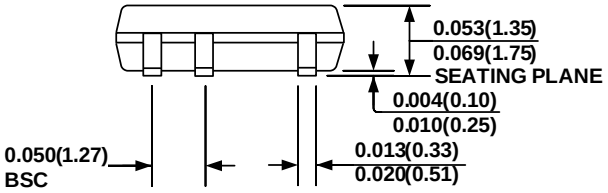
SOIC8-7A



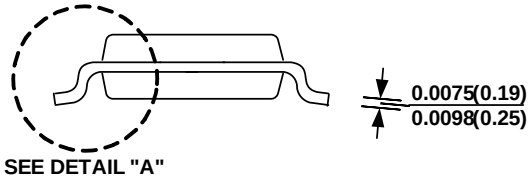
TOP VIEW



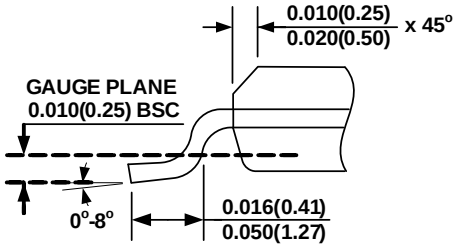
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW



DETAIL "A"

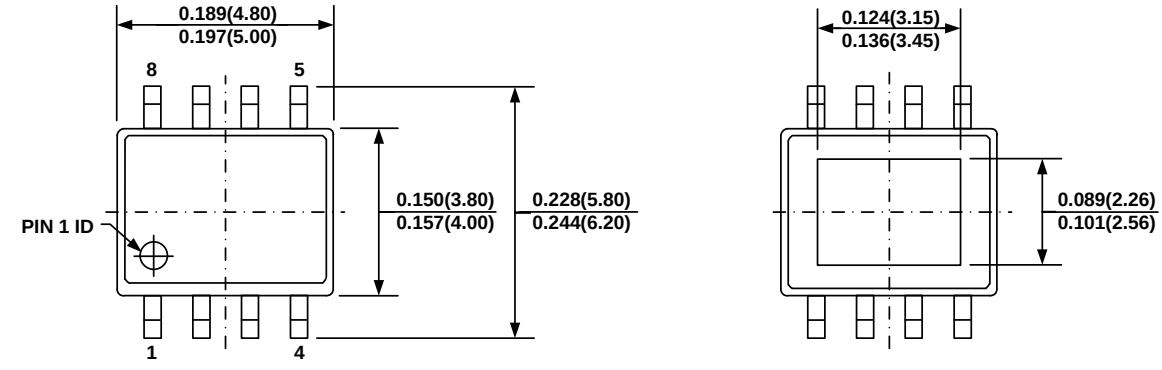
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3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
5) JEDEC REFERENCE IS MS-012.
6) DRAWING IS NOT TO SCALE

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