The Future of Analog IC Technology

MP4652

HIGH PERFORMANCE OFF-LINE TV LED DRIVER

DESCRIPTION

The MP4652 is a high-performance, off-line LED driver designed to power LEDs for high-power isolated applications, such as LCD TV backlighting. It is available in a 16-pin SOIC package.

The MP4652 can operate at a fixed operating frequency or a variable frequency controlled externally. It outputs two 180-degree phase-shifted driver signals for various external power stages, like LLC, half bridge and flyback. Its enhanced 9V gate driver can sufficiently drive the external MOSFETs and directly drives the external gate drive transformer.

The MP4652 implements fast and continuous PWM dimming for LEDs. It outputs a driver signal to directly dim the LED current through a dimming MOSFET and achieves fast PWM dimming. It provides continuous gate driver signals to the power stage to the whole PWM dimming cycle that eliminates the audible noise: the MP4652 can achieve 1000:1 PWM dimming ratio without any audible noise issue. The PWM dimming is controlled by either a DC input voltage or a direct PWM signal. The DC input PWM dimming frequency can be synchronized by an external signal.

The built-in fault management features include open LED protection, short LED protection, protection against shorts along any point of the LED string to ground, and over temperature protection. The protection interface is flexible and is easy to use. At fault protection, system can be set up with auto-recovery or latch up.

FEATURES

- LLC, Half Bridge or Flyback Controller
- Fast and Continuous PWM Dimming with Audible Noise Elimination
- 1000:1 PWM Dimming Ratio
- Input Voltage Range from 9V to 30V
- 9V Enhanced Gate Driver
- Fixed or Externally Programmable Operating Frequency
- DC or PWM Input Dimming Control
- DC Input PWM Dimming Frequency Synchronization
- Smart Fault Protection Interface
- Open and Short LED String Protection
- Protection Against Shorts Along the LED String to Ground
- Built-In Fault Management
- System Auto Recovery or Latch Up at Fault Protection
- Available in SOIC 16 Package
- Pin-to-Pin with MP4651

APPLICATIONS

- Flat-Panel Video Displays
- Street Lighting

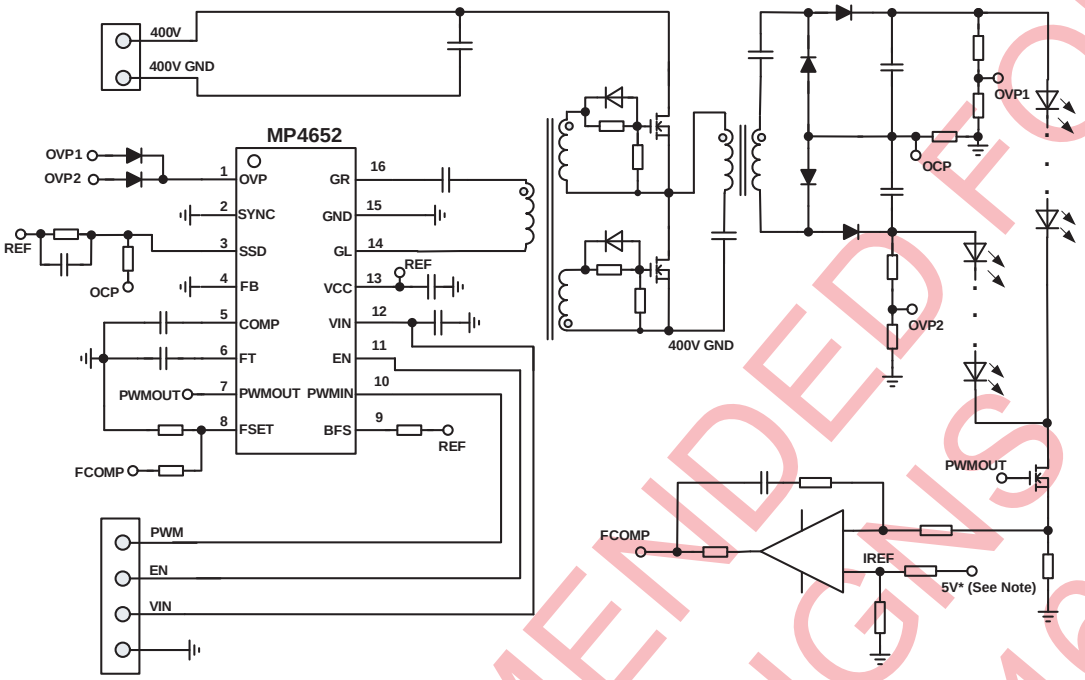
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The MP4652 is covered by US Patents 6,683,422, 6,316,881, and 6,114,814. Other Patents Pending.

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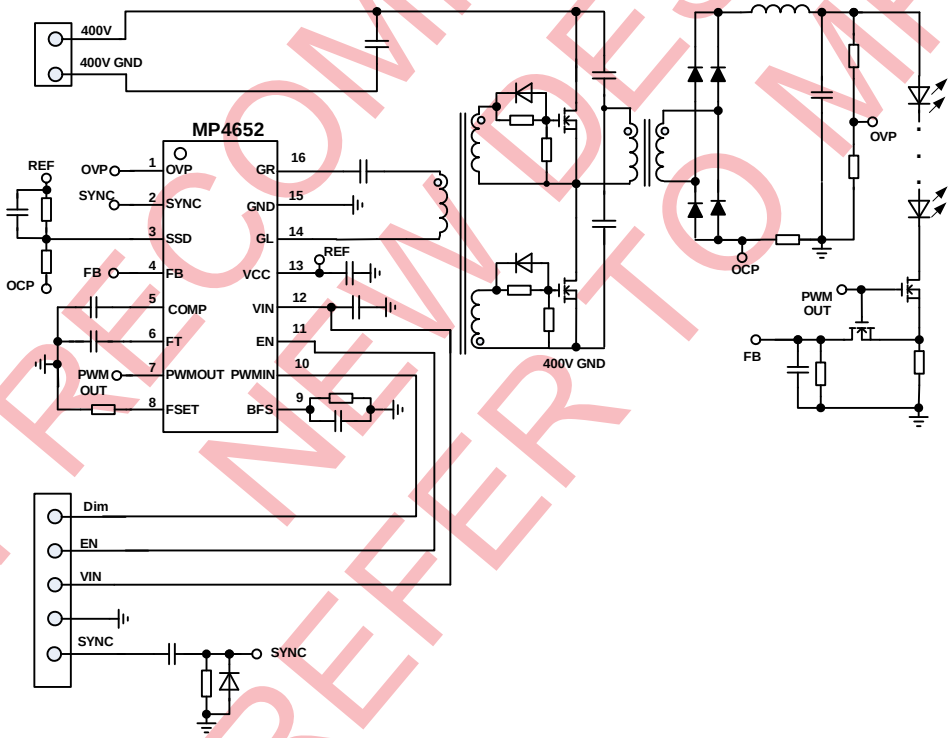
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SIMPLIFIED TYPICAL APPLICATION



MP4652 LLC Application: Recommended for PWM dimming frequencies from 100Hz to 2kHz

***Note: The 5V could be an accurate reference voltage generated from a TL431.**



Half Bridge Application: Recommended for PWM Dimming Frequencies Greater Than 2kHz

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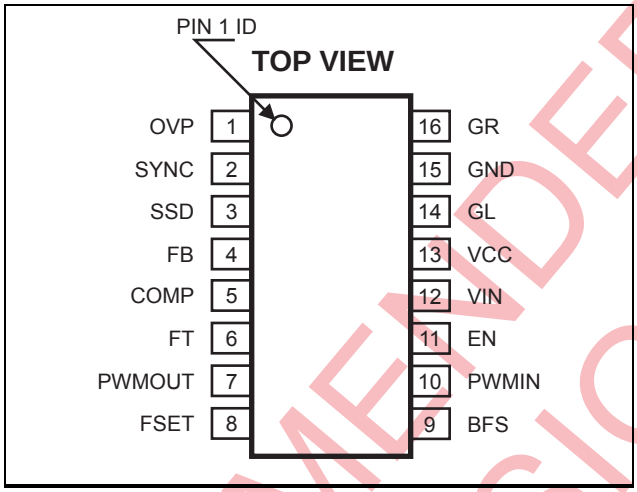
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ORDERING INFORMATION

Part Number*	Package	Top Marking	Free Air Temperature (T_A)
MP4652ES	SOIC16	MP4652ES	-20°C to +85°C

* For Tape & Reel, add suffix –Z (e.g. MP4652ES–Z)
For RoHS compliant packaging, add suffix –LF (e.g. MP4652ES–LF–Z)

PACKAGE REFERENCE



ABSOLUTE MAXIMUM RATINGS (1)

Input Voltage V_{IN} 35V
VCC, GL, GR .....-0.3V to +10.7V
FB, SSD .....-5.8V to +5.8V
Other Pins .....-0.3V to +6.5V
Continuous Power Dissipation (T_A = 25°C) (2)
.....1.56W
Junction Temperature .....150°C
Lead Temperature (Solder).....260°C
Operating Frequency ..... 20kHz to 150kHz
Storage Temperature..... -55°C to +150°C

Recommended Operating Conditions (3)

Input Voltage V_{IN} .....9V to 30V
Maximum Junction Temp. (T_J) .....125°C

Thermal Resistance (4)

	θ_{JA}	θ_{JC}
SOIC16	80	35 °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature TJ(MAX), the junction-to-ambient thermal resistance θJA, and the ambient temperature TA. The maximum allowable continuous power dissipation at any ambient temperature is calculated by PD(MAX) = (TJ(MAX)-TA)/ θJA. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB

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ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Gate Driver GL, GR						
Gate Pull-Down Resistance	R_{GD}			2		Ω
Gate Pull-Up Resistance	R_{GU}			4		Ω
Output Source Current	I_{SOURCE}			1		A
Output Sink Current	I_{SINK}			2		A
Maximum Duty Cycle	D_{MAX}			46%		
En						
EN Turn On Threshold	V_{EN-ON}		2			V
EN Turn Off Threshold	V_{EN-OFF}				1	V
Internal Pull-Down Resistor	R_{EN-IN}			60		kΩ
Brightness Dimming Control Range (PWMIN)						
PWM Full Scale	V_{PWM}	DC input PWM dimming	1.1	1.2	1.3	V
PWM Logic Input Threshold	V_{TH-PWM}	PWM dimming	1.6	1.9	2.2	V
PWM Logic Input Hysteresis	$V_{TH-PWM-Hyst}$	PWM dimming		0.1		V
Burst Frequency Set (BFS)						
Source Current	$I_{SRC(BFS)}$	V_{BFS} = 2V	120	140	170	μA
Lower Threshold	$V_{V(BFS)}$		2.2	2.4	2.6	V
Upper Threshold	$V_{P(BFS)}$		3.3	3.55	3.8	V
Supply Current						
Supply Current (Enabled)	I_{IN-EN}	No driver output		1.5	2.5	mA
Supply Current (Disabled)	I_{IN-OFF}	V_{IN} = 30V			1	μA
Operating Frequency	f_O	25kΩ FSET to GND	46.5	50	53.5	kHz
Frequency Set Voltage	V_{FSET}		1.14	1.2	1.25	V
Output PWM Dimming Signal For LED (PWMOUT)						
Logic High Voltage	$V_{H-PWMOUT}$	Normal Operation	5	6	6.5	V
Logic Low Voltage	$V_{L-PWMOUT}$	At Fault Condition, 25kΩ FSET to GND		0.1	0.6	V
Output PWM Source Current	I_{SOURCE_PWMOUT}	100pF on PWMOUT pin		3		mA
Output PWM Sink Current	I_{SINK_PWMOUT}	100pF on PWMOUT pin		20		mA
Led Current Feedback (FB)						
Magnitude	$\|V_{FB}\|$		0.57	0.6	0.63	V
Input Resistance	R_{FB_IN}			30		kΩ
Over Voltage Protection (OVP)						
Over Voltage Protection Threshold	$V_{TH(OVP)}$		2.22	2.38	2.55	V

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ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Fault Timer (FT)						
Threshold	$V_{th(FT)}$		2.2	2.4	2.6	V
Source Current	$I_{SOURCE(FT)}$			8		µA
Comp						
Clamp Voltage	V_{COMP}			0.60		V
Reference Current	I_{COMP+}	FB = 0V		20		µA
Pull Down Current At Fault Condition	$I_{COMP-FAULT}$	Fault Mode is triggered		30		µA
Burst Frequency Synchronization (SYNC)						
High Logic Level	V_{SYNC-H}		1.4			V
Low Logic Level	V_{SYNC-L}				0.7	V
Pulse Width	t_{sync}		6		20	µs
Synchronizing Frequency	f_{SYNC}	DC input PWM dimming, Compared to the frequency f_{BFS} set by BFS pin R and C	110%	120%		f_{BFS}
Fault Detection Threshold (SSD, FB)						
SSD Threshold	V_{SSD}		2.22	2.36	2.55	V
SSD Detection Delay Time	T_{D_SSD}			7		µs
FB Threshold	V_{FB}		1.1	1.2	1.3	V
FB Detection Delay Time	T_{D_FB}			7		µs
VCC						
Voltage	V_{VCC}	No load	8.7	9.7	10.5	V
Current	I_{VCC}			20		mA

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PIN FUNCTIONS

Pin #	Name	Description
1	OVP	Over Voltage Protection. The output voltage is sensed by this pin through a voltage divider. If the voltage at OVP exceeds 2.38V for 7μs, the Fault Mode is triggered.
2	SYNC	Synchronization. For burst dimming frequency. Application of a narrow-pulse synchronizing signal on this pin will synchronize the burst frequency on BFS pin. The frequency of the synchronizing signal should be higher than the frequency set by BFS pin.
3	SSD	Short String Detection. A comparator is integrated in this pin for short string protection. If the voltage on this pin falls below 2.36V for 7μs, the Fault Mode is triggered.
4	FB	LED Current Feedback Input. The average voltage at this pin is regulated to 0.6V by an internal error amplifier. The voltage on this pin is also used for short string detection. When the voltage on this pin goes higher than 1.2V for 7μs, the IC recognizes this as short string condition and triggers the Fault Mode. For fixed-operating–frequency PWM-controlled applications—such as half-bridge, flyback or other topologies—shunt a current-sensing resistor from the cathode of the LED to ground and use a sample-hold circuit to feed the LED current to FB pin. The sample-hold circuit should hold the sensed current value on FB pin at PWM off interval. For frequency controlled applications, like the LLC topology, the LED current is regulated through an external amplifier, pull FB to ground and let IC operate with maximum duty cycle.
5	COMP	Feedback Compensation Node. For fixed-operating–frequency PWM-controlled applications, connect a compensation capacitor or an R-C network from this pin to GND. For frequency controlled applications, like the LLC topology, connect a 1nF cap on this pin.
6	FT	Fault Timer. Connect a timing capacitor from this pin to GND to set the fault timer to recover the system. When the voltage on this pin goes higher than the 2.38V threshold, the IC recovers. If the system requires a latch up for Fault Mode, connect a resistor smaller than 250kΩ to this pin.
7	PWMOUT	PWM Dimming Control Output. This pin outputs the PWM dimming driver signal to the LED dimming MOSFET for fast PWM dimming. In Fault Mode PWMOUT is pulled low.
8	FSET	Frequency Set. The source current through this pin determines the operating frequency of the MP4652. For fixed-operating–frequency PWM-controlled applications, connect a resistor from this pin to GND to set the operating frequency. For typical applications, a 25kΩ resistor sets the operating frequency at 50kHz. For frequency controlled applications (like LLC), apply the control voltage (the output of the regulation loop) to this pin through a resistor. This control voltage programs the source current through the FSET pin and thus controls the operating frequency.
9	BFS	Burst Frequency Set. For DC input PWM dimming. Connect a resistor in parallel with a capacitor from BFS to GND. The resistor and capacitor programs the burst frequency. For direct PWM input PWM dimming, pull up BFS to VCC with a 20kΩ resistor and apply the PWM signal to the PWMIN pin.
10	PWMIN	PWM Dimming Control Input. For DC input PWM dimming, the voltage range from 0 V to 1.2V at PWMIN linearly sets the PWM dimming duty cycle from 0 to 100%. For direct PWM input PWM dimming, directly apply the PWM signal on this pin. The MP4652 has positive dimming polarity.

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PIN FUNCTIONS *(Continued)*

Pin #	Name	Description
11	EN	Enable Input. Pull EN high to turn on the chip, and pull EN low to turn it off.
12	VIN	Supply voltage input.
13	VCC	Linear Regulator Output and Bias Supply of the Gate Driver. It provides the supply for the gate driver and also the external control circuit, the typical value is 9.7V. Bypass VCC with a 1μF or larger ceramic capacitor.
14	GL	Driver signal output, 180 degree phase shifted from GR
15	GND	Ground.
16	GR	Driver signal output, 180 degree phase shifted of GL

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BLOCK DIAGRAM

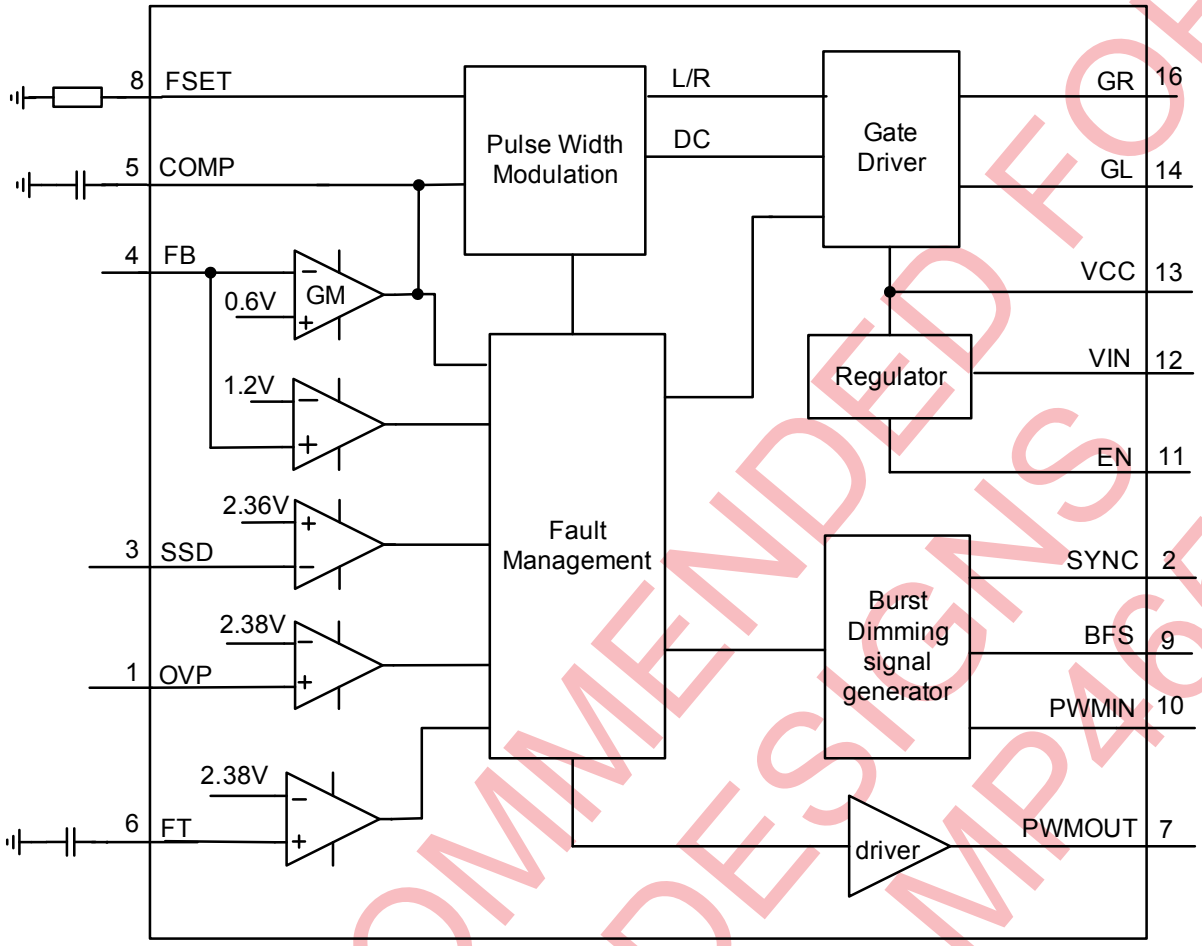


Figure 1—MP4652 Block Diagram

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OPERATION

Steady State and Enable Control

The MP4652 is a high-performance, off-line LED driver specifically designed for high-power isolated applications such as LED backlighting for TVs. Powered by a 9V to 30V input supply, the MP4652 outputs two 180-degree phase-shifted gate driver signals for external power stages. Its enhanced 9V gate driver provides adequate driver capability to the external MOSFETs and directly drives the external MOSFETs through a gate drive transformer. The MP4652 can be used to control LLC, half-bridge, flyback, and other power stages.

The MP4652 can accurately regulate the LED output current using both PWM control and a compensation network on the COMP pin. PWM control uses an external resistor connected from FSET pin to GND to set the operating frequency. The LED current feeds back to the FB pin with a sample-hold circuit and compared against an internal 0.6V reference voltage. The compensation network on the COMP pin, which connects to the output of the error amplifier, then accurately regulates the output LED current. The voltage on COMP pin is compared with the internal oscillator and generates duty cycle modulated signals to control the external power switches. This PWM control makes MP4652 suitable for half-bridge, flyback, and other power stages.

The MP4652 FSET pin can also take voltage feedback from a frequency-controlled external circuit to adjust the device frequency. Connect this feedback circuit to FSET using a resistor. This frequency control makes MP4652 suitable for LLC and other frequency-controlled power stages.

The system power is controlled by EN pin. When the chip is enabled, the built-in regulator for VCC powers up the internal circuit. When VCC exceeds its UVLO point, IC starts to operate and outputs the gate drive signals.

Brightness Control

MP4652 implements PWM dimming on the LED current by using either a DC input voltage or a direct PWM input signal. The MP4652 has a built-in burst oscillator that can generate a triangle waveform on the BFS pin.

When using a DC input voltage for PWM dimming, connect a capacitor in parallel to a resistor on BFS pin to set the burst frequency and apply the DC voltage to the PWMIN pin to program the PWM dimming duty cycle.

The burst frequency can also be synchronized to an external frequency by applying a synchronizing narrow-pulse signal on the SYNC pin. The synchronizing frequency should be higher than the burst frequency set by the BFS pin. Please refer to SYNC pin description for details.

When using a direct PWM input signal for PWM dimming, use a 20kΩ pull-up resistor between the BFS pin to VCC and apply the PWM signal on PWMIN pin.

Continuous Fast PWM Dimming

The MP4652 implements fast and continuous PWM dimming on the LED current, as shown in Figure 2. The PWM dimming signal (controlled by a DC input voltage or a direct PWM signal) outputs from the PWMOUT pin to drive the external dimming MOSFET in series with the LED string. Therefore, the LED current quickly rises when the PWM dimming signal goes high, and quickly falls when PWM dimming signal falls. This fast PWM dimming feature helps the MP4652 achieve a high PWM dimming ratio.

The MP4652 provides continuous PWM dimming to the system. It outputs continuous gate driver signals to the power stage during both PWM on and PWM off intervals. This makes the power flow continuous for magnetic components—such as transformers and inductors—which can eliminate audible noise.

With this fast and continuous PWM dimming feature, the MP4652 can achieve 1000:1 high

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PWM dimming ratio at a 120Hz PWM dimming frequency without any audible noise issue (or 500:1 PWM dimming ratio at 300Hz PWM dimming frequency).

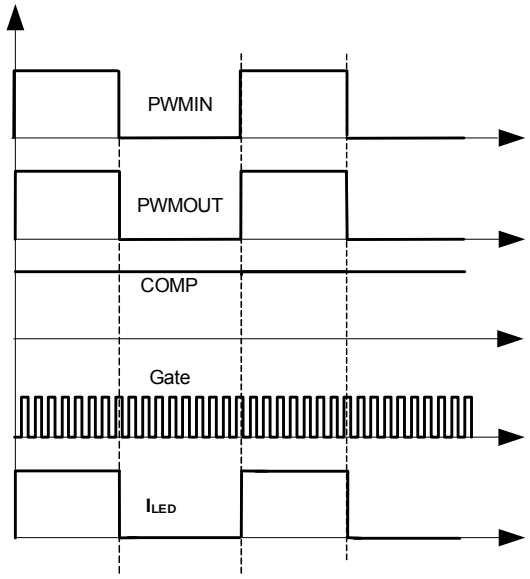


Figure 2— Fast and Continuous PWM Dimming

Fault Protection

System fault management features include open LED protection, short LED protection if at any point the LED string shorts to ground, protection against shorts along the LED string, and a delay timer for system recovery.

The output voltage is monitored by the OVP pin through a voltage divider. Once the open LED condition occurs and the voltage on the OVP pin exceeds 2.38V for 7μs, the MP4652 recognizes this as open condition and triggers the Fault Mode.

The SSD pin monitors the secondary side current. If any point of the LED string is shorted to ground, the secondary side current increases. When the voltage on SSD pin falls below 2.36V for 7μs, the MP4652 triggers the Fault Mode.

The FB pin can also function as short LED string protection. When the voltage on FB pin is higher than 1.2V for 7μs, the IC triggers the Fault Mode.

In Fault Mode, the outputs of the gate drivers GL and GR are disabled, the PWMOUT signal is pulled low, and the COMP capacitor is discharged by a 30μA current source. The fault timer then starts. An 8μA current source charges the FT capacitor, and when FT voltage hits 2.38V, the system recovers. The IC enables the output driver signals, releases the COMP, resets the fault flag, and pulls down the FT pin.

If the design requires a latch up for the IC at Fault Mode, connect a 200kΩ resistor on the FT pin.

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APPLICATION INFORMATION

Pin 1 (OVP):

This pin is used for over-voltage protection. When the output voltage to this pin exceeds 2.38V for 7μs, the Fault Mode is triggered. For applications involving multiple LED strings, apply the maximum output voltage of the LED strings to this pin.

Pin 3 (SSD):

This short string detection pin is used for protection against shorts along any point of the LED string to ground. The SSD pin monitors the secondary side current. When the voltage on this pin falls below 2.36V for 7μs, the IC treats the condition as a short and triggers the Fault Mode.

Pin 4 (FB):

This pin is used for LED current regulation. The voltage on this pin is regulated by an external circuit with a 0.6V average value. Use a sample-hold circuit to sense the LED current when the PWM goes high, and hold the value when the PWM goes low.

The FB pin also functions as short string protection. When the voltage on FB exceeds 1.2V for 7μs, the IC triggers the Fault Mode.

For frequency-controlled application like an LLC power stage, the LED current is regulated with an external-frequency control loop. Connect FB to ground and set the IC to operate at the maximum duty cycle.

Pin 5 (COMP):

This pin is used for compensation purposes. For PWM-controlled applications, such as half-bridge and flyback power stages, connect an X7R ceramic capacitor with a value between 47nF and 470nF from COMP to GND. The value of this capacitor determines the stability of the LED current regulation.

For frequency-controlled applications like the LLC power stage, connect a 1nF capacitor to the COMP pin.

Pin 6 (FT):

Connect a capacitor from this pin to GND to set the fault timer. This sets the system recovery time after detecting a fault condition.

$$T_{FT} = \frac{2.38V \times C_{FT}}{8\mu A}$$

A 10nF capacitor on FT sets the delay time to around 3ms

If the circuit requires a latch-up for Fault Mode, connect this pin to a 200kΩ resistor.

Pin 8 (FSET):

This pin is used to set the operating frequency. The source current through this pin determines the operating frequency.

For fixed-operating–frequency PWM-controlled applications—like half-bridge and flyback power stages—connect a resistor from this pin to GND to set the operating frequency (f_o). The value for this resistor R_{FSET} is calculated by

$$R_{FSET} = \frac{1.25 \times 10^9}{f_o}$$

For an operating frequency of 50kHz, R_{FSET} = 25kΩ.

For frequency-controlled applications like LLC, connect the control voltage to FSET pin through a resistor, as shown in Figure 3. This control voltage programs the source current through this pin to control the operating frequency.

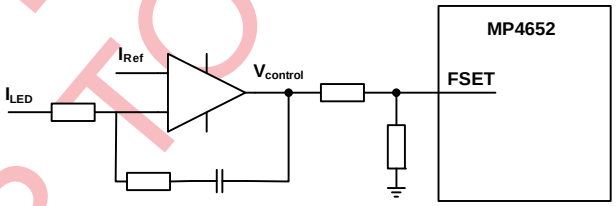


Figure 3—FSET Set Up for Frequency Controlled Application.

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Pin 7 (PWMOUT):

This pin outputs the PWM dimming signal to drive the dimming MOSFET in series with the LED string for fast PWM dimming. Connect this pin to the gate of the dimming MOSFET through a driver resistor.

Pin 10 (PWMIN):

This pin is used for PWM-dimming brightness control. For DC-input PWM dimming, the DC voltage controls the PWM dimming duty cycle on the output. The signal should be filtered for optimal operation. A voltage in the range of 0V to 1.2V on PWMIN programs the PWM dimming duty cycle from 0 to 100%.

For direct PWM input PWM dimming, pull BFS high to VCC through a 20kΩ resistor, and connect the PWMIN pin directly to the PWM source. Logic High is PWM On and Logic Low is PWM Off.

Pin 9 (BFS):

BFS pin is used to set the burst frequency for DC input PWM dimming, using the waveform shown in Figure 4. Connect a resistor (R_{BFS}) in parallel with a capacitor (C_{BFS}) on this pin to set the burst frequency.

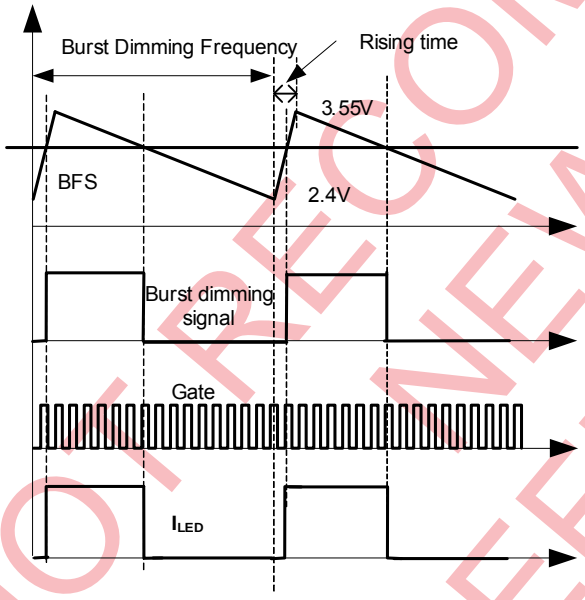


Figure 4—PWM Dimming with DC Input Voltage at PWMIN Pin

These values are determined as follows:

Set a percentage of the rising time, where:

$$D_{rise} = t_{rise} \times f_{Burst}$$

R_{BFS} and C_{BFS} are determined by:

$$R_{BFS} \approx 21.16k\left(\frac{1}{D_{rise}} - 1\right) + 21.43k$$

$$C_{BFS} = \frac{1 - D_{rise}}{f_{Burst} \times R_{BFS} \times 0.405}$$

For D_{rise} = 0.1, f_{Burst} = 200Hz, then R_{BFS} = 212kΩ, C_{BFS} = 52nF. D_{rise} is recommended between 0.1 and 0.2.

For direct PWM input PWM dimming, pull BFS high to VCC through a 20kΩ resistor and apply the PWM signal to PWMIN pin.

Pin 2 (SYNC):

This pin is used for burst frequency synchronization to synchronize the DC input PWM dimming frequency. Application of a small-pulse synchronizing frequency signal will synchronize the burst frequency.

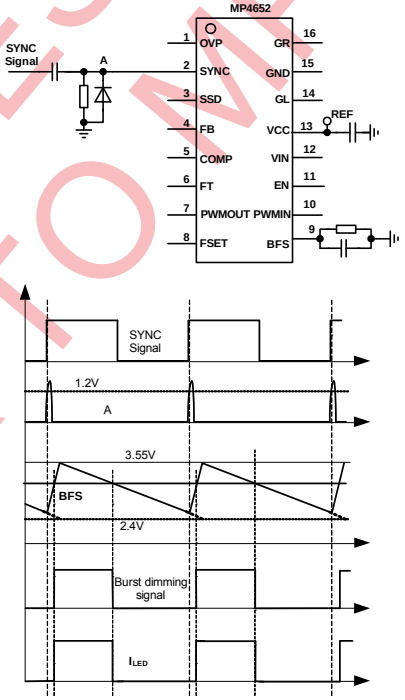


Figure 5—Synchronized DC Input PWM Dimming and Schematic

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Figure 5 shows synchronized PWM dimming with DC input. The synchronizing signal is filtered by a high pass filter. Its rising edge is caught and used to synchronize the triangle waveform on the BFS pin. The synchronizing frequency should be higher than that set by BFS pin and the amplitude of the synchronizing signal should be higher than 1.4V.

Table 1—Function Mode

Function	Pin Connection		
	PWMIN	BFS	SYNC
PWM dimming with DC Input Voltage	*0V to 1.2V	C_{BFS}, R_{BFS}	GND
PWM dimming with DC Input Voltage and Synchronizing frequency	*0V to 1.2V	C_{BFS}, R_{BFS}	R,C,D network
PWM dimming with direct PWM input	PWM	To VCC through 20kΩ resistor	GND

Note:

*:Burst Brightness Polarity: 100% duty cycle at PWM voltage 1.2V.

Pin 11 (EN):

Pull this pin high to enable the chip, and pull it low to disable the chip.

Pin 12 (VIN):

Supply voltage input. Bypass the supply voltage with a 0.1μF or larger ceramic capacitor

Pin 13 (VCC):

This pin provides the gate driver supply voltage. Its typical value is 9.7V. Connect a 1μF or greater ceramic capacitor to this pin to bypass the supply voltage. This voltage is also used to supply the external control circuit.

Pin 14(GL), Pin 16 (GR):

Gate driver signals output. GL and GR are 180-degree phase-shifted driver signals. GL and GR can directly drive the external MOSFETs in the off-line system through a gate driver transformer with enhanced driver capability. Connect two 5.1Ω resistors in series with GL and GR to reduce the EMI noise.

Place a 2.2nF Y capacitor between the primary reference ground and the secondary reference ground.

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EXAMPLE APPLICATION

TV LED Backlight

This application example introduces a high performance 2-stage LLC TV LED driver that is designed to power the LED backlights for a 40-inch TV. The total system power structure is shown in Figure 6. It uses a 2-stage structure with high efficiency and low cost. The PFC stage outputs around 390V and is controlled by the MPS PFC controller MP44010, which works in BCM (Boundary Conduction Mode). The MP4652 acts as the LED driver stage: it controls a LLC power stage to drive the LED strings. Another flyback DC/DC stage outputs the 13V power supply for the system: it uses the MPS quasi-resonant flyback controller HFC0100.

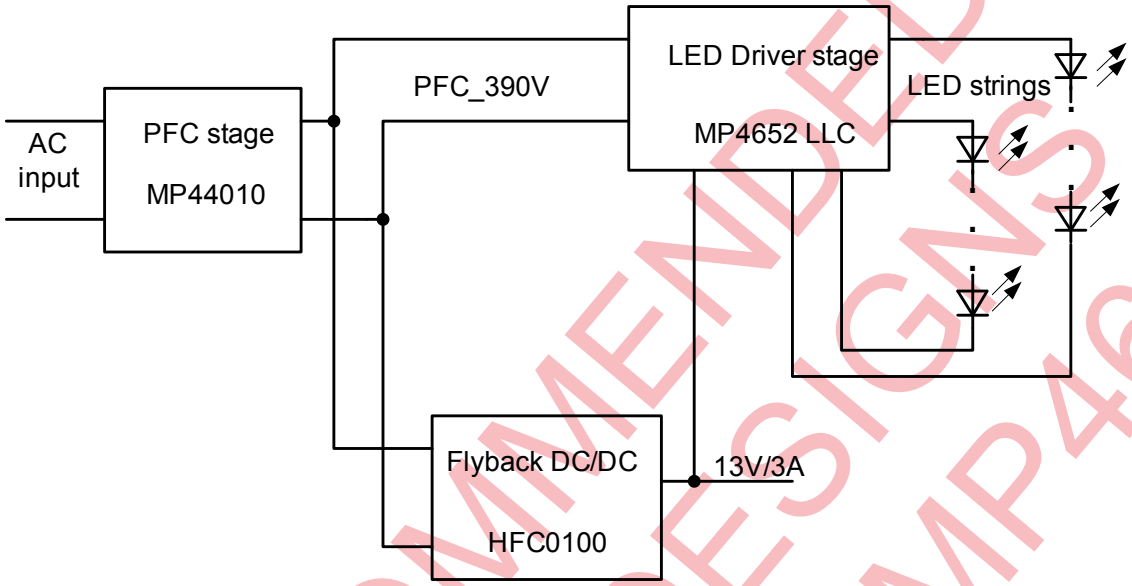


Figure 6—System Power Structure

The following introduces the detailed circuit of the LED driver stage based on MP4652. The specifications for this LED driver are listed below.

Specification:

Input: typically 390V, PFC Output.
Output: 4 strings at 55V/260mA per string, connecting 2 strings in series. It could also output 2 strings at 110V/260mA per string.
Operating frequency: ~110kHz
PWM dimming frequency: 320Hz
Protection: Open LED protection, short LED string protection, short LED+ to GND protection

Schematics:

Figure 7 shows the schematic of the LED driver stage. The parameters of the power transformer T2 are as follow:

NP: NS = 65:35, Leakage inductance = 450μH, magnetic inductance = 1.6mH.

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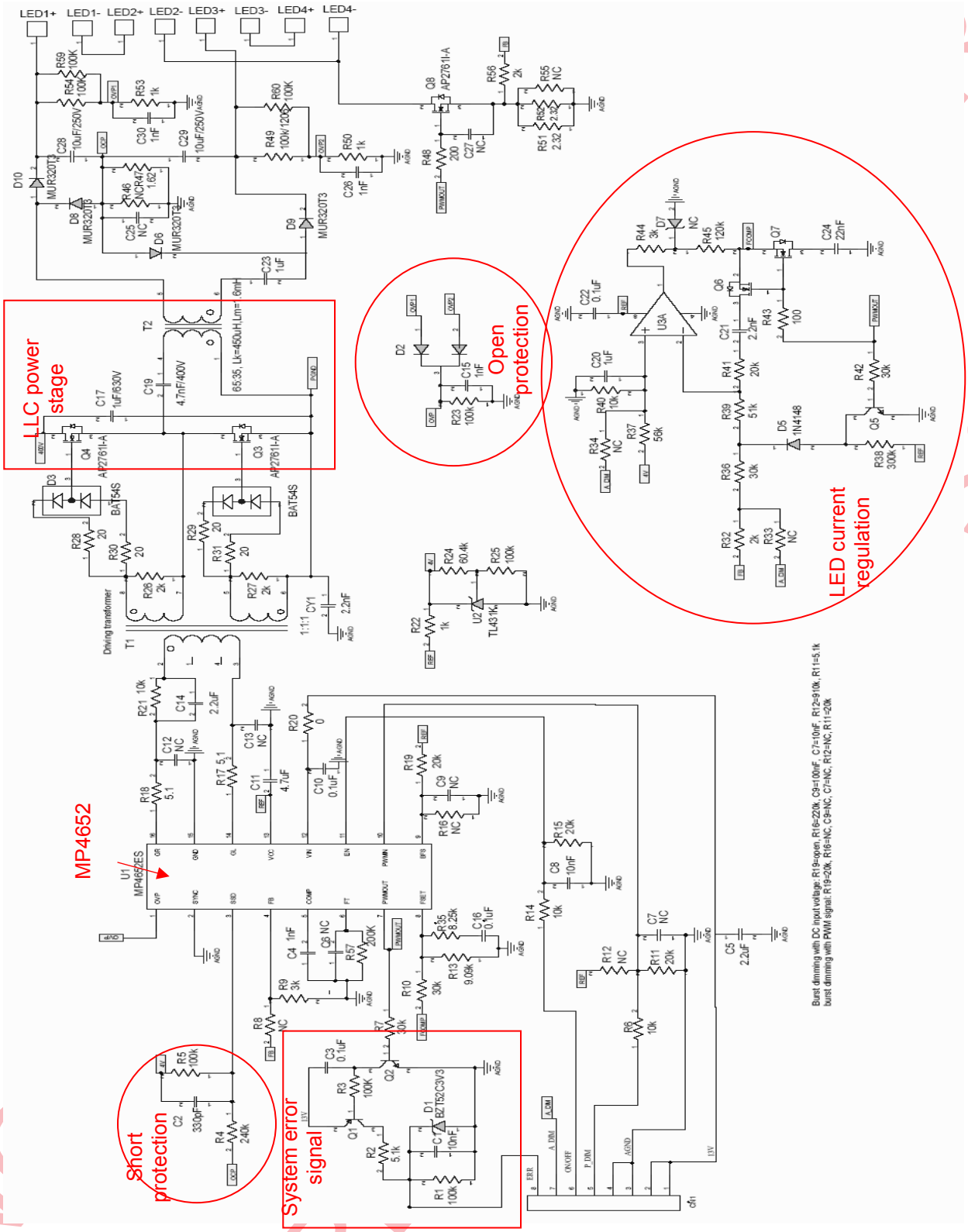


Figure 7—MP4652based 2-stage LLC TV LED Drive

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Power Stage

The power stage is a half-bridge LLC topology. The primary side is composed of Q4, Q3, C19 and T2. The LLC resonant network is composed of the leakage inductance of T2, the magnetic inductance of T2, and C19. Q4 and Q3 should be chosen to handle the input voltage and the LLC current. Consider the operating frequency, the input condition and the output condition when selecting the resonant cap, the leakage inductance, and the magnetic inductance. Refer to MP4652 LLC design notes for details.

On the secondary side, the diodes D6, D8, D9, and D10 rectify the LLC current. These diodes must be able to handle the output voltage and the output current: they are 200V/3A diodes in this circuit. The balance cap C23 blocks the different voltage of the 2 LED strings and balances the currents through them. The value of C23 is usually between 0.22μF and 1μF. Its voltage must be higher than the output voltage because of the LED string short condition. The output capacitors C28 and C29 filter the ripple current of the LLC output current to obtain a DC current for the LED strings. C28 and C29 also store the energy from the primary side at the PWM off interval, as MP4652 implements continuous gate driver at PWM off interval to eliminate the audible noise. The value of C28 and C29 must be large enough to handle this energy to prevent excessive output voltage spikes: Capacitor values from 4.7μF to 22μF are typical for this application. The voltage stress of these output capacitors should be higher than the maximum output voltage.

Control Circuit

MP4652 controls the power MOSFETs Q3 and Q4 in the power stage through the gate driver transformer T1. As MP4652 outputs regulated 9V gate driver signals, the turn ratio of T1 goes from 1:1:1 to 1:1.5:1.5. With its enhanced gate driver capability and regulated driver voltage, MP4652 can directly drive the MOSFETs through the gate driver transformer.

Because an LLC is a frequency-controlled power stage, MP4652 uses an external amplifier U3 to regulate the LED current and output the frequency control voltage. During the PWM ON interval, PWMOUT is high and the dimming MOSFET Q8 turns on. The LED current feeds back to the inverting input of U3. With the compensation network, U3 outputs the frequency control voltage and regulates the LED current. During the PWM OFF interval, the dimming MOSFET turns off, and LED current feedback goes low. An external voltage applied to the inverting input of U3 through D5 pulls the output of U3 low. This design helps the circuit work at a high frequency during the PWM OFF interval and limits the output energy delivered from the primary side to the secondary side.

Together with the output capacitors C28 and C29, this circuit helps to eliminate current overshot during PWM ON. The signal MOSFETs Q6 and Q7 are turned off during the PWM OFF interval, and C21 and C24 can hold their value during this time. This helps the control loop to respond quickly during the PWM ON interval and to achieve fast PWM dimming.

R35 and C12 on the FSET pin form a frequency soft-start circuit at start up.

The maximum output voltage is fed back to OVP pin through the voltage dividers. MP4652 can protect the open LED condition through the OVP pin. When the voltage on OVP pin is higher than 2.38V for 7μs, IC enters Fault Mode.

The secondary side current is fed back to SSD pin through R47, R46 and C25. When short condition occurs, the secondary side current grows and the SSD voltage falls. When SSD voltage falls below 2.36V for 7μs, the IC enters fault mode.

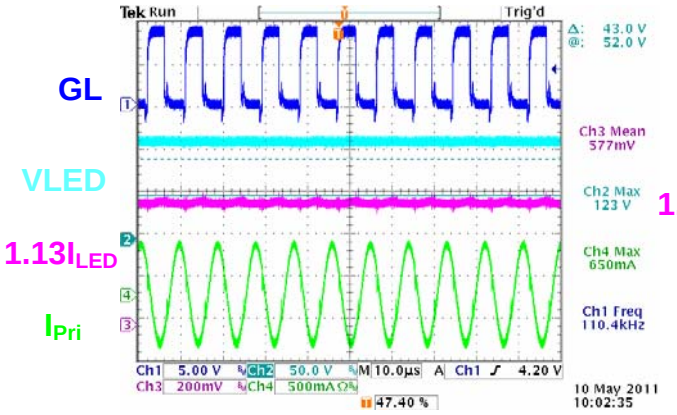
In Fault Mode, the PWMOUT pulls low. The device then outputs an error signal to the system with the addition of an external logic circuit,.

Please refer to the design notes for details of the components selection.

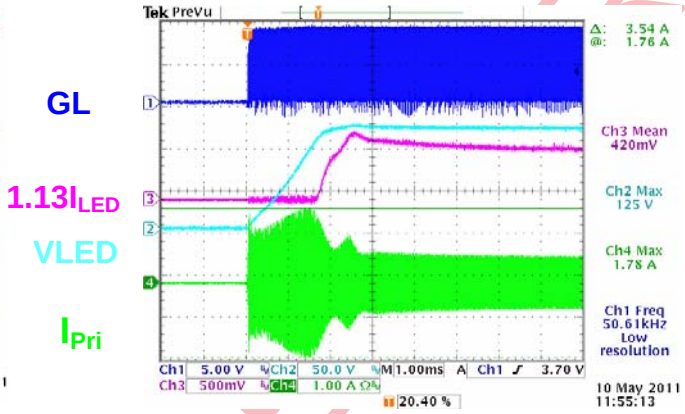
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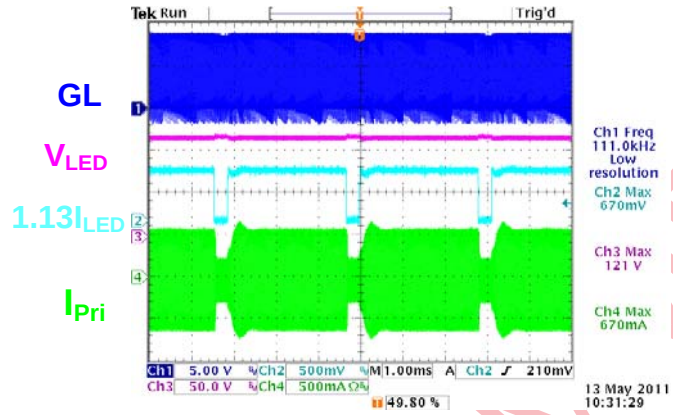
Circuit Performance



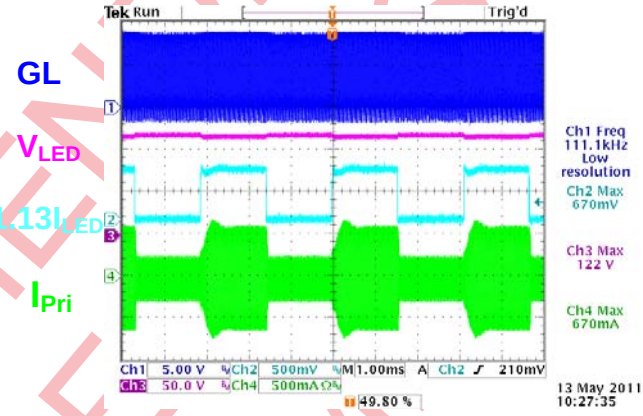
Steady State



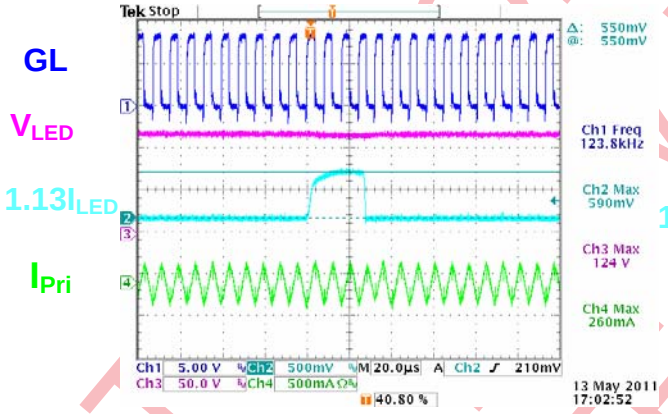
Start Up



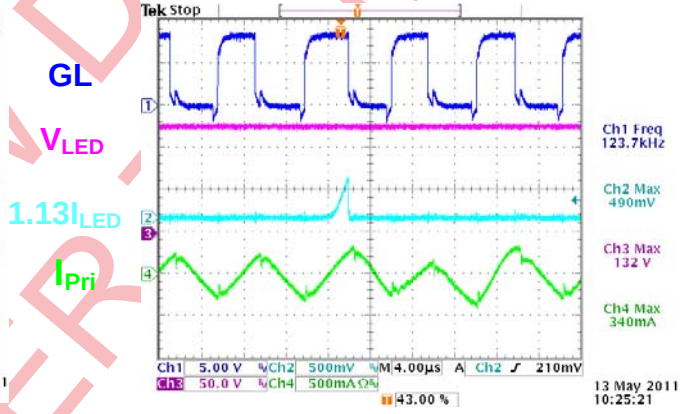
90% PWM Dimming



50% PWM Dimming



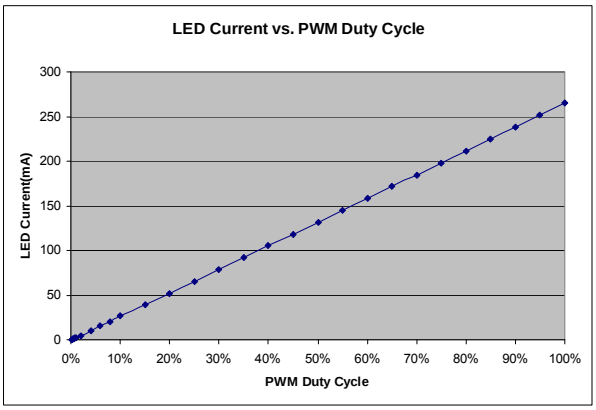
1% PWM Dimming



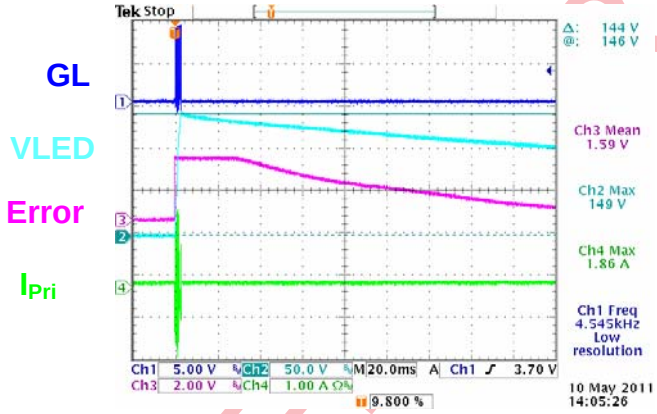
0.2% PWM Dimming

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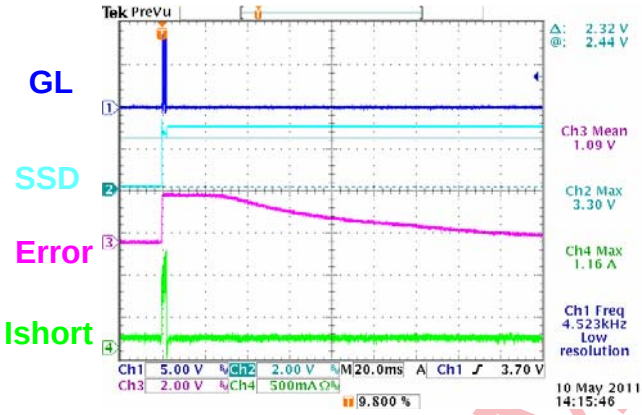
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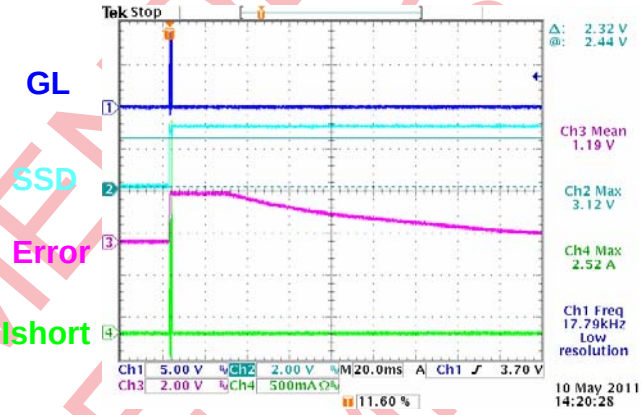
PWM Dimming Linearity



Open LED Protection



Short LED+ to LED- Protection



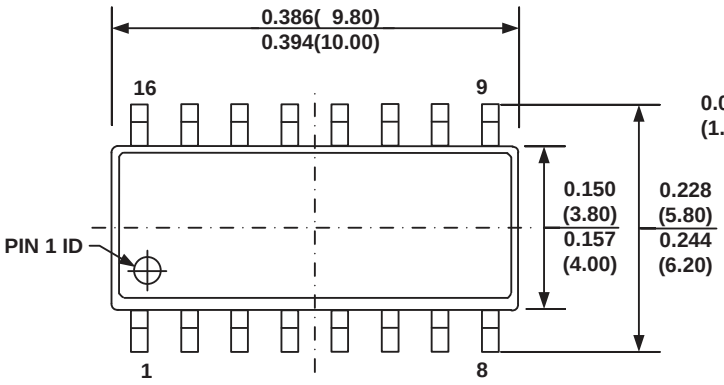
Short LED+ to GND Protection

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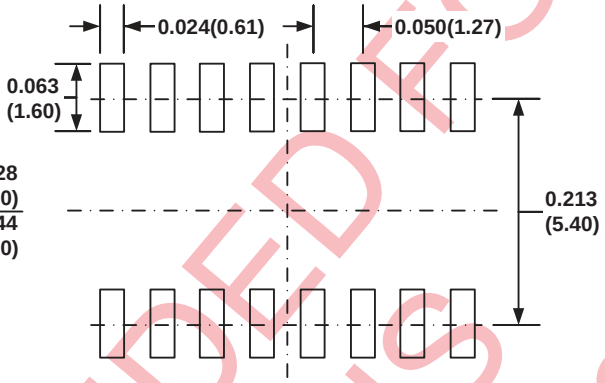
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PACKAGE INFORMATION

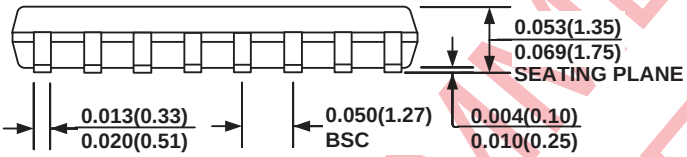
SOIC16



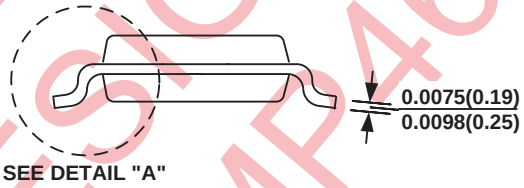
TOP VIEW



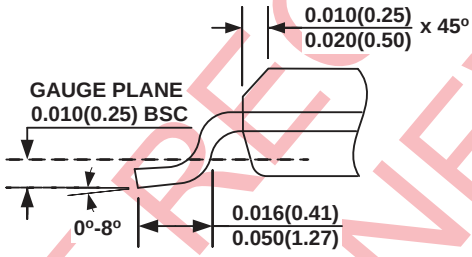
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW



DETAIL "A"

NOTE:

1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
5) DRAWING CONFORMS TO JEDEC MS-012, VARIATION AC.
6) DRAWING IS NOT TO SCALE.

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