MP4657A

Single-Stage Flyback, 4-String LED Driver and System Voltage Controller

DESCRIPTION

The MP4657A is a single-stage flyback, 4-string LED driver and system voltage controller for LED backlighting on the secondary side. The device controls the flyback power stage and an external N-channel MOSFET to regulate system output voltage and the LED current loop with integrated 4-string LED current balancing. With a 4V to 16V input voltage, the device outputs a direct driving signal to control the N-channel MOSFET for regulating the system output voltage. The device also outputs a compensation signal to control the primary-side flyback (or other power stage) through an optocoupler.

The MP4657A induces PWM dimming or analog dimming to the LED current through the ADIMP/PWM pin. Apply a pulse signal with a >5kHz frequency on this pin for analog dimming. Apply a pulse signal with a <5kHz frequency on this pin for PWM dimming.

The device uses an individual control method for the LED current and system voltage. When the PWM signal is effective, the MP4657A regulates the LED current loop through the flyback power stage and further regulates the system voltage by controlling the N-channel MOSFET. Soft switching for the N-channel MOSFET can be achieved to reduce voltage spikes. When the PWM signal is ineffective, the device directly controls the system voltage through the flyback power stage.

The MP4657A features rich protections to increase system reliability. Protections are utilized for both the system voltage stage and the LED driver stage. LED driver stage protections include LED open protection, LED short protection and LEDx pin short to ground protection. The system voltage stage protections include over-voltage protection (OVP) and feedback open loop protection. The device also has thermal protection.

The MP4657A is available in an SOIC-16 package.

FEATURES

- Single-Stage Flyback for High Efficiency LED Current and System Voltage Regulation
- Individual Control Method for the LED Driver Stage and System Voltage Stage
- 4V to 16V Supply Voltage
- 4-String, 80V LED Current Balancing
- 1.5% System Voltage Accuracy
- 1.5% LED Current Accuracy and 2% LED Current Balancing
- Low LEDx Regulation Voltage, High Efficiency
- Fast Dynamic Control, Fast Response
- System Supply Over-Voltage Protection (OVP)
- System Supply Short Protection
- LED Open, LED Short Protection
- LEDx Pin Short to Ground Protection
- Feedback Open Loop Protection for System Voltage
- Soft Switching for the External N-Channel MOSFET
- Thermal Protection
- Available in an SOIC-16 Package

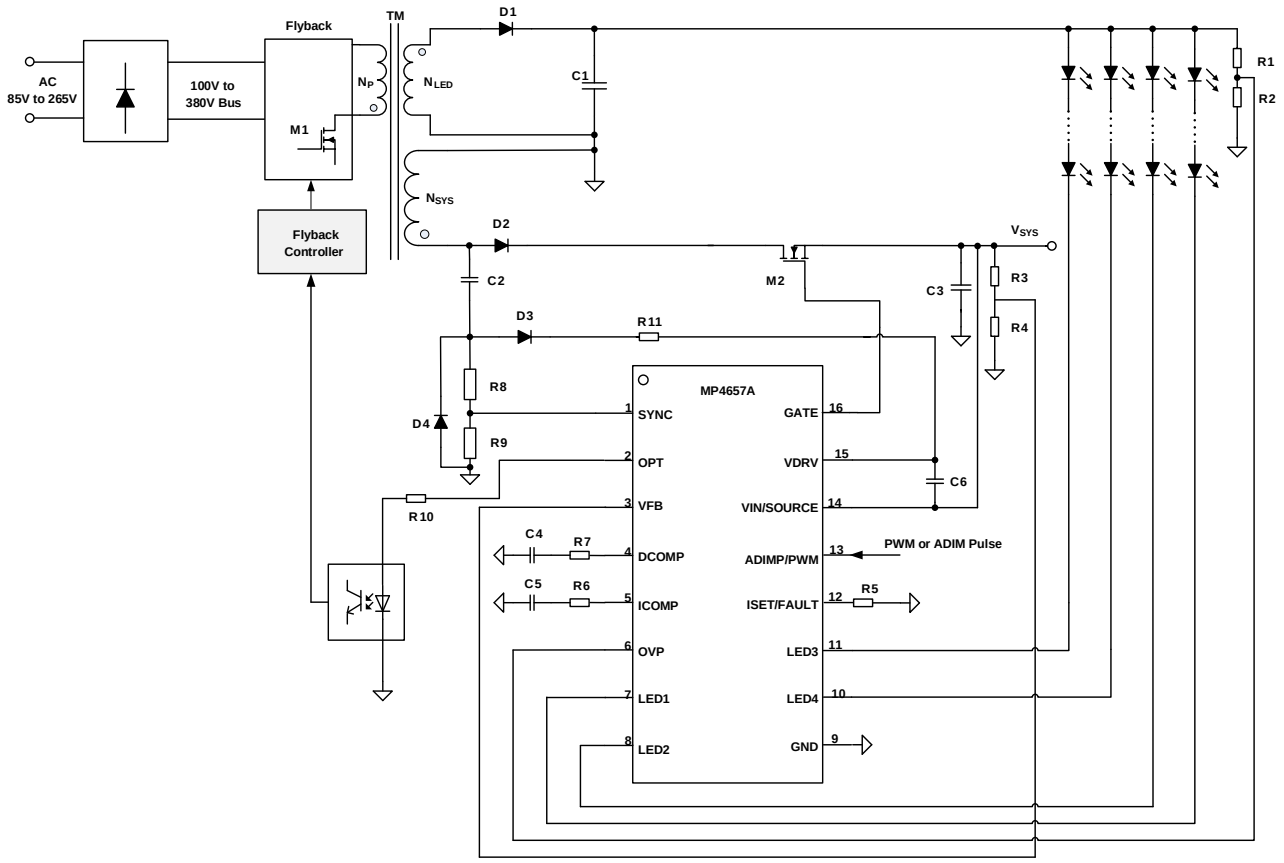
APPLICATIONS

- LCD Monitors and TVs
- Desktop LCD Flat Panel Displays
- Flat Panel Video Displays

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TYPICAL APPLICATION



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ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MP4657AGS	SOIC-16	*See Below*	2

* For Tape & Reel, add suffix -Z (e.g. MP4657AGS-Z).

TOP MARKING

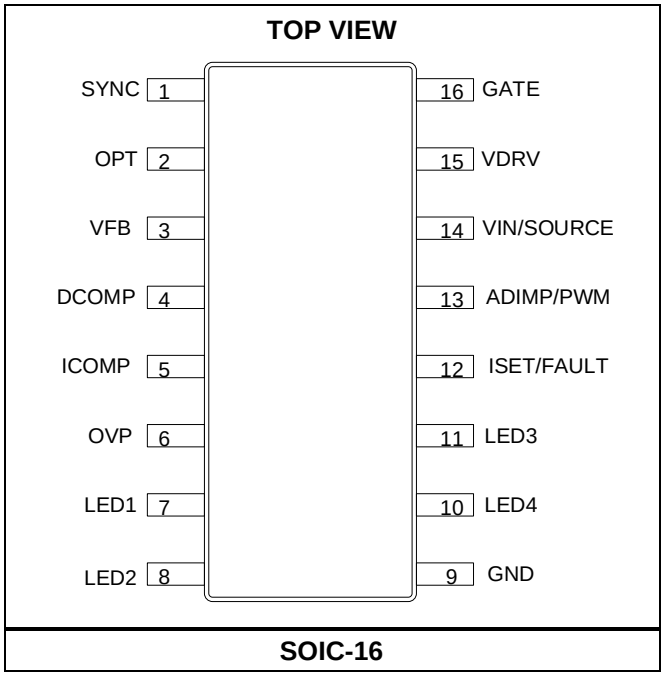
MPSYYWW

MP4657A

LLLLLLLLL

MPS: MPS prefix
YY: Year code
WW: Week code
MP4657A: Part number
LLLLLLLLL: Lot number

PACKAGE REFERENCE



SOIC-16

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PIN FUNCTIONS

Pin #	Name	Description
1	SYNC	**Synchronization pin.** This pin synchronizes the GATE signal to the input signal of the pin. Connect this pin to the secondary side winding of the flyback transformer through a voltage divider. Its falling edge synchronizes the gate signal's shutdown.
2	OPT	**Optical coupler.** This pin outputs the compensation signal. Connect this pin to the external optical coupler to control the flyback.
3	VFB	**System voltage feedback.** Connect this pin to the system voltage through a voltage divider.
4	DCOMP	**Compensation for the system voltage.** When PWM is effective, the DCOMP pin compensates the system voltage control loop and controls the duty cycle of the external N-channel MOSFET. When PWM is ineffective, this pin compensates the system voltage control loop with a different gain and controls the flyback power stage.
5	ICOMP	**Compensation for the LED driver stage.** The ICOMP pin compensates the LED driver loop and controls the flyback power stage when PWM is effective. This pin holds its voltage value when PWM is ineffective.
6	OVP	**Over-voltage protection for the LED driver stage.** Connect this pin to the output of the LED voltage through a voltage divider.
7	LED1	**LED string 1 cathode.**
8	LED2	**LED string 2 cathode.**
9	GND	**Ground.**
10	LED4	**LED string 4 cathode.**
11	LED3	**LED string 3 cathode.**
12	ISET/FAULT	**LED current setting pin and fault indicator.** This pin sets the LED current under normal conditions. Connect a resistor from ISET/FAULT to ground to set the LED current. This pin is pulled low if a fault occurs.
13	ADIMP/PWM	**Dimming signal input pin.**
14	VIN/SOURCE	**Power supply input pin.** The GATE signal is also referred to this pin.
15	VDRV	**Supply voltage for the gate driver.** Bypass this pin to VIN/SOURCE with a ceramic capacitor.
16	GATE	**Gate driver pin.** The GATE signal is referred to the VIN/SOURCE pin. This pin's maximum voltage is limited below 6V (referred to VIN/SOURCE).

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ABSOLUTE MAXIMUM RATINGS (1)

VIN/SOURCE ..... -0.3V to +18V
VDRV ..... -0.3V to +53V
LEDx..... -0.3V to +80V
GATE-VIN/SOURCE ..... -0.3V to +12V
SYNC ..... -6.5V to +6V
OPT ..... -0.3V to +5V
Other pins..... -0.3V to +6.5V
Junction temperature ..... 150°C
Lead temperature ..... 260°C
Storage temperature..... -65°C to +150°C
Continuous power dissipation (T_A = 25°C) (2)
SOIC-16 .....1.56W
Operating frequency ..... 20kHz to 350kHz

ESD Ratings

Human body model (HBM) .....±2000V
Charged device model (CDM).....±1500V

Recommended Operating Conditions (3)

Supply voltage (V_{IN}) ..... 4V to 16V
Operating frequency ..... 20kHz to 350kHz
Operating junction temp (T_J) .... -40°C to +125°C

Thermal Resistance (4) θ_{JA} θ_{JC}

SOIC-16 ..... 80 ..... 35... °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can cause excessive die temperature, and the device may go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

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ELECTRICAL CHARACTERISTICS

V_{IN} = 13V, T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
VIN Supply						
VIN supply range	V_{IN}		4		16	V
VIN UVLO	V_{UVLO_VIN}		3.3	3.6	3.9	V
VIN UVLO hysteresis	$V_{HYS_UVLO_VIN}$			350		mV
Quiescent current	I_Q	PWM = 0, GATE = high, V_{IN} = 5V, no load			0.5	mA
Gate Driver Supply Voltage (VDRV, Referred to VIN/SOURCE, Unless Otherwise Noted)						
Voltage range	V_{DRV}	Refer to GND	6.5		48	V
VDRV UVLO		V_{IN} = 5V	5.3	5.8	6.3	V
Hysteresis for VDRV UVLO				210		mV
Gate Driver (Gate for External MOSFET on V_{SYS})						
GATE voltage (refer to VIN/SOURCE)	V_{GATE}	VDRV - VIN/SOURCE = 14V		5.7		V
Output source current	I_{SOURCE_GATEN}	With 1nF load		0.5 (5)		A
Output sink current	I_{SINK_GATEN}	With 1nF load		1 (5)		A
Analog and PWM Dimming (ADIMP/PWM)						
ADIMP/PWM logic high	V_{ADIMP_HI}		1.5		6	V
ADIMP/PWM logic low	V_{ADIMP_LO}				0.7	V
ADIMP/PWM pull-down resistor	R_{ADIMP_DOWN}			1.6		MΩ
Analog dimming input frequency range			5		100	kHz
Duration time to disable LED loop		EN LED		25		ms
SYNC						
SYNC logic high threshold	V_{SYNC_HI}				1.3	V
SYNC logic low threshold	V_{SYNC_LOW}		0.1			V
SYNC input frequency range			20		350	kHz

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ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 13V, T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
OPT						
OPT output voltage range		Normal operation H (typical maximum output voltage during normal operation)		2.3		V
		Normal operation L (typical minimum output voltage during normal operation)		0.8		
OPT output voltage when latched off				3.3		V
Source current capability	I_{OPT}		20			mA
Compensation Loop for LED Driver (ICOMP)						
Gain bandwidth product	GB_I	75pF on ICOMP		1.0 (5)		MHz
Open loop DC gain	A_{V_I}	ICOMP open		70 (5)		dB
Input common-mode range	V_{CM_I}	For design	-0.3 (5)		+4 (5)	V
Transconductance	G_{M_I}	PWM = high		720		µA/V
Saturated output current	I_{SAT_I}			90		µA
Low level clamp voltage	V_{ICOMP_L}	Normal operation	0.93	0.98	1.03	V
High level clamp voltage	V_{ICOMP_H}	Normal operation	2.35	2.47	2.6	V
Output for System Voltage Feedback (VFB)						
Reference voltage	V_{REF_VFB}		1.182	1.2	1.218	V
Leakage current	I_{LKG_VFB}	Normal operation			0.2	µA
System over-voltage protection threshold	V_{OVP_VFB}			124%		V_{REF_VFB}
System open feedback protection threshold		DCOMP saturated		50%		V_{REF_VFB}
System open feedback protection delay time		DCOMP saturated		1024		cycles
Compensation Loop for System Voltage and Duty Cycle of the External MOSFET (DCOMP)						
Gain bandwidth product	GB_V	75pF on DCOMP		1.0 (5)		MHz
Open loop DC gain	A_{V_V}	DCOMP open		70 (5)		dB
Low level clamp voltage	V_{DCOMP_L}	Normal operation	0.93	0.98	1.03	V
High level clamp voltage	V_{DCOMP_H}	Normal operation	2.35	2.48	2.6	V
Transconductance when PWM is on	$G_{M_DCOMP_ON}$	PWM = high		680		µA/V
Transconductance when PWM is off	$G_{M_DCOMP_OFF}$	PWM = low		260		µA/V
Saturated output current when PWM is on	$I_{SAT_DCOMP_ON}$			90		µA
Saturated output current when PWM is off	$I_{SAT_DCOMP_OFF}$			45		µA

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ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 13V, T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
LED Driver Protection (OVP, LED Short)						
LED over voltage protection (OVP) threshold	V_{TH_OVP}		2.25	2.40	2.55	V
OVP threshold hysteresis				200		mV
OVP to latch IC threshold				3		V
LEDx threshold for open LED string mark off		OVP triggered (test mode required)		100		mV
LEDx slow over voltage threshold (for short LED protection)	$V_{TH_LEDxOV_SLOW}$			4.9		V
LED short delay time slow	$t_{D_LEDxOV_SLOW}$			5.8		ms
LEDx fast over voltage threshold	$V_{TH_LEDxOV_FAST}$			20		V
All LED strings short delay time at low voltage				200		ms
All LED strings short delay time at high voltage				12		ms
Thermal protection threshold		Rising edge		150 (5)		°C
Thermal protection hysteresis				25 (5)		°C
LED Current Regulation (V_{LEDx}, I_{SET})						
ISET voltage	V_{ISET}		1.53	1.58	1.63	V
LEDx average current	I_{LED}	R_{ISET} = 320kΩ (trim), 50mA	-1.5%	50	+1.5%	mA
		40% dimming 20mA	-3%	20.3	+3%	mA
Current matching		I_{LED} = 50mA		0.3	2	%
		I_{LED} = 20mA (40%)		0.6	2.5	%
Minimum LEDx regulation voltage	V_{LEDx}	I_{LED} = 200mA		560		mV
		I_{LED} = 60mA		176		mV
Fault voltage (ISET/FAULT pin voltage if a fault occurs)		Fault condition occurs			0.2	V

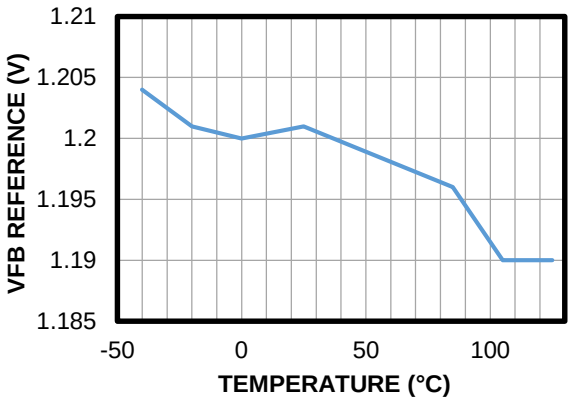
Note:

5) Not tested in production. Guaranteed by characterization.

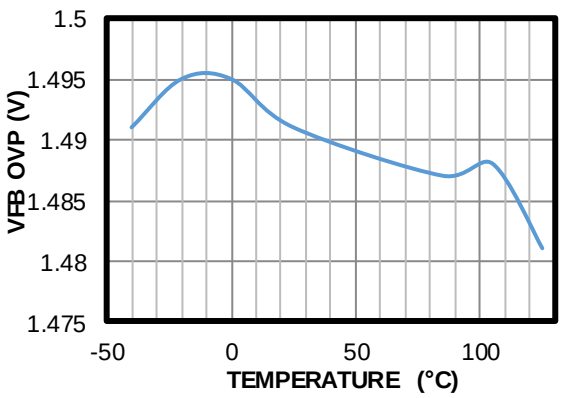
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TYPICAL CHARACTERISTICS

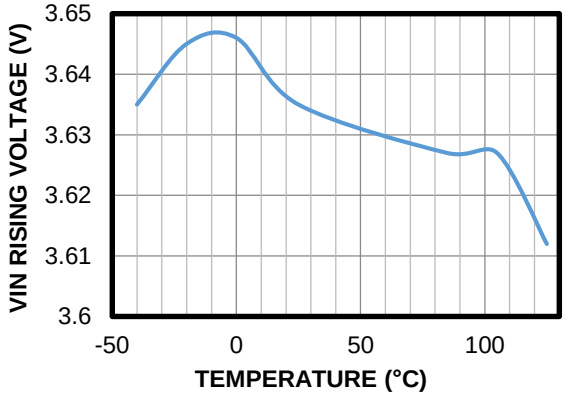
VFB Reference vs. Temperature



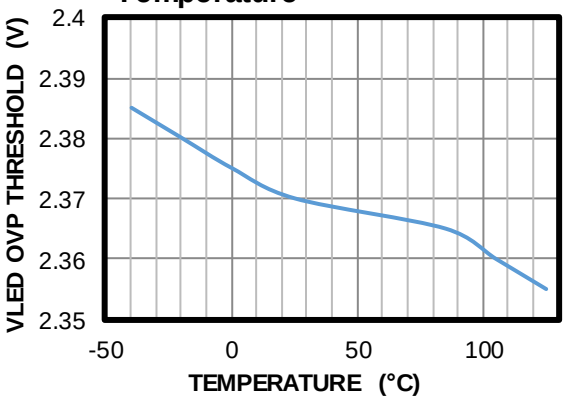
VFB OVP vs. Temperature



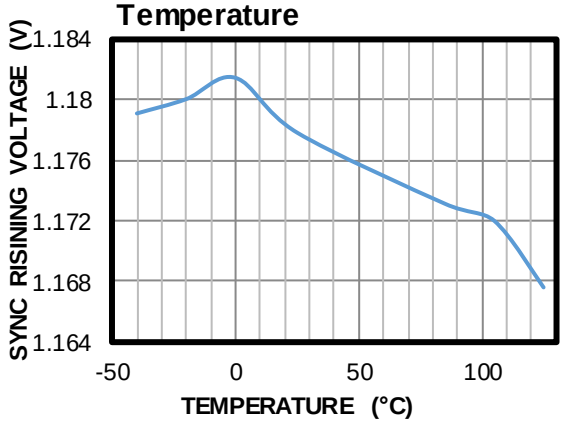
VIN Rising Voltage vs. Temperature



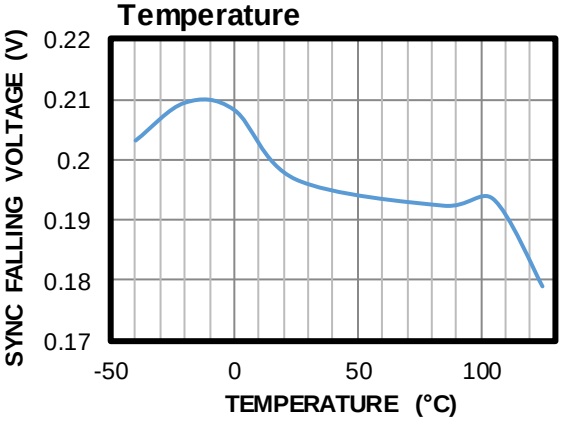
VLED OVP Threshold vs. Temperature



SYNC Rising Voltage vs. Temperature



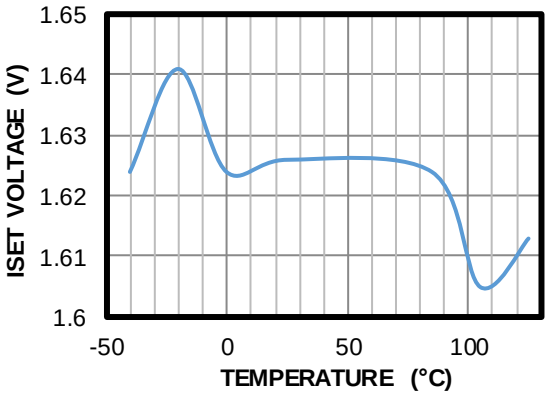
SYNC Falling Voltage vs. Temperature



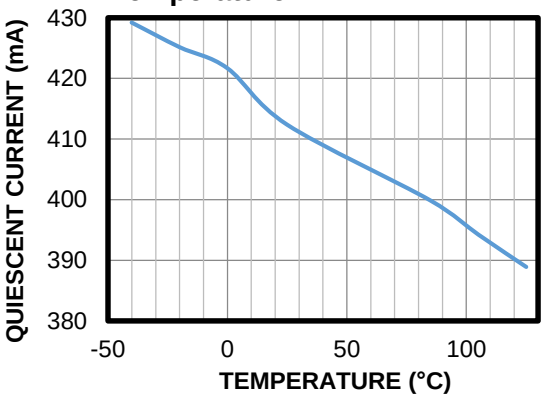
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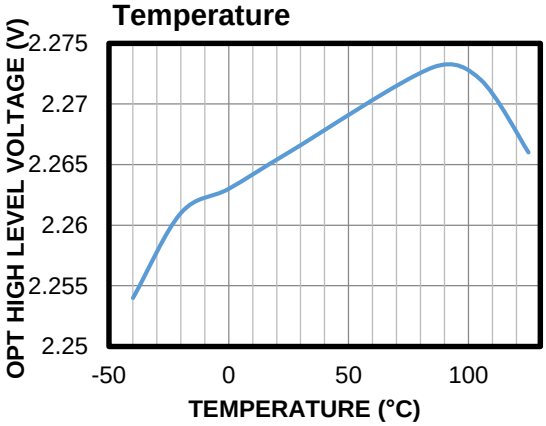
ISET Voltage vs. Temperature



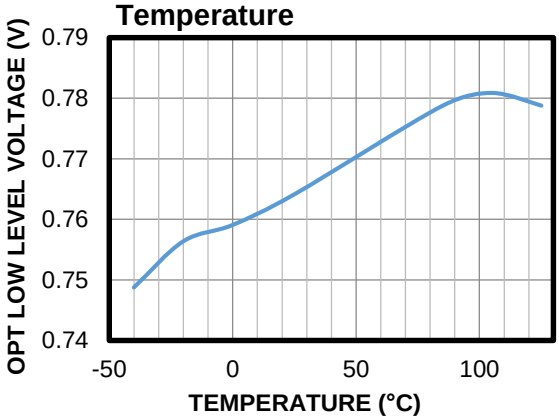
Quiescent Current vs. Temperature



OPT High Level Voltage vs. Temperature



OPT Low Level Voltage vs. Temperature



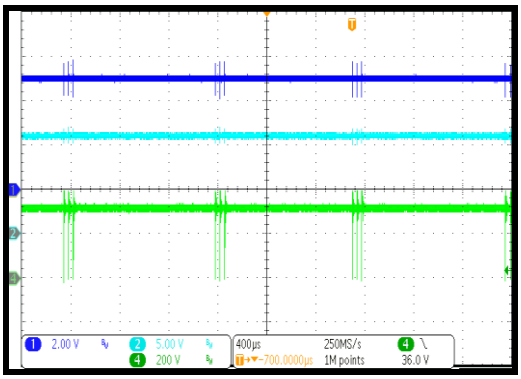
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TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN_AC} = 220V_{AC}, V_{LED} = 44V, 150mA/string, 4 strings, analog dimming, V_{SYS} = 5V, I_{SYS} = 3A, T_A = 25°C, unless otherwise noted.

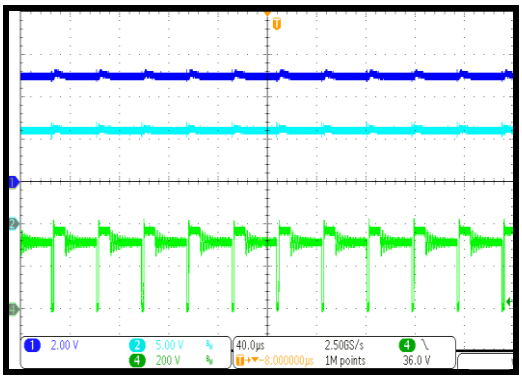
Standby Mode

Constant voltage mode, I_{SYS} = 0mA



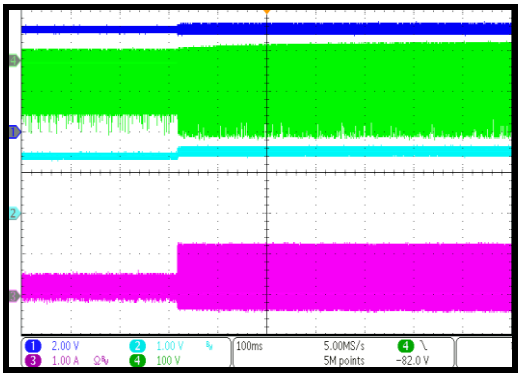
Steady State

Constant voltage mode



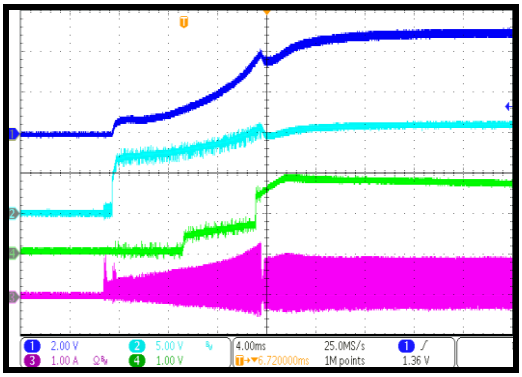
Load Transient

Constant voltage mode, I_{SYS} = 0.2A to 3A



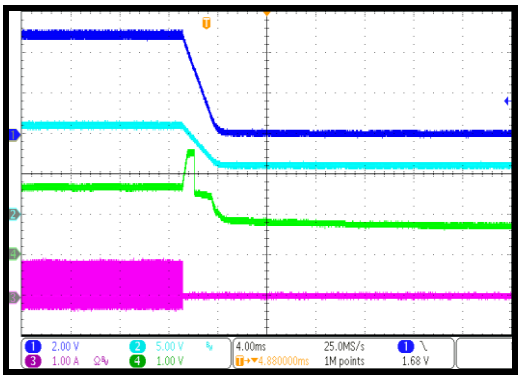
Start-Up

Constant voltage mode

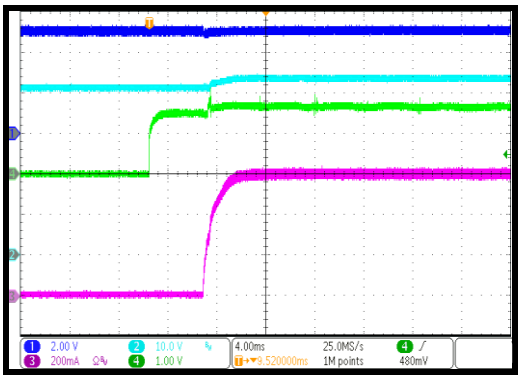


Shutdown

Constant voltage mode



LED Enabled

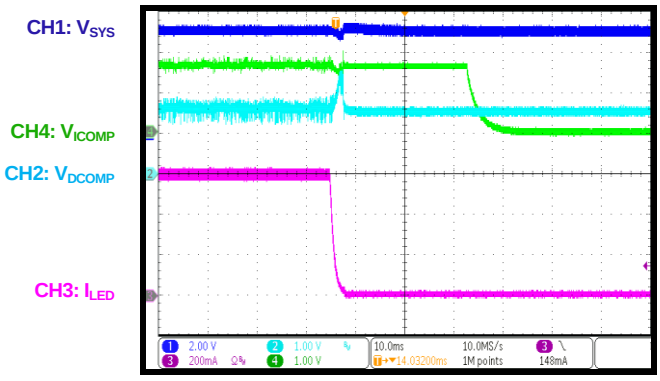


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TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

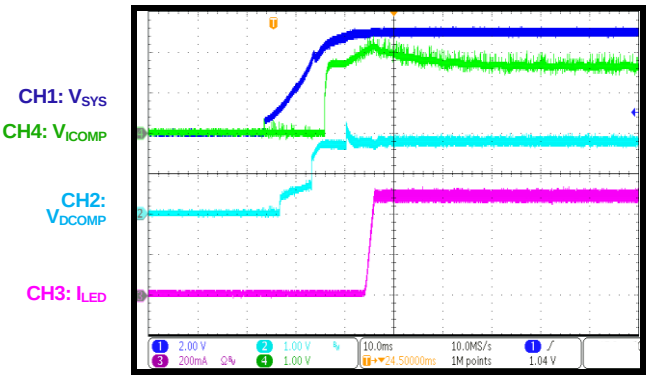
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LED Disabled



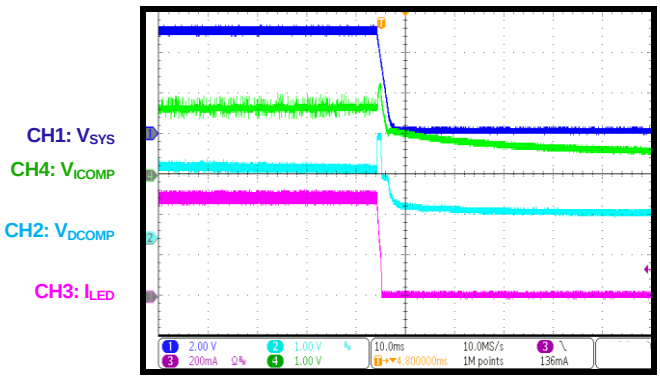
Start-Up

Constant current mode, duty = 80%



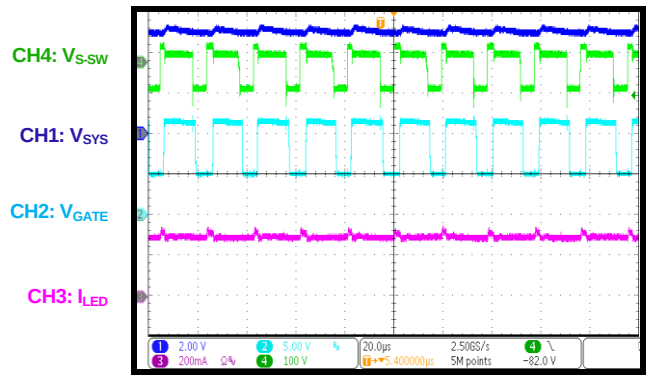
Shutdown

Constant current mode, duty = 80%



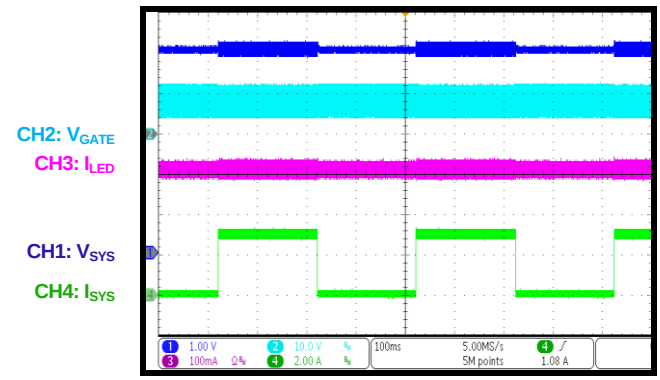
Steady State

Constant current mode, duty = 50%



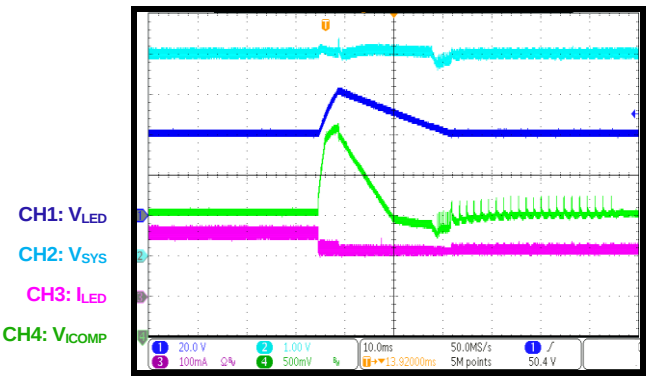
Load Transient

Duty = 50%, I_{SYS} = 0A to 3A



One-String LED Open Fault

Constant current mode, duty = 50%



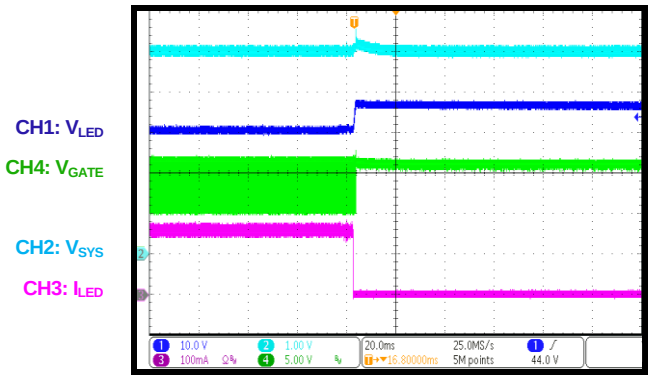
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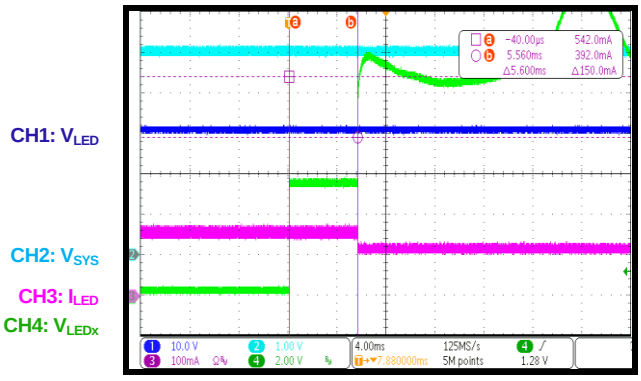
LED String Open Fault (All)

Constant current mode, duty = 25%



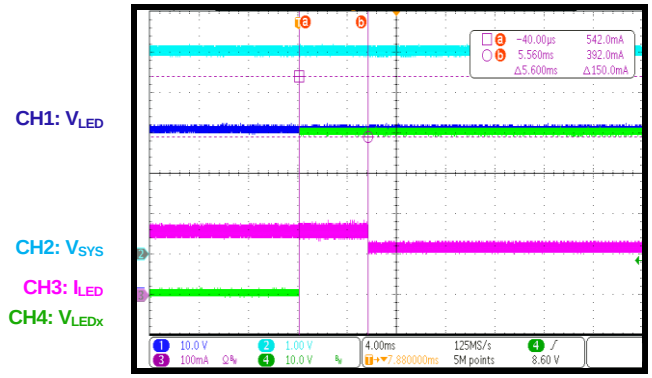
One-String Short Fault (2 LEDs)

Constant current mode, duty = 25%



One-String Short Fault (LED+ to LED-)

Constant current mode, duty = 25%



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FUNCTIONAL BLOCK DIAGRAM

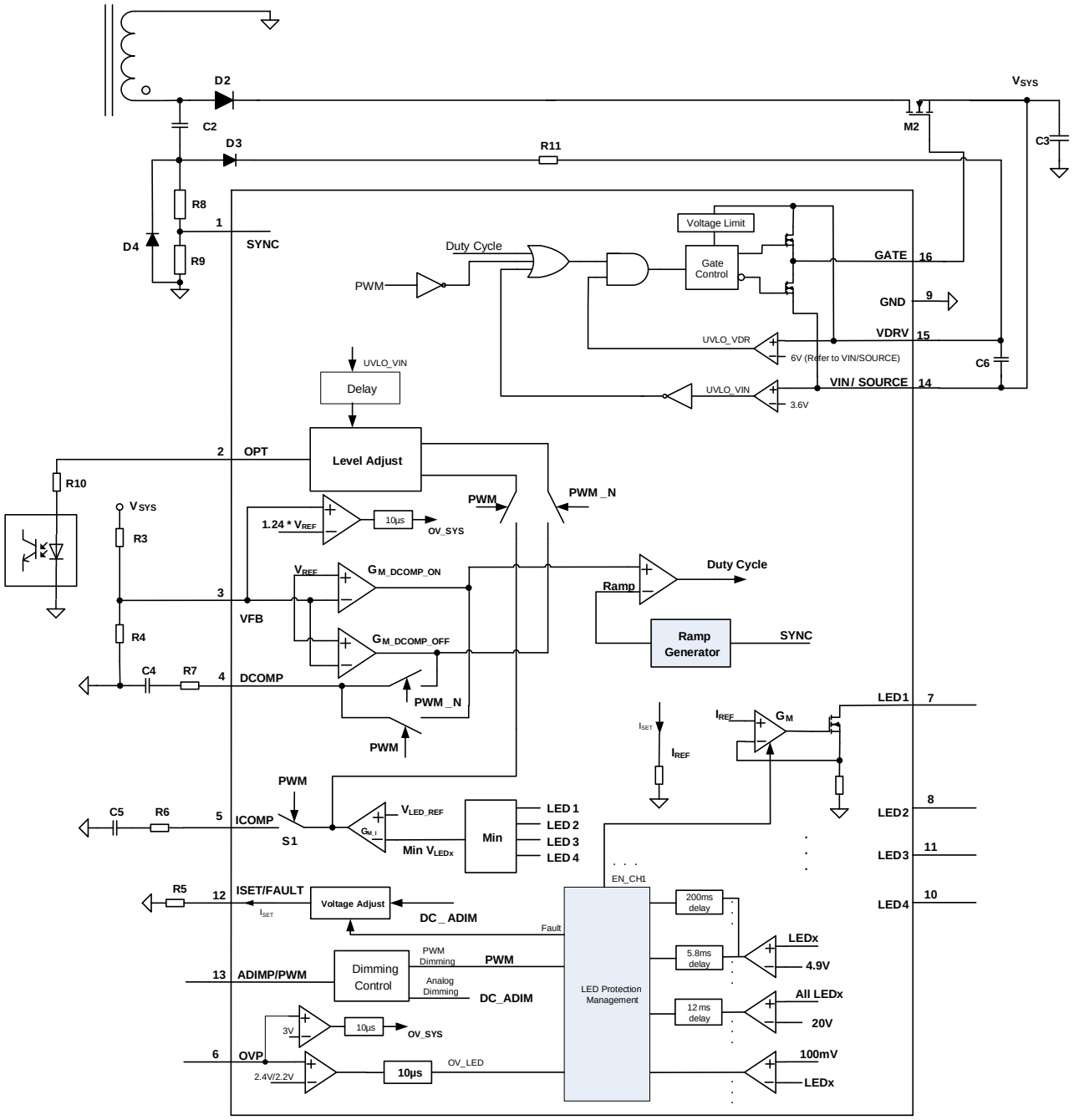


Figure 1: Functional Block Diagram

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OPERATION

The MP4657A is a single-stage flyback, 4-string LED driver and system voltage controller for LED backlighting on the secondary side. It controls the flyback power stage and an external N-channel MOSFET to regulate the system output voltage and LED current loop with integrated 4-string LED current balancing. With a 4V to 16V input voltage (V_{IN}), the device outputs a direct driving signal to control the N-channel MOSFET to regulate the system output voltage. The device also outputs a compensation signal to control the primary-side flyback (or other power stage) through an optocoupler.

The device uses an individual control method for both the LED current and system voltage. When the PWM signal is effective, the MP4657A regulates the LED current loop through the flyback power stage and further regulates the system voltage by controlling the turning on and off of the external N-channel MOSFET. Soft switching can be achieved for the N-channel MOSFET to reduce voltage spikes. When the PWM signal is ineffective, the device directly controls the system voltage through the flyback power stage.

Gate Driver and System Start Up

Figure 2 shows the MP4657A's gate driver start-up. VDRV supplies the GATE driver, and the GATE signal's amplitude (refer to VIN/SOURCE) is limited to 6V.

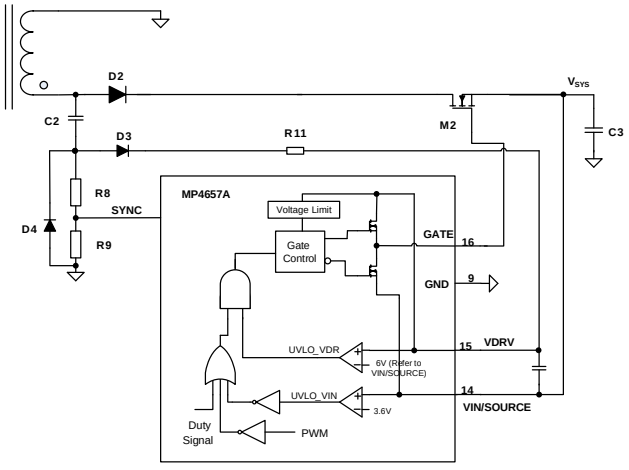


Figure 2: MP4657A Gate Driver and Start Up

Before start-up, the VIN/SOURCE voltage is below the under-voltage lockout (UVLO) threshold, and the MP4657A monitors the VDRV voltage. After VDRV reaches its UVLO threshold, the MP4657A turns on the external N-channel MOSFET to regulate V_{SYS}. The VIN/SOURCE voltage is charged until it reaches its UVLO threshold. Then the system logic starts to work. Next, the duty cycle signal and the PWM signal determine whether the external N-channel MOSFET should be turned on or off.

Switching Sequence and Soft-Switching

Figure 3 shows the MP4657A's operating sequence. The device GATE signal's falling edge is synchronized to the primary flyback gate signal's rising edge through the SYNC pin.

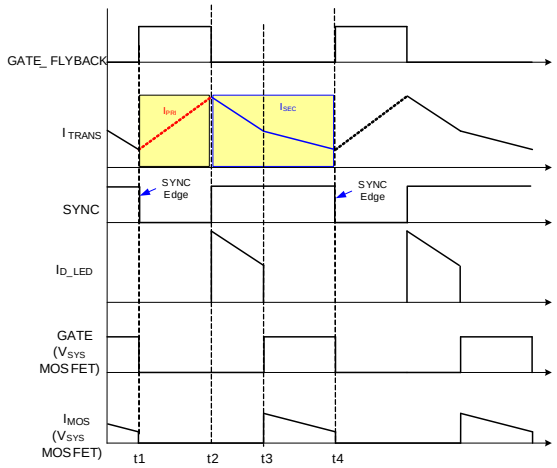


Figure 3: MP4657A Switching Sequence

The falling edge of the SYNC signal synchronizes the falling edge of the GATE signal. This means that the N-channel MOSFET turns off when the primary-side flyback switch turns on. For most applications, the N-channel MOSFET turns off when the secondary side winding current is as low as 0A, thus voltage spikes are less likely to occur. The GATE signal's turning on and duty cycle are controlled by the DCOMP. Before the N-channel MOSFET turns on, the secondary-side current goes through the LED winding. When the N-channel MOSFET turns on, the secondary-side current starts to transfer from the LED winding to the system voltage winding. Because there is leakage inductance, the N-channel MOSFET can turn on with zero current. Therefore, the switching loss for the N-channel MOSFET is very small.

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LED Current and System Voltage Regulation

The MP4657A accurately regulates both the LED current loop and the system voltage with a single flyback power stage.

When the PWM signal is ineffective and the LED stage is disabled, the MP4657A regulates the system output voltage by controlling the flyback power stage and the N-channel MOSFET is fully on (see Figure 4).

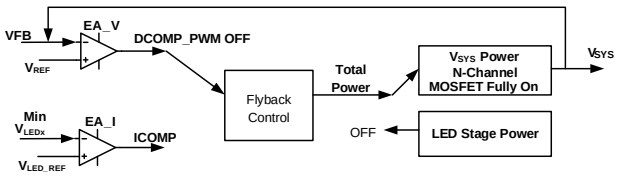


Figure 4: MP4657A Control Scheme when PWM Signal is Ineffective

When the PWM signal is effective, the MP4657A regulates the LED current loop through the flyback power stage (see Figure 5). The system voltage is regulated through the duty cycle control of the N-channel MOSFET. The integrated, individual control for the N-channel MOSFET achieves soft switching without voltage spikes.

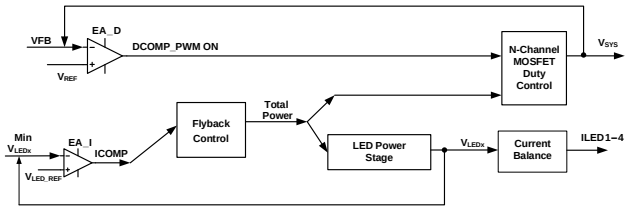


Figure 5: MP4657A Control Scheme when PWM Signal is Effective

LED Current Loop Regulation when PWM Signal is Effective (ICOMP Loop)

In the LED current regulation loop, the minimum V_{LEDx} is fed back and compared to the internal reference V_{LED_REF} (this reference changes with the set current). The internal error amplifier (EA) regulates the average value of the minimum V_{LEDx} to the V_{LED_REF}. EA's output is connected to the external current-loop compensation network on the ICOMP pin through an inner switch (S1).

When PWM signal is effective, S1 is on, and the output of the error amplifier is connected to the external compensation network on the ICOMP pin. The minimum V_{LEDx} is regulated by this control loop and the flyback power is configured by the ICOMP voltage. When PWM signal is ineffective, S1 turns off and the compensation network on ICOMP is disconnected from the error amplifier. ICOMP holds its voltage value until the PWM signal is effective again. The error amplifier output is pulled low when PWM is ineffective.

System Output Voltage Regulation (DCOMP Loop)

The system voltage is fed back to the VFB pin through a voltage divider. When PWM signal is ineffective, the MP4657A regulates the system voltage by controlling the flyback power stage while the N-channel MOSFET is fully on. The internal voltage loop error amplifier regulates the average value of the V_{FB} voltage to the reference voltage. The error amplifier output is connected to the external voltage loop compensation network on the DCOMP pin. The system voltage is regulated by this control loop, and the flyback power is configured by the DCOMP voltage.

When PWM signal is effective, the flyback power is controlled by ICOMP, and the system voltage is regulated by DCOMP controlling the N-channel MOSFET's duty cycle. The VFB pin feeds back the system voltage, which is compared to the internal reference voltage. The error amplifier outputs an error signal to the DCOMP pin. The error amplifier's gain when PWM is effective is different from that when PWM is ineffective. The DCOMP voltage determines the duty cycle of the N-channel MOSFET (see Figure 6).

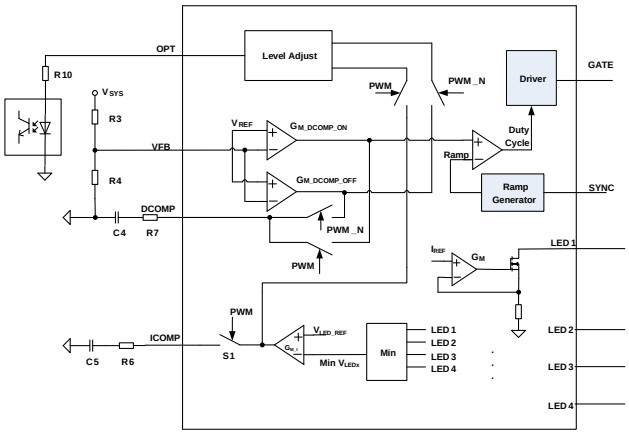


Figure 6: MP4657A Control Diagram

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Dimming Control

The MP4657A provides analog dimming and PWM dimming for the LED current through the ADIMP/PWM pin. For analog dimming, apply a pulse signal with frequency exceeding 5kHz to this pin. In this mode, the PWM signal is always effective unless it is removed. The duty cycle of the PWM signal configures the LED current amplitude. For PWM dimming, apply a pulse signal with frequency below 5kHz to this pin. In this mode, the PWM signal is effective when the pulse is high and is ineffective when the pulse is low. The LED current is chopped by the PWM signal.

Protections

The MP4657A integrates rich protections for the system voltage stage and the LED driver stage.

System Voltage Stage Protections

The protections for the system voltage stage include system over-voltage protection (OVP) and feedback open loop protection.

System Over-Voltage Protection (OVP)

The VFB pin senses the system voltage for regulation and over-voltage protection (OVP). If the VFB voltage exceeds the reference voltage by 24%, system OVP is triggered. In this case, if PWM signal is ineffective, the OPT pin is clamped to 3.3V to stop primary switching. If system OVP is triggered when PWM signal is effective, the GATE signal turns off. If OVP pin voltage exceeds 3V, the IC latches off. This function protects the system voltage from damaging the device.

Feedback Open Loop Protection

If the VFB voltage drops below 50% of the reference voltage and DCOMP is saturated for 1024 switching cycles, the IC latches off and the fault indicator is pulled low.

LED Driver Stage Protections

Fault protections for the LED driver stage include LED open protection, LED short protection and LEDx pin short to ground protection.

LED Open Protection

The output voltage of the LED strings is sensed on the OVP pin. LED open protection is achieved by monitoring the OVP pin and LEDx (x = 1~4) voltages. If one or more LED strings have an open condition, the respective LEDx voltage is pulled to ground while the LED voltage keeps increasing until the OVP pin voltage reaches the OVP threshold (about 2.4V). When the OVP pin voltage exceeds 2.4V for 10μs, LED open protection is triggered. The control loop for the LED stage is disabled, and the MP4657A regulates the system voltage as in PWM ineffective condition. The IC marks off the open LED strings that have a V_{LEDx} below 100mV. The remaining LED strings discharge the LED stage output voltage, so the OVP pin voltage decreases. After the voltage drops below the OVP threshold, the LED control loop recovers, and the minimum LEDx voltage of the remaining LED strings is regulated. The fault indicator does not function in this condition when there are functional LED strings.

If all LED strings have an open condition, they are all marked off, and the LED control loop is disabled. The system voltage is regulated as in PWM ineffective condition and the fault indicator is pulled low.

LED Short Protection

The LEDx voltage is monitored for LED short conditions. If an LED string is shorted, the respective LEDx voltage rises. If this voltage exceeds 4.9V for 5.8ms, the IC marks off the string for having a short condition. Meanwhile, all other strings continue working.

If all of the LEDx voltages (except the marked off strings) exceed 4.9V, it takes 200ms to trigger LED short protection. This prevents mis-triggering short protection if OVP is triggered or if the duty cycle of analog dimming changes. If all of the LEDx voltages (except the marked off strings) exceed 20V for 12ms, all LED strings short protection is triggered.

LEDx Short to Ground Protection

If ICOMP is saturated and the LEDx voltage is low for 100ms, the IC triggers LEDx short to ground protection. The LED control loop is disabled and the fault indicator is pulled low.

To recover the LED loop from this fault, toggle the ADIMP/PWM pin. Pull ADIMP/PWM low for longer than 25ms, then pull it high. The fault indictor is reset and the ISET pin sets the LED current.

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Thermal Protection

Thermal protection is integrated in the MP4657A. If the die temperature exceeds the over-temperature threshold, the IC stops working until the die temperature drops to its safe range. Then the IC returns to normal operation.

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APPLICATION INFORMATION

Gate Signal Synchronization (SYNC)

The SYNC pin synchronizes the GATE signal. Its falling edge synchronizes the GATE signal's turning off. Connect a voltage divider from the secondary winding to this pin to indicate the turning on of the primary-side MOSFET.

System Voltage Feedback (VFB)

The VFB pin feeds back the system voltage. Connect this pin to the system voltage with a voltage divider. This voltage divider determines the system voltage, calculated with Equation (1):

$$V_{SYS} = \frac{1.2V \times (R_{VFBH} + R_{VFBL})}{R_{VFBL}} \quad (1)$$

Where R_{VFBH} and R_{VFBL} are the high-side and low-side resistor of the voltage divider, respectively.

The VFB pin is monitored for system over-voltage protection. If the VFB voltage exceeds the reference voltage by 24% for 10µs, system OVP is triggered.

LED Open Protection

The OVP pin monitors the output LED voltage and can trigger LED open protection. Connect this pin to the output LED voltage through a voltage divider. The over-voltage protection threshold can be estimated with Equation (2):

$$V_{OV_LED} = \frac{2.4V \times (R_{OVPH} + R_{OVPL})}{R_{OVPL}} \quad (2)$$

Where R_{OVPH} and R_{OVPL} are the high-side and low-side resistors of the voltage divider, respectively.

LED Current Setting (ISET/FAULT)

The LED current (I_{LED}) is set by the resistor on the ISET/FAULT pin. The ISET/FAULT pin outputs a 1.6V voltage and its sourcing current determines each channel's LED current. I_{LED} can be estimated with Equation (3):

$$I_{LED}(mA) = \frac{80k\Omega \times 200mA}{R_{ISET}(k\Omega)} \quad (3)$$

Gate Driver Supply and GATE (VDRV, GATE)

The VDRV pin supplies power to the gate driver (refer to the VIN/SOURCE pin). Connect a sufficient voltage source to this pin to supply the gate driver, and bypass this supply to the VIN/SOURCE pin with a 1µF ceramic capacitor. The VDRV pin can handle a maximum 53V voltage (refer to GND), and the GATE signal is limited to 6V (refer to VIN/SOURCE).

In primary flyback power stage applications, the VDRV can generally be supplied from the secondary side winding of the power transformer.

Connect the GATE signal to the N-channel MOSFET directly or using a driving resistor.

Selecting the Turn Ratios of the Power Transformer

The power transformer includes three power windings: the primary-side winding (N_P), the secondary LED winding (N_{LED}) and the secondary system voltage winding (N_{SYS}). To design the turn ratios of the power transformer, follow the instructions below:

1. Design the turn ratio between the primary-side winding and the secondary LED winding (N_P:N_{LED}).

   The maximum voltage stress on the primary-side switch which occurs at maximum input AC voltage and the maximum output LED voltage can be calculated with Equation (4):

   $$V_{DS_PRI} = 1.414 \times V_{IN_AC_MAX} + (V_{OV_LED} + V_{DIODE}) \times \frac{N_p}{N_{LED}} \quad (4)$$

   Where $V_{IN_AC_MAX}$ is the maximum input AC voltage, V_{DIODE} is the forward voltage of the rectifier diode, and V_{OV_LED} is over-voltage protection point of the output LED voltage.

   Consider the leakage inductance of the flyback transformer, and assume there is a 60V spike voltage on the primary-side switch, as well as a 10% derating of the switch voltage capability. V_{DS_PRI} can be estimated with Equation (5):

   $$V_{DS_PRI} + 60 \le 0.9 \times V_{RATING_PRI} \quad (5)$$

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Where V_{RATING_PRI} is the rating voltage of the primary switch.

Calculate N_P:N_{LED} with Equation (6):

$$N_P : N_{LED} = \frac{(0.9 \times V_{RATING_PRI} - 60V - 1.414 \times V_{IN_AC_MAX})}{V_{OV_LED} + V_{DIODE}} \quad (6)$$

2. Design the turn ratio between the LED winding and the system voltage winding (N_{LED}:N_{SYS}).

   Ensure that the system voltage is below the reflecting voltage from the LED winding under the minimum output LED voltage. This relationship can be estimated with Equation (7):

$$V_{SYS} + V_{DIODE} < \frac{V_{LED_MIN} + V_{DIODE}}{\frac{N_{LED}}{N_{SYS}}} \quad (7)$$

   Where V_{LED_MIN} is the minimum output LED voltage. Choose a 15% margin for production design, calculated with Equation (8):

$$N_{LED} : N_{SYS} = \frac{0.85 \times (V_{LED_MIN} + V_{DIODE})}{V_{SYS} + V_{DIODE}} \quad (8)$$

Selecting the External N-Channel MOSFET

The voltage stress on the external N-channel MOSFET can be estimated with Equation (9):

$$V_{DS_EXT} = \frac{1.414 \times V_{IN_AC_MAX} \times N_{SYS}}{N_p} + V_{SYS} \quad (9)$$

The maximum voltage stress occurs at the maximum input AC voltage. Considering the small voltage spike and the derating of the MOSFET voltage, choose a 20% margin. Estimate the voltage rating of the external N-channel MOSFET with Equation (10):

$$V_{RATING_EXT} = \left(\frac{1.414 \times V_{IN_AC_MAX} \times N_{SYS}}{N_P} + V_{SYS}\right) / 0.8 \quad (10)$$

The average current flowing through the N-channel MOSFET is equal to the output current of the system voltage. This flowing current is a pulse waveform, and its RMS current is much greater than the average value. Assume that the RMS current is 1.5 to 2 times greater than the average current, estimated with Equation (11):

$$I_{RMS_EXT} \approx 2 \times I_{SYS} \quad (11)$$

Where I_{RMS_EXT} is the RMS current through the N-channel MOSFET, and I_{SYS} is the output current of the system output voltage.

The switching loss from the N-channel MOFET's soft switching is generally low. The rating current for the N-channel MOSFET should be 2 to 3 times of the RMS current.

Consider thermal loss and power loss when selecting the $R_{DS(ON)}$ and package size for the N-channel MOSFET.

PCB Layout Guidelines

Efficient PCB layout is important to achieve reliable operation, good EMI performance and excellent thermal performance. For the best results, follow the guidelines below:

1. Minimize the power stage loop area. This includes the primary loop (input capacitor, transformer, and MOSFET-sense resistor), as well as the secondary winding loop (transformer, rectifier, and diode-output capacitor).
2. The output loop GND and control circuit GND should be separated, and only connected at GND pin.
3. Place the peripheral electronic components (such as those for VIN/SOURCE, VFB, SYNC, DCOMP, and ICOMP) close to the IC to decouple noise.

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TYPICAL APPLICATION CIRCUT

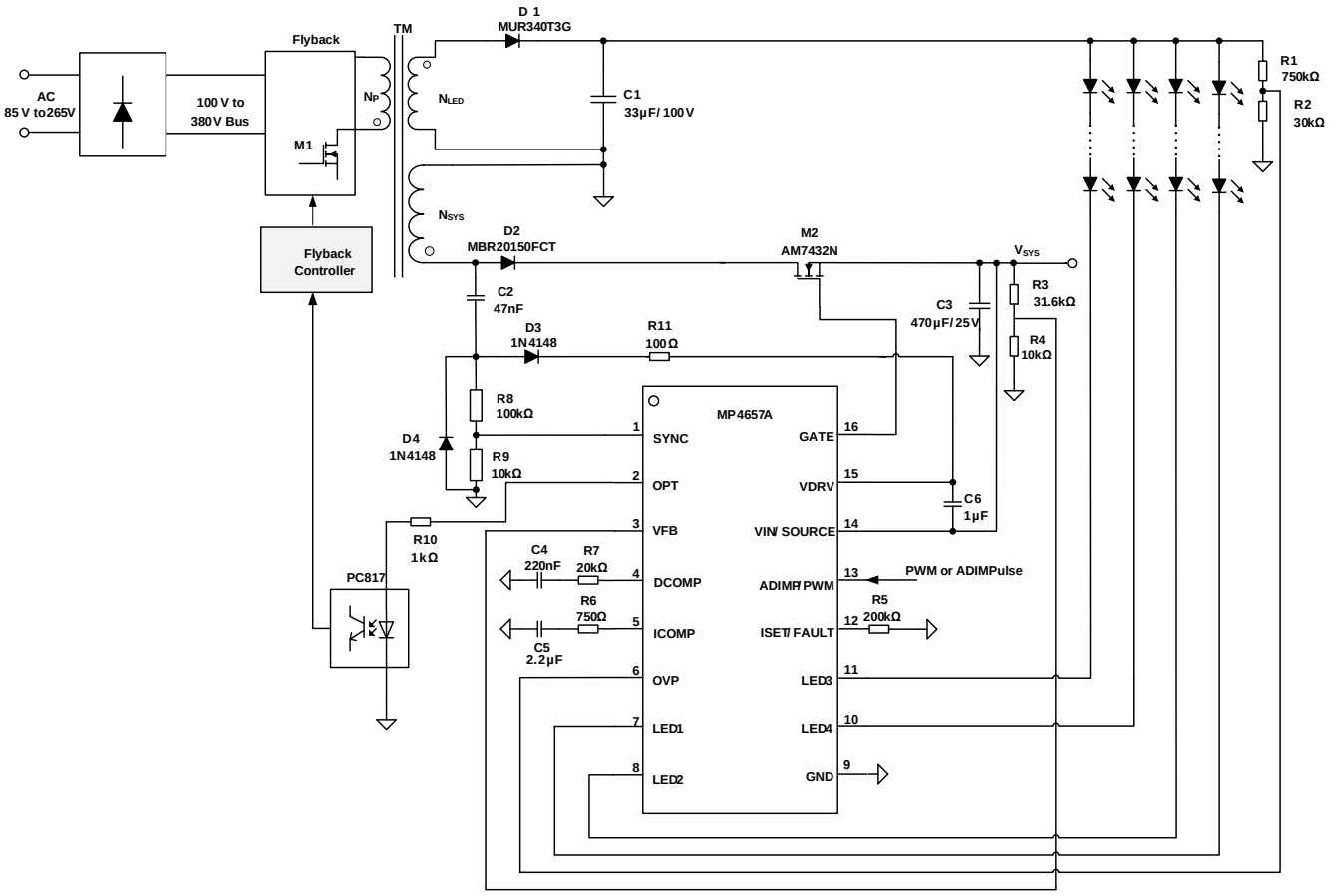
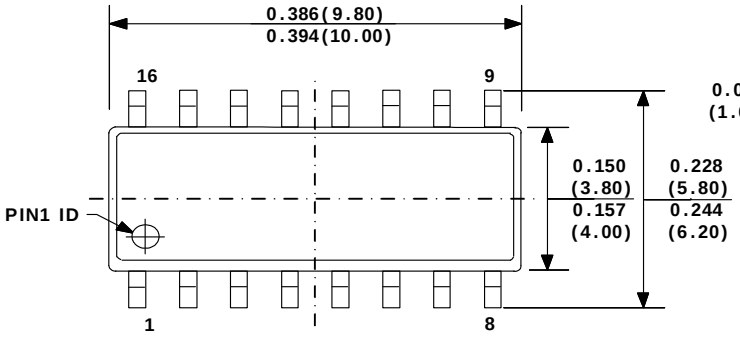


Figure 7: Typical Application Circuit (MP4657A Flyback 4-String LED Driver and System Voltage Regulation Scheme)

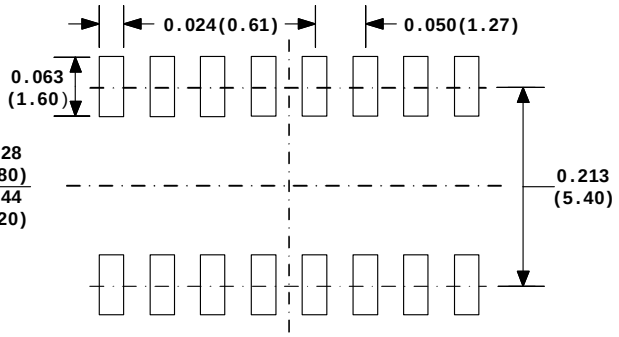
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PACKAGE INFORMATION

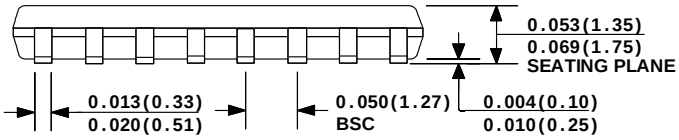
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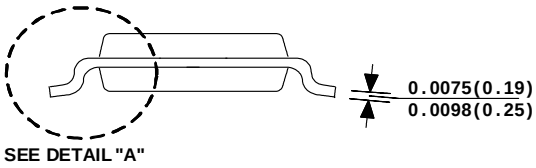
TOP VIEW



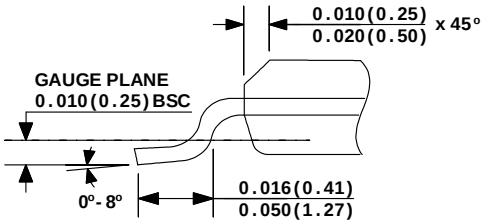
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW



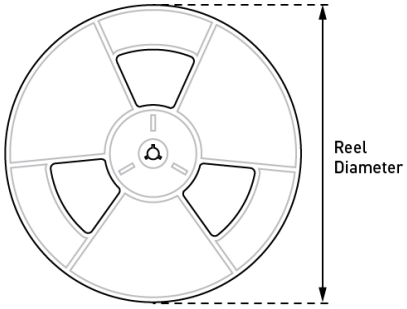
DETAIL "A"

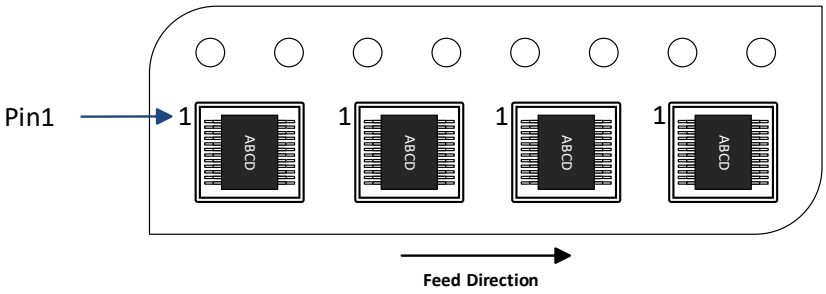
NOTE:

1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURR.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
5) DRAWING CONFORMS TO JEDEC MS-012, VARIATION AC.
6) DRAWING IS NOT TO SCALE.

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CARRIER INFORMATION





Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP4657AGS-Z	SOIC-16	2500	50	N/A	13in	16mm	8mm

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REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	11/03/2021	Initial Release	-

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