MP4657B

Single-Stage Flyback, 4-String LED Driver and System Voltage Controller

DESCRIPTION

The MP4657B is a single-stage flyback, 4-string LED driver and system voltage controller for LED backlighting on the secondary side. The device controls the flyback power stage and an external N-channel MOSFET to regulate the system supply voltage and LED current loop with integrated 4-string LED current balancing. With a 4V to 16V input voltage (V_{IN}), the device outputs a direct driving signal to control the N-channel MOSFET for regulating the system supply voltage. The device also outputs a compensation signal to control the primary-side flyback (or other power stage) through an optocoupler.

The MP4657B induces pulse-width modulation (PWM) dimming and analog dimming to the LED current through the ADIMP/PWM pin. For analog dimming, apply a pulse signal with a >5kHz frequency to this pin. For PWM dimming, apply a pulse signal with a <5kHz frequency.

The device uses an individual control method for the LED current (I_{LED}) and system voltage (V_{SYS}). When the PWM signal is effective, the MP4657B regulates the I_{LED} loop through the flyback power stage and further regulates V_{SYS} by controlling the N-channel MOSFET. Soft switching for the N-channel MOSFET can be achieved to reduce voltage spikes. When the PWM signal is ineffective, the device directly controls V_{SYS} through the flyback power stage.

The MP4657B features numerous protections to increase system reliability. Protections are utilized for both the system voltage stage and the LED driver stage. LED driver stage protections include LED open protection, LED short protection, and LEDx pin short-to-ground protection. System voltage stage protections include over-voltage protection (OVP) and feedback open-loop protection. The device also offers thermal protection.

The MP4657B is available in an SOIC-16 package.

FEATURES

- Single-Stage Flyback for High-Efficiency LED Current and System Voltage Regulation
- Individual Control Method for the LED Driver Stage and System Voltage Stage
- 4V to 16V Supply Voltage
- 4-String, 80V LED Current Balancing
- 1.5% System Voltage Accuracy
- 1.5% LED Current Accuracy and 2% LED Current Balancing
- High-Efficiency, Low LEDx Regulation Voltage
- Fast Dynamic Control, Fast Response
- System Supply Over-Voltage Protection (OVP)
- System Supply Short Protection
- LED Open, LED Short Protection
- LEDx Pin Short-to-Ground Protection
- Feedback Open-Loop Protection for the System Voltage
- Soft Switching for the External N-Channel MOSFET
- Thermal Protection
- Available in an SOIC-16 Package

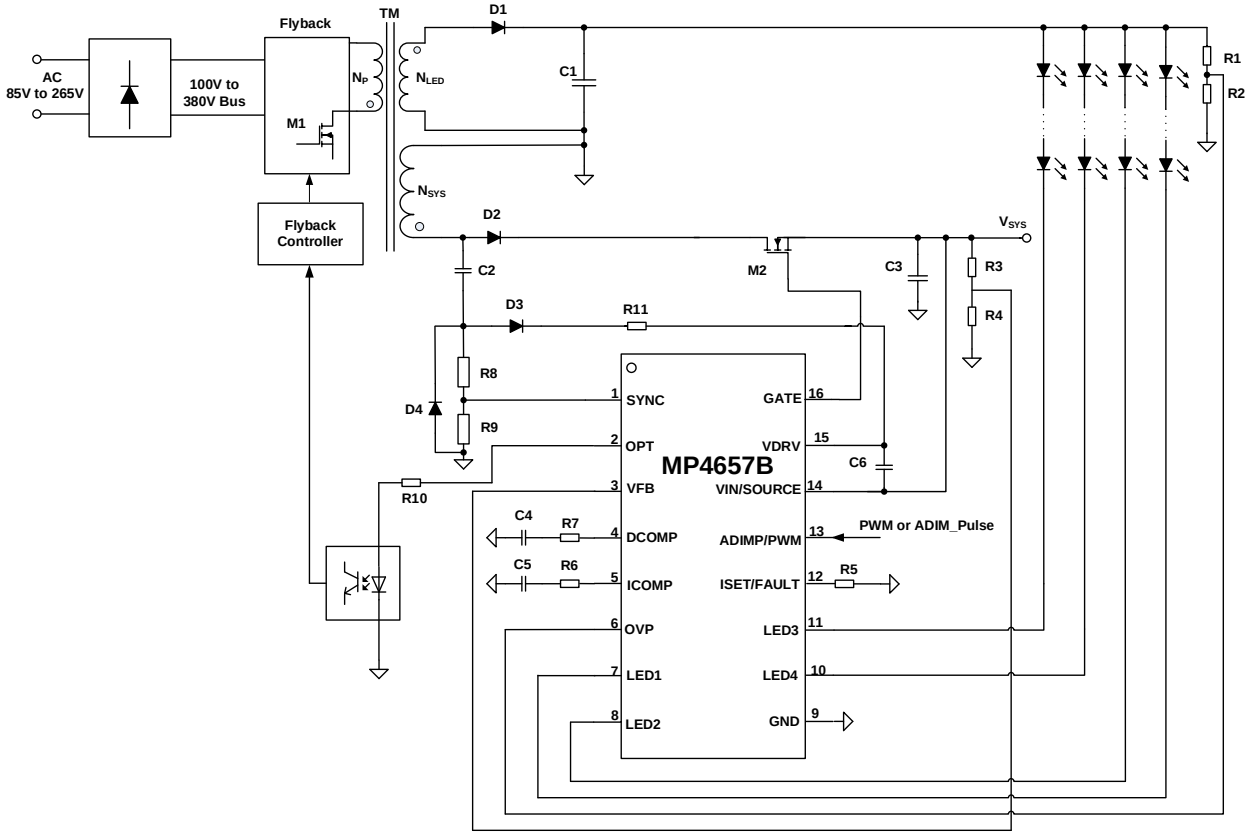
APPLICATIONS

- LCD Monitors and TVs
- Desktop LCD Flat-Panel Displays
- Flat-Panel Video Displays

All MPS parts are lead-free, halogen-free, and adhere to the RoHS directive. For MPS green status, please visit the MPS website under Quality Assurance. “MPS”, the MPS logo, and “Simple, Easy Solutions” are trademarks of Monolithic Power Systems, Inc. or its subsidiaries.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2021 MPS. All Rights Reserved.

TYPICAL APPLICATION



MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2021 MPS. All Rights Reserved.

ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MP4657BGS	SOIC-16	*See Below*	2

* For Tape & Reel, add suffix -Z (e.g. MP4657BGS-Z).

TOP MARKING

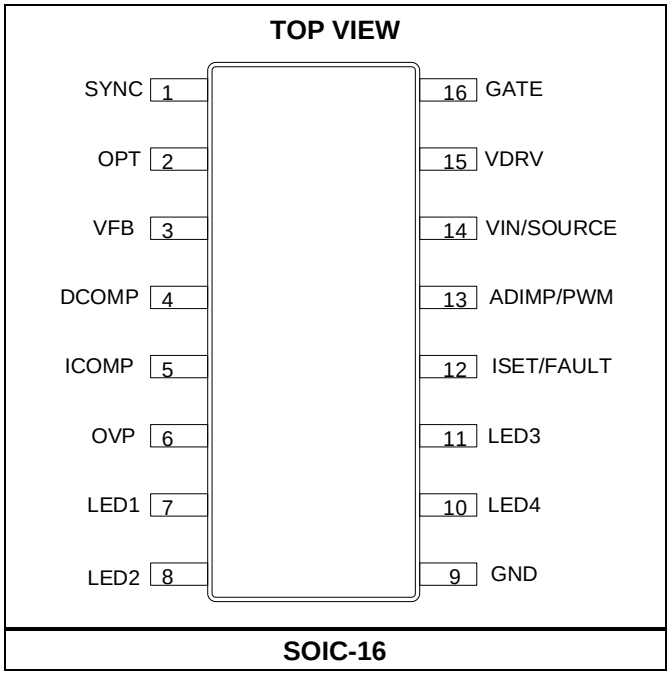
MPSYYWW

MP4657B

LLLLLLLLL

MPS: MPS prefix
YY: Year code
WW: Week code
MP4657B: Part number
LLLLLLLLL: Lot number

PACKAGE REFERENCE



SOIC-16

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2021 MPS. All Rights Reserved.

PIN FUNCTIONS

Pin #	Name	Description
1	SYNC	**Synchronization pin.** This pin synchronizes the gate signal to the input signal of SYNC pin. Connect this pin to the secondary-side winding of the flyback transformer through a voltage divider. Its falling edge synchronizes the gate signal turning off.
2	OPT	**Optocoupler.** This pin outputs the compensation signal. Connect this pin to the external optocoupler to control the flyback.
3	VFB	**System voltage feedback.** Connect this pin to the system voltage (V_{SYS}) through a voltage divider.
4	DCOMP	**Compensation for the system voltage.** When PWM is effective, the DCOMP pin compensates the system voltage control loop, and controls the duty cycle of the external N-channel MOSFET. When PWM is ineffective, this pin compensates the system voltage control loop with a differential gain and controls the flyback power stage.
5	ICOMP	**Compensation for the LED driver stage.** The ICOMP pin compensates the LED driver loop and controls the flyback power stage when the PWM signal is effective. This pin holds its voltage value when the PWM signal is ineffective.
6	OVP	**Over-voltage protection (OVP) for the LED stage.** Connect this pin to the output of the LED voltage through a voltage divider.
7	LED1	**LED string 1 cathode.**
8	LED2	**LED string 2 cathode.**
9	GND	**Ground.**
10	LED4	**LED string 4 cathode.**
11	LED3	**LED string 3 cathode.**
12	ISET/FAULT	**LED current setting pin and fault indicator.** This pin sets the LED current (I_{LED}) under normal conditions. Connect a resistor from the ISET/FAULT pin to ground to set I_{LED}. This pin is pulled low if a fault occurs.
13	ADIMP/PWM	**Dimming signal input pin.**
14	VIN/SOURCE	**Power supply input pin.** The gate signal is also referred to this pin.
15	VDRV	**Supply voltage for the gate driver.** Bypass this pin to VIN/SOURCE with a ceramic capacitor.
16	GATE	**Gate driver pin.** The gate signal is referred to the VIN/SOURCE pin. This pin's maximum voltage is limited below 6V (Referred to VIN/SOURCE).

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2021 MPS. All Rights Reserved.

ABSOLUTE MAXIMUM RATINGS (1)

VIN/SOURCE ..... -0.3V to +18V
VDRV ..... -0.3V to +53V
LEDx..... -0.3V to +80V
GATE - VIN/SOURCE..... -0.3V to +12V
SYNC ..... -6.5V to +6V
OPT ..... -0.3V to +5V
Other pins..... -0.3V to +6.5V
Junction temperature ..... 150°C
Lead temperature ..... 260°C
Storage temperature..... -65°C to +150°C
Continuous power dissipation (T_A = 25°C) (2)
SOIC-16 .....1.56W
Operating frequency ..... 20kHz to 350kHz

ESD Ratings

Human body model (HBM) .....±2000V
Charged device model (CDM).....±1500V

Recommended Operating Conditions (3)

Supply voltage (V_{IN}) ..... 4V to 16V
Operating frequency ..... 20kHz to 350kHz
Operating junction temp (T_J) .... -40°C to +125°C

Thermal Resistance (4) θ_{JA} θ_{JC}

SOIC-16 ..... 80 ..... 35... °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can cause excessive die temperature, and the regulator may go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2021 MPS. All Rights Reserved.

ELECTRICAL CHARACTERISTICS

V_{IN} = 13V, T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
V_{IN} Supply						
V_{IN} supply range			4		16	V
V_{IN} UVLO	V_{UVLO_VIN}		3.3	3.6	3.9	V
V_{IN} UVLO hysteresis	$V_{HYS_UVLO_VIN}$			350		mV
Quiescent current	I_Q	PWM = 0, GATE = high, V_{IN} = 5V, no load			0.5	mA
Gate Driver Supply Voltage (VDRV, Referred to VIN/SOURCE, Unless Otherwise Noted)						
Voltage range	V_{DRV}	Refer to GND	6.5		48	V
VDRV UVLO		V_{IN} = 5V	5.3	5.8	6.3	V
Hysteresis for VDRV UVLO				210		mV
Gate Driver (GATE, for External MOSFET on V_{SYSTEM})						
GATE voltage (refer to VIN/SOURCE)	V_{GATE}	VDRV - VIN/SOURCE = 14V		5.7		V
Output source current	I_{SOURCE_GATEN}	With 1nF load		0.5 (5)		A
Output sink current	I_{SINK_GATEN}	With 1nF load		1 (5)		A
Analog and PWM Dimming (ADIMP/PWM)						
ADIMP/PWM logic high	V_{ADIMP_HI}		1.5		6	V
ADIMP/PWM logic low	V_{ADIMP_LO}				0.7	V
ADIMP/PWM pull-down resistor	R_{ADIMP_DOWN}			1.6		MΩ
Analog dimming input frequency range			5		100	kHz
Duration time to disable the LED loop		EN LED		25		ms
SYNC						
SYNC logic high threshold	V_{SYNC_HI}				1.3	V
SYNC logic low threshold	V_{SYNC_LOW}		0.1			V
SYNC input frequency range			20		350	kHz

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2021 MPS. All Rights Reserved.

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 13V, T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
OPT						
OPT output voltage range		Normal operation H (typical maximum output voltage during normal operation)		2.3		V
		Normal operation L (typical minimum output voltage during normal operation)		0.8		V
OPT output voltage when latched off				3.3		V
Source current capability	I_{OPT}		20			mA
Compensation Loop for LED Driver (ICOMP)						
Gain bandwidth product	GB_I	75pF on ICOMP		1 (5)		MHz
Open-loop DC gain	A_{V_I}	ICOMP open		70 (5)		dB
Input common-mode range	V_{CM_I}	For design	-0.3 (5)		+4 (5)	V
Transconductance	G_{M_I}	PWM=High		720		µA/V
Saturated output current	I_{SAT_I}			90		µA
Low-level clamp voltage	V_{ICOMP_L}	Normal operation		1		V
High-level clamp voltage	V_{ICOMP_H}	Normal operation		2.5		V
Output for System Voltage Feedback (V_{FB})						
Reference voltage	V_{REF_VFB}		1.182	1.2	1.218	V
Leakage current	I_{LKG_VFB}	Normal operation			0.2	µA
System over-voltage protection (OVP) threshold	V_{OVP_VFB}			1.24		V_{REF_VFB}
System open feedback protection threshold		DCOMP saturated		0.5		V_{REF_VFB}
System open feedback protection delay time		DCOMP saturated		1024		cycles
Compensation Loop for System Voltage and Duty Cycle of the Extra MOSFET (DCOMP)						
Gain bandwidth product	GB_V	75pF on DCOMP		1 (5)		MHz
Open-loop DC gain	A_{V_V}	DCOMP open		70 (5)		dB
Low-level clamp voltage	V_{DCOMP_L}	Normal operation		1		V
High-level clamp voltage	V_{DCOMP_H}	Normal operation		2.5		V
Transconductance when the PWM is on	$G_{M_DCOMP_ON}$	PWM = high		680		µA/V
Transconductance when the PWM is off	$G_{M_DCOMP_OFF}$	PWM = low		260		µA/V
Saturated output current when the PWM is on	$I_{SAT_DCOMP_ON}$			90		µA
Saturated output current when the PWM is off	$I_{SAT_DCOMP_OFF}$			45		µA

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2021 MPS. All Rights Reserved.

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 13V, T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
LED Driver Protection (OVP, LED Short)						
LED over-voltage protection (OVP) threshold	V_{TH_OVP}		2.25	2.40	2.55	V
OVP threshold hysteresis				200		mV
OVP to latch IC threshold				3		V
LEDx UVLO threshold	V_{LEDX_UVLO}	OVP triggered (test mode required)		100		mV
LEDX slow over-voltage (OV) threshold (for LED short protection)	$V_{TH_LEDxOV_SLOW}$			4.9		V
LED short delay time slow	$t_{D_LEDxOV_SLOW}$			5.8		ms
LEDx fast OV threshold	$V_{TH_LEDxOV_FAST}$			20		V
All LED strings short delay time at low voltages				200		ms
All LED strings short delay time at high voltages				12		ms
Thermal protection threshold		Rising edge		150 (5)		°C
Thermal protection hysteresis				25 (5)		°C
LED Current Regulation (V_{LEDx}, I_{SET})						
ISET voltage	V_{ISET}		1.53	1.58	1.63	V
LEDx average current	I_{LED}	R_{ISET} = 320kΩ (trim), 50mA	-1.5%	50	+1.5%	mA
		40% dimming, 20mA	-3%	19.2	+3%	mA
Current matching		I_{LED} = 50mA		0.3	2	%
		I_{LED} = 20mA (40%)		0.6	2.5	%
Minimum LEDx regulation voltage	V_{LEDx}	I_{LED} = 200mA		560		mV
		I_{LED} = 60mA		176		mV
Fault voltage (ISET/FAULT pin voltage if a fault occurs)		Fault condition occurs			0.2	V

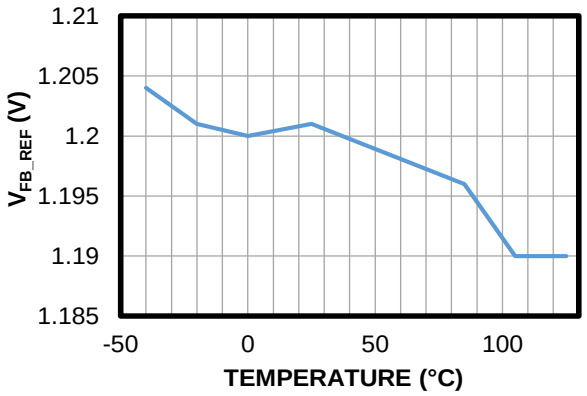
Note:

5) Not tested in production. Guaranteed by characterization.

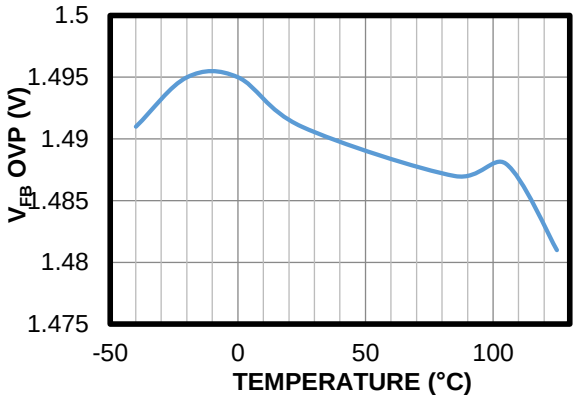
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2021 MPS. All Rights Reserved.

TYPICAL CHARACTERISTICS

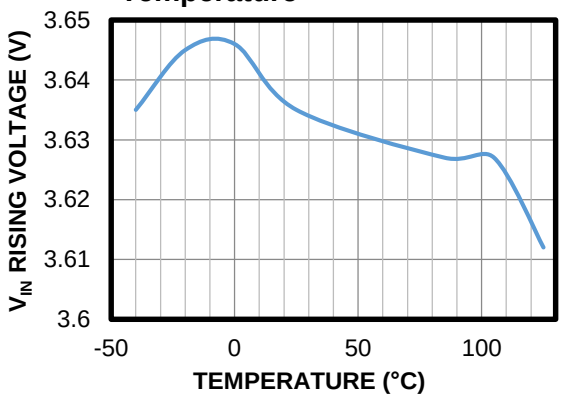
V_{FB} Reference vs. Temperature



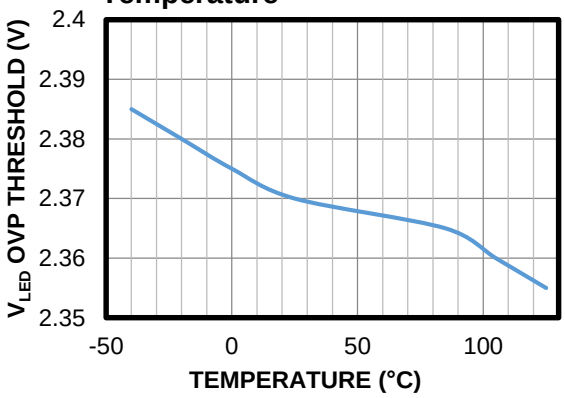
V_{FB} OVP vs. Temperature



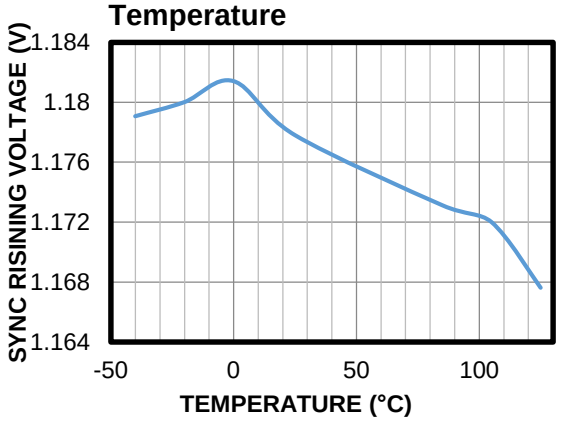
V_{IN} Rising Voltage vs. Temperature



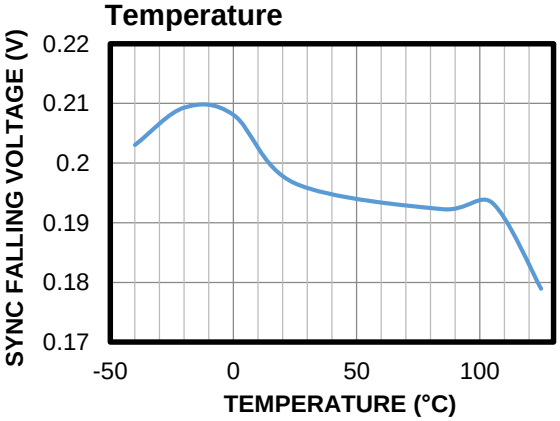
V_{LED} OVP Threshold vs. Temperature



SYNC Rising Voltage vs. Temperature



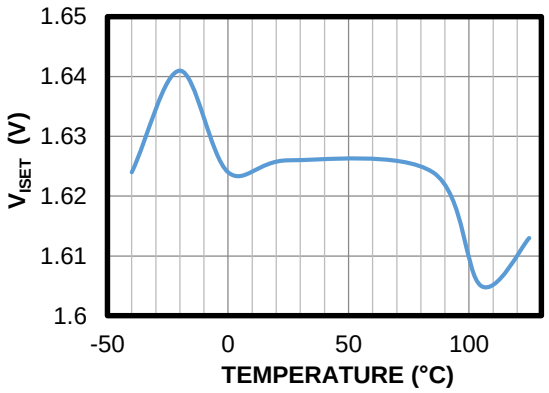
SYNC Falling Voltage vs. Temperature



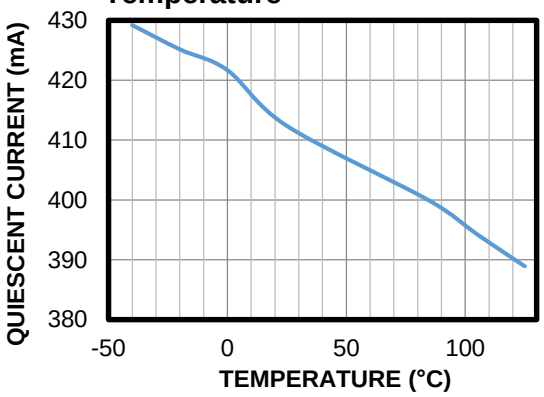
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2021 MPS. All Rights Reserved.

TYPICAL CHARACTERISTICS *(continued)*

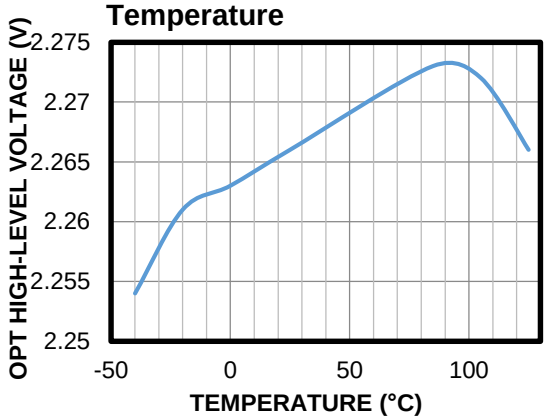
ISET Voltage vs. Temperature



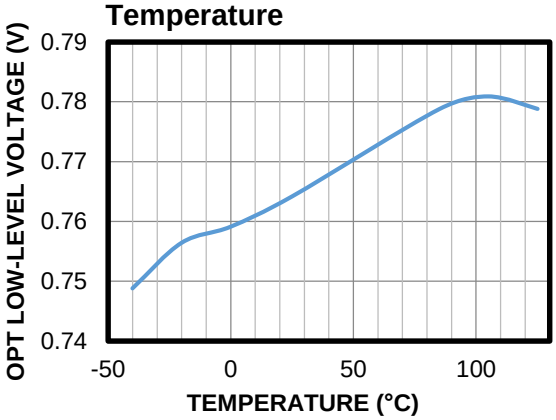
Quiescent Current vs. Temperature



OPT High-Level Voltage vs. Temperature



OPT Low-Level Voltage vs. Temperature



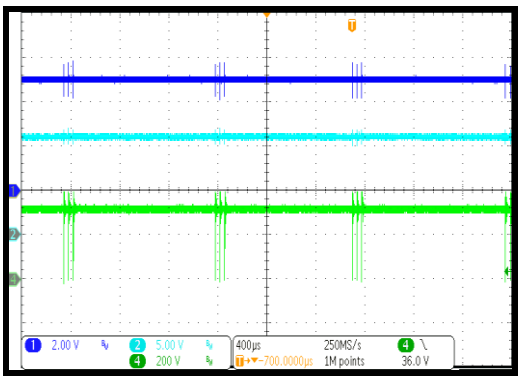
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2021 MPS. All Rights Reserved.

TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN_AC} = 220V_{AC}, V_{LED} = 44V, 150mA/string, 4 strings, analog dimming, V_{SYS} = 5V, I_{SYS} = 3A, T_A = 25°C, unless otherwise noted.

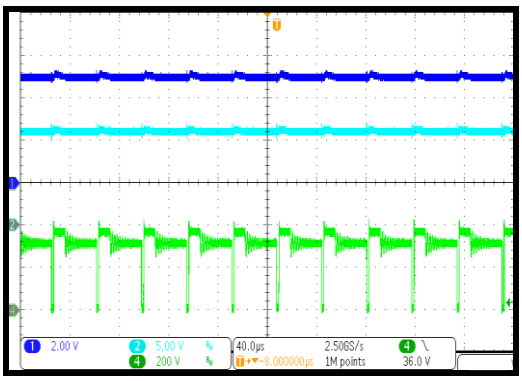
Standby Mode

Constant voltage mode, I_{SYS} = 0A



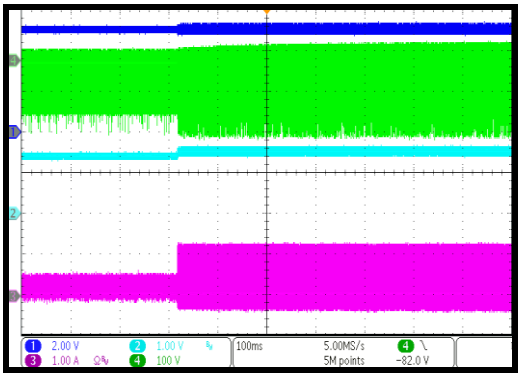
Steady State

Constant voltage mode



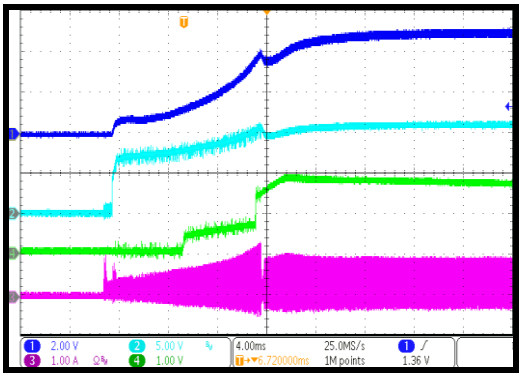
Load Transient

Constant voltage mode, I_{SYS} = 0.2A to 3A



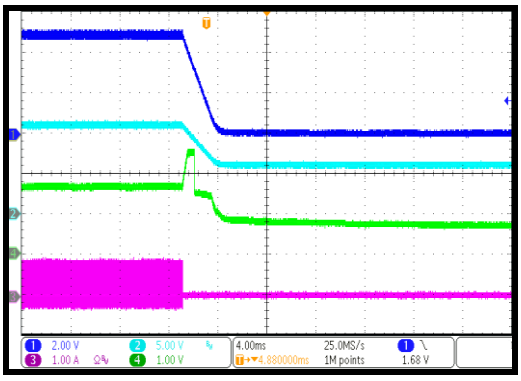
Start-Up

Constant voltage mode

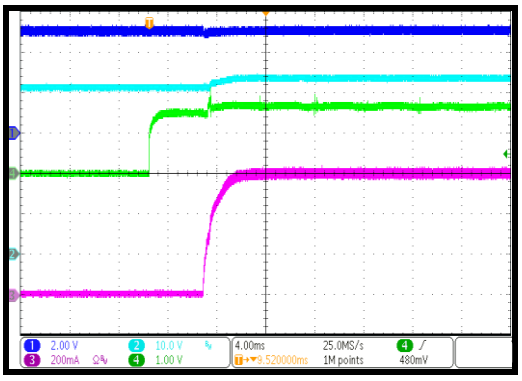


Shutdown

Constant voltage mode



LED Enable

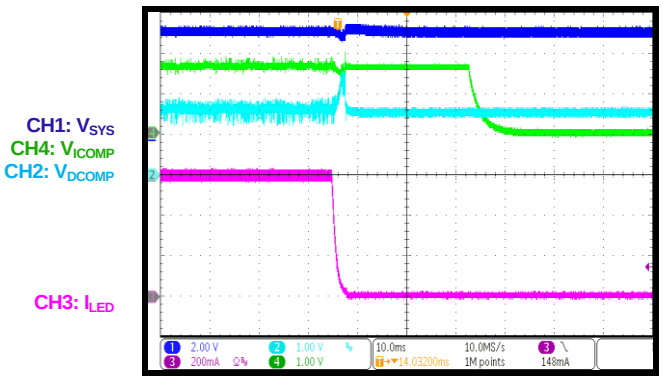


MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2021 MPS. All Rights Reserved.

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

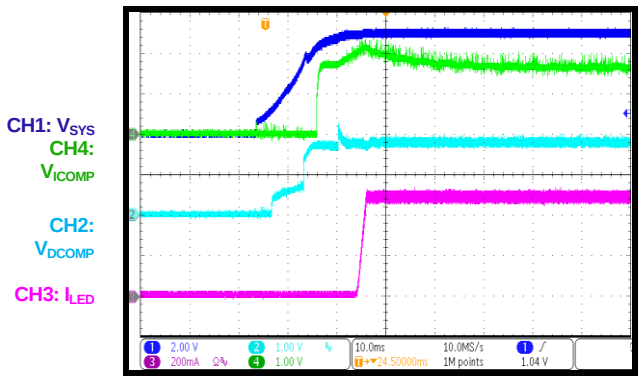
V_{IN_AC} = 220V_{AC}, V_{LED} = 44V, 150mA/string, 4 strings, analog dimming, V_{SYS} = 5V, I_{SYS} = 3A, T_A = 25°C, unless otherwise noted.

LED Disable



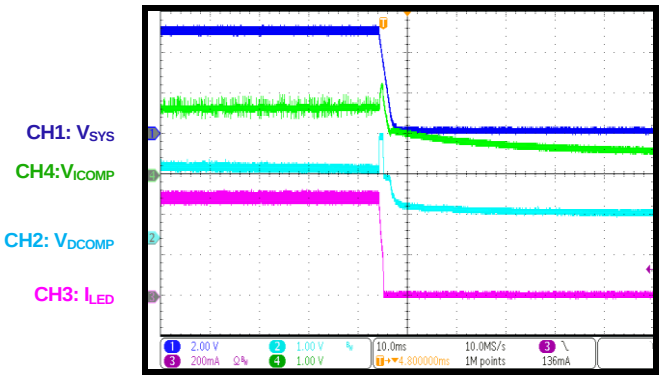
Start-Up

Constant current mode, duty = 80%



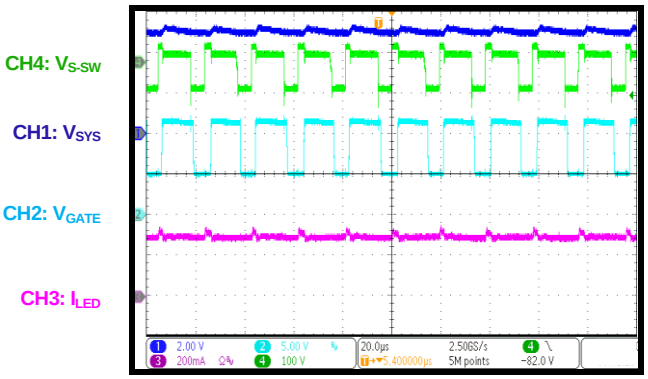
Shutdown

Constant current mode, duty = 80%



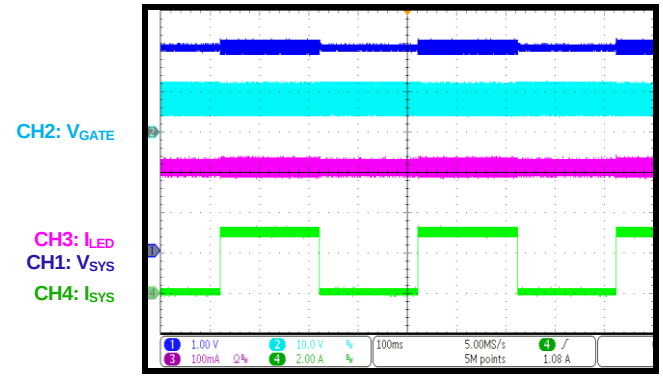
Steady State

Constant current mode, duty = 50%



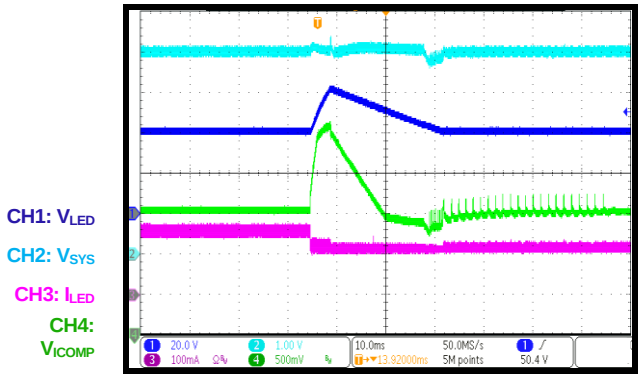
Load Transient

Duty = 50%, I_{SYS} = 0A to 3A



One-String LED Open Fault

Constant current mode, duty = 50%



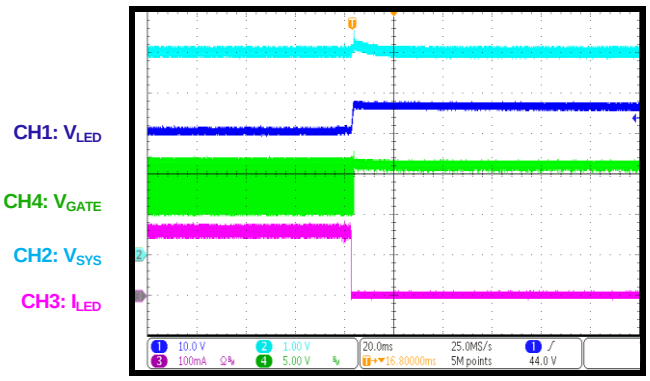
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2021 MPS. All Rights Reserved.

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN_AC} = 220V_{AC}, V_{LED} = 44V, 150mA/string, 4 strings, analog dimming, V_{SYS} = 5V, I_{SYS} = 3A, T_A = 25°C, unless otherwise noted.

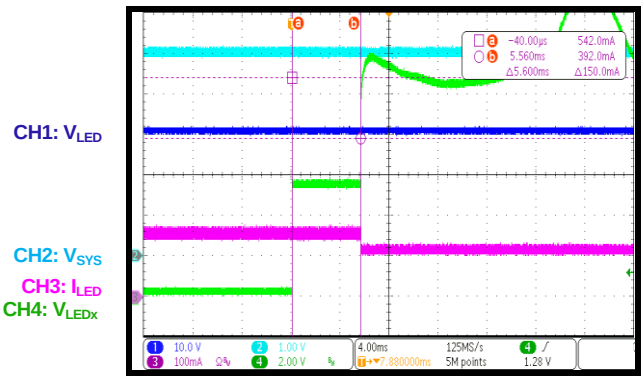
LED String Open Fault (All)

Constant current mode, duty = 25%



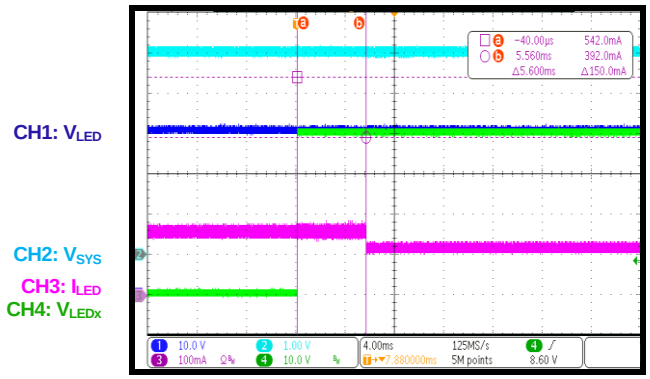
Short One String, 2 LEDs

Constant current mode, duty = 25%



One-String Short Fault (LED+ to LED-)

Constant current mode, duty = 25%



MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2021 MPS. All Rights Reserved.

FUNCTIONAL BLOCK DIAGRAM

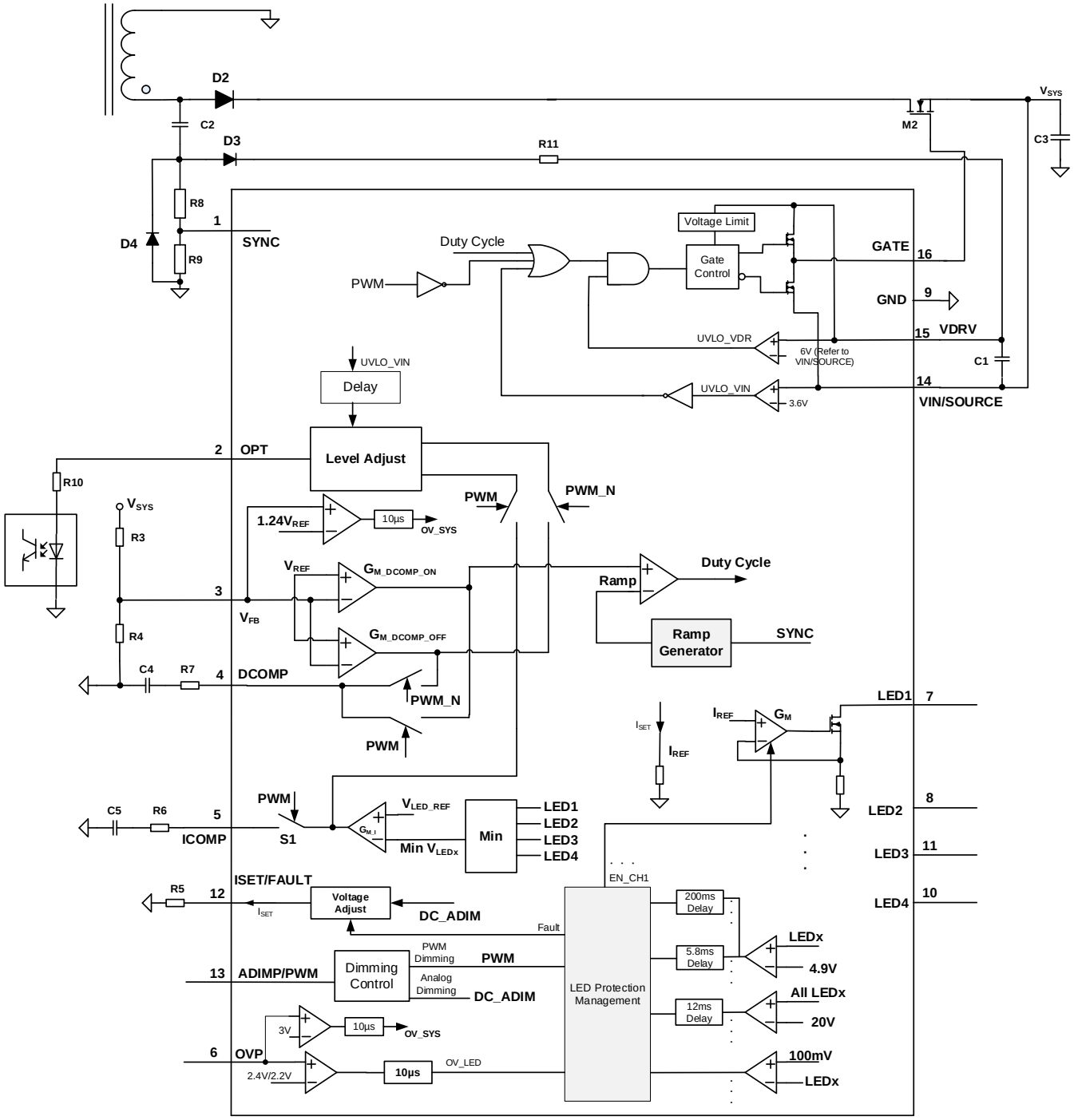


Figure 1: Functional Block Diagram

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2021 MPS. All Rights Reserved.

OPERATION

The MP4657B is a single-stage flyback, 4-string LED driver and system voltage controller for LED backlighting on the secondary side. It controls the flyback power stage plus an external N-channel MOSFET to regulate the LED current loop and system supply voltage, and includes integrated 4-string LED current balancing. With a 4V to 16V input voltage (V_{IN}), the device outputs a direct driving signal to control the N-channel MOSFET to regulate the system supply voltage. The device also outputs a compensation signal to control the primary-side flyback (or other power stage) through an optocoupler.

The device uses an individual control method for both the LED current (I_{LED}) and system voltage (V_{SYS}). When the PWM signal is effective, the MP4657B regulates the I_{LED} loop through the flyback power stage and further regulates V_{SYS} by controlling the N-channel MOSFET's turning on and off functionality. Soft switching for the N-channel MOSFET can be achieved to reduce voltage spikes. When the PWM signal is ineffective, the device directly controls V_{SYS} through the flyback power stage.

Gate Driver and System Start-Up

Figure 2 shows the MP4657B's gate driver start-up. The VDRV pin supplies the gate driver. The GATE signal's amplitude (refer to VIN/SOURCE) is limited to 6V.

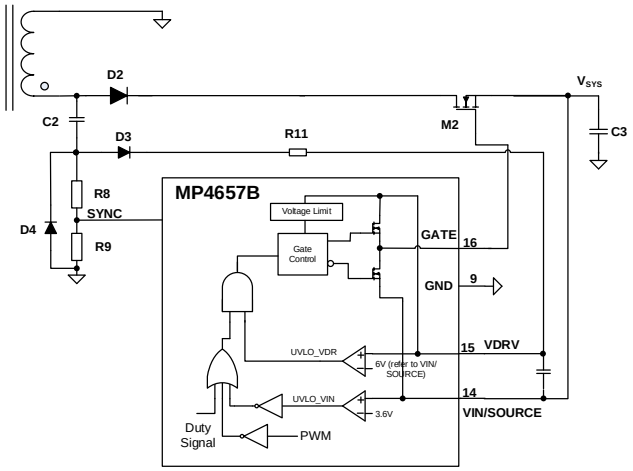


Figure 2: MP4657B Gate Driver and Start-Up

Before start-up, the VIN/SOURCE voltage is below the under-voltage lockout (UVLO) threshold, and the MP4657B monitors the VDRV voltage (V_{DRV}). After V_{DRV} reaches its UVLO threshold, the MP4657B turns on the external N-channel MOSFET. The VIN/SOURCE voltage is charged until it reaches its UVLO threshold. Then the system logic starts to work. Next, the duty cycle signal and the PWM signal determine whether the external N-channel MOSFET should be turned on or off.

Switching Sequence and Soft Switching

Figure 3 shows the MP4657B's operating sequence. The device's GATE signal's falling edge is synchronized to the primary flyback gate signal's rising edge through the SYNC pin.

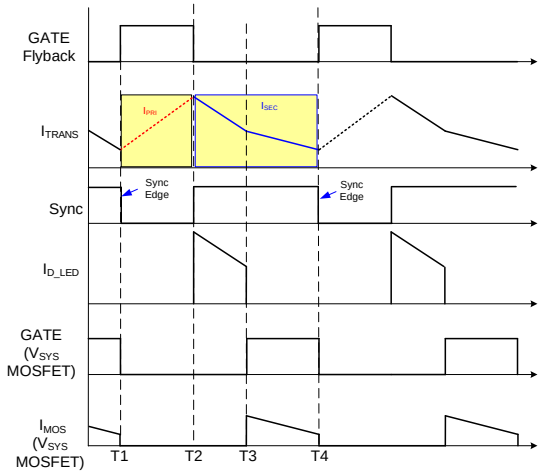


Figure 3: MP4657B Switching Sequence

The falling edge of the SYNC signal synchronizes to the falling edge of the GATE signal. This means that the N-channel MOSFET turns off when the MOSFET of primary-side flyback turns on. For most applications, the N-channel MOSFET turns off when the secondary-side winding current reaches 0A, since voltage spikes are less likely to occur.

The GATE signal's turning on and duty cycle is controlled by the DCOMP. Before the N-channel MOSFET turns on, the secondary-side current goes through the LED winding. When the N-channel MOSFET turns on, the secondary-side current starts to transfer from the LED winding to the V_{SYS} winding. Because there is leakage inductance, the N-channel MOSFET can turn on with zero current. Therefore, the switching loss for the N-channel MOSFET is very small.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2021 MPS. All Rights Reserved.

LED Current and System Voltage (V_{SYS}) Regulation

The MP4657B accurately regulates both the I_{LED} and the V_{SYS} with a single flyback power stage.

When the PWM signal is ineffective and the LED stage is disabled, the MP4657B regulates V_{SYS} by controlling the flyback power stage, and the N-channel MOSFET is fully on (see Figure 4).

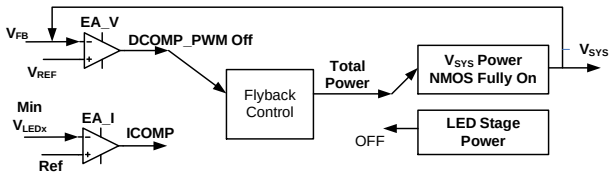


Figure 4: MP4657B Control Scheme when the PWM Signal Is Ineffective

When the PWM signal is effective, the MP4657B regulates the I_{LED} loop through the flyback power stage (see Figure 5). V_{SYS} is regulated through the duty cycle control of the N-channel MOSFET. The integrated, individual control for the N-channel MOSFET achieves soft switching without voltage spikes.

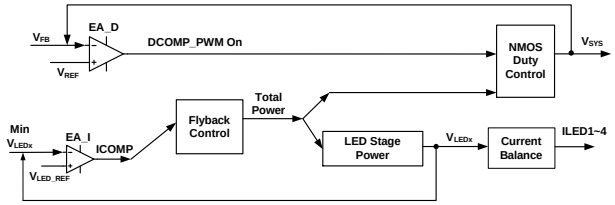


Figure 5: MP4657B Control Scheme when the PWM Signal Is Effective

LED Current Loop Regulation when PWM Signal Is On (ICOMP Loop)

In the I_{LED} regulation loop, the minimum V_{LEDx} is fed back and compared to the internal reference voltage (V_{LED_REF}, which changes with the set current). The internal error amplifier (EA) regulates the average value of the minimum LEDx voltage (V_{LEDx}) signal to this V_{LED_REF}. The EA's output is connected to the external current-loop compensation network on the ICOMP pin through an inner switch (S1).

When the PWM signal is effective, S1 is on and the EA's output is connected to the external compensation network on the ICOMP pin. The minimum V_{LEDx} is regulated by this control loop, and the flyback power is programmed by ICOMP voltage (V_{ICOMP}). When the PWM signal is ineffective, S1 turns off. Then the compensation network on ICOMP is disconnected from the EA and holds its voltage value until the PWM signal is effective again.

System Output Voltage Regulation (DCOMP Loop)

V_{SYS} is fed back to the VFB pin through a voltage divider. When the PWM signal is ineffective, the MP4657B regulates V_{SYS} by controlling the flyback power stage while the N-channel MOSFET is fully on. The internal voltage loop EA regulates the average value of the VFB pin's voltage (V_{FB}) to V_{REF}. EA's output is connected to the external voltage-loop compensation network on the DCOMP pin. V_{SYS} is regulated by this control loop, and the flyback power is determined by the DCOMP voltage.

When the PWM signal is effective, the flyback power is controlled by ICOMP, and V_{SYS} is regulated by the DCOMP pin controlling the duty cycle of the N-channel MOSFET. The V_{FB} is compared to the internal V_{REF}. The EA outputs an error signal to DCOMP pin. The EA's gain with an effective PWM signal is different from that with an ineffective PWM signal. The DCOMP pin's voltage determines the duty cycle of the N-channel MOSFET (see Figure 6).

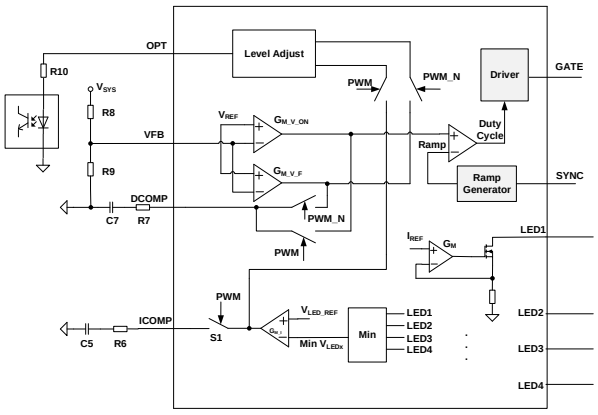


Figure 6: MP4657B Control Diagram

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2021 MPS. All Rights Reserved.

Dimming Control

The MP4657B provides analog dimming and PWM dimming for LED current through the ADIMP/PWM pin. For analog dimming, apply a pulse signal with a >5kHz frequency to this pin. In this mode, the PWM signal is always effective unless the pulse signal is removed. For PWM dimming, apply a pulse signal with a <5kHz frequency. In this mode, I_{LED} is chopped by the pulse signal. During PWM dimming, the PWM signal is effective when the pulse is high, and is ineffective when the pulse is low.

Protection Features

The MP4657B integrates sufficient protections for the system voltage stage and the LED driver stage.

System Voltage Stage Protections

The protections for the V_{SYS} stage, include system over-voltage protection (OVP) and open-loop feedback protection.

System Over-Voltage Protection (OVP)

The VFB pin senses V_{SYS} for regulation and over-voltage protection (OVP). If the V_{FB} exceeds V_{REF} by 24%, system OVP is triggered. The OPT pin is clamped to 3.3V to stop primary switching when the PWM signal is ineffective. If system OVP is triggered when PWM is effective, the GATE signal turns off. If the OVP pin's voltage exceeds 3V, the IC latches off. This function protects V_{SYS} from damaging the device.

Feedback Open-Loop Protection (V_{SYS} Stage)

If V_{FB} is below 50% of V_{REF} and DCOMP is saturated for 1024 consecutive switching cycles, the IC latches off and the fault indicator is pulled low.

LED Driver Stage Protections

Fault protections for the LED driver stage include LED open protection, LED short protection, and LEDx pin short-to-ground protection.

LED Open Protection

The output voltage of the LED stage (V_{LED}) is sensed on the OVP pin. LED open protection is achieved by monitoring the OVP pin and LEDx (x = 1~4) voltages. If one or more LED strings have an open condition, the respective LEDx voltage (V_{LEDx}) is pulled to ground while V_{LED} continue increasing until the OVP pin's voltage reaches the OVP threshold (about 2.4V). When the OVP pin voltage exceeds 2.4V for 10µs, LED open protection is triggered. The control loop for the LED stage is disabled, and MP4657B regulates V_{SYS} as an ineffective PWM signal condition. The IC marks off the open LED strings that have V_{LEDx} below 100mV. The remaining LED strings discharge V_{LED}, and the OVP pin voltage decreases until it drops below the OVP threshold. Then the LED control loop recovers, and the minimum V_{LEDx} of the remaining LED strings are regulated. The fault indicator does not function in this condition when there are functional LED strings. If all LED strings have an open condition, they are all marked off, and the LED control loop is disabled. V_{SYS} is also regulated as an ineffective PWM signal condition, and the fault indicator is pulled low.

LED Short Protection

V_{LEDx} is monitored for LED short conditions. If an LED string is shorted, the respective V_{LEDx} rises. If V_{LEDx} exceeds 4.9V for 5.8ms, the IC marks off the string that has a short condition. Meanwhile, all other strings continue working. If all of the LEDx voltages (except the marked-off strings) exceed 4.9V, it takes 200ms to trigger LED short protection. This prevents mistriggering short protection if OVP is triggered, or if the duty of analog dimming changes. If all of the LEDx voltages (except the marked-off strings) exceed 20V for 12ms, all LED strings short protection is triggered.

LEDx Pin Short-to-Ground Protection

If ICOMP is saturated and V_{LEDx} is low for 100ms, the IC triggers LEDx short-to- ground protection. The LED control loop is disabled and the fault indicator is pulled low. To recover the LED loop from this fault, toggle the ADIMP/PWM pin. Pull ADIMP/PWM low for longer than 25ms, then pull it high. The fault indictor resets, and the ISET pin sets I_{LED}.

Thermal Protection

Thermal protection is integrated into the MP4657B. If the die temperature exceeds the over-temperature (OT) threshold, the IC stops working until the die temperature is reduced. Once the temperature returns to within its safe range, the IC resumes normal operation.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2021 MPS. All Rights Reserved.

APPLICATION INFORMATION

Gate Signal Synchronization (SYNC)

The SYNC pin synchronizes the GATE signal. Its falling edge synchronizes the GATE signal turning off. Connect a voltage divider from the secondary winding to this pin to indicate the primary-side MOSFET turning on.

System Voltage Feedback (VFB)

The VFB pin feeds back the system voltage (V_{SYS}). Connect this pin to V_{SYS} with a voltage divider. This voltage divider determines V_{SYS}, calculated with Equation (1):

$$V_{SYS} = \frac{1.2V \times (R_{VFBH} + R_{VFBL})}{R_{VFBL}} \quad (1)$$

Where R_{VFBH} and R_{VFBL} are the high-side and low-side resistors of the voltage divider, respectively.

The VFB pin is monitored for system OVP. If V_{FB} exceeds V_{REF} by 24% for 10µs, system OVP is triggered.

LED Open Protection

The OVP pin monitors the output LED voltage (V_{LED}) and can trigger LED open protection. Connect this pin to V_{LED} through a voltage divider and set the OVP point (V_{OV_LED}) using Equation (2):

$$V_{OV_LED} = \frac{2.4V \times (R_{OVPH} + R_{OVPL})}{R_{OVPL}} \quad (2)$$

Where R_{OVPH} and R_{OVPL} are the voltage dividers' high-side and low-side resistors, respectively.

LED Current Setting (ISET/FAULT)

The LED current (I_{LED}) is set by the resistor on the ISET/FAULT pin. The ISET/FAULT pin outputs 1.6V, and its source current determines each channel's I_{LED}. I_{LED} can be estimated with Equation (3):

$$I_{LED}(mA) = \frac{80k\Omega \times 200mA}{R_{ISET}(k\Omega)} \quad (3)$$

Gate Driver Supply and GATE (VDRV, GATE)

The VDRV pin supplies power to the gate driver (refer to the VIN/SOURCE pin). Connect a sufficient voltage source to this pin to supply the gate driver, and bypass this supply to the VIN/SOURCE pin with a 1µF ceramic capacitor. The VDRV pin can handle a maximum 53V voltage (refer to GND), and the GATE signal is limited to 6V (refer to VIN/SOURCE).

In primary flyback power stage applications, VDRV can typically be supplied by the secondary-side winding of the power transformer.

Connect the GATE signal directly to the N-channel MOSFET, or use a driving resistor.

Selecting the Turn Ratios of the Power Transformer

The power transformer includes three power windings: the primary-side winding (N_P), the secondary LED winding (N_{LED}), and the secondary system voltage winding (N_{SYS}). To design the turn ratios of the power transformer, follow the instructions below:

Design the turn ratio between the primary-side winding and the secondary LED winding (N_P:N_{LED}).

The maximum voltage stress (V_{DS_PRI}) on the primary-side MOSFET, which occurs at the maximum input AC voltage and the maximum output LED voltage, can be calculated with Equation (4):

$$V_{DS_PRI} = 1.414 \times V_{IN_AC_MAX} + (V_{OV_LED} + V_{DIODE}) \times \frac{N_P}{N_{LED}} \quad (4)$$

Where $V_{IN_AC_MAX}$ is the maximum input AC voltage, V_{DIODE} is the forward voltage of the rectifier diode, and V_{OV_LED} is OVP point of V_{LED}.

Consider the leakage inductance of the flyback transformer, and assume there is a 60V spike voltage on the primary-side MOSFET, as well as a 10% derating of the switch voltage capability. V_{DS_PRI} can be estimated with Equation (5):

$$V_{DS_PRI} + 60 \le 0.9 \times V_{RATING_PRI} \quad (5)$$

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2021 MPS. All Rights Reserved.

Where V_{RATING_PRI} is the rating voltage of the primary-side MOSFET.

Calculate N_P:N_{LED} with Equation (6):

$$N_P : N_{LED} = \frac{(0.9 \times V_{RATING_PRI} - 60V - 1.414 \times V_{IN_AC_MAX})}{V_{OV_LED} + V_{DIODE}} \quad (6)$$

Design the turn ratio between the LED winding and the V_{SYS} winding (N_{LED}:N_{SYS}).

Ensure that V_{SYS} is below the reflecting voltage from the LED winding under the minimum V_{LED}. This relationship can be estimated with Equation (7):

$$V_{SYS} + V_{DIODE} < \frac{V_{LED_MIN} + V_{DIODE}}{\frac{N_{LED}}{N_{SYS}}} \quad (7)$$

Where V_{LED_MIN} is the minimum output LED voltage. Choose a 15% margin for production design, calculated with Equation (8):

$$N_{LED} : N_{SYS} = \frac{0.85 \times (V_{LED_MIN} + V_{DIODE})}{V_{SYS} + V_{DIODE}} \quad (8)$$

Selecting the External N-Channel MOSFET

The voltage stress on the external N-channel MOSFET can be estimated with Equation (9):

$$V_{DS_EXT} = \frac{V_{INAC_MAX} \times N_{SYS}}{N_P} \quad (9)$$

The maximum voltage stress occurs at $V_{IN_AC_MAX}$. Considering the small voltage spike and the MOSFET voltage derating, it is recommended to choose a 20% margin. Estimate the voltage rating (V_{RATING_EXT}) with Equation (10):

$$V_{RATING_EXT} = \frac{V_{IN_AC_MAX} \times N_{SYS}}{N_P \times 0.8} \quad (10)$$

The average current flowing through the N-channel MOSFET is equal to the output current of V_{SYS}. This flowing current is a pulse waveform, and its RMS current is much greater than the average value. Assume that the RMS current (I_{RMS_EXT}) is 1.5 to 2 times greater than the average current; estimate this value using Equation (11):

$$I_{RMS_EXT} \approx 2 \times I_{SYS} \quad (11)$$

Where I_{RMS_EXT} is the RMS current through the N-channel MOSFET, and I_{SYS} is the output current of V_{SYS}.

The switching loss from the N-channel MOFET's soft switching is typically low. The rating current for the N-channel MOSFET should be 2 to 3 times that of the RMS current.

Consider thermal loss and power loss when selecting the $R_{DS(ON)}$ and package size for the N-channel MOSFET.

PCB Layout Guidelines

Efficient PCB layout is important to achieve reliable operation, good EMI performance, and good thermal performance. For the best results, refer to Figure 7 and follow the guidelines below:

1. Minimize the power stage loop area. This includes the primary loop (input capacitor, transformer, and MOSFET sense resistor), as well as the secondary winding loop (transformer, rectifier, and diode output capacitor).
2. Separate the output loop GND and control circuit GND, and only connect them at the GND pin.
3. Place peripheral electronic components (such as those for VIN/SOURCE, VFB, SYNC, DCOMP, and ICOMP) close to the IC to decouple noise.

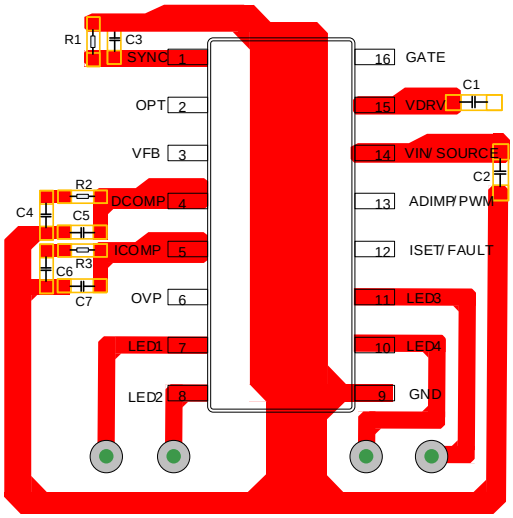


Figure 7: Recommended PCB Layout for a 1-Layer Board

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2021 MPS. All Rights Reserved.

TYPICAL APPLICATION CIRCUIT

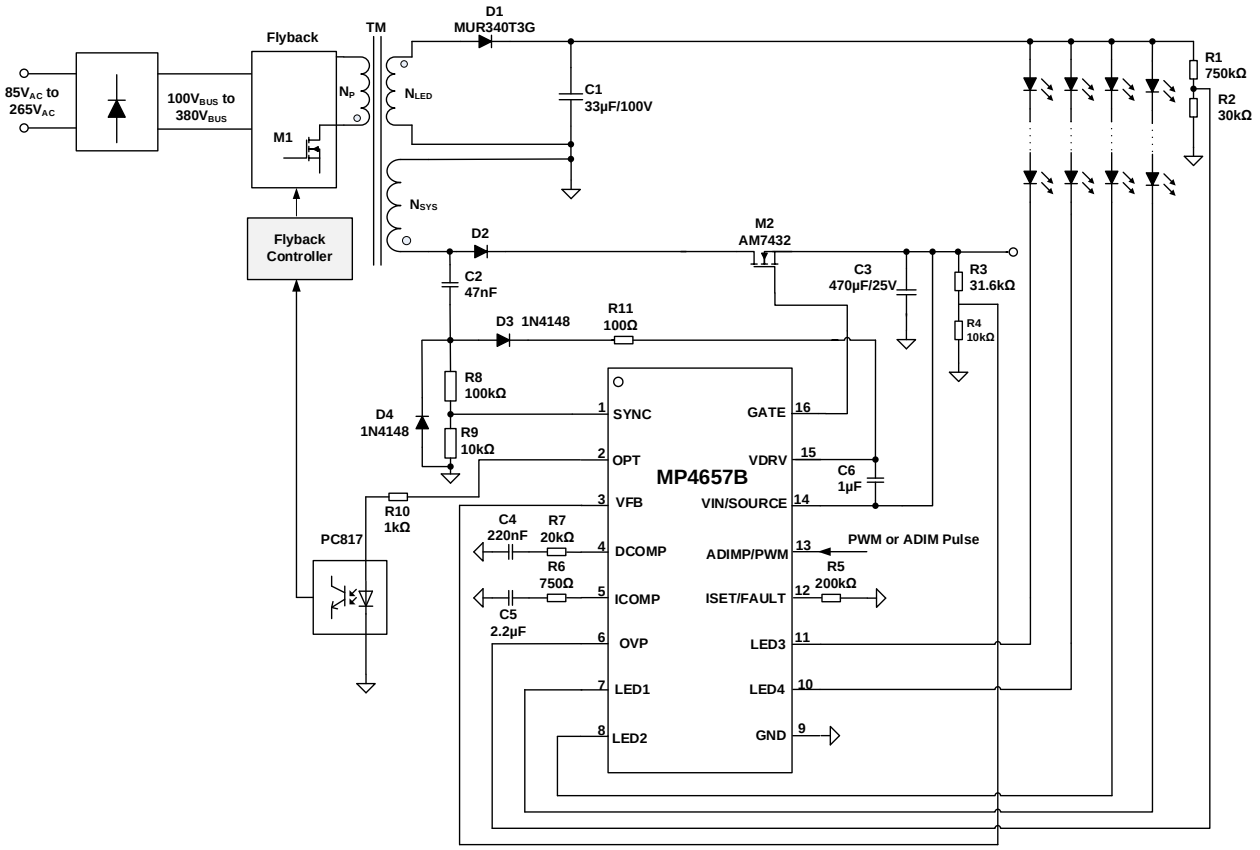
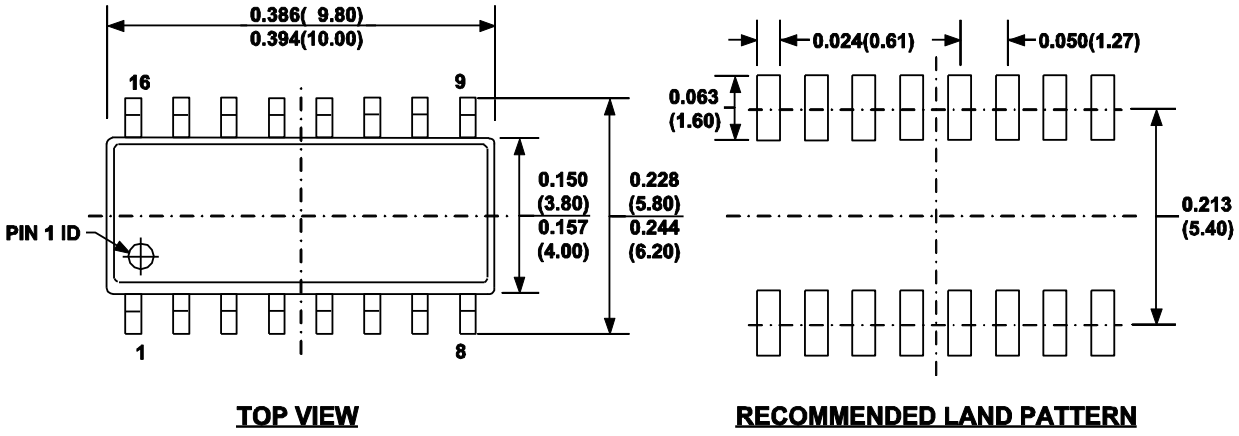


Figure 8: Typical Application Circuit (MP4657B Flyback 4-String LED Driver and System Voltage Regulation Scheme)

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2021 MPS. All Rights Reserved.

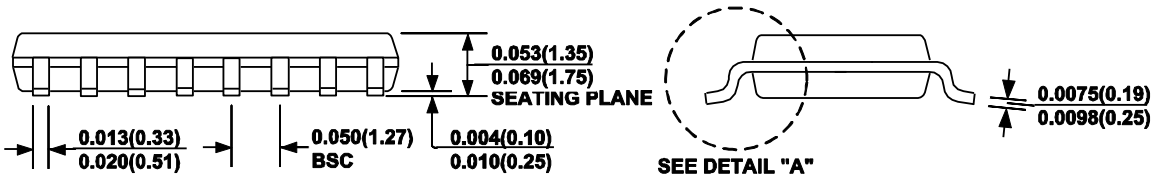
PACKAGE INFORMATION

SOIC-16



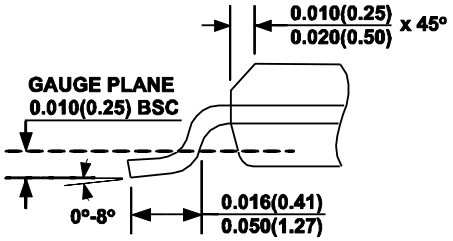
TOP VIEW

RECOMMENDED LAND PATTERN



FRONT VIEW

SIDE VIEW



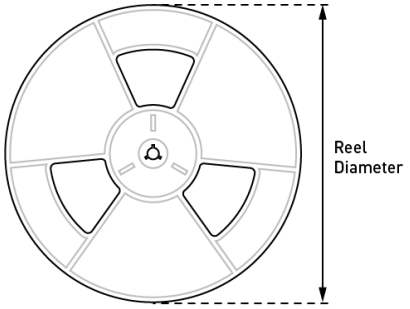
DETAIL "A"

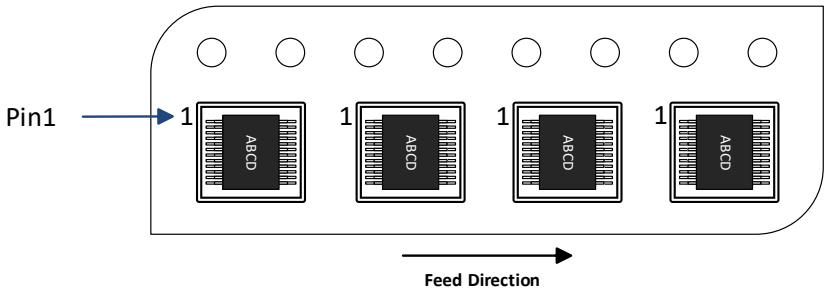
NOTE:

1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
5) DRAWING CONFORMS TO JEDEC MS-012, VARIATION AC.
6) DRAWING IS NOT TO SCALE.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2021 MPS. All Rights Reserved.

CARRIER INFORMATION





Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP4657BGS-Z	SOIC-16	2500	50	N/A	13in	16mm	8mm

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2021 MPS. All Rights Reserved.

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	11/11/2021	Initial Release	-

Notice: The information in this document is subject to change without notice. Please contact MPS for current specifications. Users should warrant and guarantee that third-party Intellectual Property rights are not infringed upon when integrating MPS products into any application. MPS will not assume any legal responsibility for any said applications.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2021 MPS. All Rights Reserved.