MP5021

12V, 7mΩ R_{DSon} Hot-Swap Protection Device with Current Monitoring

The Future of Analog IC Technology

DESCRIPTION

The MP5021 is a hot-swap protection device designed to protect circuitry on its output from transients on its input. It also protects its input from undesired shorts and transients coming from its output.

At start up, the slew rate at the output limits the in-rush current. An external capacitor at the SS pin controls the slew rate.

The maximum output load is current limited using a sense FET topology whereby a low-power resistor from the ISET pin to ground controls the magnitude of the current limit.

An internal charge pump drives the gate of the power device, allowing for a power FET with a very low ON resistance of 7mΩ.

The MP5021 includes an IMON option to produce a voltage proportional to the current through the power device, as set by a resistor from the IMON pin to ground.

The MP5021 includes an optional discharge function that provides a discharge path for the external output capacitor when the part is disabled. Fault protections include current-limit protection, thermal shutdown, and damaged-MOSFET detection. Both the current limit and thermal shutdown have user-settable auto-retry and latch-off mode. The device also features over-voltage protection and under-voltage protection

The MP5021 is available in a 3mm×5mm QFN package.

FEATURES

- Integrated 7mΩ Power FET
- Adjustable Current Limit (5A to 15A)
- Output Current Measurement
- ±5% Current Limit and Monitor Accuracy
- Fast Response (<200ns) for Short Protection
- PG Detector and FLTB Indication
- PG Assert Low at VIN=0
- Damaged MOSFET Detection
- External Soft-Start
- Programmable EN Blanking Time
- Under/Over-Voltage Lockout
- Thermal Protection
- Small 3mm×5mm QFN Package

APPLICATIONS

- Hot Swappable:
  - PC Cards
  - Disk Drives
  - Laptops

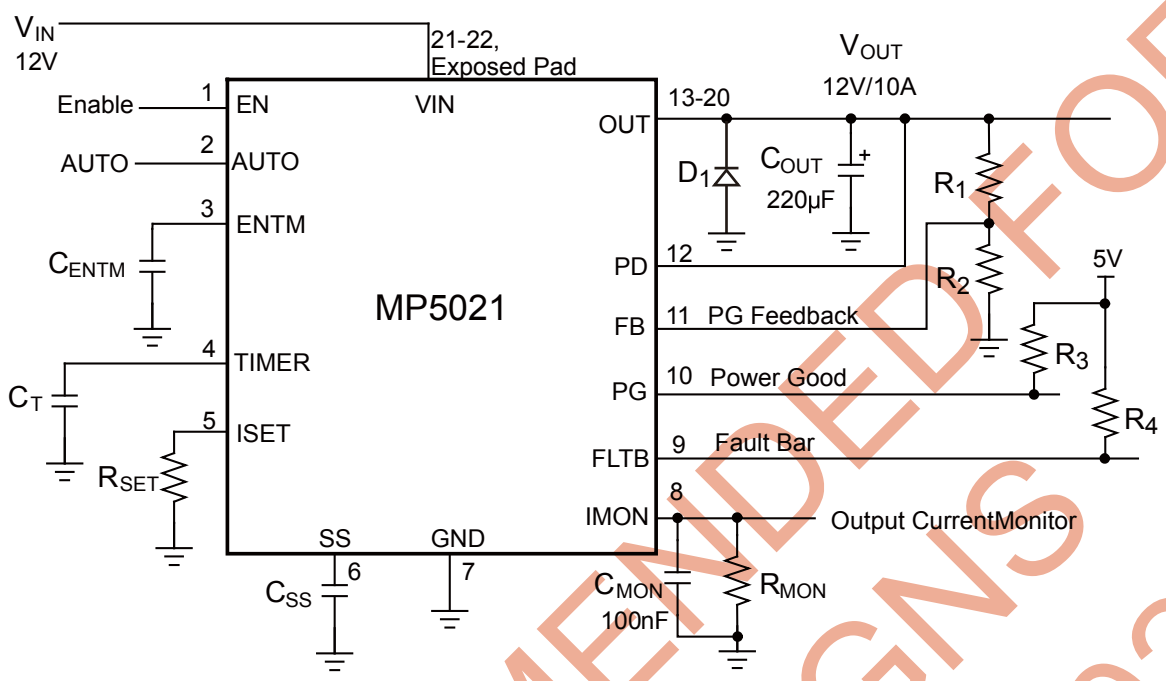
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TYPICAL APPLICATION



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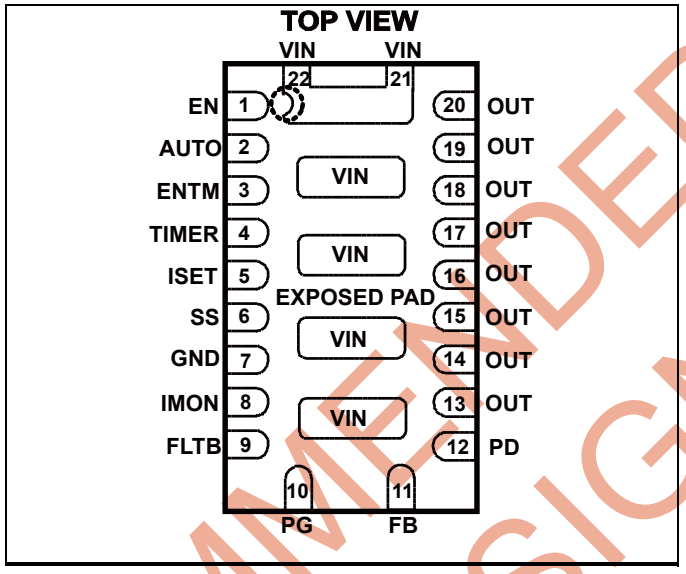
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ORDERING INFORMATION

Part Number*	Package	Top Marking
MP5021GQV	QFN22 (3×5mm)	MP5021

For Tape & Reel, add suffix –Z (e.g. MP5021GQV–Z)

PACKAGE REFERENCE



ABSOLUTE MAXIMUM RATINGS (1)

V_{IN} .....-0.3V to 36V
OUT, PD .....-0.3V to 20V
EN, FLTB, PG, ISET, TIMER, IMON, SS, AUTO, ENTM, FB (2).....-0.3V to 6.5V
Continuous Power Dissipation (T_A = +25°C) (3) 2.7W
Power Dissipation (T_A = +25°C, 10ms Single Pulse) 215W
Maximum Current (T_A = +25°C) 25A
Storage Temperature..... -65°C to +155°C
Operating Temperature..... -40°C to +150°C

Recommended Operating Conditions (4)

Input Voltage Operating Range ..... 8V to 16V
Operating Junction Temp. (T_J). -40°C to +125°C

Thermal Resistance (5)

	θ_{JA}	θ_{JC}
QFN22	46	10 ... °C/W

Notes:

1) Exceeding these ratings may damage the device..
2) Maximum Input Voltage to be≤6.0V if Vcc ≥ 6.0V. Maximum Input Voltage to be Vcc if Vcc ≤ 6.0V.
3) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
4) The device is not guaranteed to function outside of its operating conditions.
5) Measured on JESD51-7 4-layer board.

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ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, R_{SET}=10k, C_{OUT}= 220µF, T_J=25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Supply Current						
Quiescent Current	I_Q	EN=high, No load		1	2.0	mA
		Fault latch off		0.7		mA
		EN=0, V_{IN}=16V			170	µA
Power FET						
ON Resistance	R_{DSon}	T_J=25°C		7	8.5	mΩ
		T_J=85°C(6)		9		
Off-State Leakage Current	I_{OFF}	V_{IN}=36V, EN=0V			1	µA
Maximum Continuous Current	I_{OUT_MAX}		10			A
Thermal Shutdown						
Shutdown Temperature(6)	τ_{STD}			145		°C
Hysteresis	τ_{HYS}	Auto-Retry Mode Only		20		°C
Under/Over Voltage Protection						
Under-Voltage Lockout Threshold	V_{UVLO}	UVLO, Rising Threshold	5.85	6.6	7.35	V
UVLO Hysteresis	$V_{UVLOHYS}$			300		mV
Over-Voltage Lockout Threshold	V_{OVLO}	OVLO, Rising Threshold	16.5	17.66	18.96	V
OVLO Hysteresis	$V_{OVLOHYS}$			460		mV
AUTO Pin						
Low-Level Input Voltage	V_{AUTOL}	Latch Off Mode			1	V
High-Level Input Voltage	V_{AUTOH}	Auto Retry Mode	2.5			V
Soft Start						
SS Pull-Up Current	I_{SS}	I_{SS} changes with input	10	12	14	µA
Current Limit						
Current Limit at Normal Operation	I_{Limit_NO}	R_{set}=10k	11.4	12.6	13.7	A
Current Monitor Accuracy	I_{MONACC}	5A<I_{OUT}<10A	-3		+3	%
		-40°C to +85°C(6)	-5		+5	%
Current Limit Response Time(6)	τ_{CL}	I_{Limit}=3A, add 3Ω load		20		µs
Secondary Current Limit	I_{LimitH}	Any value of R_{ISET}		25		A
Short-Circuit Protection Response Time (6)	τ_{SC}			200		ns
Timer						
Upper Threshold Voltage	V_{TMRH}		1.187	1.23	1.273	V
Lower Threshold Voltage	V_{TMRL}	Over current restart cycles		0.200		V
Fault Restart Duty Cycle	V_{FAULT}			0.25		%
Insertion Delay Charge Current	I_{INSERT}			38.5		µA
Fault Detection Charge Current	I_{FLTD}			200		µA
Fault Restart Sink Current	I_{FLTS}			0.5		µA
Discharge R_{ON}	R_{FLTE}	I_{OUT} < I_{Limit}		35		Ω
EN Blanking Timer (ENTM pin)						
Upper Threshold Voltage	V_{ENTMRH}		1.187	1.23	1.273	V
Charge Current	I_{ENTMCC}			0.85		µA

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ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, R_{SET}=10k, C_{OUT}= 220µF, T_J=25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Enable						
Rising Threshold	V_{ENRS}		1.5	2	2.3	V
Hysteresis	V_{ENHYS}			200		mV
FB (Power Good Feedback)						
Feedback Rising Threshold	V_{FBH}		0.567	0.600	0.633	V
Hysteresis	V_{FBHYS}		54	65	75	mV
Fault Bar/Power Good						
Low-Level Output Voltage	V_{OL}	Sink current 1mA			0.3	V
Off-State Leakage Current	$I_{PG_FLT_LKG}$	V_{PG}=5V, V_{FLTB}=5V			1	µA
Fault Bar Propagation Delay	τ_{PDE}			21		µs
PG Low-Level Output Voltage	V_{OL_100}	V_{IN}=0V, Pull up to 3.3V through 100kΩ resistor		580	700	mV
	V_{OL_10}	V_{IN}=0V, Pull up to 3.3V through 10kΩ resistor		700	750	mV

Notes:

6) Guaranteed by design.

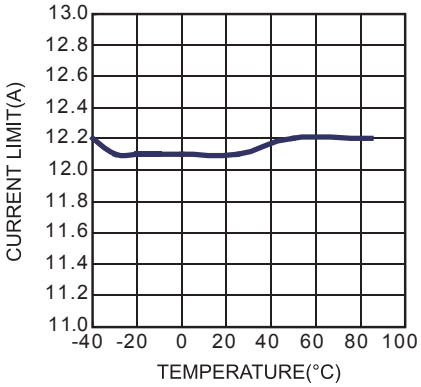
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TYPICAL CHARACTERISTICS

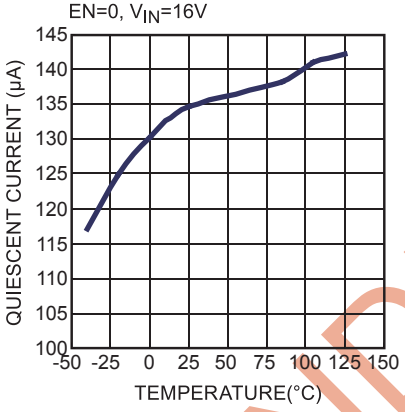
V_{IN}=12V, C_{OUT}=220µF, C_{ENTM}=1µF, C_T=220nF, C_{SS}=47nF, R_{SET}=10kΩ, T_A=+25°C, unless otherwise noted.

Current Limit vs. Temperature



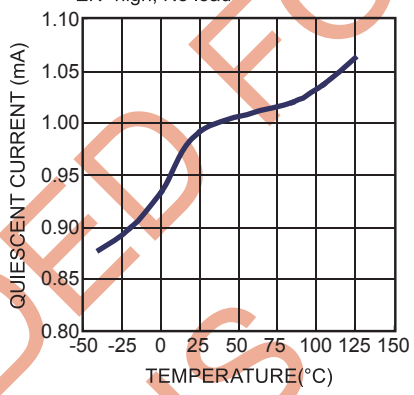
Quiescent Current vs. Temperature

EN=0, V_{IN}=16V

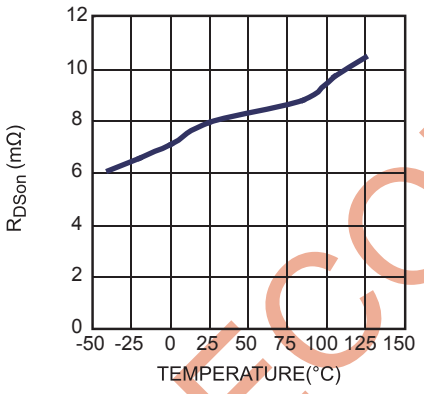


Quiescent Current vs. Temperature

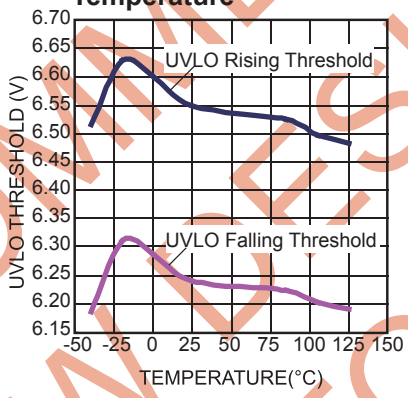
EN=high, No load



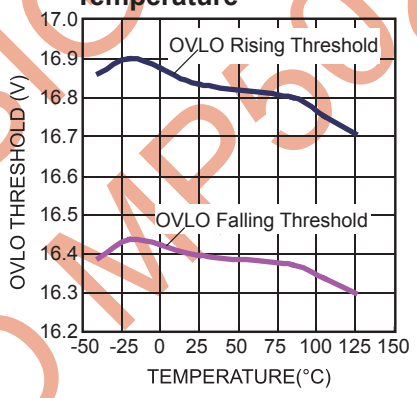
R_{DSon} vs.Temperature



UVLO Threshold vs. Temperature

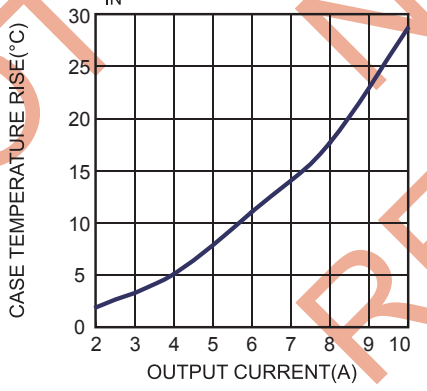


OVLO Threshold vs. Temperature

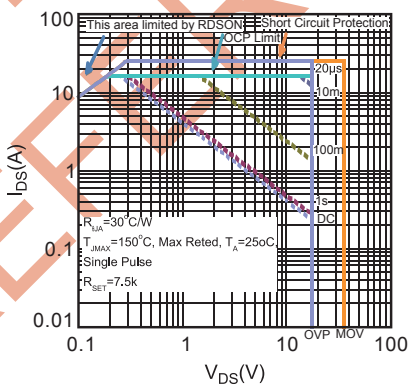


Case Temperature Rise vs. Output Current

V_{IN}=16V



MP5021 Safe Operation Area



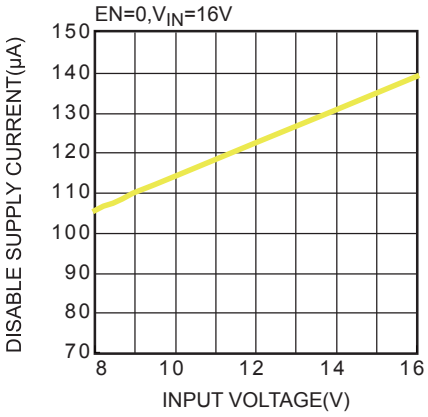
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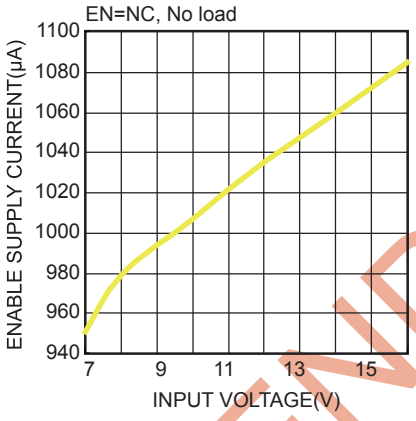
TYPICAL PERFORMANCE CHARACTERISTICS

Performance waveforms are tested on the evaluation board of the Design Example section. V_{IN}=12V, C_{OUT}=220µF, C_{ENTM}=1µF, C_T=220nF, C_{SS}=47nF, R_{SET}=10kΩ, T_A=+25°C, unless otherwise noted.

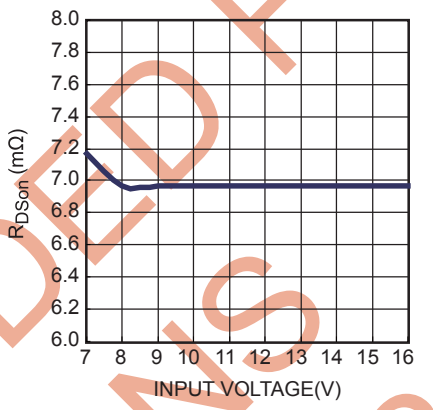
Disable Supply Current vs. Input Voltage



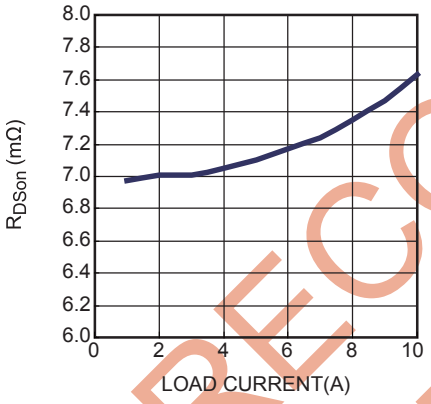
Enable Supply Current vs. Input Voltage



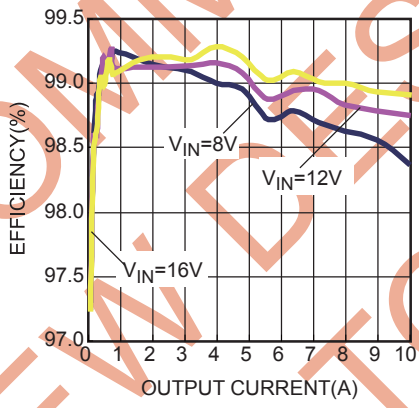
R_{DSon} vs. Input Voltage



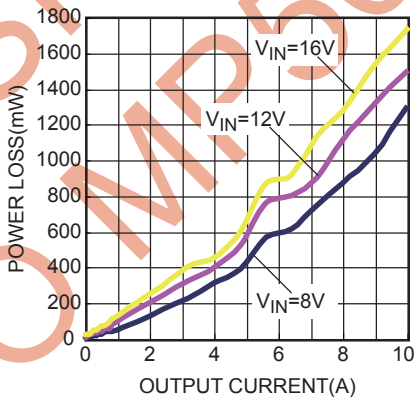
R_{DSon} vs. Load Current



Efficiency vs. Load Current



Power Loss vs. Load Current



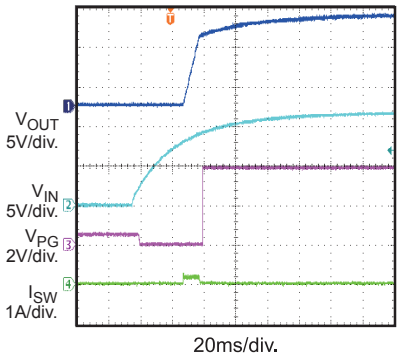
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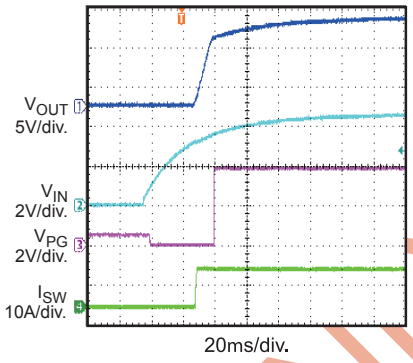
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

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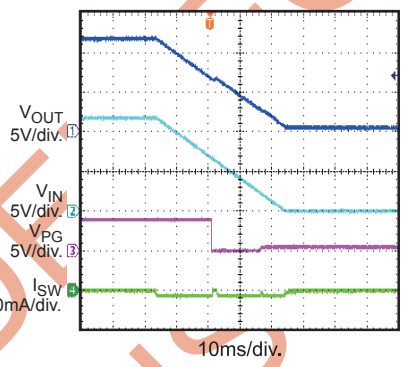
Start Up through VIN
I_{OUT}=0A



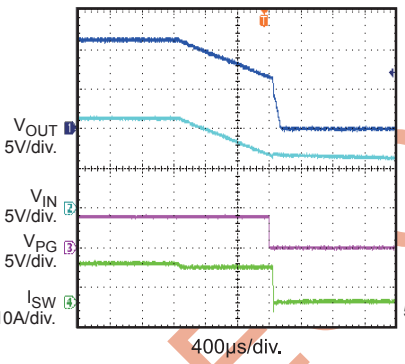
Start Up through VIN
I_{OUT}=10A



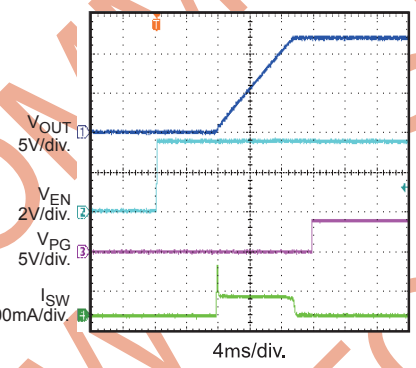
Shut Down through VIN
I_{OUT}=0A



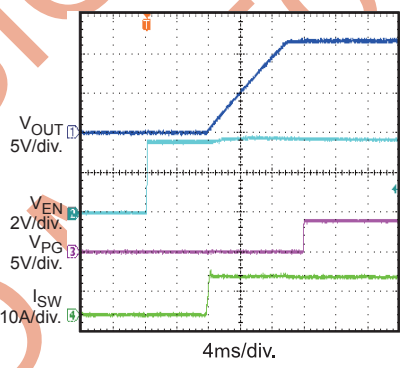
Shut Down through VIN
I_{OUT}=10A



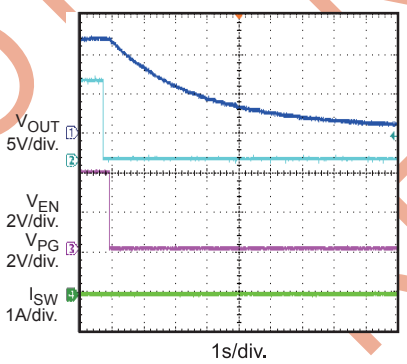
Start Up through EN
I_{OUT}=0A



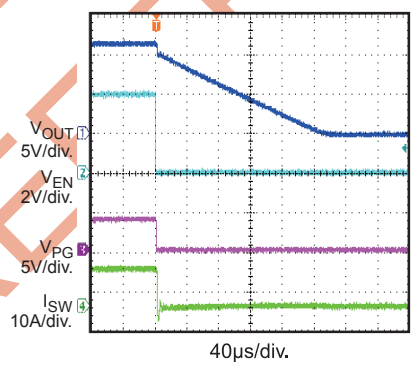
Start Up through EN
I_{OUT}=10A



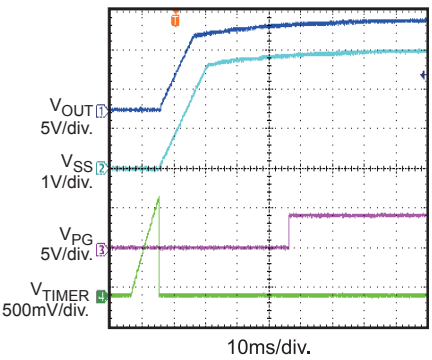
Shut Down through EN
I_{OUT}=0A



Shut Down through EN
I_{OUT}=10A



Start-Up Sequence



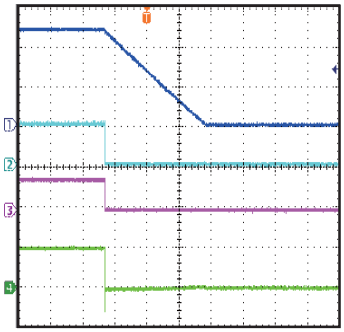
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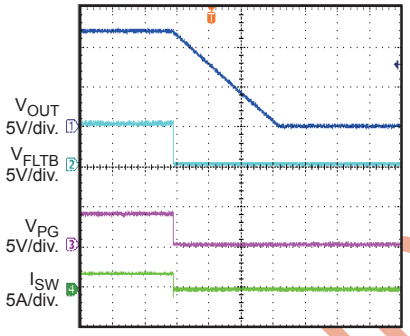
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

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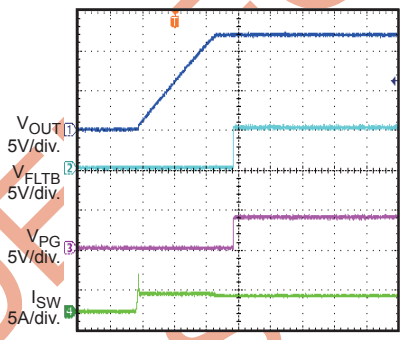
Thermal Shutdown
I_{OUT}=2A, Latch mode



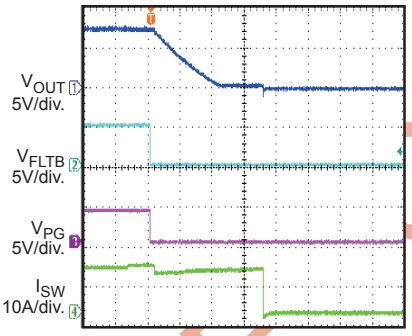
Thermal Shutdown
I_{OUT}=2A, Retry mode



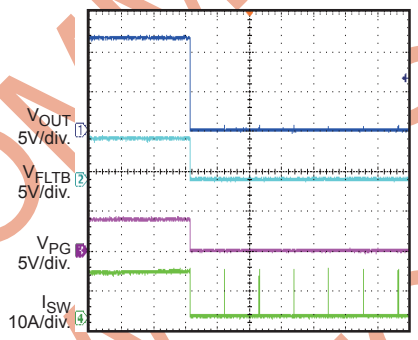
Thermal Recovery
I_{OUT}=2A, Retry mode



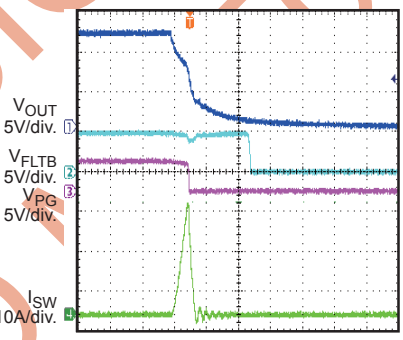
OCP
V_{IN}=12V, Latch mode



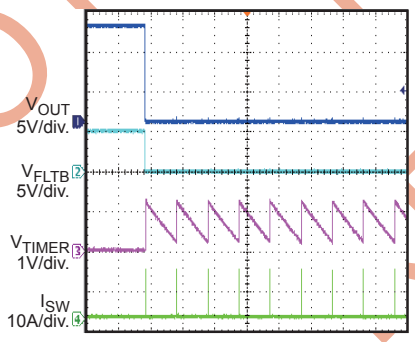
OCP
V_{IN}=12V, Retry mode



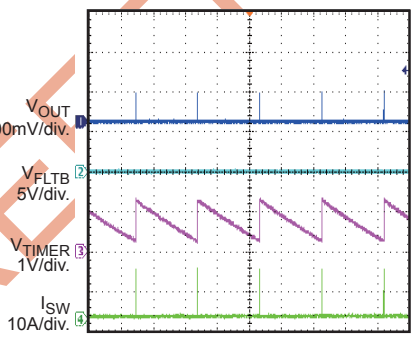
SCP Entry
V_{IN}=12V, Latch mode



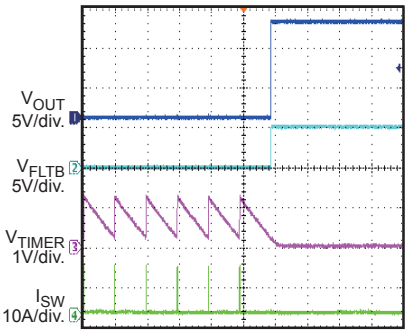
SCP Entry
V_{IN}=12V, Retry mode



SCP Steady State
V_{IN}=12V, Retry mode



SCP Recovery
V_{IN}=12V, Retry mode



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PIN FUNCTIONS

Pin #	Name	Description
1	EN	Enable Input. Pull this pin below threshold to shut the chip down. Pull it above threshold or leaving it floating to enable the chip.
2	AUTO	Auto Reset Enable. Float to enable auto reset upon fault removal. Ground to cause the part to latch off when a fault occurs.
3	ENTM	Enable-Blanking–Time Set. Connect an external capacitor to set the EN blanking time. Once EN is active, the timer starts and the EN deassertion is blanked. The switch shuts down in the presence of a fault, but EN-low during blanking has no effect.
4	TIMER	Timer Set. An external capacitor sets the hot-plug-insertion time delay, fault timeout period, and restart time.
5	ISET	Current Limit Set. Place a resistor to ground to set the value of the current limit.
6	SS	Soft-Start. An external capacitor connected sets the soft-start time of the output voltage. The internal circuit controls the slew rate of the output voltage at turn-on. Float this pin to set the soft-start time at its minimum of 1ms.
7	GND	Ground
8	IMON	Output Current Monitor. Provides a voltage proportional to the current flowing through the power device. Place a resistor to ground to set the gain.
9	FLTB	Fault Bar. This is an open drain output that drives to ground when an over-current or a thermal shutdown occurs. Pull-up to an external power supply through a 100kΩ resistor.
10	PG	Power Good. This is an open drain output. Pull-up to external power supply through 100kΩ resistor. High = power-good. Low indicates output is outside UVLO/OVLO window. PG starts to work when the pull-up supply is enabled, even if the VIN and EN are still disabled.
11	FB	Feedback. An external resistor divider from the output sets the output voltage where the PG pin switches. The rising threshold is 0.6V with 65mV hysteresis.
12	PD	Output Discharge. Connect to the output to provide a 500Ω load to discharge the output when the part is disabled. No Connect disables this function.
13-20	OUT	Output. Voltage controlled by the IC. Place a Schottky diode between the OUT pin and GND pin.
21-22, Exposed Pads	VIN	Input Power Supply.

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BLOCK DIAGRAM

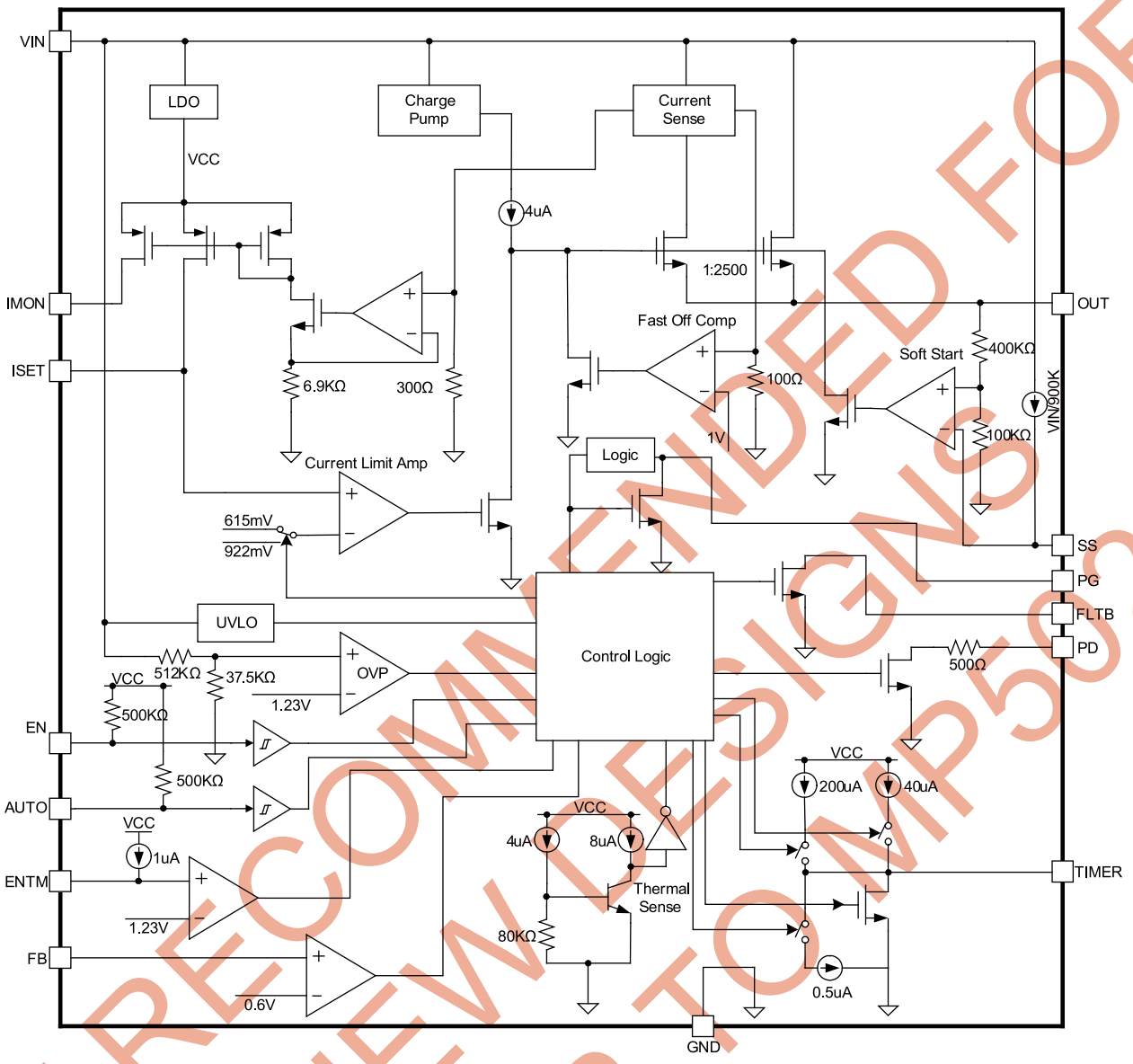


Figure 1: Functional Block Diagram

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OPERATION

The MP5021 limits the in-rush current to the load when a circuit card is inserted into a live backplane power source; thereby limiting the backplane's voltage drop and the dV/dt of the voltage to the load. It provides an integrated solution to monitor the input voltage, output voltage, output current, and die temperature to eliminate the need for an external current-sense power resistor, power MOSFET, and thermal sense device.

Current Limit

The MP5021 provides a constant current limit that can be programmed by an external resistor. Once the device reaches its current limit threshold, the internal circuit regulates the gate voltage to hold the current in the power FET constant. In order to limit the current, the gate to source voltage needs to drop from 5V to around 1V. The typical response time is about 20μs and the output current may have a small overshoot during this time period.

When the current limit triggers, the fault timer starts. If the output current falls below the current limit threshold before the end of the fault timeout period, the MP5021 resumes normal operation. Otherwise, if the current limit duration exceeds the fault timeout period, the power FET turns off. The subsequent behavior relates to the AUTO pin configuration. If the temperature reaches the thermal protection threshold during the fault timeout period, the power FET turns off.

When the AUTO pin is floating, the part functions in hiccup mode for over-current protection (OCP). The part enters latch-off mode when the AUTO pin to pulls to ground once it detects an over-current condition and the duration exceeds the preset value.

When the device reaches either its current limit or its over-temperature threshold, the FLTB pin is driven low with a 10μs propagation delay to indicate a fault. The desired current limit at normal operation is a function of the external current limit resistor.

Short-Circuit Protection

If the load current increases rapidly due to a short circuit, the current may exceed the current limit threshold by a lot before the control loop can respond. If the current reaches a 25A secondary current limit level, a fast turn-off circuit activates to turn off the power FET using a 100mA pull-down gate discharge current, as shown in Figure 2. This limits the peak current through the switch to limit the input voltage drop. The total short circuit response time is about 200ns. And the FLTB switches low once it reaches a 25A current limit, and asserts low until the circuit resume to normal.

Fault Timer & Restart

When the current reaches its over current limit threshold, a 200μA fault timer current source charges the external capacitor C_T at the TIMER pin. If the current limit state ceases before the TIMER pin reaches 1.23V, the MP5021 returns to normal operation mode and a low-value resistor discharges C_T after the TIMER voltage reaches 1.23V. If the current limit state continues after the TIMER pin voltage reaches 1.23V, the power FET switches off. The subsequent restart procedure then depends on the selected retry configuration.

If the AUTO pin connects to ground or low, the MP5021 will latch off. Restart the input power or cycle the EN signal to resume function.

Floating the AUTO pin causes the device to work in hiccup mode, as shown in Figure 3. At the end of the fault timeout period, the power switch turns off, and a low current sink of 0.5μA discharges the external capacitor C_T.

When the TIMER voltage reaches the low threshold 0.2V, the part restarts. If the fault condition remains, the fault timeout period and restart timer repeat.

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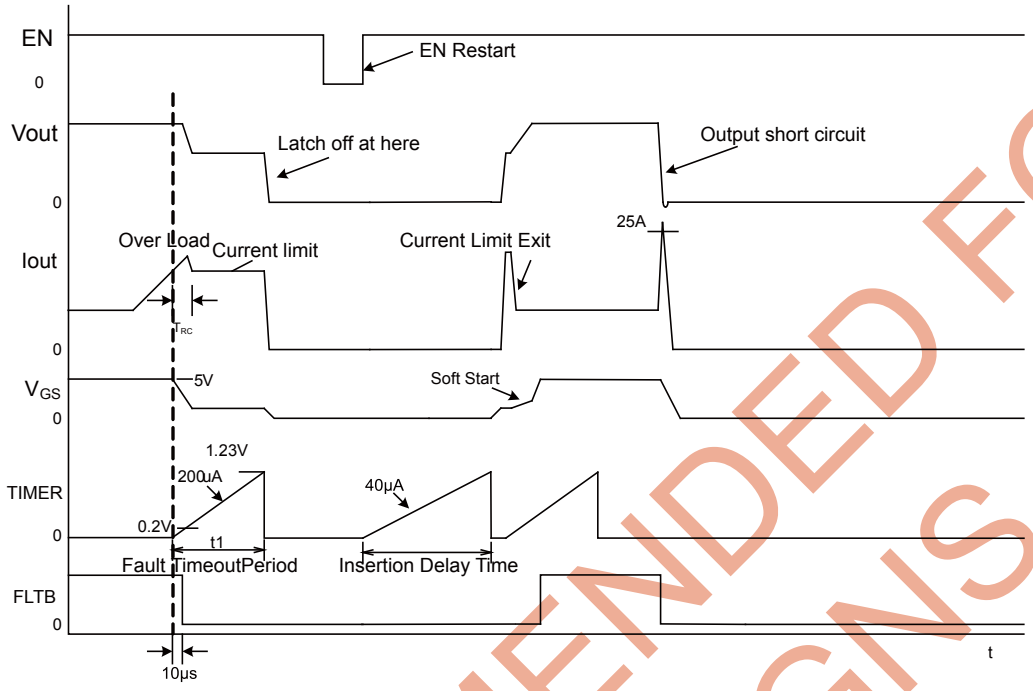


Figure 2: Over-Current Protection (Latch-Off Mode, AUTO=Low)

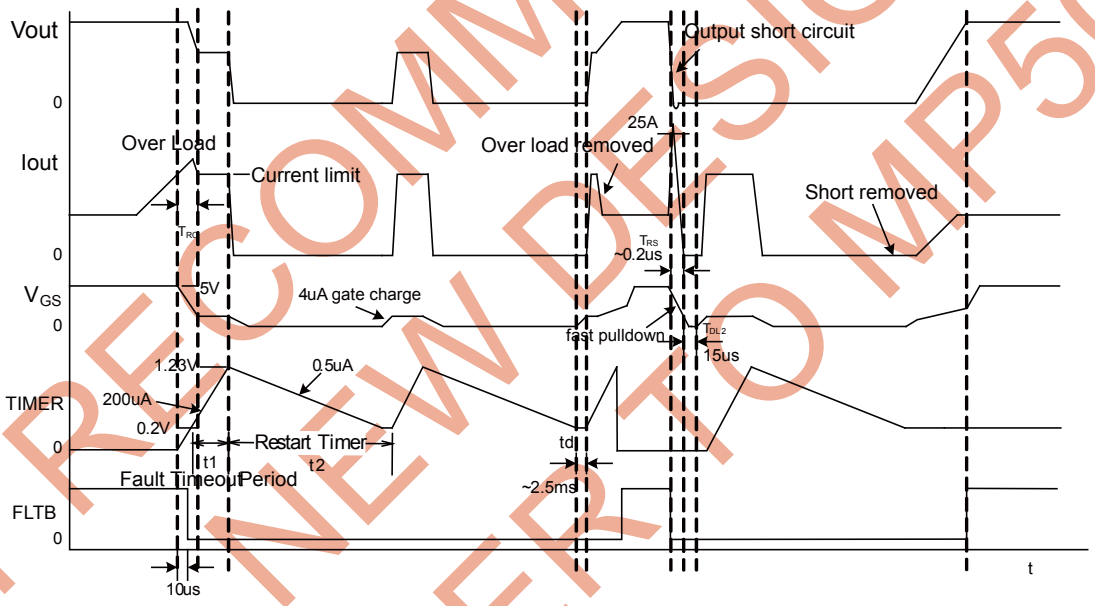


Figure 3: Over-Current Protection (Auto-Retry Mode, AUTO=High)

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Power-Good

The power-good indicates whether the output voltage is in the normal range relative to the input voltage, and is the open drain of a FET. Pull up the PG pin to the external power supply through a 100kΩ resistor. During power-up the power-good output is driven low. This directs the system to remain off and minimize the OUT load to reduce in-rush current and power dissipation during start-up.

When the device reaches the following conditions:

A. V_{FB}>0.6V
B. V_{GS}>3V
C. V_{OUT}> V_{IN}-1V

The power-good signal is pulled high. The system can now draw full power.

When the FB voltage drops below 0.535V, the power FET's V_{GS} voltage is less than a 3V or the output voltage is less than V_{IN}-1V, PG is switched low.

The PG output is pulled low when either the EN pin is below its threshold or the input UVLO/OVLO is triggered.

With no input, the power good stays at a logic low level in the presence of a pull-up supply.

FLTB Pin

The fault bar (FLTB) pin is an open drain output used to indicate that a fault has occurred. Pull up the FLTB pin to external power supply through a 100kΩ resistor.

When the device reaches its current limit, the die temperature exceeds the thermal shutdown threshold, or the MOSFET is shorted before power-up, the fault output is driven low with a 10μs propagation delay. If a short occurs and the current reaches its 25A secondary current limit, the FLTB will switch low with an ~8μs delay.

The FLTB goes high when the MP5021 resumes normal operation, which means the output voltage exceeds the setting voltage of the PG-rising threshold and power FET is fully ON (V_{GS}>3V).

External Pull-Up Voltage for PG and FLTB

The PG and FLTB need an external power supply. The open-drain output of PG can work well from the external pull-up voltage even when V_{IN}=0 and EN is disabled. Use a 100kΩ pull-up resistor for PG and FLTB.

Power-Up Sequence

For hot-swappable applications, the input of the MP5021 can experience a voltage spike or transient during the hot-plug procedure. This spike is caused by the parasitic inductance of the input trace and the input capacitor. An insertion delay determined by the external capacitor at the TIMER pin stabilizes the input voltage.

As per Figure 4 (EN floating), the input voltage rises immediately, and a 30Ω resistor pulls the internal V_{GS} voltage low .

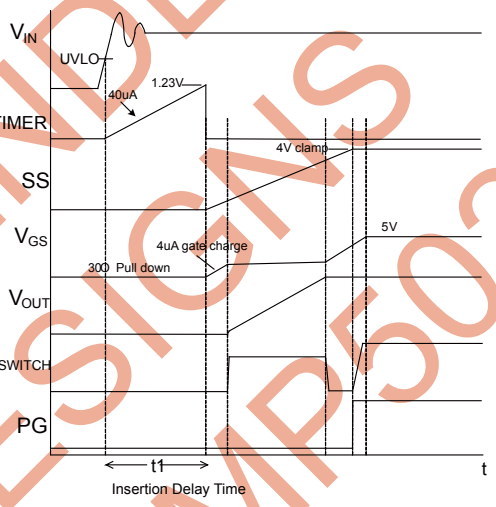


Figure 4: Start-Up Sequence

The TIMER pin charges through a 40μA constant-current source when the input voltage reaches the UVLO threshold. When the TIMER pin voltage reaches 1.23V, a 4μA current source pulls up the power FET's gate-source voltage. Meanwhile, the TIMER pin voltage drops. Once the gate voltage reaches its threshold, V_{GSTH}, the output voltage rises. The soft-start capacitor determines the rise time.

Soft-Start

A capacitor connected to the SS pin determines the soft-start time: When the insertion delay time ends, a constant-current source that is proportional to the input voltage ramps up the voltage on the SS pin. The output voltage rises at a similar slew rate to the SS voltage.

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The SS capacitor value is given by

$$C_{SS} = \frac{5 \cdot \tau_{SS}}{R_{SS}}$$

Where:

τ_{SS}=soft start time

R_{SS}=1MΩ

For example, a 100nF capacitor gives a soft-start time of 20ms.

If the load capacitance is extremely large, the current required to maintain the preset soft-start time will exceed the current limit. Then the load capacitor and the current limit control the rise time.

Float the SS pin to generate a fast ramp-up voltage. A 4μA current source pulls up the gate of the power FET. The gate charge current controls the output voltage rise time. The approximate soft-start time is about 1ms, which is the minimum soft-start time.

Enable Pin and EN Blanking Time

The EN pin enables the part when HIGH and disables the part when low. Floating the EN pin sets the part to auto-startup thanks to an internal 1μA pull-up current source.

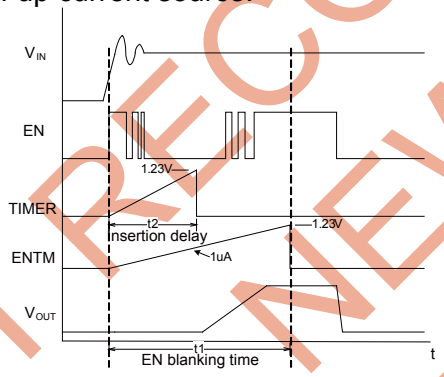


Figure 5: EN Blanking Time

As shown in Figure 5, EN has a programmable blanking time of up to 1s that prevents EN from de-asserting during the blanking time. All fault functionality continues to operative during the start-up so that the power switch shuts down if a fault was detected; however, the switch will not turn off if EN goes LOW during this blanking time.

At the end of the blanking time, EN behaves normally.

Set the blanking time with a capacitor connected to the ENTM pin. The following estimates a value for the blanking timer capacitor:

$$C_{ENB} = \frac{\tau_{ENB} \cdot 10^{-6}}{1.23}$$

Where:

τ_{ENB}=EN blanking time

C_{ENB}=EN blanking time capacitor

For example, a 1μF capacitor gives a blanking time of 1.23s.

Floating the ENTM pin generates a fast ramp-up voltage on the ENTM pin. The blanking time during this period is negligible.

When EN enables the part, the insertion delay timer starts. When the insertion delay time ends, the internal 4μA current source charges the power FET's gate. Charging takes about 1.5ms for V_{GS} to reach its threshold. Then the output voltage rises following the SS-controlled slew rate.

Damaged MOSFET Detection

The MP5021 can detect a shorted pass FET during power-up by treating an output voltage that exceeds V_{IN}-1V during power-up as a short on the MOSFET. The FLTB pin goes low to indicate a fault condition and the power switch remains off. Once the $V_{OUT} \leq V_{IN}$-1, the part starts up normally.

Internal VCC Sub-Regulator

The MP5021 has an internal 5V linear sub-regulator that steps down the input voltage to generate a 5V power supply that powers low-voltage circuitry. The regulator is enabled when V_{IN} exceeds its UVLO threshold and EN is high. In EN shutdown mode, the internal VCC regulator is disabled to reduce power dissipation.

PD Pin

When the PD pin connects to the output, the part is in pull-down mode. In this mode, when the enable pin is low, an integrated 500Ω pull-down

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resistor attached to the output discharges the output. Adding a resistor between the PD pin and the output results in a slower output drop. If the PD pin is floating, pull-down mode is disabled.

AUTO Pin

When the AUTO pin is floating, the part is in auto-retry mode. In auto-retry mode, the part turns off when it exceeds its thermal limit or current limit timeout, and turns back on when the part cools by 20°C or the restart timer completes.

When the AUTO pin is tied to ground, the part is in latched-fault mode. In the latched-fault mode, a thermal fault or current limit fault latches the output off until the enable line is toggled from low to high or the input voltage restarts.

Under/Over-Voltage Lockout

If the input supply falls below the UVLO threshold or above the OVLO threshold, the output is disabled and the PG pin goes low.

When the supply exceeds the UVLO threshold without exceeding the OVLO threshold, the output is enabled and the PG line is released.

Monitoring the Output Current

The IMON pin provides a voltage proportional to the output current (the current through the power device). Place a 100nF capacitor from IMON to GND to smooth the indicator voltage.

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APPLICATION INFORMATION

Setting the Current Limit (R_{SET})

The MP5021 current limit value should exceed the normal maximum load current, allowing the tolerances in the current sense value. Estimate the current limit from the following equation:

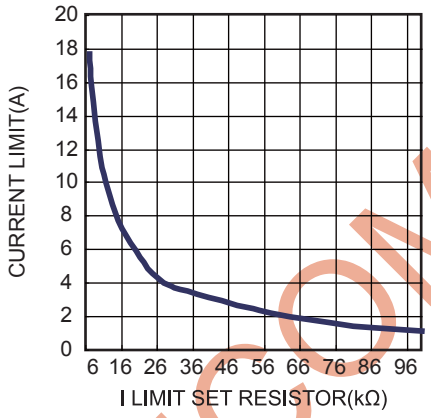
$$I_{limit} = \frac{0.6(V)}{R_{SET}} \times 20 \times 10^4 (A)$$

The table below gives the bench results from the evaluation board.

Current Limit vs. Current Limit Resistor

Current Limit Resistor (kΩ)	7.5	10	20
Current Limit (A)	15.9	12.1	6.08

R_{SET} VS. Current Limit



Current Monitor

MP5021 provides a power-MOSFET-current monitoring function. Place a resistor (R_{MON}) to ground to set the gain of the output as per the following equation:

$$IIMON = \frac{I_{powerfet}}{10^5}$$

Where $I_{powerfet}$ is the power MOSFET current.

For example:

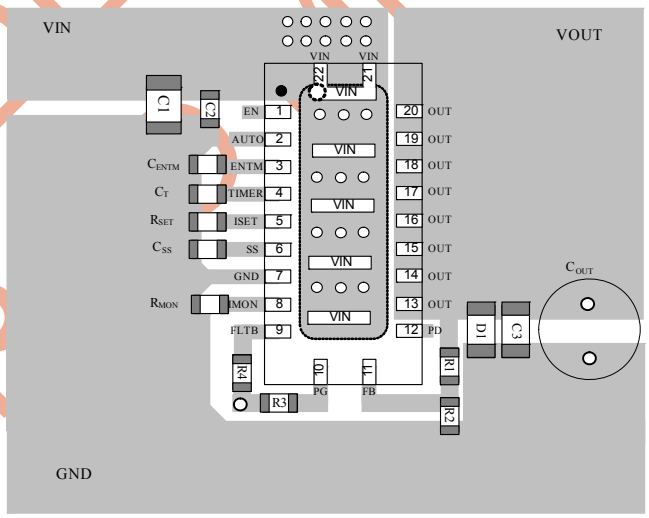
R_{MON} = 100kΩ→1V/A.

R_{MON} = 10kΩ→100mV/A.

PCB Layout Guide

Use the following layout guidelines for the MP5021:

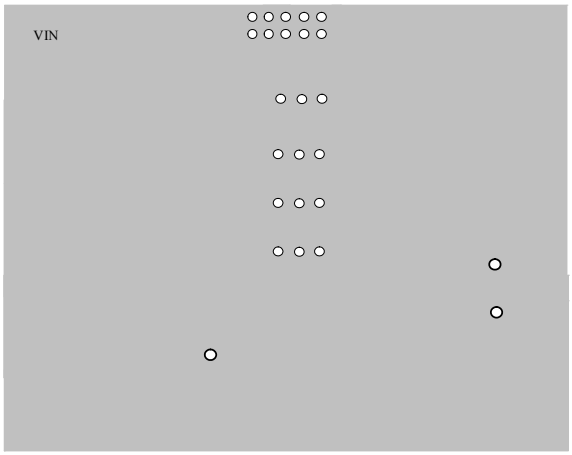
1. Place the high-current paths (GND, IN, and OUT) very close to the device using short, direct, and wide traces.
2. Place the input capacitors as close to the IN and GND pins as possible.
3. Place the external feedback resistors next to the FB pin. Avoid placing any vias on the FB trace
4. Place the Schottky diode close to the OUT and GND pins. This Schottky diode can limit the Vout negative excursion at the OUT pin when the load current shuts off.
5. Connect the IN and GND pads to large copper to achieve better thermal performance.
6. Place a small capacitor, (for example 1nF) directly adjacent the VIN and GND pins to minimize transients on the input supply line.
7. Put vias in the thermal pad and provide a large copper area near the IN pin to improve thermal performance.



Top Layer

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Bottom Layer

Figure 6: PCB Layout

Design Example

The detailed application schematic is shown in Figure 7. The typical performance and circuit waveforms have been shown in the Typical Performance Characteristics section. For more detailed device applications, please refer to the related Evaluation Board Datasheets of MP5021.

TYPICAL APPLICATION

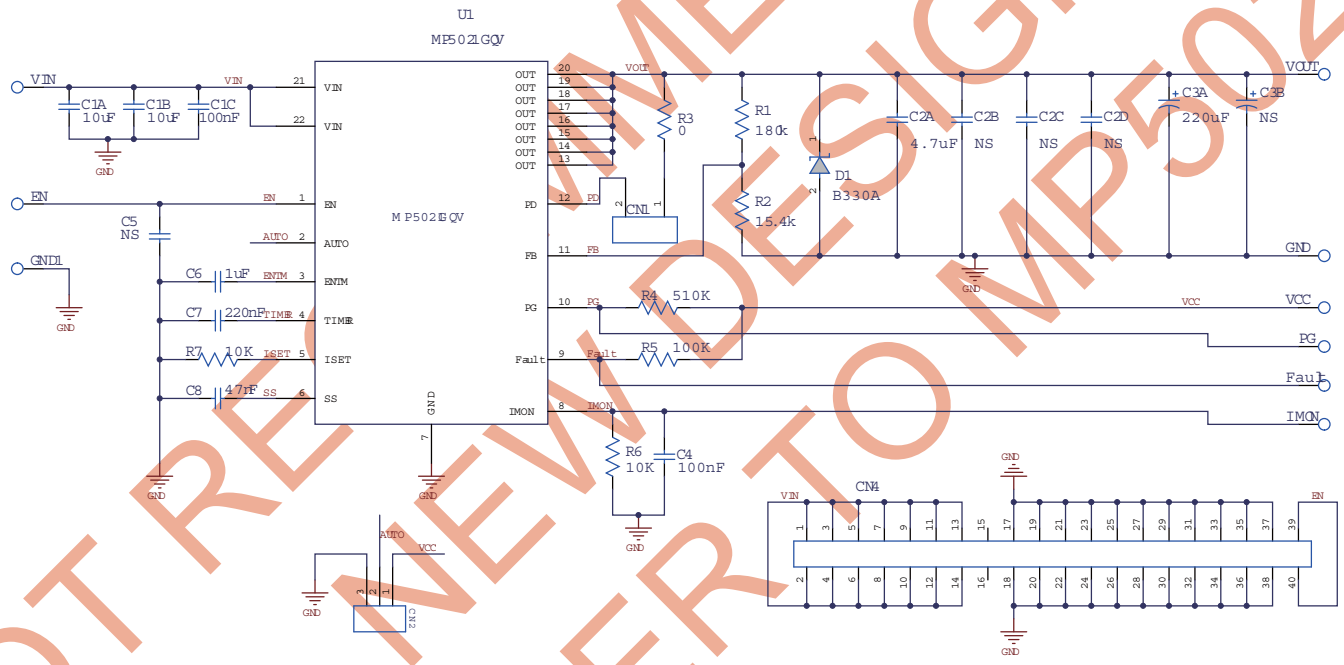


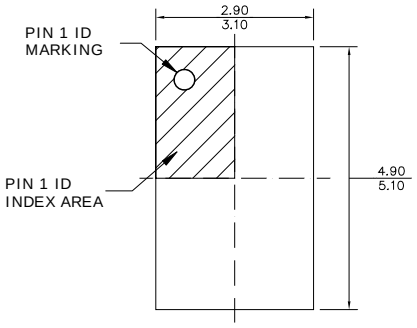
Figure 7: Typical Application Circuit with Soft Start time 10ms, Current Limit 12A

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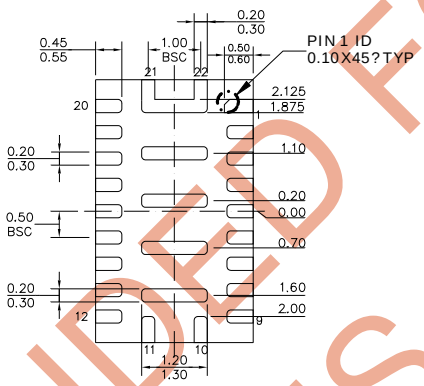
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PACKAGE INFORMATION

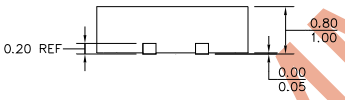
QFN22 (3x5mm)



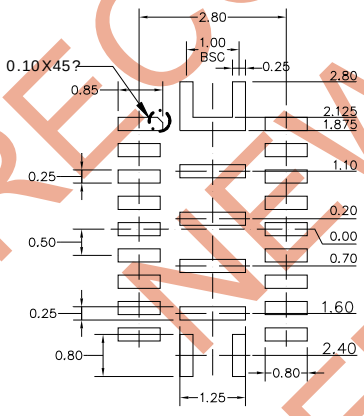
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

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