MP5048

60V, 15A, 7mΩ $R_{DS(ON)}$ Hot-Swap Intelli-Fuse Solution

DESCRIPTION

The MP5048 is a monolithic, integrated controller and switch. It contains a high-side MOSFET and circuitry that enable it to operate as a standalone device, or to be controlled by a hot-swap controller. The MP5048 is capable of driving up to 15A of continuous current per MP5048 device.

The device limits the inrush current to the load when a circuit card is inserted into a live backplane power source. This limits the backplane's voltage drop. The MP5048 also limits the internal MOSFET current by controlling the gate voltage through the current-limit reference input.

The MP5048 offers many features to simplify the system design. It provides an integrated solution to monitor the output current and the die temperature, eliminating the need for an external current-sense power resistor, power MOSFET, or thermal sense.

The MP5048 detects the power FET gate, source, and drain short conditions, and provides feedback for the controller. The device can be paralleled for higher current applications.

The MP5048 is available in an QFN-30 (5mmx5mm) package.

FEATURES

- 24V to 60V Operating Input Range
- Maximum 15A Output Current
- Integrated 7mΩ Power FET
- Built-In MOSFET Driver
- Integrated Current Sensing with Sense Output
- Separate Current Sensing Output Used to Configure the Over-Current Value
- Built-In Soft Start and Insertion Delay
- Output Short-Circuit Protection
- Over-Temperature Protection
- Built-In Fuse Health Diagnostics
- Fault Signal Output
- Parallel Operation for Higher Current Applications
- Integrated Intelli-Fuse Temperature Sense
- Output Voltage Power-Down Control
- Available in an QFN-30 (5mmx5mm) Package

APPLICATIONS

- Industrial Applications
- Servers
- Networking

All MPS parts are lead-free, halogen-free, and adhere to the RoHS directive. For MPS green status, please visit the MPS website under Quality Assurance. "MPS", the MPS logo, and "Simple, Easy Solutions" are trademarks of Monolithic Power Systems, Inc. or its subsidiaries.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2021 MPS. All Rights Reserved.

TYPICAL APPLICATIONS

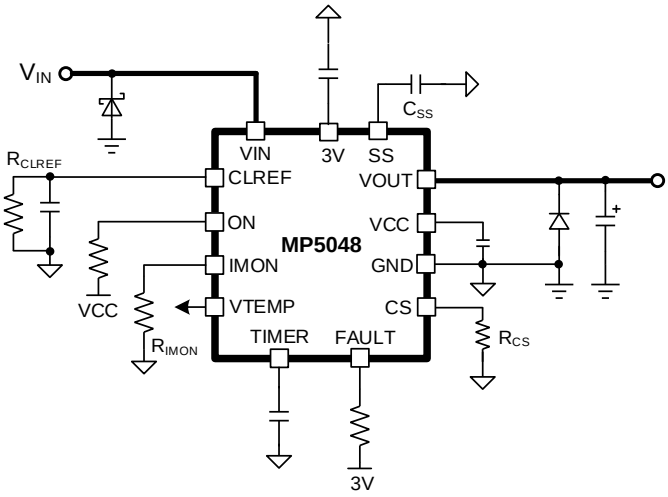


Figure 1: MP5048 Standalone Operation (Set $R_{IMON} \geq R_{CS}$)

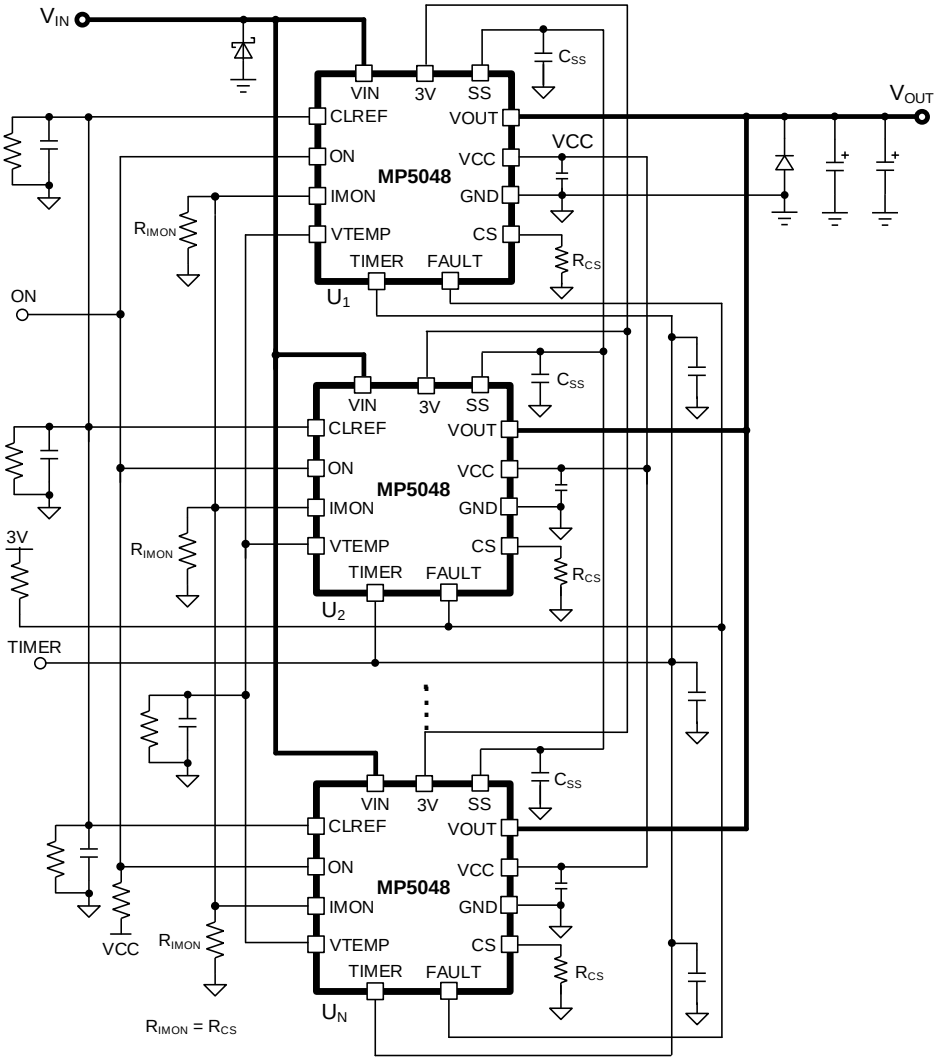


Figure 2: MP5048 Parallel Operation

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2021 MPS. All Rights Reserved.

TYPICAL APPLICATIONS *(continued)*

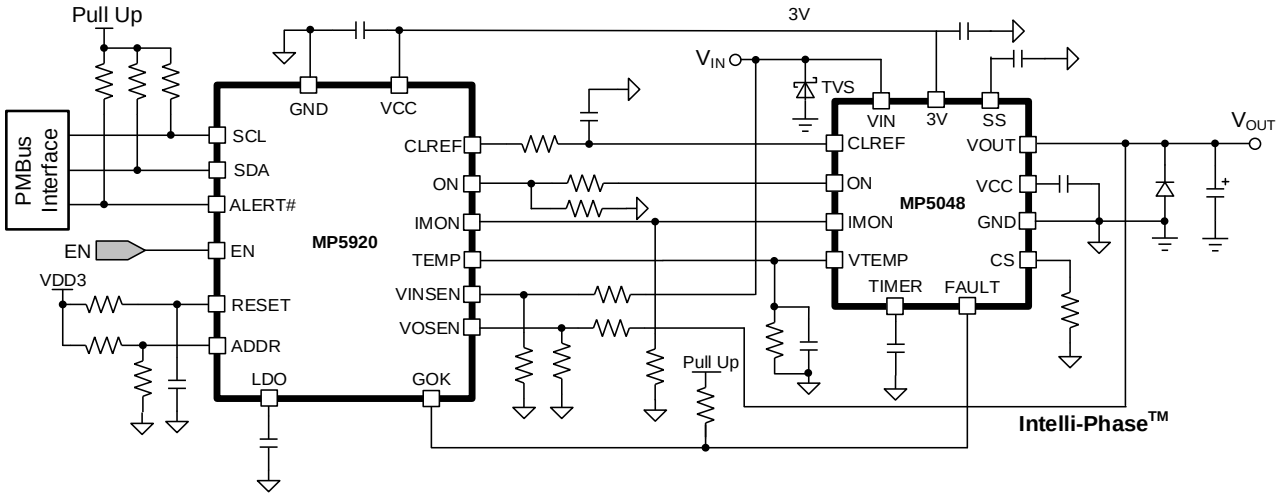


Figure 3: MP5048 Controlled by Hot-Swap Controller

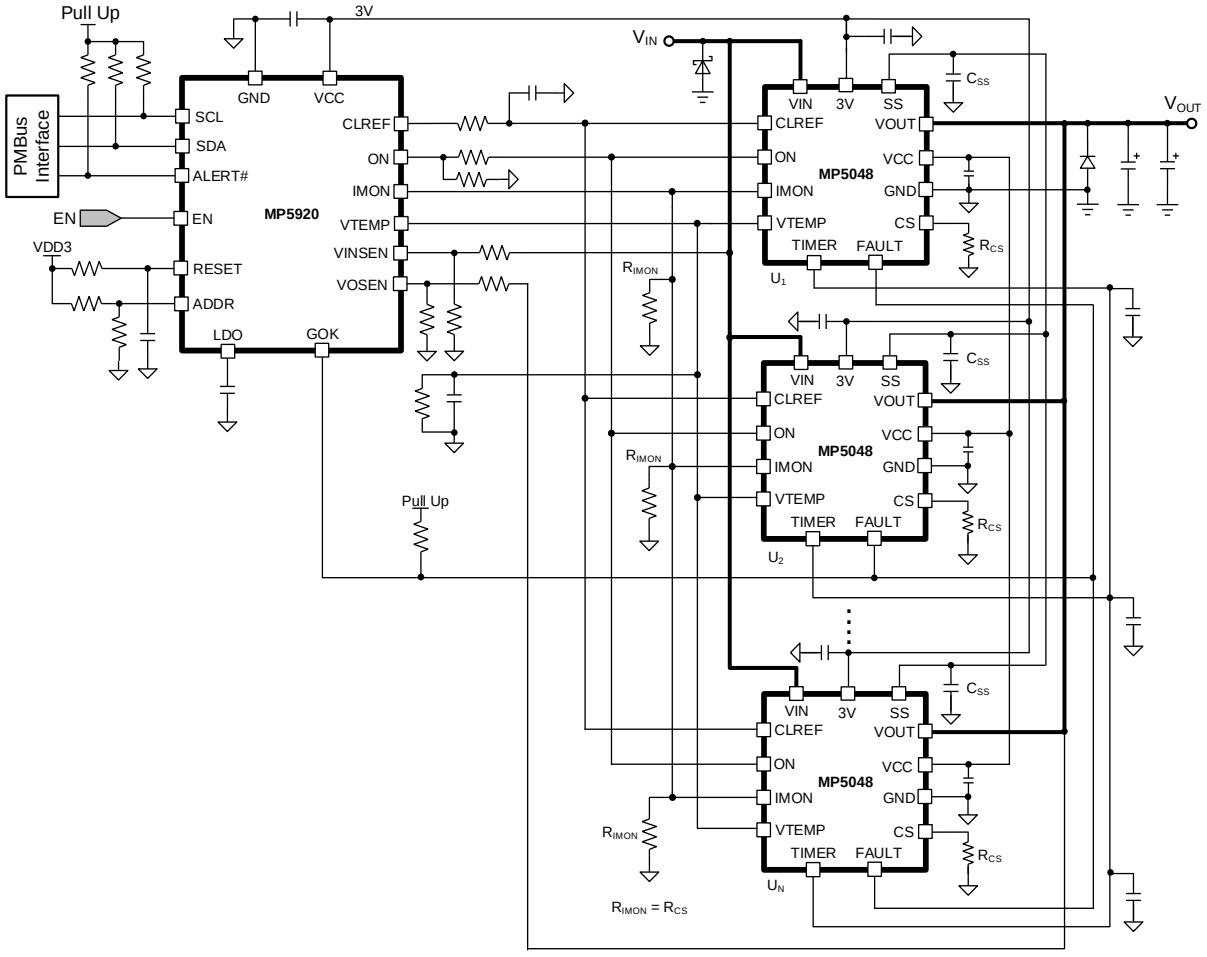


Figure 4: MP5048 Controlled by Hot-Swap Controller in Parallel Operation

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2021 MPS. All Rights Reserved.

ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MP5048GU	QFN-30 (5mmx5mm)	*See Below*	1

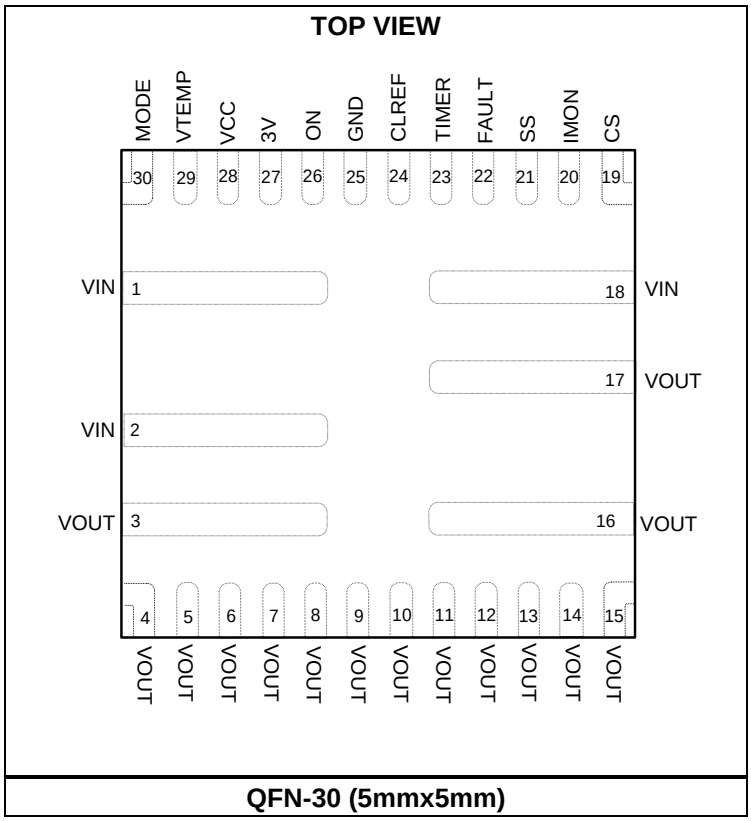
* For Tape & Reel, add suffix -Z (e.g. MP5048GU-Z).

TOP MARKING

MPSYYWW
MP5048
LLLLLLL

MPS: MPS prefix
YY: Year code
WW: Week code
MP5048: Part number
LLLLLLL: Lot number

PACKAGE REFERENCE



QFN-30 (5mmx5mm)

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2021 MPS. All Rights Reserved.

PIN FUNCTIONS

Pin #	Name	Description
1, 2, 18	VIN	**System input power supply.** The MP5048 operates from a 24V to 60V input rail.
3–17	VOUT	**Output voltage controlled by the IC.** VOUT is connected to the source of the integrated MOSFET.
19	CS	**Current-sense output.** CS requires an external resistor. The CS voltage (V_{CS}) is compared to CLREF to determine the current limit.
20	IMON	**Current monitor output.** The output current is proportional to the current flowing through the power device. Place a resistor (R_{IMON}) to GND to set the output gain.
21	SS	**Soft-start set.** An external capacitor connected to SS sets the output voltage soft-start time. The internal circuit controls the slew rate of the output voltage during start-up.
22	FAULT	**Fault indication.** Open-drain output. FAULT indicates that a fault condition has occurred.
23	TIMER	**Timer set.** An external capacitor sets the insertion delay, over-current protection (OCP) delay time, and the retry time.
24	CLREF	**Current-limit reference voltage input.** The CLREF pin sets the voltage reference for the over-current prtotection (OCP) level. Connect a resistor to GND, or drive via an external source.
25	GND	**Ground.**
26	ON	**Power FET on/off control.** Drive the ON pin high to enable the MP5048.
27	3V	**Internal 3V LDO output.** Place a 2.2µF decoupling capacitor close to 3V and GND.
28	VCC	**Internal 4.5V LDO output.** VCC can be driven with an external 4.5V to reduce loss from VIN. Place a 2.2µF decoupling capacitor close to VCC and GND.
29	VTEMP	**Junction temperature sense output.** Output of the internal temperature sensor
30	MODE	**Latch or hiccup operation.** When the MODE pin is pulled high, the part latches off if a fault occurs. It can be configured to latch-off mode by pulling the MODE pin up to 5V externally, or floating this pin since MODE is internally pulled up. When MODE is pulled low externally, the part operates in auto-retry mode.

ABSOLUTE MAXIMUM RATINGS (1)

$V_{IN(DC)}$ ..... -0.3V to +65V
$V_{IN(25ns)}$ 72V
V_{OUT} ..... -0.3V to +65V
All other pins ..... -0.3V to +6.5V
Continuous power dissipation (T_A = 25°C) (2) 5.58W
Junction temperature ..... 150°C
Lead temperature ..... 260°C
Storage temperature ..... -65°C to +155°C

Recommended Operating Conditions (3)

Input voltage operating range ..... 24V to 60V
Operating junction temp (T_J) .... -40°C to +125°C

Thermal Resistance (4) θ_{JA} θ_{JC}

QFN-30 (5mmx5mm)..... 22.4 ..... 9.6.. °C/W

Notes:

1) Exceeding these ratings may damage the MP5048.
2) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the MP5048 from permanent damage.
3) The MP5048 is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2021 MPS. All Rights Reserved.

ELECTRICAL CHARACTERISTICS

V_{IN} = 48V, R_{CS} = 3.6kΩ, C_{OUT} = 1000µF, T_J = 25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Supply Current						
Quiescent current	I_Q	ON = high, no load		2.2	3	mA
		ON = 0, V_{IN} = 48V		1.6	2.4	mA
VCC Regulator and UVLO						
VCC regulator	V_{CC}		4.45	4.6	4.75	V
VCC load regulation		I_{CC} = 10mA		5		%
VCC under-voltage lockout rising threshold	VCC_{VTH}		3.5	3.65	3.8	V
VCC under-voltage lockout threshold hysteresis	VCC_{HYS}			380		mV
3V regulator	V_{3V}		2.9	3	3.1	
VIN Under-Voltage/Over-Voltage Protection (UVP, OVP)						
VIN under-voltage protection rising	VIN_{UVR}	V_{CC} = 5V		5.25		V
VIN under-voltage protection falling	VIN_{UVF}	V_{CC} = 5V		5		V
VIN OV fault threshold	VIN_{OVP}	ON = 0V		64		V
VIN OV hysterisis	$VINI_{OV_HYS}$			2		V
Power FET						
On resistance	$R_{DS(ON)}$	T_J = 25°C		7		mΩ
		T_J = 85°C (5)		9		
Off state leakage current	I_{OFF}	ON = 0V			5	µA
Maximum continuous current (5)	I_{OUT_MAX}				15	A
Thermal Shutdown and Recovery						
Shutdown temperature (5)	t_{STD}			153		°C
Hysteresis (5)	t_{HYS}	Auto-retry mode only		26		°C
CLREF						
Internal current source	I_{CLREF}			26		µA
Soft-start current limit	SS_{LIMIT}			8		µA
CS						
CS gain accuarcy		1A ≤ I_{OUT} ≤ 15A	-2.5		+2.5	%
CS gain				25		µA/A
Soft Start						
SS pull-up current	I_{SS}	V_{IN} = 48V		11.5		µA
Current Limit						
Primary current limit during normal operation	I_{LIMIT_PRIM}	R_{CS} = 3.6kΩ, R_{CLREF} = 53.6kΩ		15.5		A
Primary current limit response time (5)	t_{CL_PRIM}	I_{LIMIT} = 15A		20		µs
Secondary current limit (5)	I_{LIMIT_SCD}	Regardless of R_{CS}		26		A
Short-circuit protection response time (5)	t_{SC}			200		ns
Output Current Monitor						
I_{IMON}/I_{OUT} gain	A_{IMON}			25		µA/A
I_{IMON}/I_{OUT} gain accuracy	A_{IMON_ACCR}	1A ≤ I_{OUT} ≤ 15A	-1.5		+1.5	%

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2021 MPS. All Rights Reserved.

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 48V, R_{ISET} = 3.6kΩ, C_{OUT} = 1000µF, T_J = 25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Maximum IMON pin voltage (5)	V_{IMON}				2	V
FET Short Detection						
Fault flag for FET drain-to-source short	V_{OUT_DSTH}			0.9 x V_{IN}		V
Fault release high flag when removing drain-to-source short	V_{OUT_FAULTH}			0.7 x V_{IN}		V
FET gate-to-source short detection time	t_{GS_SHRT}			270		ms
Maximum soft-start time	t_{SS_MAX}			270		ms
ON						
Rising threshold	V_{ON_VTH}		1.13	1.23	1.31	V
Hysteresis	V_{ON_HYS}			450		mV
MODE						
Rising threshold	V_{MODE_VTH}		1	1.2	1.4	V
Hysteresis	V_{MODE_HYS}			450		mV
Mode pull-up current source	I_{MODE_SRC}			4		µA
Fault						
Output low voltage	V_{OL_FAULT}	Sink current 1mA			0.2	V
Fault off-state leakage current	I_{FAULT_LKG}	V_{FAULT} = 5V			5	µA

Note:

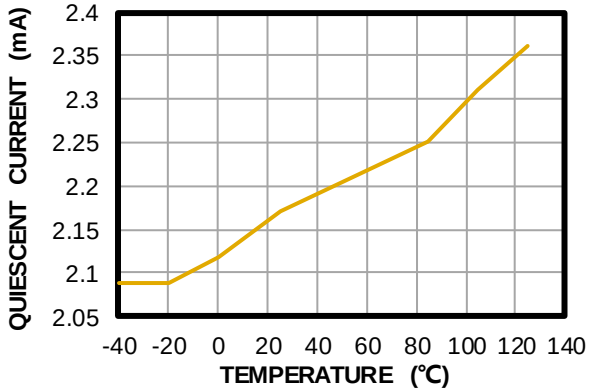
5) Guaranteed by design.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2021 MPS. All Rights Reserved.

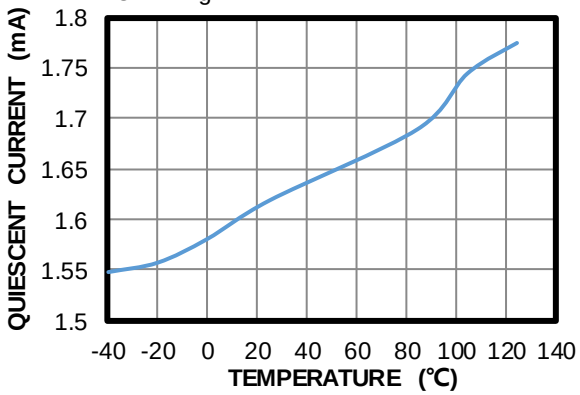
TYPICAL CHARACTERISTICS

V_{IN} = 48V, R_{CS} = 3.6kΩ, C_{OUT} = 1000µF, T_A = 25°C, unless otherwise noted.

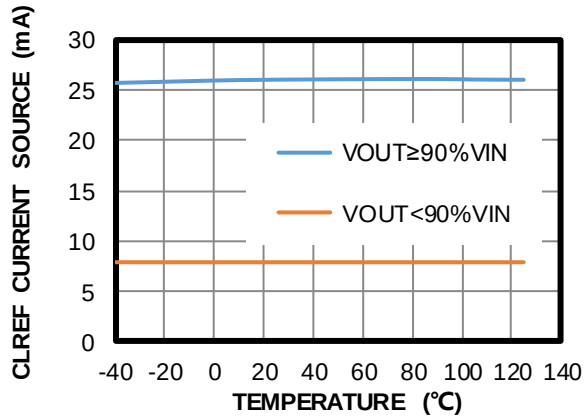
Quiescent Current vs. Temperature
ON = low



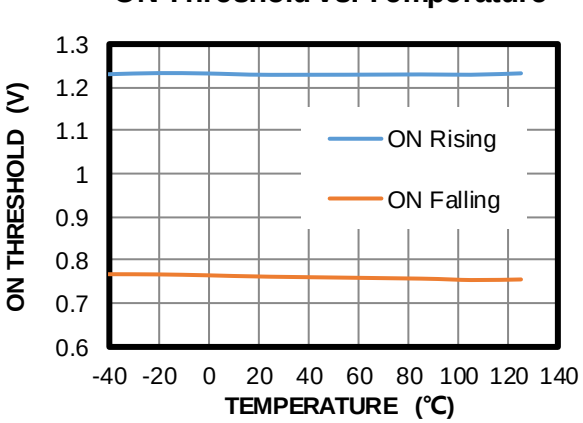
Quiescent Current vs. Temperature
ON = high



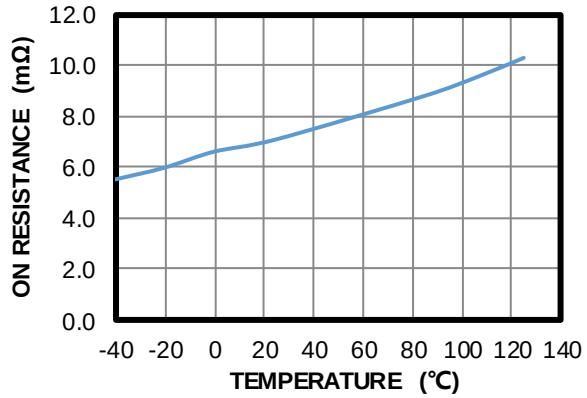
I_{CLREF} vs. Temperature



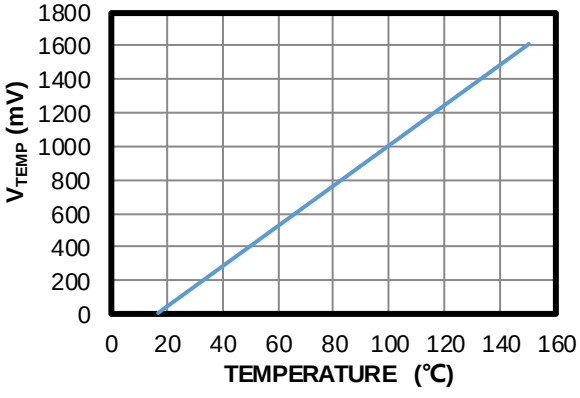
ON Threshold vs. Temperature



$R_{DS(ON)}$ vs. Temperature
I_{OUT} = 1A



No-Load V_{TEMP} vs. Temperature

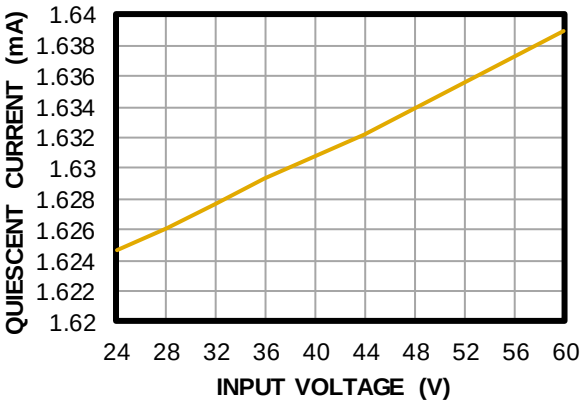


MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2021 MPS. All Rights Reserved.

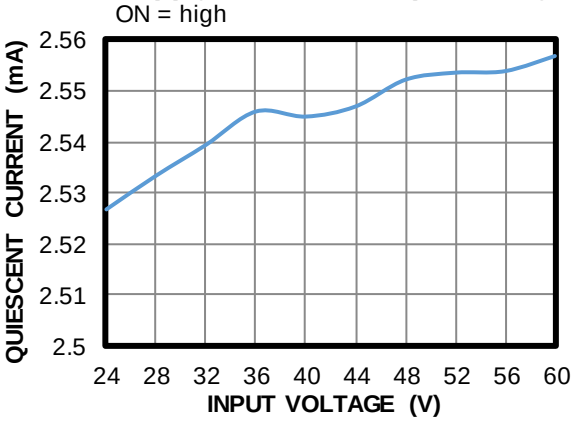
TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 48V, R_{CS} = 3.6kΩ, C_{OUT} = 1000µF, T_J = 25°C, unless otherwise noted.

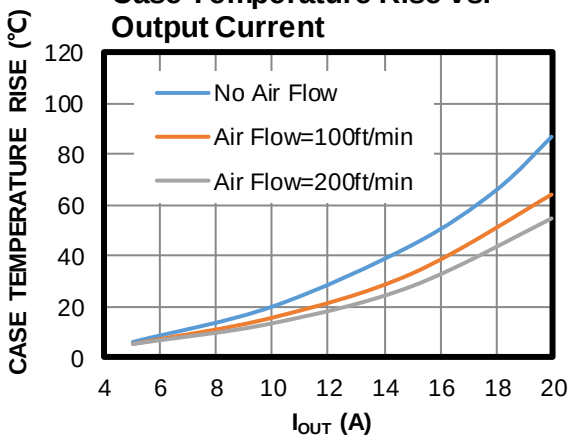
Supply Current vs. Input Voltage
ON = low



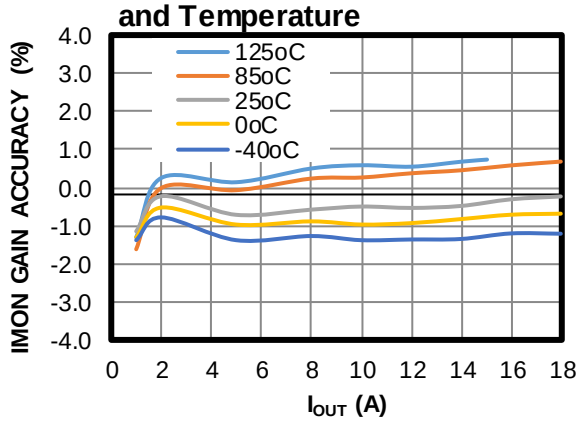
Supply Current vs. Input Voltage
ON = high



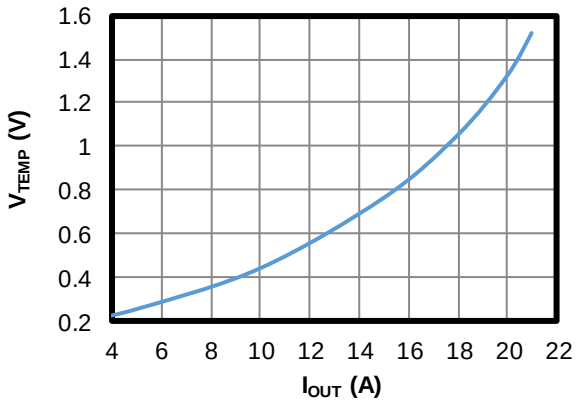
Case Temperature Rise vs. Output Current



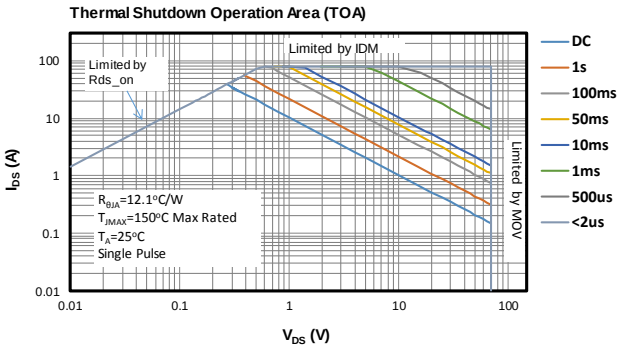
IMON Gain vs. Output Current and Temperature



V_{TEMP} vs. Output Current



Thermal Shutdown Operation Area (TOA)



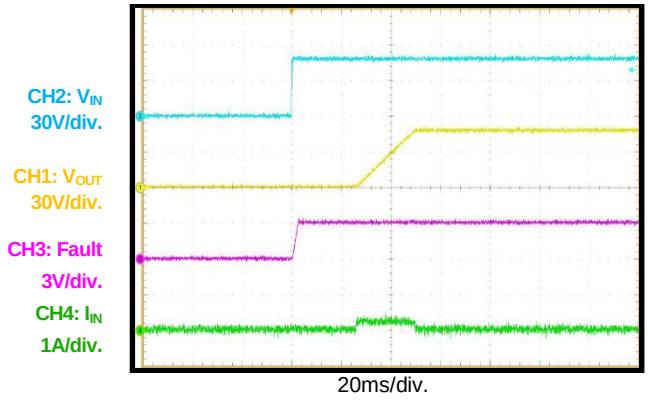
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2021 MPS. All Rights Reserved.

TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 48V, C_{OUT} = 1000µF, R_{CS} = R_{IMON} = 3.6kΩ, C_{TIMER} = 10nF, T_J = 25°C, unless otherwise noted.

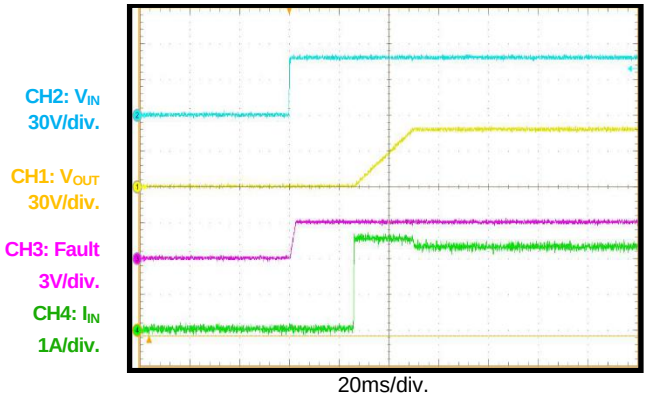
VIN Hot Swap

I_{OUT} = 0A



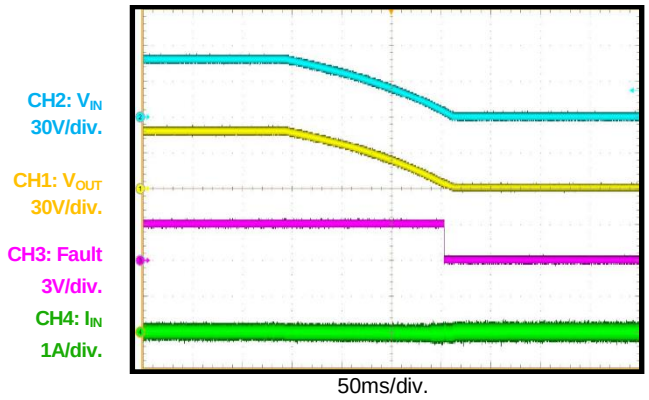
VIN Hot Swap

I_{OUT} = 2A



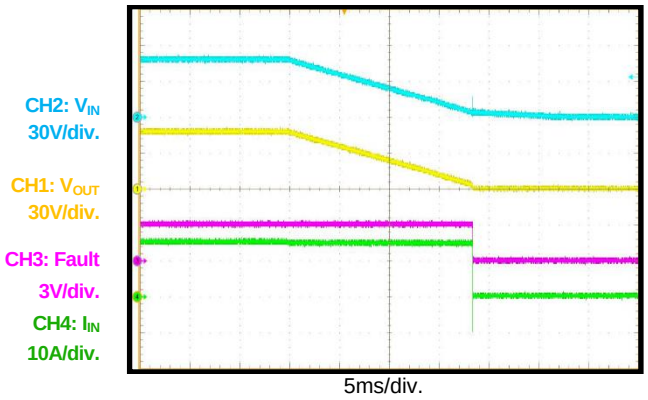
Shutdown through VIN

I_{OUT} = 0A



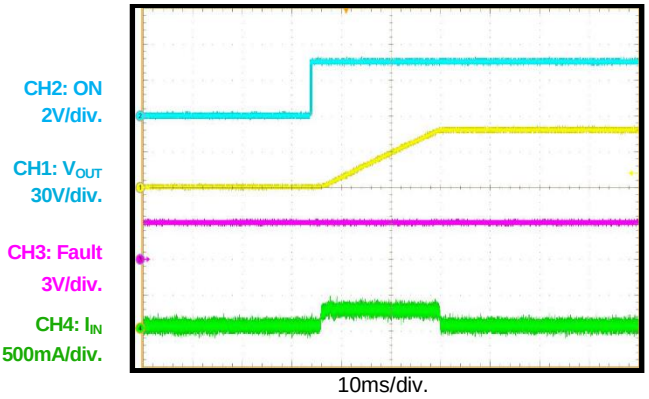
Shutdown through VIN

I_{OUT} = 15A



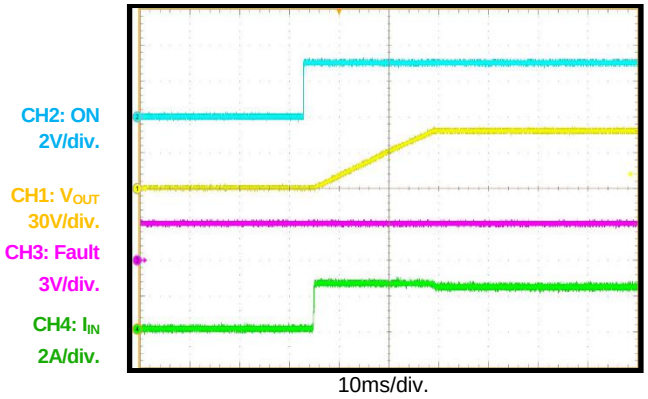
Start-Up through ON

I_{OUT} = 0A



Start-Up through ON

I_{OUT} = 2A



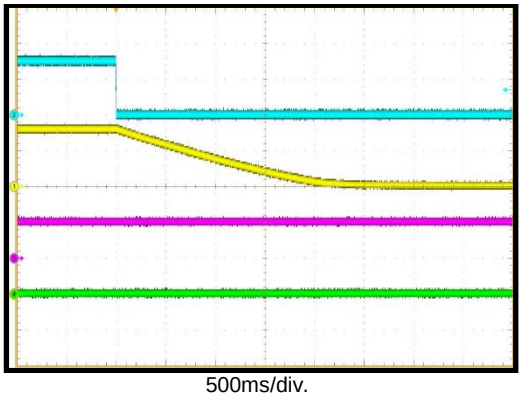
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2021 MPS. All Rights Reserved.

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 48V, C_{OUT} = 1000µF, R_{CS} = R_{IMON} = 3.6kΩ, C_{TIMER} = 10nF, T_J = 25°C, unless otherwise noted.

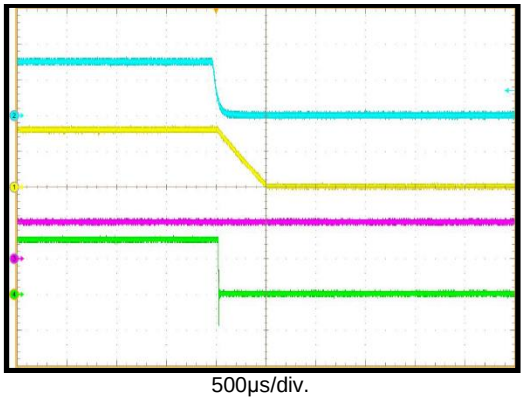
Shutdown through ON

I_{OUT} = 0A



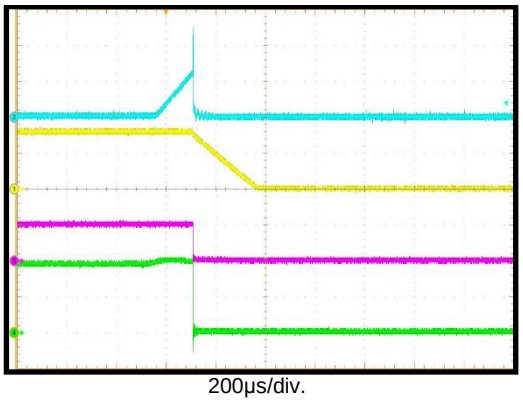
Shutdown through ON

I_{OUT} = 15A



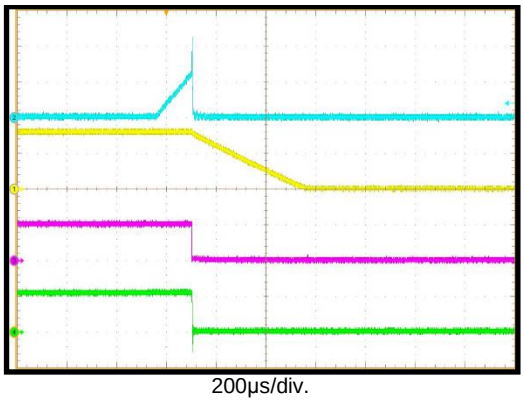
OCP

I_{LIMIT} = 18A



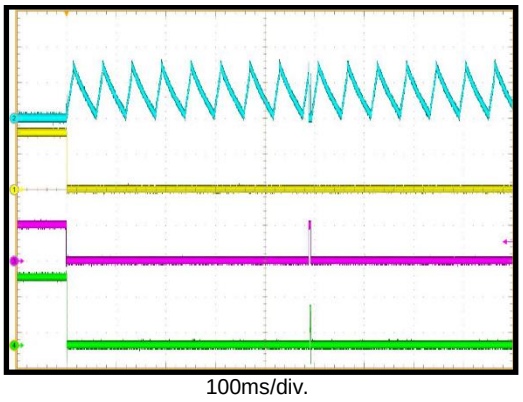
OCP

I_{LIMIT} = 10A

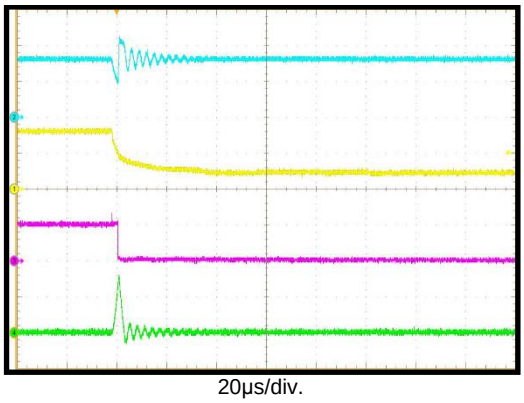


OCP

I_{LIMIT} = 18A, hiccup mode



SCP Entry (V_{IN} Decreases Slowly)



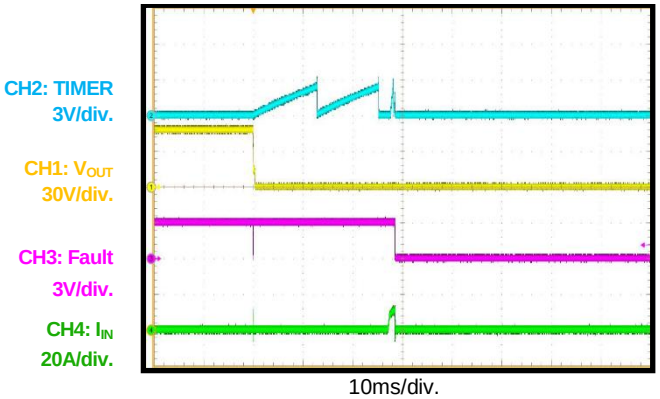
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2021 MPS. All Rights Reserved.

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 48V, C_{OUT} = 1000µF, R_{CS} = R_{IMON} = 3.6kΩ, C_{TIMER} = 10nF, T_J = 25°C, unless otherwise noted.

SCP Entry (V_{IN} Decreases Quickly)

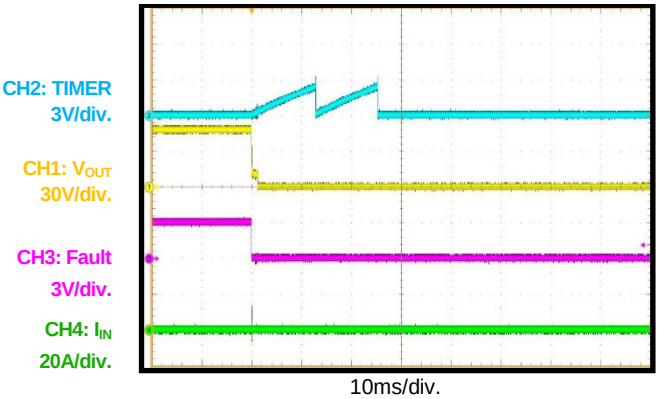
Latch off by SS current limit



10ms/div.

SCP Entry (V_{IN} Descreases Quickly)

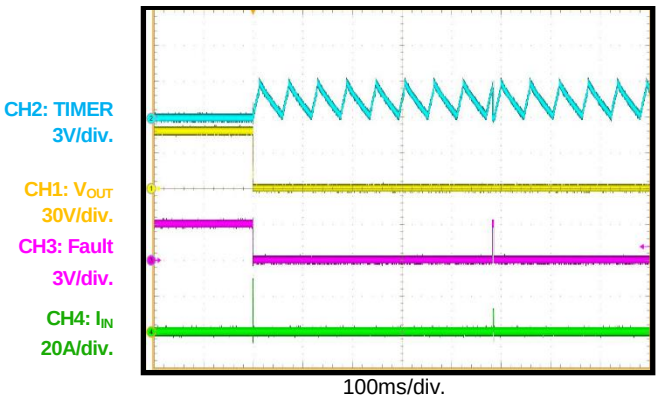
Latch off by SCP condition



10ms/div.

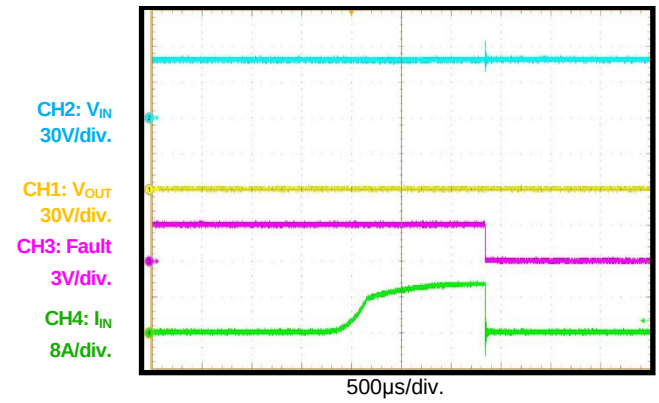
SCP

Hiccup mode



100ms/div.

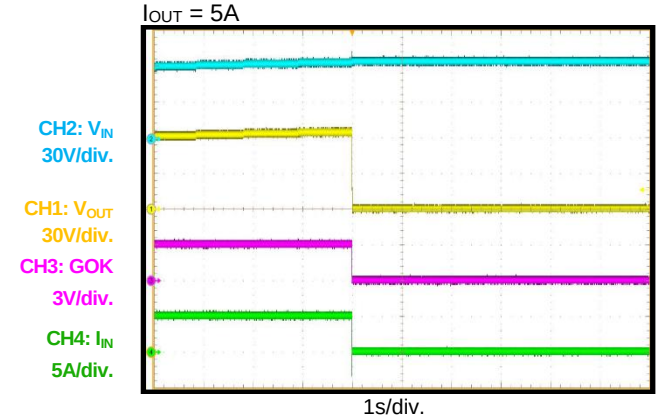
Short Circuit Start-Up



500µs/div.

V_{IN} OVP

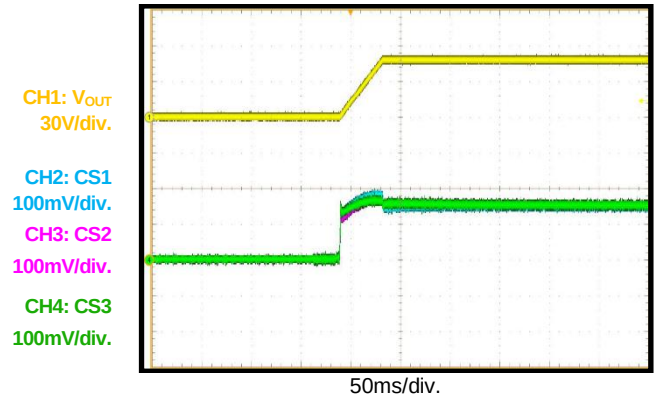
I_{OUT} = 5A



1s/div.

Current Blance during Start-Up with Parallel Operation

Three MP5048 devices in parallel, I_{OUT} = 5A, R_{IMON} = R_{CS} per MP5048 device



50ms/div.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2021 MPS. All Rights Reserved.

FUNCTIONAL BLOCK DIAGRAM

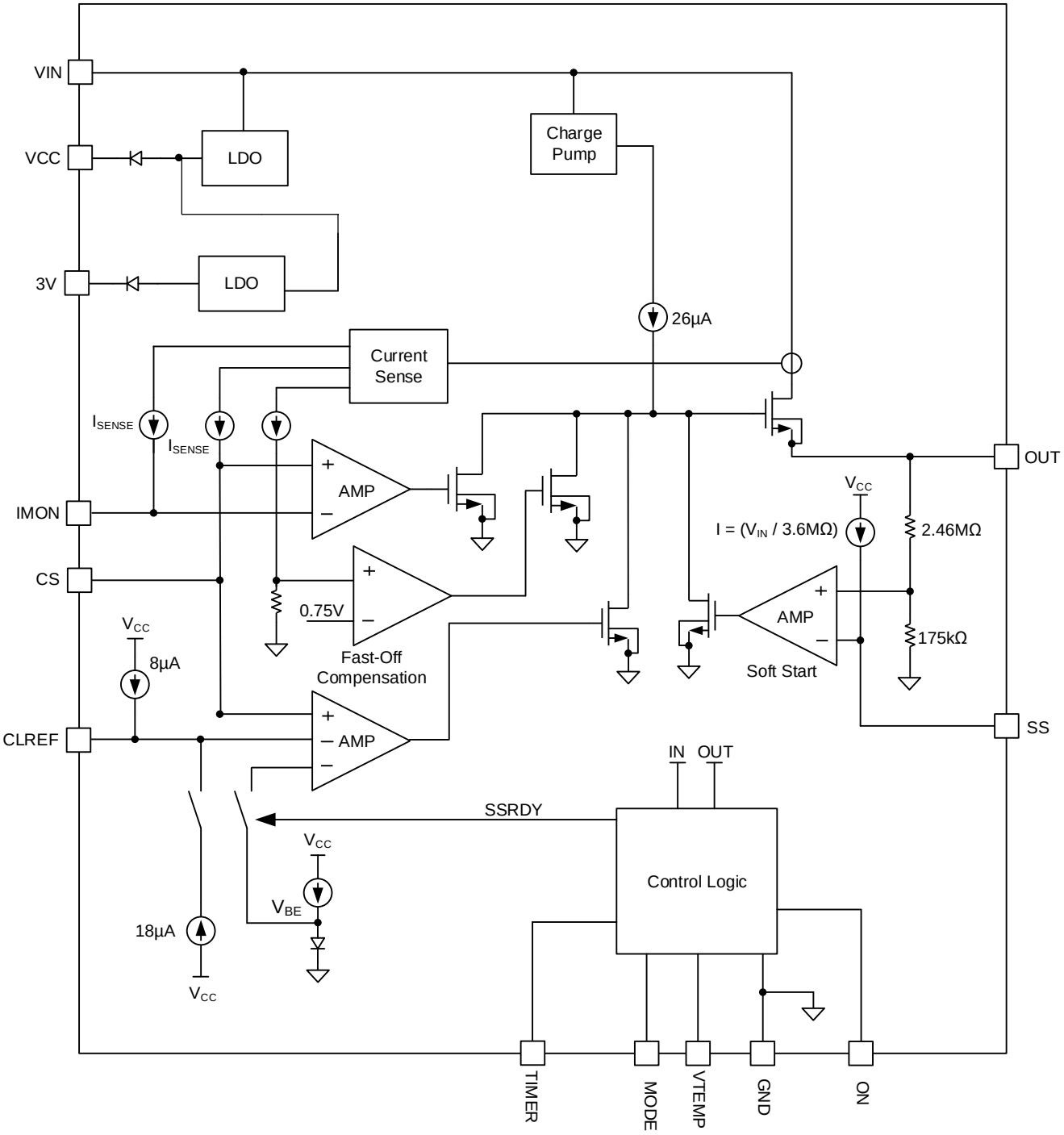


Figure 5: Functional Block Diagram

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2021 MPS. All Rights Reserved.

OPERATION

The MP5048 is a monolithic, integrated controller and switch. It has a high-side MOSFET (HS-FET) with 7mΩ $R_{DS(ON)}$, which makes it ideal for multi-fuse hot-swap or e-fuse applications. The MP5048 can operate in standalone mode, or it can be sequenced with the MP5920/MP5922 controller. Multiple MP5048 devices can be used in parallel to support all power levels required by the system. All devices working in parallel actively share current during soft start, which distributes the load current evenly during soft start (SS) and ensures that each part works in the thermal shutdown operation area (TOA). The MP5048 supports 15A of continuous current per device at room temperature.

The MP5048 provides a controlled start-up voltage and limits the inrush current when a circuit card is inserted into an active power source. The MP5048 provides support for e-fuse and hot-swap applications. It also provides an integrated solution with a MOSFET, temperature-sense, current monitoring, current protection, temperature protection, and power sequencing all in a single device. The MP5048 has integrated on-die current-sense to monitor the current through the MP5048 and die temperature, eliminating the need for an external sense resistor and thermal sensing.

Power-Up Sequence

There are two operation modes for the MP5048: it can be controlled by a hot-swap controller, or act as a standalone device.

If the MP5048 is controlled by a hot-swap controller, the power FET remains off until the ON pin is pulled high.

The MP5048 has configurable settings for the insertion delay, over-current protection (OCP) time, and auto-retry time via a capacitor on the TIMER pin. The insertion delay time starts when V_{IN} reaches the under-voltage lockout (UVLO) threshold. When the ON signal goes high and the insertion delay time ends, the power FET charges up by the internal charge pump. Once the MP5048 power FET voltage (V_{GS}) reaches its threshold (V_{GSTH}), V_{OUT} rises (see Figure 6).

V_{OUT} rises following the soft-start controlled slew rate, and the rise time is determined by the SS capacitor.

During the soft-start turn-on time, the current limit is reduced by an internal limit (called the SS limit). Once soft start has completed, the current limit moves to the full-scale current limit set by the CLREF resistor.

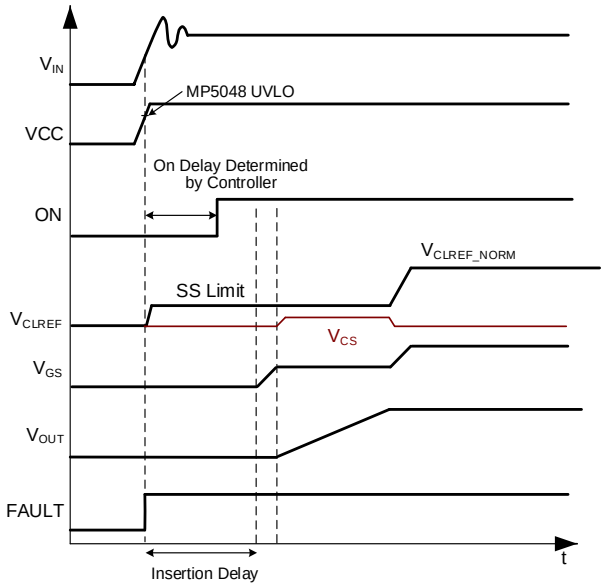


Figure 6: Start-Up When MP5048 Is Controlled by Hot-Swap Controller

The ON pin is low by default, since it's pulled low to ground internally through a 1.1MΩ resistor. If the MP5048 works in standalone mode, ON should be pulled up externally to the VCC (see Figure 7).

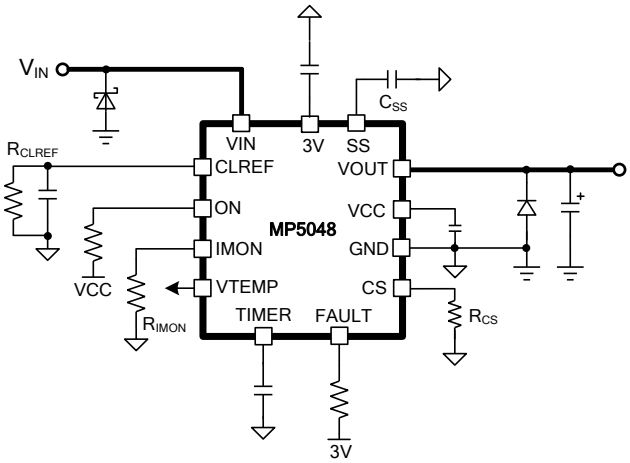


Figure 7: MP5048 Schematic When Operating in Standalone Mode

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2021 MPS. All Rights Reserved.

If the ON voltage exceeds the rising threshold when the insertion delay time ends, the power FET charges up via the internal 26μA current source. The power FET turns on when V_{GS} reaches V_{GSTH}, and then the output voltage rises (see Figure 8).

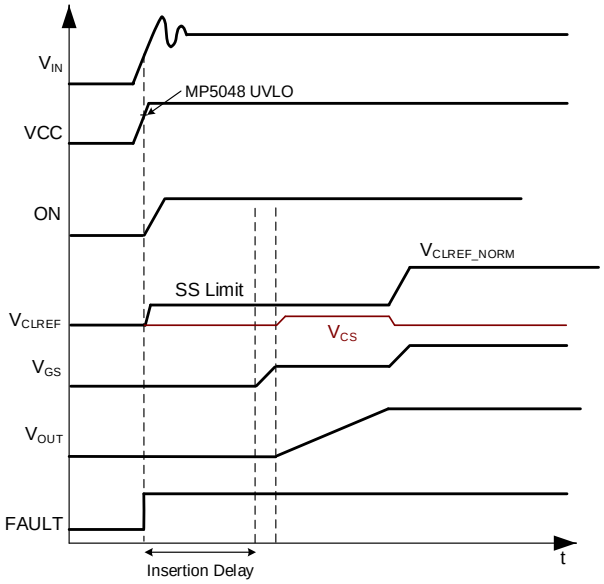


Figure 8: Start-Up when the MP5048 Operates in Standalone Mode

Soft Start (SS)

A capacitor connected to the SS pin determines the soft-start (SS) time. When the ON pin is pulled high and the insertion delay time ends, a constant current source proportional to the input voltage charges up the SS voltage. The output voltage rises at a similar slew rate to the SS voltage.

The SS capacitor value can be calculated with Equation (1):

$$C_{SS} = \frac{15 \times t_{SS}}{R_{SS}} \quad (1)$$

Where t_{SS} is the soft-start time (ms), C_{SS} is the soft-start capacitor (nF), and R_{SS} is 3.6MΩ.

For example, a 100nF capacitor provides a soft-start time of 24ms. If the load capacitance is extremely large, the current required to maintain the preset SS time exceeds the start-up current limit. In this case, the rise time is controlled by the load capacitor and the start-up current limit. Float SS to generate a fast ramp-up voltage.

A 26μA current source pulls up the power FET gate. The gate charge current controls the output voltage rise time. The approximate soft-start time is 1.5ms, which is the minimum output voltage soft start time.

When the MP5048 is used in multi-phases application, all SS pins should be connected together, which ensures all devices have the same SS time.

If a fault condition occurs, the fault and SS pins are pulled low. If the MP5048 is configured for auto-retry mode, the SS pin is held low until the retry time has expired. When the retry time ends, the MP5048 can re-enable the FET, then enter the soft start turn-on sequence.

TIMER Pin

The TIMER pin serves 4 functions:

1. Insertion delay
2. Turns on the short-circuit protection (SCP) timer
3. Over-current protection (OCP) timer
4. Sets the retry time

When the MP5048 passes internal power-on reset (POR), the insertion delay begins by charging the capacitor with a 2μA current source. When the voltage reaches the threshold, the TIMER pin is pulled up by the internal 4V source for 3.5μs (the actual pull-up voltage depends on the external timer capacitor), then resets quickly to GND for 7.5μs. The timer repeats this, and then the insertion delay time is completed (see Figure 9).

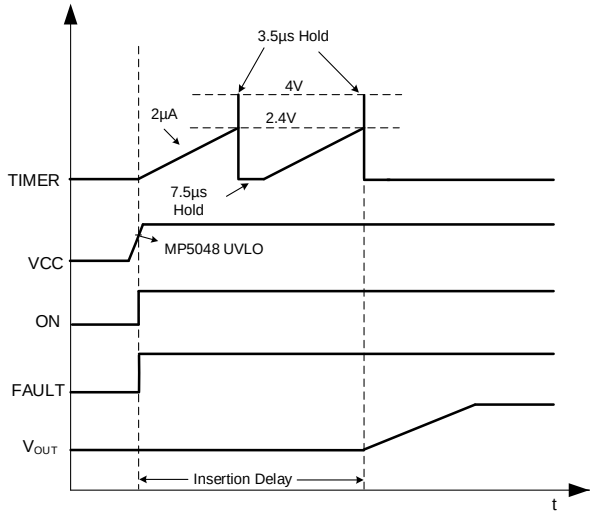


Figure 9: MP5048 Insertion Delay Time

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2021 MPS. All Rights Reserved.

If V_{OUT} drops below 20% of V_{IN} during start-up and the power FET current is regulated by the V_{CLREF} SS limit for the SCP timer, the power FET turns off and FAULT is pulled low (see Figure 10). If no fault occurs, the MP5048 follows the normal start-up sequence, and the voltage rises on the output of the device based on the SS rate.

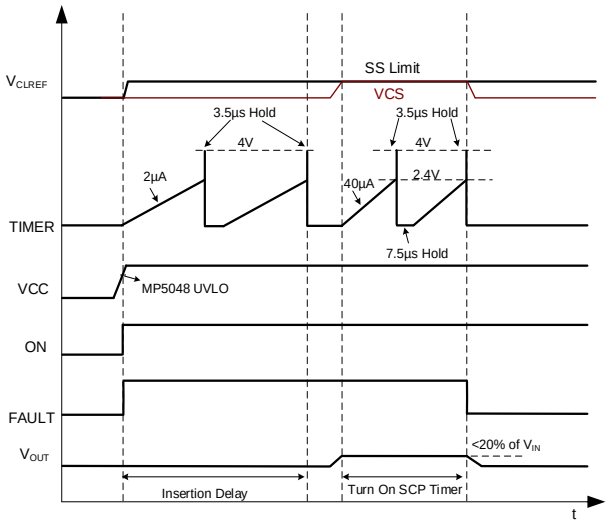


Figure 10: MP5048 Turn On SCP Time

An over-current condition occurs if the current through the MP5048 reaches the configured threshold and is held for the configured over-current protection (OCP) time.

When V_{CS} reaches the CLREF voltage (V_{CLREF_NORM}), a 40µA source charges the capacitor on the TIMER pin. As long as V_{CS} equals V_{CLREF}, the current charges up the capacitor. If the voltage on the TIMER pin reaches the trip threshold (0.6V), the power FET turns off and the FAULT pin is de-asserted to indicate OCP has occurred (see Figure 11).

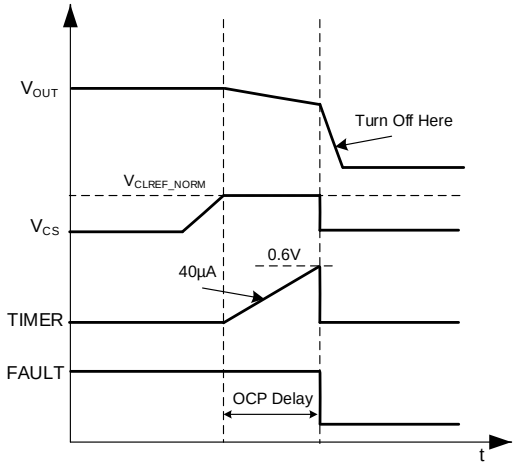


Figure 11: MP5048 OCP Time

The timer allows the OCP time to be adjusted so that the system can endure a current transient event without forcing a shutdown. A current transient can cause a current that exceeds the OCP threshold for a small amount of time; adjusting the timer can accommodate this brief OC condition.

If a fault occurs, the FAULT pin is pulled low to indicate a fault condition has occurred. If the MODE pin is set to auto-retry mode, the MP5048 charges and discharges the TIMER pin nine times using the same rates as the insertion delay. After the ninth cycle, the MP5048 automatically retries a start-up sequence (see Figure 12).

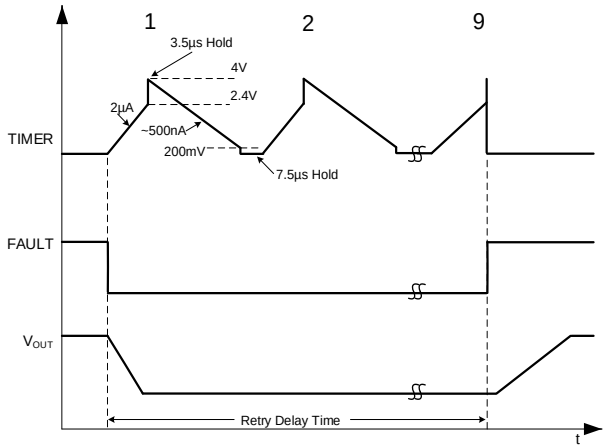


Figure 12: MP5048 Auto-Retry

Current Limit at Start-Up

The MP5048 load current is limited by the current limit reference input and the CS external resistor. The CS voltage (V_{CS}) is compared to the current limit reference through an amplifier to regulate the power FET gate voltage. This prevents the Intelli-Fuse current from exceeding the current limit defined by the reference.

The current limit reference voltage is set through CLREF, which is clamped low internally during soft start to control V_{OUT} and allow it to ramp up gradually. Once V_{OUT} is close to V_{IN}, the current limit reference can be raised to the full current limit set by the CLREF voltage. At this point, the power FET gate is fully enhanced, and the e-fuse is ready to deliver full power from the input.

To protect the MP5048 from overheating during start-up, the current limit internal maximum clamp voltage and CS limit reference configuration current change based on V_{IN} and V_{OUT} (see Figure 13).

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2021 MPS. All Rights Reserved.

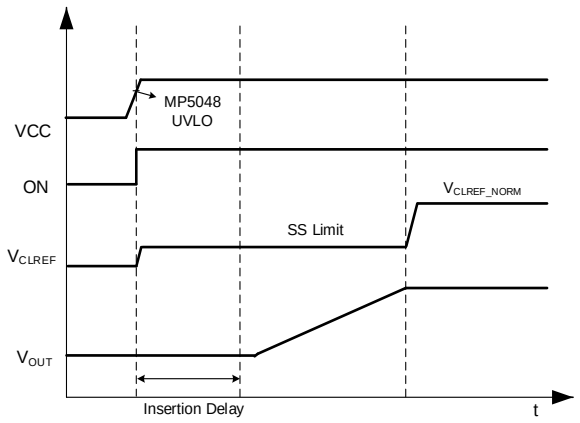


Figure 13: MP5048 SS Current Limit

If V_{OUT} drops below 90% of V_{IN}, the current limit reference is clamped to V_{BE} (660mV with a negative temperature coefficient), and the thermal shutdown threshold is 153°C.

If the CS limit reference configuration current is 8μA, then the external CLREF voltage depends on the CLREF external resistor. If the external CLREF voltage drops below the clamp voltage (V_{CLREF_CLAMP}), the actual current limit reference voltage is determined by the external CLREF voltage.

If V_{OUT} ≥ 90% of V_{IN}, the internal maximum current limit reference voltage is disabled. The CS limit reference configuration current ranges between 8μA and 26μA (8μA + 18μA), and CS is limited by the CLREF's externally configured value (typically limited to 2V).

If V_{CS} exceeds the SS limit during start-up, the power FET gate voltage is regulated to hold the FET current constant. If the power FET remains on while V_{OUT} remains below 90% of V_{IN} within the 200ms maximum soft-start time, the power FET shuts down when the 200ms time ends. If the value of the SS limit is higher, the power FET start-up instantaneous loss is large and a thermal shutdown is triggered before the 200ms time ends. In this case, FAULT is driven low (see Figure 14).

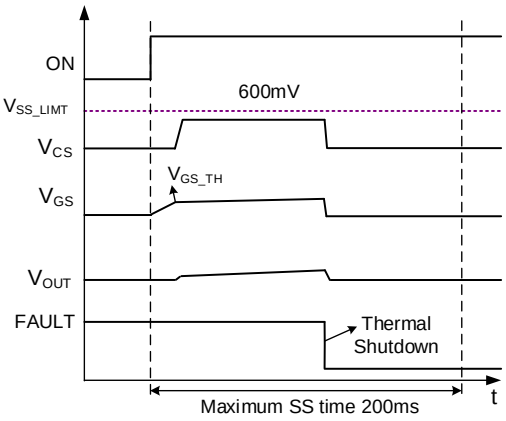


Figure 14: Failed Start-Up Within 200ms

If V_{OUT} drops below 20% of V_{IN} during start-up and the power FET current is regulated by V_{SS_LIMIT} for the start-up SCP timer, the power FET turns off with a fault latch condition, and FAULT is pulled low.

Current Limit During Normal Operation

When the MP5048 detects that start-up has finished, the part enters normal operation.

During normal operation, once V_{CS} (which is configured by an external resistor) exceeds the normal CLREF threshold, the internal circuit regulates the gate voltage to hold the power FET constant. To limit the current, the gate-to-source voltage must be regulated from 5V to about V_{TH}. The typical response time is about 14μs. The output current may have a small overshoot during this time period.

If the current limit is reached, the internal fault timer starts. If the output current falls below the current limit threshold before the end of the over-current protection (OCP) fault timeout period, the MP5048 resumes normal operation. If the current exceeds the fault timeout period, the power FET latches off and FAULT is pulled low.

The desired current limit during normal operation is a function of CS's external resistor (R_{CS}).

The MP5048 current limit value can exceed the normal maximum load current, allowing tolerances in the current-sense value. The current limit can be estimated with Equation (2):

$$I_{LIMIT} = \frac{V_{CLREF_NORM}}{G_{CS} \times R_{CS}} \quad (2)$$

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2021 MPS. All Rights Reserved.

Where V_{CLREF_NORM} is the CLREF voltage in normal operation, and G_{CS} is the current-sense gain when the power FET is fully on (typically 25μA/A).

The FET works in the linear region.

Short-Circuit Protection (SCP)

If the load current increases rapidly due to a short circuit condition, the current may exceed the current limit threshold before the hot-swap control loop can respond. If the Intelli-Fuse current reaches 26A, a fast turn-off circuit in the Intelli-Fuse is activated to turn off the power FET. The total short-circuit response time is about 200ns. The FAULT signal pulls low when the power FET current reaches the 26A current limit and asserts low.

If the device is in latch mode, there will be no retry response after short-circuit detection. The FAULT pin remains low and the device remains off. To clear the fault, the ON pin must be pulled low and then high. This clears the fault condition, and then the MP5048 initiates a new soft start. If the short circuit condition is still present, the device repeats this process. If the short circuit condition has been removed, the MP5048 ramps up V_{OUT} following the soft-start ramp.

If the device is in hiccup mode, the retry timer counts 9 cycles on the timer pin (see Figure 12 on page 17). At the end of the retry timer count, the MP5048 tries to turn on again. If the short condition persists, the process continues at the rate of the retry timer for the hiccup process. If the short has been removed, the MP5048 ramps the output voltage up at the SS ramp rate.

V_{IN} Fast Droop

In some conditions with a fast rising current due to an SCP/OCP condition, the input voltage (V_{IN}) supply may collapse due to parasitics and PSU capability.

If V_{IN} decreases rapidly, SCP is triggered. This may cause the SCP current level at which the device turns off to be lower than expected. If this event occurs, the device is re-enabled after an insertion delay. The delay occurs even if the device is set to latch-off mode. If the fault condition is removed on the subsequent start-up, the device turns on normally. If the fault condition has not been removed, the device regulates at the soft-start current limit or SCP condition, and latches off.

FAULT Report

FAULT is an open-drain, active-low signal to report fault conditions. FAULT monitors the following fault events in the Intelli-Fuse:

1. Over-current protection: If the CS voltage exceeds the CLREF threshold during normal operation, the FAULT signal is pulled low after a configured gate regulation time.
2. Short-circuit protection: If the Intelli-Fuse load current reaches 26A quickly, FAULT is pulled low immediately.
3. Intelli-Fuse power FET drain-source, gate-drain, or gate-source short detection: See the Damaged Intelli-Fuse MOSFET Detection section below for more details.
4. Over-temperature protection when the junction temperature >153°C: If an over-temperature protection fault is detected, FAULT is pulled down.

If a latch fault occurs, FAULT is pulled low. The latch can be released by cycling the power on VIN or ON.

Damaged Intelli-Fuse MOSFET Detection

Damaged Intelli-Fuse power FET detection includes FET drain-source short, gate-drain short, and gate-source short detection. These conditions are described in greater detail below.

Drain-Source Short Detection During Start-Up

Once V_{CC} on the Intelli-Fuse exceeds the under-voltage lockout (UVLO) rising threshold, the Intelli-Fuse starts to detect the drain-source short during start-up. In this instance, it treats any output voltage that exceeds 90% of V_{IN} during start-up as a short on the FET. The FAULT signal remains low when the Intelli-Fuse detects that V_{OUT} has exceeded 90% of V_{IN} during start up. Once the short is removed and the Intelli-Fuse detects that V_{OUT} is once again below 70% of V_{IN}, the FAULT signal is released to high again, and the MP5048 starts up normally.

Gate-Drain Short Detection During Start-Up

During power-up, the Intelli-Fuse detects a power FET gate-drain short by monitoring its drain-to-gate voltage (V_{DG}) and gate-to-source

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2021 MPS. All Rights Reserved.

voltage (V_{GS}). If V_{GS} exceeds a fault threshold voltage, or V_{DG} drops below the fault threshold, the FAULT signal remains low until the short is removed.

Gate-Source Short Detection During Start-Up

For gate-source short detection during the FET turn-on period (if V_{OUT} drops below 90% of V_{IN} after the internal maximum 200ms soft-start time), FAULT is pulled low. Remove the short and cycle the power on VIN or ON to turn on the fuse again.

Gate-Source or Gate-Drain Short Detection During Normal Operation

If V_{OUT} exceeds 90% of V_{IN} while the part operates normally, the Intelli-Fuse detects the power FET gate-source or gate-drain short by checking if V_{CP} - V_{GATE} (where V_{CP} is the internal charge pump voltage) is below 2V after 200ms (with no other fault occurring). If this occurs, FAULT is pulled low. Remove the short and cycle the power on VIN or ON to turn on the fuse again.

FAULT

Fault is an open-drain, active-low output that reports faults detected in the IC.

FAULT Reset

If a fault condition occurs, the MP5048 can be restarted by pulling the ON pin low, then high again. This clears the fault, and the MP5048 begins the power-on sequence.

V_{IN} Over-Voltage Protection (OVP)

V_{IN} over-voltage protection (OVP) has a fixed limit of 64V. If this level is reached, the power FET turns off. If the device is in latch mode, the fault can be released by cycling the power on VIN or ON. If the device is set for hiccup mode, the power FET will not turn on until the input voltage falls below 60V.

Under-Voltage Lockout (UVLO)

The under-voltage lockout (UVLO) threshold can be configured using a resistor divider from the input to the ON pin. The network can be adjusted by setting the voltage at which the MP5048 is able to turn on via VIN.

Current-Sense Output (CS)

CS provides a current proportional to the output current (the current through the power device). The current-sense gain is 25μA/A when the power FET is fully on. There is a resistor (R_{CS}) connected to CS to form an external voltage. The CS pin current (I_{CS}) can be estimated with Equation (3):

$$I_{CS} = I_{OUT} \times 25\mu A/A \quad (3)$$

Calculate the reference voltage with Equation Equation (4):

$$V_{CS} = I_{CS} \times R_{CS} \quad (4)$$

If V_{CS} reaches the CLREF current limit threshold, the internal circuit regulates the gate voltage to hold the current in the power FET constant.

Current Monitor Output (IMON)

The current monitor gain is 25μA/A. There is a resistor (R_{IMON}) connected from IMON to ground. The IMON voltage should be between 0V and 2.5V to keep IMON's output current linearly proportional to the output current. The current can be calculated with Equation (5):

$$I_{MON} = I_{OUT} \times 25\mu A/A \quad (5)$$

Estimate the reference voltage with Equation (6):

$$V_{IMON} = I_{MON} \times R_{IMON} \quad (6)$$

The MP5048 current monitor output can be used by the controller to accurately monitor the output current. Place a 100nF capacitor from IMON to GND to smooth the indicator voltage.

Temperature-Sense Output (VTEMP)

VTEMP reports the junction temperature when there is no thermal gradient on the IC. VTEMP has a voltage output proportional to the junction temperature when V_{CC} exceeds its under-voltage lockout (UVLO) threshold and the MP5048 is in active mode. The VTEMP output voltage is 10mV/°C, and can be calculated with Equation (7):

$$V_{TEMP} = (T_{JUNCTION} \times 12.1 - 200)\ mV \quad (7)$$

For example, if the junction temperature is 100°C, the VTEMP voltage is about 1V. If VTEMP is 0V, the junction temperature is about 0°C. The total temperature-sense range is between 0°C and 150°C. If the junction temperature drops below 0°C, the VTEMP voltage remains at 0V.

In multi-fuse operation, the VTEMP pins of each Intelli-Fuse can be connected to the temperature monitor pin of the controller (see Figure 15).

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2021 MPS. All Rights Reserved.

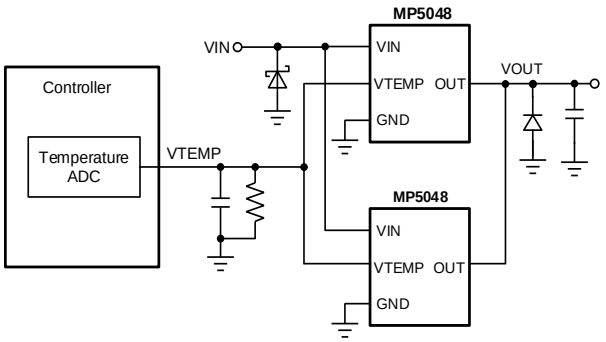


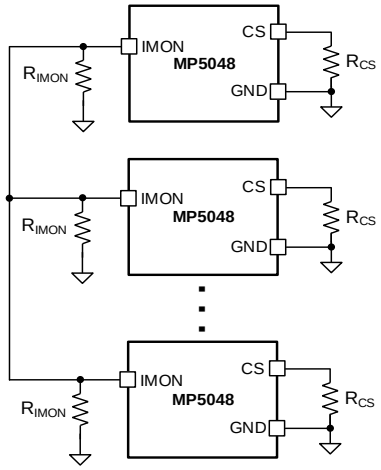
Figure 15: Multi-Fuse Temperature-Sense Utilization during Parallel Operation

Current Balance for Parallel Operation

Multiple MP5048 devices can be used in parallel for high-current applications. The current balance loop in the MP5048 balances the start-up current per active channel. All IMON pins must be connected together.

The sensed currents from each active MP5048 IMON are summed together and divided by the number of active channels. The resulting average load current provides a measure of the total load current.

The MP5048 current balance is achieved by comparing the sensed current of CS pin in each MP5048 to the average current, to make an appropriate adjustment to the power FET gate voltage of each Intelli-Fuse during start-up. The equivalent average IMON resistor can be calculated by R_{CS} / N, where N is the number of active MP5048 devices (see Figure 16).



$$R_{IMON} = R_{CS}$$

$$R_{IMON_AVG} = \frac{R_{CS}}{N}$$

Figure 16: Multi-MP5048 IMON and CS Connections in Parallel Application

The start-up current balance is essential in achieving the thermal advantage of parallel operation. With good current balance, the power loss is dissipated equally over multiple devices and a greater area.

MP5920 Controller and MP5048

The MP5048 can be combined with the MP5920 to provide PMBus telemetry, power sequencing, and black box capabilities (see Figure 17).

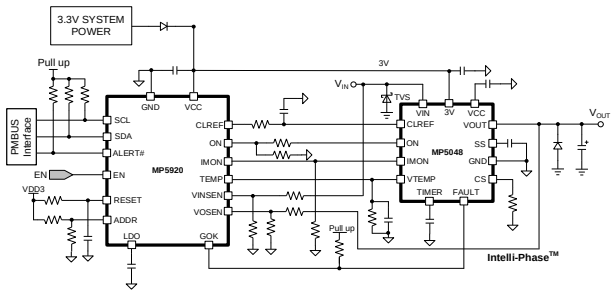


Figure 17: MP5048 and MP5920 Operation

Using the internal 3V LDO, the MP5920 can be powered directly by the MP5048, which allows for power sequencing when only 48V is available. The 3V LDO can be used as a bootstrap source to power on the MP5920, but it cannot be used for continuous operation. It is expected that a 3.3V source will power the MP5920 device after initial start-up. The 3V LDO can be connected to the main system 3.3V supply through a diode. This disables current drawing from the internal 3V LDO, and uses the system's 3.3V to power the MP5920.

Maximum Output Current

Figure 18 shows the case temperature rise vs. the output current at different air conditions.

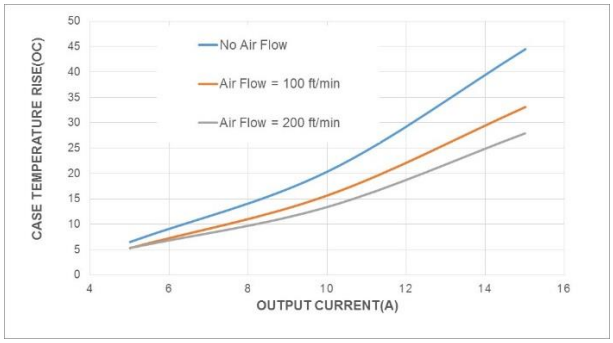


Figure 18: MP5048 Output Current vs. Temperature Rise

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2021 MPS. All Rights Reserved.

APPLICATION INFORMATION

PCB Layout Guidelines

Efficient PCB layout is critical for optimal performance. A 4-layer layout is strongly recommended to achieve better thermal performance. For the best results, refer to Figure 19 and follow the guidelines below:

1. Place the MP5048 close to the board's input connector to minimize trace inductance.
2. Place a small capacitor (C_{IN}, 100nF) close to the MP5048's VIN and GND pins to minimize transients, which may occur on the input supply line. Transients of several volts can occur easily when the load current is shut off.
3. Place a 2.2µF capacitor as close to VCC as possible.
4. Keep the high-current path from the board's input to load close to the return path, and in parallel, to minimize loop inductance.
5. An analog signal ground (AGND) plane is used in the MP5048. Connect AGND to the PCB power ground planes at a single point.
6. If the MP5048 is paired with a hot-swap controller, connect the reference ground of all signal pins to the reference ground of the controller.

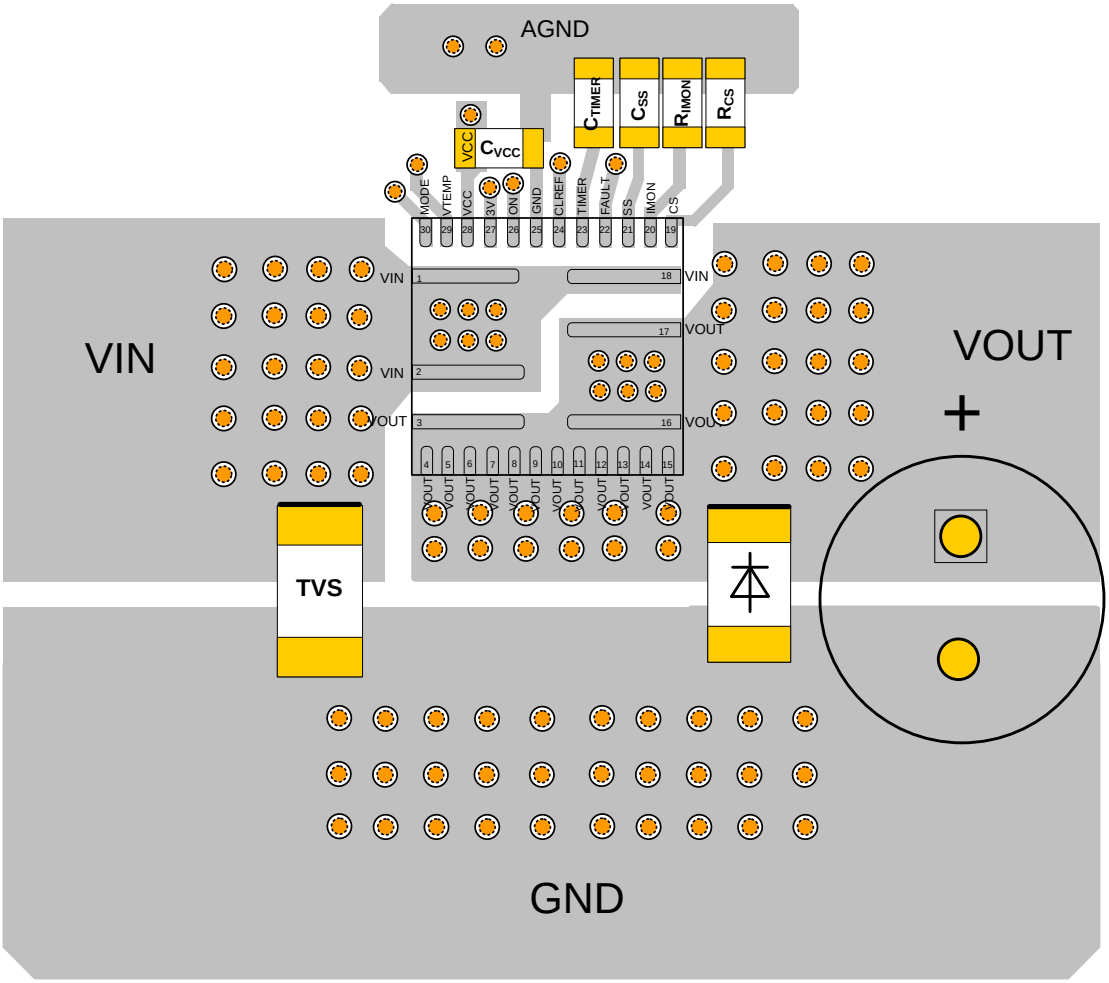


Figure 19: Recommended PCB Layout (Placement and Top-Layer PCB)

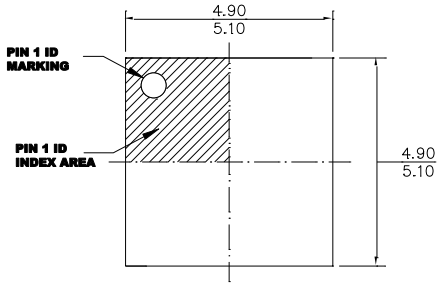
VIN TVS: 5.0SMDJ51A

VOUT DIODE: B380-13-F

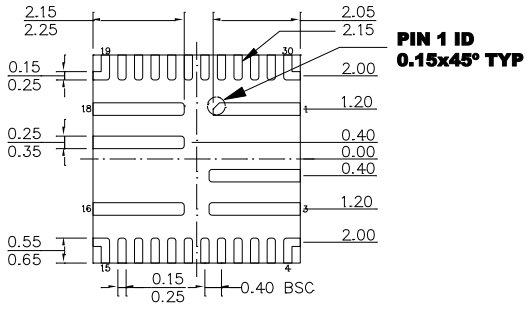
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2021 MPS. All Rights Reserved.

PACKAGE INFORMATION

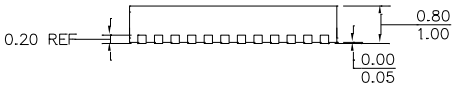
QFN-30 (5mmx5mm)



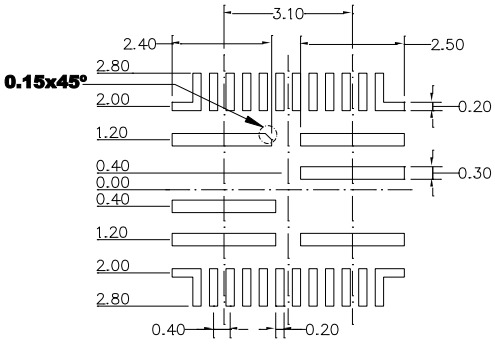
TOP VIEW



BOTTOM VIEW



SIDE VIEW



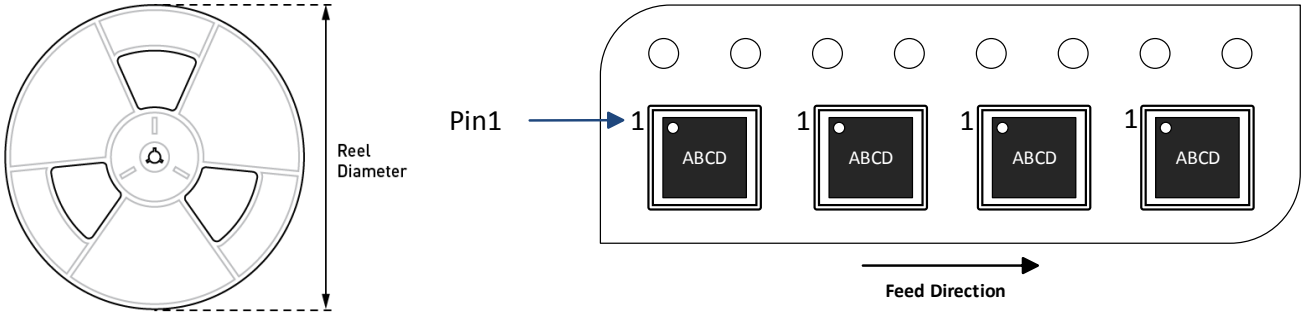
RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
3) REFERENCEIS MO-220.
4) DRAWING IS NOT TO SCALE.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2021 MPS. All Rights Reserved.

CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP5048GU-Z	QFN-30 (5mmx5mm)	5000	N/A	N/A	13in	12mm	8mm

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2021 MPS. All Rights Reserved.

Revision History

Revision #	Revision Date	Description	Pages Updated
1.0	7/15/2020	Initial Release	-
1.1	4/30/2021	1. Change VIN/VOUT AMV from +62V to +65V; 2. Update the soft start OTP description.	P5/P17

Notice: The information in this document is subject to change without notice. Please contact MPS for current specifications. Users should warrant and guarantee that third-party Intellectual Property rights are not infringed upon when integrating MPS products into any application. MPS will not assume any legal responsibility for any said applications.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2021 MPS. All Rights Reserved.