MP6527

40V, 0.8A, 10-Channel, Half-Bridge Motor Driver with Serial Input Control

DESCRIPTION

The MP6527 is a ten-channel, half-bridge DMOS output driver with integrated power MOSFETs. It can achieve up to 0.8A of output current (I_{OUT}) across a wide 5.5V to 40V input voltage (V_{IN}) range from.

The device's ten half-bridges can be controlled separately via a standard serial data interface, and each channel has various diagnostic functions. The MP6527 has very low quiescent current (I_Q) in standby mode.

Full protection features include short-circuit protection (SCP), over-temperature protection (OTP), under-voltage lockout (UVLO) protection, over-voltage lockout (OVLO) protection, and thermal shutdown with pre-warning.

The MP6527 requires a minimal number of readily available, standard external components, and is available in a TSSOP-28EP package.

FEATURES

- Wide 5.5V to 40V Operating Input Voltage (V_{IN}) Range
- High-Side MOSFETs (HS-FETs) and Low-Side MOSFETs (LS-FETs) Connected in Half-Bridge Configurations
- Up to 0.8A Output Current (I_{OUT})
- Typical 1.3Ω HS-FET and LS-FET $R_{DS(ON)}$
- Low Quiescent Current (I_Q) in Standby Mode
- Short-Circuit Protection (SCP)
- Over-Temperature Protection (OTP)
- Under-Voltage Lockout (UVLO) and Over-Voltage Lockout (OVLO) Protection
- Serial Data Interface
- Diagnostic Functions:
  - Shorted Output
  - Open-Load Detection
  - Over-Temperature (OT)
  - Over-Voltage (OV)
  - Under-Voltage (UV)
- Up to 5MHz Serial Interface Clock Frequency
- Compliance with 3.3V and 5V Systems
- Available in a TSSOP-28EP Package

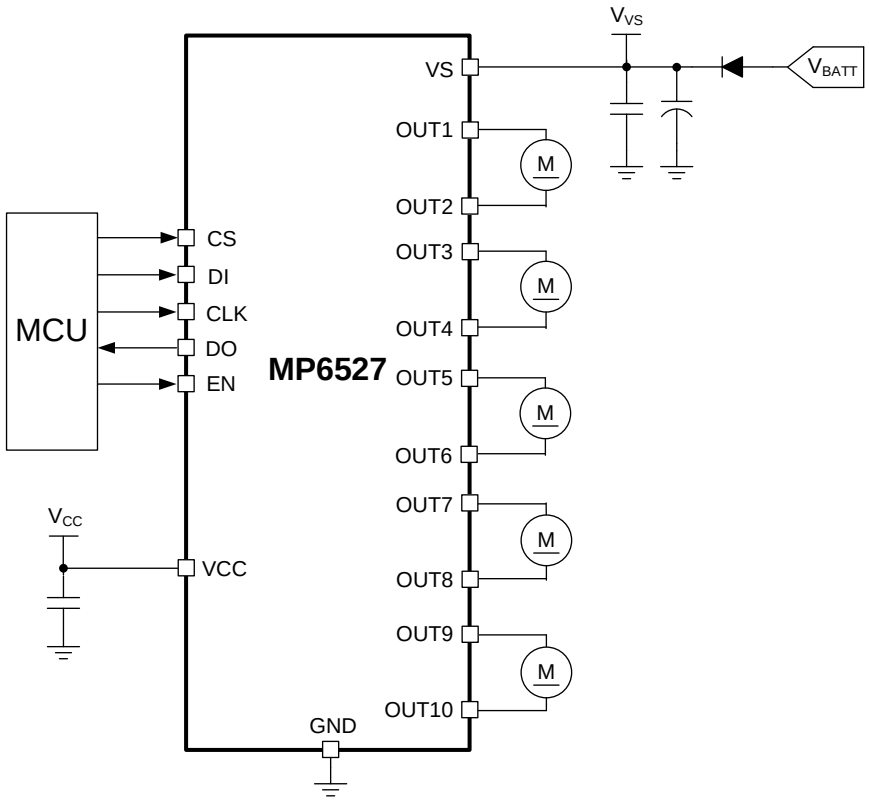
APPLICATIONS

- Automotive and Industrial Applications
- DC Motors

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TYPICAL APPLICATION



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ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MP6527GF	TSSOP-28EP	*See Below*	2A

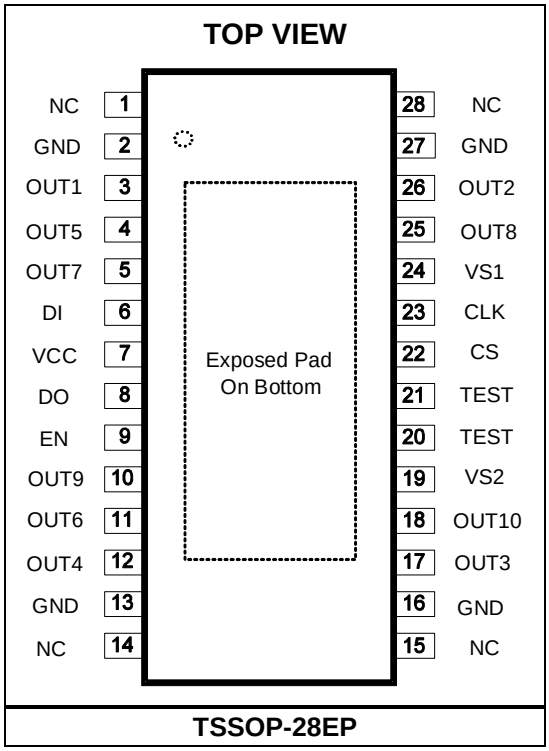
* For Tape & Reel, add suffix -Z (e.g. MP6527GF-Z).

TOP MARKING

MPSYYWW
MP6527
LLLLLLLLL

MPS: MPS prefix
YY: Year code
WW: Week code
MP6527: Part number
LLLLLLLLL: Lot number

PACKAGE REFERENCE



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PIN FUNCTIONS

Pin #	Name	Description
1, 14, 15, 28	NC	**No connection.**
2, 13, 16, 27	GND	**Ground.**
3	OUT1	**Half-bridge output 1.**
4	OUT5	**Half-bridge output 5.**
5	OUT7	**Half-bridge output 7.**
6	DI	**Serial data input.**
7	VCC	**Logic supply voltage.**
8	DO	**Serial data output.**
9	EN	**Enable (EN).** Pull the EN pin low for standby mode; pull EN high for normal operation.
10	OUT9	**Half-bridge output 9.**
11	OUT6	**Half-bridge output 6.**
12	OUT4	**Half-bridge output 4.**
17	OUT3	**Half-bridge output 3.**
18	OUT10	**Half-bridge output 10.**
19	VS2	**Power supply for drivers 3, 4, 6, 9 and 10.** This pin must be connected to VS1 externally.
20, 21	TEST	**Internal test pin.** Connect the TEST pin to GND.
22	CS	**Chip select input, active low.**
23	CLK	**Serial clock input.**
24	VS1	**Power supply for drivers 1, 2, 5, 7, and 8; the internal LDO; and the charge pump.** This pin must be connected to VS2 externally.
25	OUT8	**Half-bridge output 8.**
26	OUT2	**Half-bridge output 2.**

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ABSOLUTE MAXIMUM RATINGS (1)

Supply voltage (V_{VS}) 45V
V_{OUTx} .....-0.3V to V_{IN} +0.3V
Logic supply voltage (V_{VCC})..... -0.3V to +6V
Logic input voltage..... -0.3 to V_{VCC} + 0.3V
Logic output voltage..... -0.3 to V_{VCC} + 0.3V
All other pins..... -0.3V to +6.5V
Continuous power dissipation (T_A = +25°C) (2)
TSSOP-28EP 3.9W
Junction temperature .....150°C
Lead temperature .....260°C
Storage temperature.....-65°C to +150°C

ESD Ratings (3)

Human body model (OUTx and VS pins).....4kV
Human body model (all other pins) 2kV
Machine mode (MM).....200V
Charge device model (CDM).....750V

Recommended Operating Conditions (4)

Supply voltage (V_{VS}) ..... 5.5V to 40V
Logic supply voltage V_{VCC} ..... 3.15V to 5.25V
Operating junction temp (T_J) .... -40°C to +125°C

Thermal Resistance (5) θ_{JA} θ_{JC}

TSSOP-28EP…… 32 …... 6…°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can cause excessive die temperature, and the regulator may go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) Devices are ESD-sensitive. It is recommended to use extra caution when handling.
4) The device is not guaranteed to function outside of its operating conditions.
5) Measured on JESD51-7, 4-layer PCB.

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ELECTRICAL CHARACTERISTICS

5.5V ≤ V_{VS} ≤ 40V, 3.15V ≤ V_{VCC} ≤ 5.25V, EN = V_{VCC}, T_A = 25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
VS supply current	I_{VS}	V_{VS} < 28V, EN = V_{CC}, no load		5.5	6.5	mA
VCC supply current	I_{VCC}	3.15V < V_{VCC} < 5.25V, EN = high, DI = CLK = low, CS = high, no load		100	150	µA
VS quiescent current	I_{Q_VS}	V_{VS} = 13.2V, V_{VCC} = 0V or V_{VCC} = 5V, EN = low		1	5	µA
VCC quiescent current	I_{Q_VCC}	3.15V < V_{VCC} < 5.25V, EN = low, DI = CLK = low, CS = high		1	5	µA
VS discharge current	$I_{VS_DISCHARGE}$	V_{VS} = 40V, EN = low			3	mA
Start-up reset threshold	V_{VCC}	VCC increasing	2.3	2.7	3	V
Start-up reset delay		After switching on V_{VCC}	30	100	160	µs
VS under-voltage lockout (UVLO) threshold	V_{UVLO_VS}	VS decreasing	3.5		4.5	V
VS UVLO threshold hysteresis	V_{UVOFF}		0.1	0.3	0.5	V
VS UVLO delay time			7		21	ms
VS over-voltage lockout (OVLO) threshold	V_{OVLO_VS}	OVLO = 1, VS increasing	33	36	39	V
VS OVLO threshold hysteresis			1	2.5	4	V
Output Specifications						
HS-FET and LS-FET on resistance	$R_{DS(ON)}$			1.3	1.6	Ω
Over-current (OC) limit	I_{OCP}	V_{VS} = 13.2V	1	1.3	2.5	A
OC shutdown delay time	t_{dOC}		10	25	50	µs
Open-load detection (OLD) current	I_{OLD}	V_{VS} = 13.2V, LS-FET is on	1	16	45	mA
OLD delay time	t_{DELAY_OLD}		200	350	600	µs
Output enable time		V_{VS} = 13.2V, R_{LOAD} = 50Ω		50	65	µs
Output disable time				50	65	
Delay time		HBCNFx high to OUTx high, V_{VS} = 13.2V, R_{LOAD} = 50Ω		75	105	
		HBCNFx low to OUTx low, V_{VS} = 13.2V, R_{LOAD} = 50Ω		65	95	
Output rise time		V_{VS} = 13.2V, 10% to 90% V_{OUT}, R_{LOAD} = 50Ω	13	27	42	µs
Output fall time			11	20	27	µs
Dead time		V_{VS} = 13V, R_{LOAD} = 50Ω	1.5			µs
Enable (EN) Input						
EN low threshold					0.6	V
EN high threshold			2			V
EN threshold hysteresis				0.4		V
Pull-down resistor		V_{EN} = V_{VCC}		125		kΩ
Serial Interface: Logic Inputs (DI, CLK, CS)						
Input low-level threshold					0.6	V
Input high-level threshold			2			V
Input threshold hysteresis				150		mV
DI pull-down resistor, CLK pin		V_{DI}, V_{CLK} = V_{VCC}		125		kΩ
CS pull-up current		V_{CS} = 0V		125		kΩ
Input capacitance (6)	C_{IN}				15	pF

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ELECTRICAL CHARACTERISTICS *(continued)*

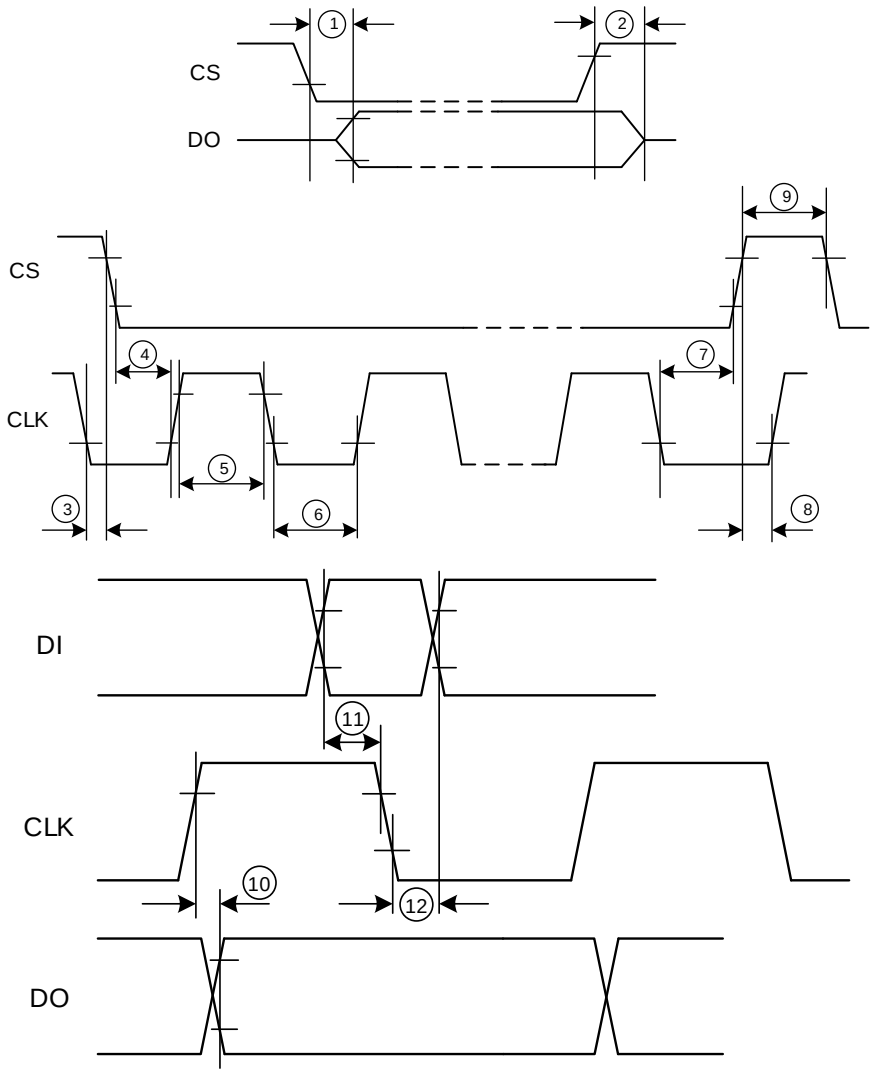
5.5V ≤ V_{VS} ≤ 40V, 3.15V ≤ V_{VCC} ≤ 5.25V, T_A = 25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Serial Interface: Logic Output (DO)						
Output low level					0.4	V
Output high level			V_{VCC} - 0.6			V
Leakage current (tri-state)		0V < V_{DO} < V_{VCC}, V_{CS} = V_{VCC}	-5		+5	µA
Thermal Shutdown and Pre-Warning (6)						
Thermal pre-warning threshold	T_{JW}		120	140	170	°C
Thermal pre-warning hysteresis				20		°C
Thermal shutdown threshold	T_{JSD}		150	175	200	°C
Thermal shutdown hysteresis				20		°C
Ratio for thermal shutdown and thermal pre-warning			1.05	1.2		
CLK frequency	f_{CLK}				5	MHz
CLK period time	t_{PCLK}	V_{CC} = 5V	200			ns
		V_{CC} = 3.3V	500			
CLK high time	t_5		85			ns
CLK low time	t_6		85			ns
CLK set-up time (high to low)	t_7		85			ns
CLK set-up time (low to high)	t_3		85			ns
DI set-up time	t_{11}		50			ns
DI hold time	t_{12}		50			ns
CS set-up time (low to high)	t_8		100			ns
CS set-up time (high to low)	t_4		100			ns
CS high time	t_9		5			µs
DO enable after CS falling edge	t_1	C_{DO} = 40pF			200	ns
DO disable after CS rising edge	t_2	C_{DO} = 40pF			200	ns
DO fall/rise time		C_{DO} = 40pF		10	25	ns
DO valid time	t_{10}	C_{DO} = 40pF		20	50	ns
EN low valid time		V_{CC} = 5V, EN high to low, 50% to OUTx turning off 50%		50		µs
EN high to serial peripheral interface (SPI) valid					100	µs
Time between two consecutive SRR commands			100			ms

Note:

6) Not subject to production testing. Guaranteed by design.

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Inputs DI, CLK, CS: High Level = 0.7 x V_{CC}, Low Level = 0.3 x V_{CC}
Output DO: High Level = 0.8 x V_{CC}, Low Level = 0.2 x V_{CC}

Figure 1: Serial Interface Timing Diagram

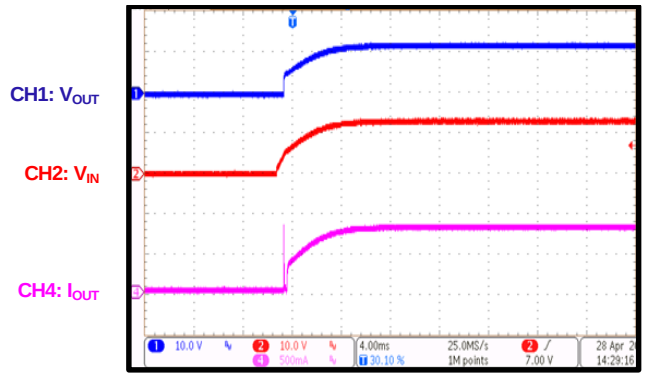
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TYPICAL PERFORMANCE CHARACTERISTICS

V_{VS} = 13V, V_{VCC} = 3.3V, T_A = 25°C, unless otherwise noted.

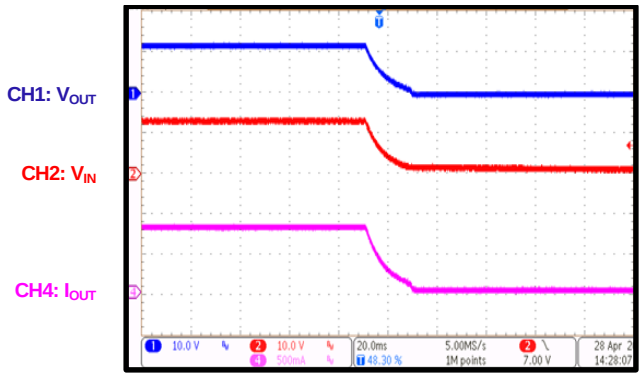
Start-Up through VIN

HS-FET on, I_{OUT} = 800mA



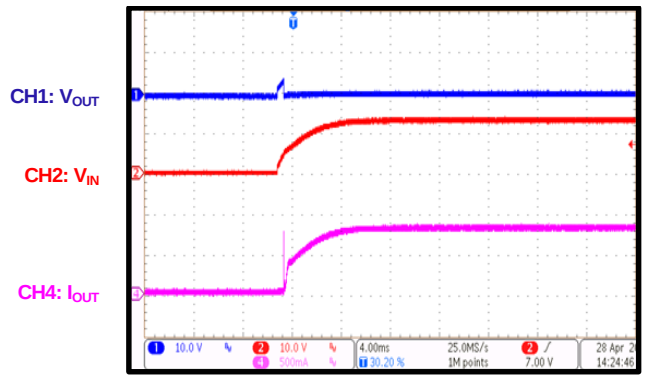
Shutdown through VIN

HS-FET on, I_{OUT} = 800mA



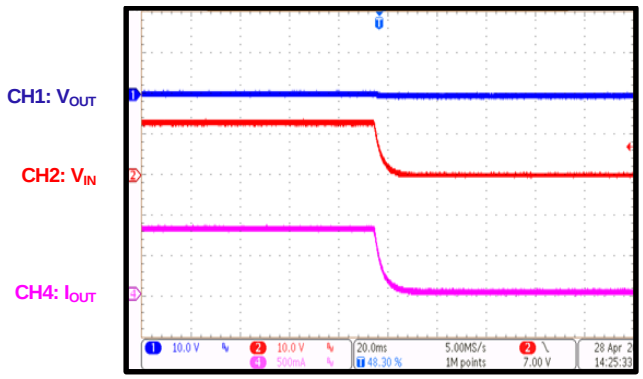
Start-Up through VIN

LS-FET on, I_{OUT} = 800mA



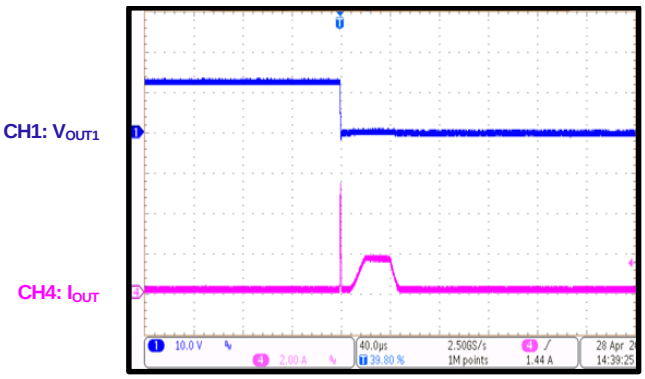
Shutdown through VIN

LS-FET on, I_{OUT} = 800mA



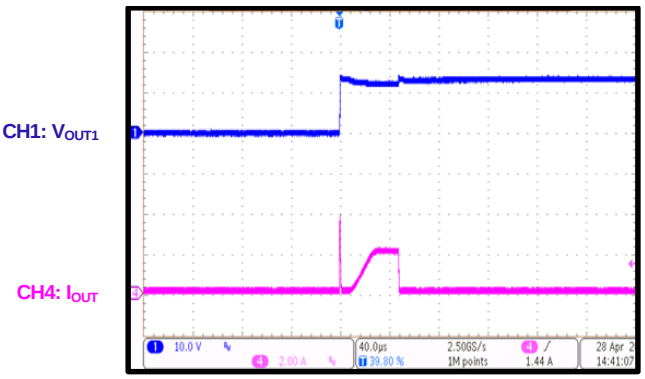
Over-Current Protection

OUT short to GND



Over-Current Protection

OUT short to VIN



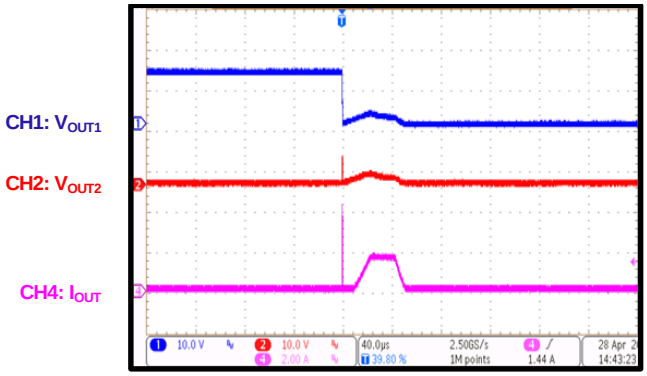
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TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{VS} = 13V, V_{VCC} = 3.3V, T_A = 25°C, unless otherwise noted.

OCP

OUT short to OUT



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FUNCTIONAL BLOCK DIAGRAM

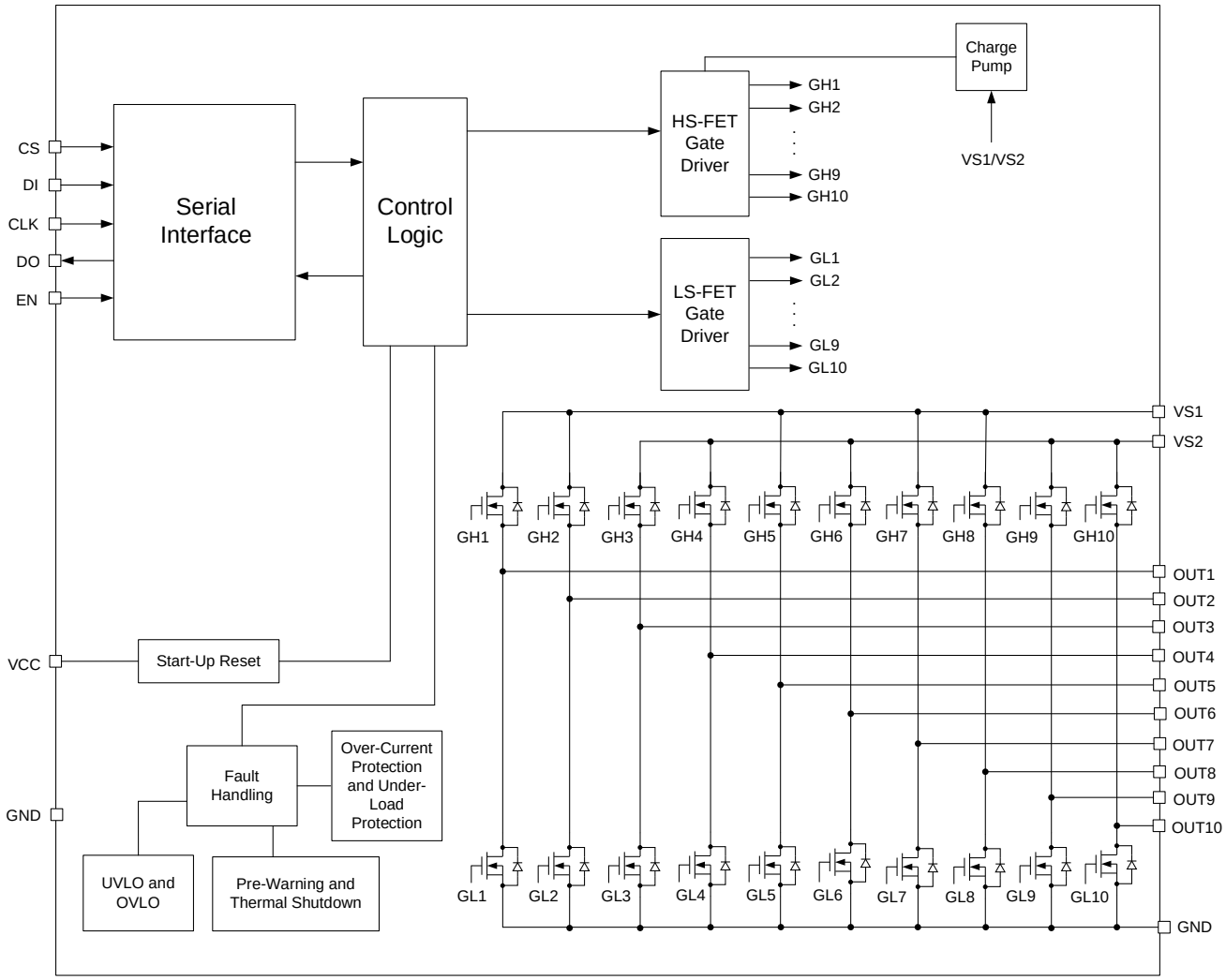


Figure 2: Functional Block Diagram

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OPERATION

The MP6527 is a 10-channel, half-bridge double-DMOS output driver with integrated power MOSFETs. The IC's 10 half-bridges can be controlled separately via a standard serial data interface, and have various diagnostic functions.

Serial Interface

Data transfer starts with the falling edge signal of the CS pin. Execution of new input data is enabled on the rising edge of the CS signal. Data must appear at the DI pin synchronized to the CLK pin, and is accepted on the falling edge of the CLK signal. For DI, the MSB (SRR, bit[15]) must be transferred first. The last 16 bits clocked into DI are transferred to the device's data register if there is no frame error. Otherwise, all DI data is ignored and the previous input data is preserved.

The output data at the DO pin is enabled on the falling edge of CS. In addition to the 16-bit status data, a pseudo-bit (PRE_15) can also be retrieved from the DO output. The latched thermal shutdown (TSD) status bit (PRE_15) is available on DO until the first rising CLK edge after CS goes low. The output data changes their state with the CLK rising edge, and remains stable until the next CLK rising edge appears. When CS is high, DO is in a tri-state condition.

The following conditions must be met for a valid TSD read to be captured:

1. CLK and DI are low before the CS cycle begins.
2. CS transitions from high to low.
3. The CS set-up time is satisfied.

Figure 3 shows the SPI communication. Table 1 and Table 2 show the input control registers. Table 3 and Table 4 show the output diagnostic registers.

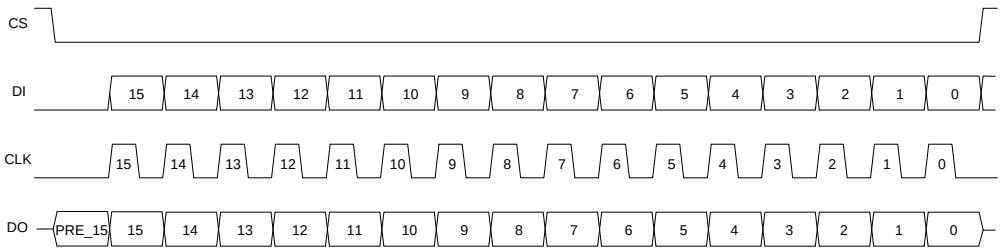


Figure 3: Data Transfer

Table 1: Input Control Registers (Channels 1 to 6, Input Bit[14] = 0)

Channels 1 to 6 (Input Bit[14] = 0)		
Bit	**Input Register**	**Function**
15	SRR	Status register reset. 1: Reset, the error bits of the corresponding status register in the output data register are set to low 0: Not reset, SRR is invalid
14	CH_SEL	This bit selects the channel group. 1: Half-bridge, bits[10:7] 0: Half-bridge, bits [6:1]
13	OLSD_EN	This bit enables open-load detection shutdown (OLD_SD) for half-bridge 1 (HB1) to half-bridge 6 (HB6). This feature allows the affected output stage to switch off if a true open-load or under-load condition is detected. 1: Enabled 0: Disabled
12	HBEN6	Enables half-bridge 6. 1: Half-bridge 6 is active 0: Half-bridge 6 is in Hi-Z

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11	HBEN5	Enables half-bridge 5. 1: Half-bridge 5 is active 0: Half-bridge 5 is in Hi-Z
10	HBEN4	Enables half-bridge 4. 1: Half-bridge 4 is active 0: Half-bridge 4 is in Hi-Z
9	HBEN3	Enables half-bridge 3. 1: Half-bridge 3 is active 0: Half-bridge 3 is in Hi-Z
8	HBEN2	Enables half-bridge 2. 1: Half-bridge 2 is active 0: Half-bridge 2 is in Hi-Z
7	HBEN1	Enables half-bridge 1. 1: Half-bridge 1 is active 0: Half-bridge 1 is in Hi-Z
6	HBCNF6	Configures half-bridge 6. 1: The high-side (HS) half-bridge is on and the low-side (LS) half-bridge is off 0: The HS half-bridge is off and the LS half-bridge is on
5	HBCNF5	Configures half-bridge 5. 1: The HS half-bridge is on and the LS half-bridge is off 0: The HS half-bridge is off and the LS half-bridge is on
4	HBCNF4	Configures half-bridge 4. 1: The HS half-bridge is on and the LS half-bridge is off 0: The HS half-bridge is off and the LS half-bridge is on
3	HBCNF3	Configures half-bridge 3. 1: The HS half-bridge is on and the LS half-bridge is off 0: The HS half-bridge is off and the LS half-bridge is on
2	HBCNF2	Configures half-bridge 2. 1: The HS half-bridge is on and the LS half-bridge is off 0: The HS half-bridge is off and the LS half-bridge is on
1	HBCNF1	Configures half-bridge 1. 1: The HS half-bridge is on and the LS half-bridge is off 0: The HS half-bridge is off and the LS half-bridge is on
0	OVLO	Enables VSx over-voltage lockout (OVLO). 1: Enabled 0: Disabled

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Table 2: Input Control Registers (Channels 7 to 10, Input Bit[14] = 1)

Channels 7 to 10 (Input Bit[14] = 1)		
Bit	**Input Register**	**Function**
15	SRR	Status register reset. 1: Reset, the error bits of the corresponding status register in the output data register are set to low 0: Not reset, SRR is invalid
14	CH_SEL	This bit selects the channel group. 1: Half-bridge, bits[10:7] 0: Half-bridge, bits[6:1]
13	OLSD_EN	This bit enables open-load detection shutdown (OLD_SD) for half-bridge 7 (HB7) to half-bridge 10 (HB10). This feature allows the affected output stage to switch off if a true open-load or under-load condition is detected. 1: Enabled 0: Disabled
12	RESERVED	Not used.
11	RESERVED	Not used.
10	HBEN10	Enables half-bridge 10. 1: Half-bridge 10 is active 0: Half-bridge 10 is in Hi-Z
9	HBEN9	Enables half-bridge 9. 1: Half-bridge 9 is active 0: Half-bridge 9 is in Hi-Z
8	HBEN8	Enables half-bridge 8. 1: Half-bridge 8 is active 0: Half-bridge 8 is in Hi-Z
7	HBEN7	Enables half-bridge 7. 1: Half-bridge 7 is active 0: Half-bridge 7 is in Hi-Z
6	RESERVED	Not used.
5	RESERVED	Not used.
4	HBCNF10	Configures half-bridge 10. 1: The HS half-bridge is on and the LS half-bridge is off 0: The HS half-bridge is off and the LS half-bridge is on
3	HBCNF9	Configures half-bridge 9. 1: The HS half-bridge is on and the LS half-bridge is off 0: The HS half-bridge is off and the LS half-bridge is on
2	HBCNF8	Configures half-bridge 8. 1: The HS half-bridge is on and the LS half-bridge is off 0: The HS half-bridge is off and the LS half-bridge is on

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1	HBCNF7	Configures half-bridge 7. 1: The HS half-bridge is on and the LS half-bridge is off 0: The HS half-bridge is off and the LS half-bridge is on
0	OVLO	Enables VSx OVLO. 1: Enabled 0: Disabled

Note:

7) All input bits are set to 0 after V_{CC} power-on reset.

Table 3: Output Diagnostic Registers (Channels 1 to 6, Input Bit[14] = 0)

Channels 1 to 6 (Input Bit[14] = 0)		
Bit	**Input Register**	**Function**
PRE_15	TSD	Latched thermal shutdown (TSD). This bit is latched, and the corresponding output is switched off. This bit can only be reset via status register reset (SRR) or a power-on reset. 1: Fault 0: No fault
15	OC (HB [6:1])	Latched over-current (OC) shutdown. This bit is set and latched if a half-bridge from HB1 to HB6 has an overload or short-circuit. The corresponding output is also switched off. This bit can only be reset via SRR or a power-on reset. 1: Fault 0: No fault
14	PSF	Power supply failure. This bit is set and latched if a VS1, VS2, or VS1 and VS2 over-voltage (OV) or under-voltage (UV) conditions occurs. All outputs are switched off. This bit resets automatically if VSx returns to its normal operating range. 1: Fault 0: No fault
13	OLD (HB [6:1])	Open-load error. This bit is set and latched if a half-bridge from HB1 to HB6 experiences an open-load or under-load error condition. The corresponding output is also switched off if input bit[13] (OLD_SD) is high. This bit can only be reset via SRR or a power-on reset. 1: Fault 0: No fault
12	SHBEN6	Returns half-bridge 6's output status. 1: HB6 is active 0: HB6 is in Hi-Z
11	SHBEN5	Returns half-bridge 5's output status. 1: HB5 is active 0: HB5 is in Hi-Z
10	SHBEN4	Returns half-bridge 4's output status. 1: HB4 is active 0: HB4 is in Hi-Z

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9	SHBEN3	Returns half-bridge 3's output status. 1: HB3 is active 0: HB3 is in Hi-Z
8	SHBEN2	Returns half-bridge 2's output status. 1: HB2 is active 0: HB2 is in Hi-Z
7	SHBEN1	Returns half-bridge 1's output status. 1: HB1 is active 0: HB1 is in Hi-Z
6	HBCNF6	Returns half-bridge 6's configuration status. 1: The HS half-bridge is on and the LS half-bridge is off 0: The HS half-bridge is off and the LS half-bridge is on
5	HBCNF5	Returns half-bridge 5's configuration status. 1: The HS half-bridge is on and the LS half-bridge is off 0: The HS half-bridge is off and the LS half-bridge is on
4	HBCNF4	Returns half-bridge 4's configuration status. 1: The HS half-bridge is on and the LS half-bridge is off 0: The HS half-bridge is off and the LS half-bridge is on
3	HBCNF3	Returns half-bridge 3's configuration status. 1: The HS half-bridge is on and the LS half-bridge is off 0: The HS half-bridge is off and the LS half-bridge is on
2	HBCNF2	Returns half-bridge 2's configuration status. 1: The HS half-bridge is on and the LS half-bridge is off 0: The HS half-bridge is off and the LS half-bridge is on
1	HBCNF1	Returns half-bridge 1's configuration status. 1: The HS half-bridge is on and the LS half-bridge is off 0: The HS half-bridge is off and the LS half-bridge is on
0	TW	Thermal warning. This bit is treated as a pre-warning to TSD, and goes high if the junction temperature reaches TJW. The output remains on until one or more sensors reach TSD. This bit automatically resets if the junction temperature drops below the thermal warning recovery point. 1: Fault 0: No fault

Table 4: Output Diagnostic Registers (Channels 7 to 10, Input Bit[14] = 1)

Channels 7 to 10 (Input Bit[14] = 1)		
Bit	**Input Register**	**Function**
PRE_15	TSD	Latched thermal shutdown (TSD). This bit is set and latched, and the corresponding output is switched off. This bit can only be reset via SRR or a power-on reset. 1: Fault 0: No fault

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15	OC (HB [10:7])	Latched over-current (OC) shutdown. This bit is set and latched if a half-bridge from HB7 to HB10 experiences an overload or short-circuit. The corresponding output is also switched off. This bit can only be reset via SRR or a power-on reset. 1: Fault 0: No fault
14	PSF	Power supply failure. This bit is set if a VS1, VS2, or VS1 and a VS2 OV or UV condition occurs. All outputs are switched off. This bit resets automatically if VSx returns to within its normal operating range. 1: Fault 0: No fault
13	OLD (HB [10:7])	Open-load error. This bit is set and latched if a half-bridge from HB7 to HB10 experiences an open-load or under-load error condition. The corresponding output is also switched off if input bit[13] (OLD_SD) is high. This bit can only be reset via SRR or a power-on reset. 1: Fault 0: No fault
12	RESERVED	Not used.
11	RESERVED	Not used.
10	SHBEN10	Returns half-bridge 10's output status. 1: Half-bridge 10 is active 0: Half-bridge 10 is in Hi-Z
9	SHBEN9	Returns half-bridge 9's output status. 1: Half-bridge 9 is active 0: Half-bridge 9 is in Hi-Z
8	SHBEN8	Returns half-bridge 8's output status. 1: Half-bridge 8 is active 0: Half-bridge 8 is in Hi-Z
7	SHBEN7	Returns half-bridge 7's output status. 1: Half-bridge 7 is active 0: Half-bridge 7 is in Hi-Z
6	RESERVED	Not used.
5	RESERVED	Not used.
4	HBCNF10	Returns half-bridge 10's configuration status. 1: The HS half-bridge is on and the LS half-bridge is off 0: The HS half-bridge is off and the LS half-bridge is on
3	HBCNF9	Returns half-bridge 9's configuration status. 1: The HS half-bridge is on and the LS half-bridge is off 0: The HS half-bridge is off and the LS half-bridge is on

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2	HBCNF8	Returns half-bridge 8's configuration status. 1: The HS half-bridge is on and the LS half-bridge is off 0: The HS half-bridge is off and the LS half-bridge is on
1	HBCNF7	Returns half-bridge 7's configuration status. 1: The HS half-bridge is on and the LS half-bridge is off 0: The HS half-bridge is off and the LS half-bridge is on
0	TW	Thermal warning. This bit is treated as a pre-warning to TSD, and goes high if the junction temperature reaches TJW. The output remains on until one or more sensors reach TSD. This bit automatically resets if the junction temperature drops below the thermal warning recovery point. 1: Fault 0: No fault

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Enable Control

The MP6527 enters low-power mode (or sleep mode) when the EN pin is set to low. The EN input has an internal pull-down resistor. In sleep mode, all output stages are turned off and the SPI register banks are reset. The output stages can be activated again by setting EN to high.

Status Register Reset (SRR)

The status register reset (SRR) command bit is executed after the SPI transmission determines whether a fault has been cleared.

Sending 1 to SSR clears the status memory and reactivates faulted outputs for channels (as selected by CH_SEL).

If a fault remains present after SRR, the corresponding protection can be re-engaged and shutdown can recur. The device can also be reset by toggling the EN pin or by a VCC power-on reset.

Open-Load Detection (OLD)

When the device is on, open-load detection (OLD) is implemented in the low-side MOSFET (LS-FET) switches of the bridge outputs. If the current through the low-side (LS) transistor is below the reference current (I_{OLD}) for longer than the OLD delay time (t_{DOLD}), then the corresponding open-load diagnosis bit is set. If an under-load condition occurs in another channel after the global timer has started, the delay for any subsequent under-load condition becomes the remainder of the timer. The timer runs continuously with a persistent under-load condition.

If the OLSD_EN bit is set and an open load is detected on the LS-FET, the respective output is disabled and the open-load error bit is latched. Otherwise, the output remains on and the open-load error bit is set. The bit remains latched and the output remains off until an SRR or power-on reset is performed. The channel group select (CH_SEL) input bit determines which channels are affected by SRR and which half-bridges are latched off via the OLSD_EN command bit. This has the added advantage of independently diagnosing and isolating error flags to the corresponding failed output.

Figure 4 shows an H-bridge open-load example, where a motor is connected between OUT1 and OUT2 with a broken wire.

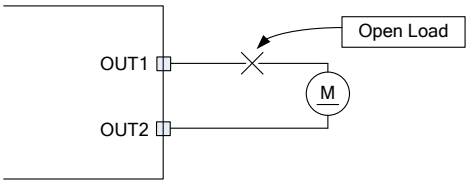


Figure 4: H-Bridge Open Load Example

Table 5 shows an example of the resulting diagnostic information.

Table 5: Open-Load Diagnostic Example

Control				Diagnostic Information	
				Motor Connected	Motor Disconnected
LS1	HS1	LS2	HS2	OLD (output bit[13])	
0	0	0	0	0	0
1	0	0	1	0	1
0	1	1	0	0	1
0	1	0	1	0	0
1	0	1	0	1	1

In motor applications, it is often desirable to actively brake the motor by turning on both HS drivers or LS drivers in two half-bridge channels. If two LS drivers are used (an LS brake), an under-load condition occurs as the motor current decays normally. It is recommended to use an HS brake instead to avoid the under-load condition.

Discharge Circuit

Many typical applications use an inverse-polarity protection diode. Figure 5 shows the functional principle of a discharger circuit, with an inverse-polarity protection diode (D1).

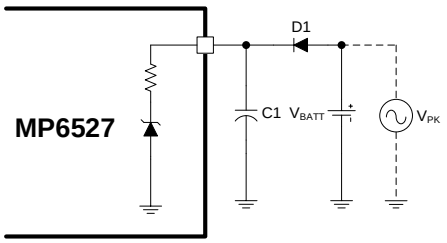


Figure 5: Functional Principle of a Discharger Circuit

However, this method poses certain risks. During inhibit mode, the IC consumes an extremely low discharge current (I_{VS}), typically

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20µA max. Any peaks on the supply voltage gradually charge the blocking capacitor. D1 prevents the capacitor from discharging via the power supply. Due to the extremely small quiescent current (I_Q), discharging via the IC is negligible. During long periods of time in inhibit mode, the IC's supply voltage could increase continuously until the maximum supply voltage limit (40V) is exceeded, which can damage the IC. To avoid this, the MP6527 features a discharge circuit. If the VS pin voltage (V_{VS}) exceeds the 37V threshold, the blocking capacitor is discharged via an integrated resistor until V_{VS} falls below the threshold.

Table 6 shows the diagnostic classes and functions of the different faults.

Table 6: Diagnostic Classes and Functions of Different Faults

Fault	Qualifier	State and Recovery	
		OUTx	Output Register
TSD	-	Hi-Z, need SRR to reset	TSD: 1, need SRR to reset
OC shutdown	-		OC: 1, need SRR to reset
OLD	OLSD_EN: 1		OLD: 1, need SRR to reset
	OLSD_EN: 0	Unaffected	
OVLO	OVLO: 1	Hi-Z, Unlatched (8)	PSF: 1, unlatched (9)
	OVLO: 0	Unaffected	
UVLO	-	Hi-Z, Unlatched (8)	
Thermal warning	-	Unaffected	TW: 1, unlatched (9)

Notes:

8) OUTx returns to its previous state or new state once the fault is removed. If DI changes, then DO changes accordingly.
9) The corresponding output register returns to its no-fault state once the fault is removed.

Over-Current Protection (OCP)

The MP6527 has internal overload protection (OLP) and short-circuit protection (SCP). The currents in both the HS-FET and LS-FET are measured. If the current through the HS-FET or LS-FET exceeds the current limit, an internal timer starts. When a permanent over-current shutdown delay time (t_{OC}) is reached, the short-circuit detection bit (OC) is set and the shorted output is disabled. By writing 1 to the SRR bit in the input register, the OC bit resets and the disabled outputs are enabled. The channel group select (CH_SEL) input bit determines which channels are affected by SRR.

Thermal Shutdown (TSD) and Pre-Warning

The MP6572 has integrated thermal monitoring for each half-bridge via the driver pair's thermal sensor. If the junction temperature (T_J) exceeds the thermal pre-warning threshold, then the temperature pre-warning bit (TW) in the output register is set. When the temperature falls below the thermal pre-warning threshold, TW is reset.

If T_J exceeds the thermal shutdown (TSD) threshold, then the channel's HS-FETs and LS-FETs are latched off, TW remains set, and the TSD bit (PRE_15) is set. Once T_J falls below the TSD threshold and a high has been written to the SRR bit in the input register, then TSD is cleared and all the affected channels in a group resume normal operation. The channel group select (CH_SEL) input bit determines which channels are affected by SRR.

Thermal pre-warning and the TSD threshold have hysteresis of 20°C.

VS Under-Voltage Lockout (UVLO)

If V_{VS} falls below the under-voltage lockout (UVLO) threshold, an internal timer starts. When a permanent UVLO delay time is reached, the power supply fail bit (PSF) in the output register is set and all outputs are disabled. Once V_{VS} exceeds the UVLO threshold and the PSF bit is cleared, the MP6527 resumes normal operation.

VCC UVLO

The SPI interface does not function if V_{CC} is below the UVLO threshold. In this circumstance, all outputs turn off and clear the command input and status output registers.

Once V_{CC} exceeds the UVLO threshold, the UVLO resets and SRR is functional again.

VS Over-Voltage Lockout (OVLO)

If V_{VS} exceeds the switch-off voltage (V_{OVOFF}), all outputs are switched off by the set over-voltage lockout (OVLO) input bit (OVLO = 1, CH_SEL = X) and the PSF error bit. The error is not latched, meaning if V_{VS} drops below the switch-on threshold voltage, the power stages restart and the error flags are reset.

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APPLICATION INFORMATION

PCB Layout Guidelines

Efficient PCB layout is critical for stable operation. For the best results, refer to Figure 6 and follow the guidelines below:

1. Place a bulk capacitor on the VIN pin to absorb the energy flowing from the motor or power supply. The capacitor should be sized according to the application requirements.
2. Place a supply bypass capacitor as close to the IC as possible. It is recommended to use a X5R or X7R dielectric capacitor.
3. Place as much copper on the long pads as possible.
4. Place multiple thermal vias inside the pad area to move heat to the copper layers. If the vias cannot be placed inside the pad area, place the vias just outside the pad area.

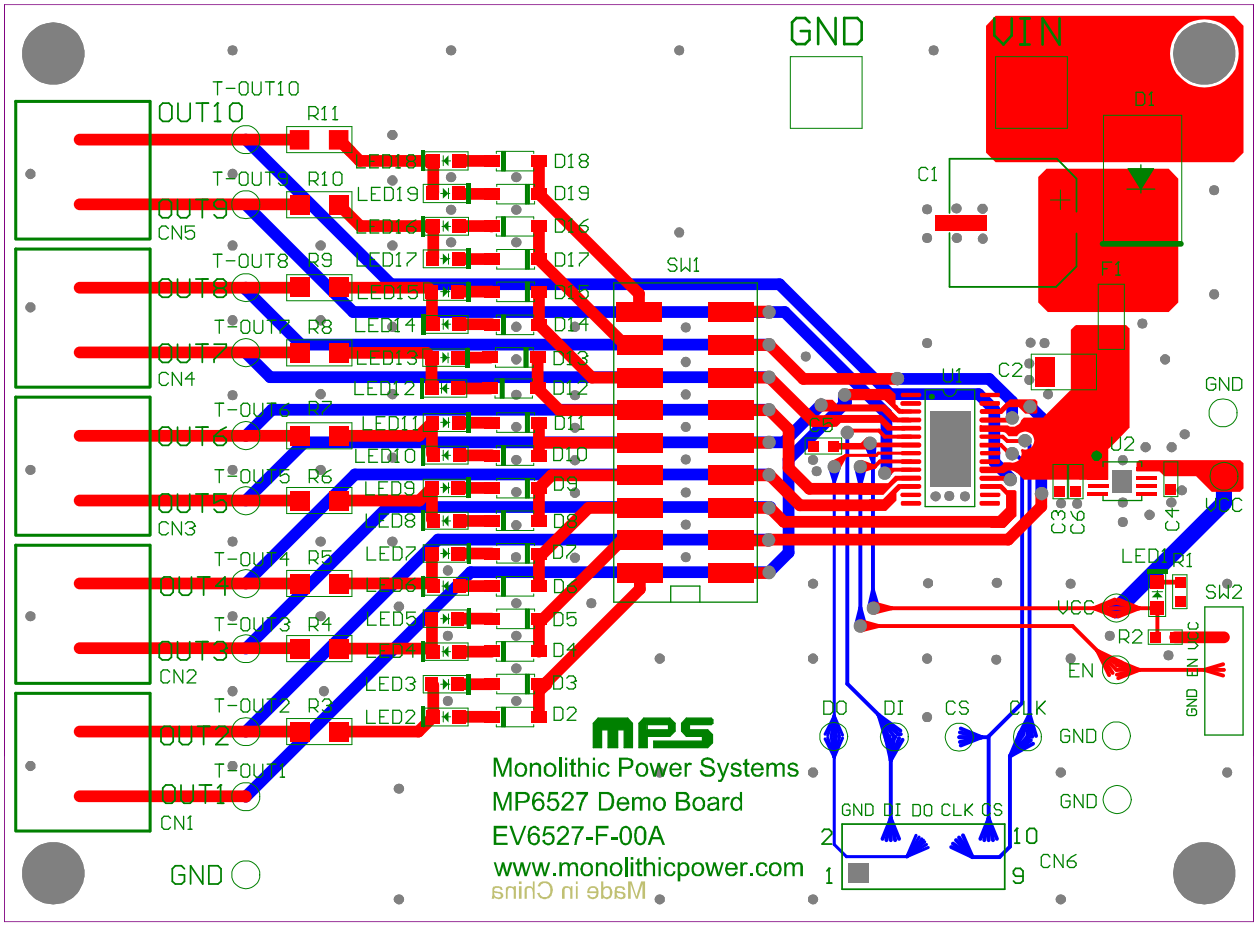
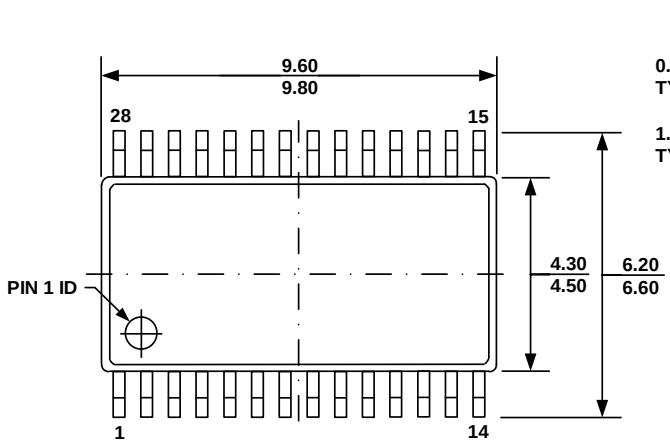


Figure 6: Recommended PCB Layout

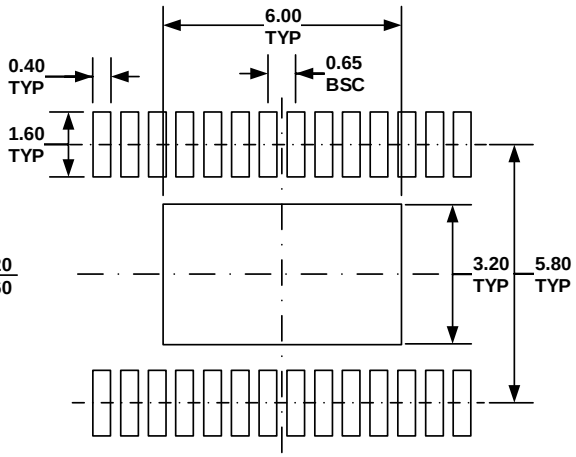
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PACKAGE INFORMATION

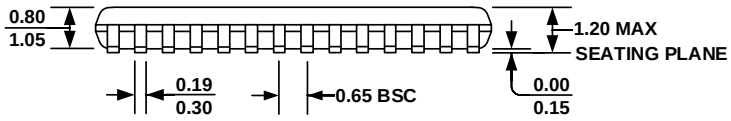
TSSOP-28EP



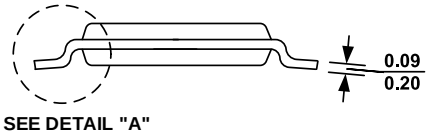
TOP VIEW



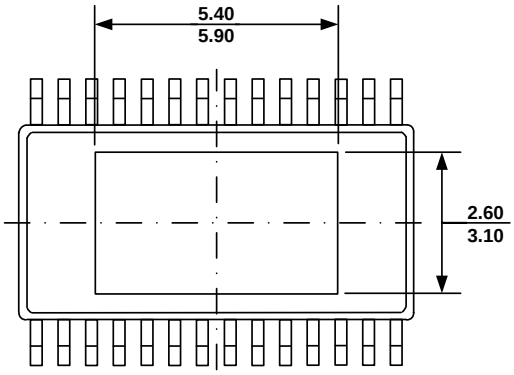
RECOMMENDED LAND PATTERN



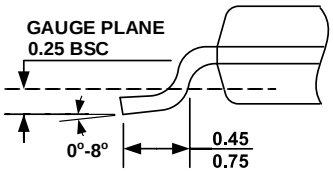
FRONT VIEW



SIDE VIEW



BOTTOM VIEW



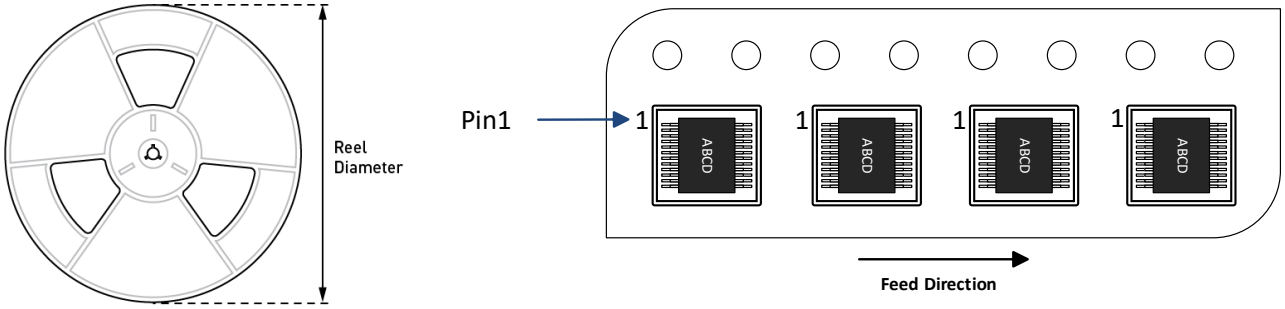
DETAIL "A"

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION, OR GATE BURR.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.1 MILLIMETERS MAX.
5) DRAWING CONFORMS TO JEDEC MO-153, VARIATION AET.
6) DRAWING IS NOT TO SCALE.

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CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP6527GF–Z	TSSOP-28EP	2500	50	13in	16mm	8mm

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REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	9/23/2021	Initial Release	-

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