MP7720

20W Class D Mono Single Ended Audio Amplifer

The Future of Analog IC Technology

DESCRIPTION

The MP7720 is a mono 20W Class D Audio Amplifier. It is one of MPS' second generation of fully integrated audio amplifiers which dramatically reduces solution size by integrating the following:

180mΩ power MOSFETs

Startup / Shutdown pop elimination

Short circuit protection circuits

Mute / Standby

The MP7720 utilizes a single ended output structure capable of delivering 20W into 4Ω speakers. MPS Class D Audio Amplifiers exhibit the high fidelity of a Class A/B amplifier at efficiencies greater than 90%. The circuit is based on the MPS' proprietary variable frequency topology that delivers excellent PSRR, fast response time and operates on a single power supply.

EVALUATION BOARD REFERENCE

Board Number	Dimensions
EV0030	2.4"X x 3.5"Y x 1.2"Z

FEATURES

- 20W Output at V_{DD} = 24V into a 4Ω load
- THD+N = 0.04% at 1W, 8Ω
- 93% Efficiency at 20W
- Low Noise (190μV Typical)
- Switching Frequency Up to 1MHz
- 9.5V to 24V Operation from a Single Supply
- Integrated Startup and Shutdown Pop Elimination Circuit
- Thermal Protection
- Integrated 180mΩ Switches
- Mute/Standby Modes (Sleep)
- Available in Tiny 8-Pin SOIC and PDIP Packages

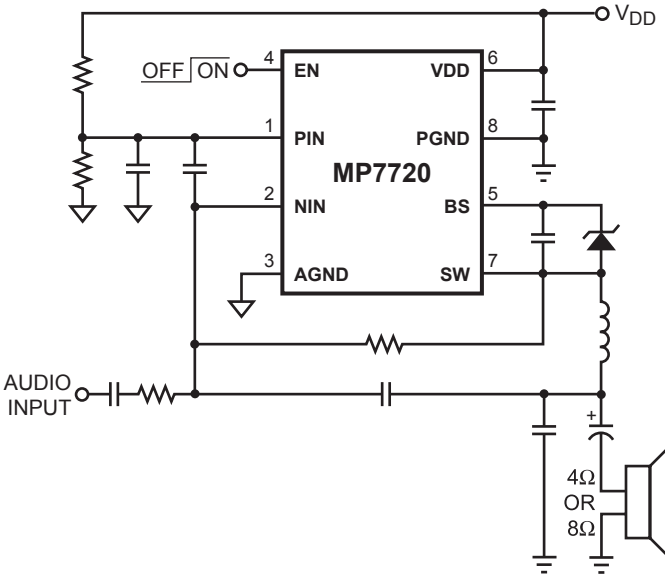
APPLICATIONS

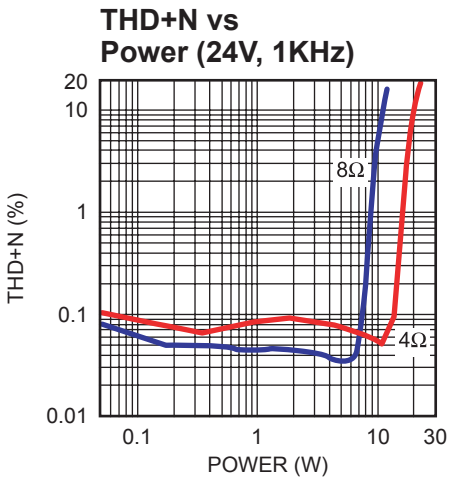
- Surround Sound DVD Systems
- Televisions
- Flat Panel Monitors
- Multimedia Computers
- Home Stereo Systems

"MPS" and "The Future of Analog IC Technology" are Registered Trademarks of Monolithic Power Systems, Inc.

AAM (Analog Adaptive Modulation) is a Trademark of Monolithic Power Systems, Inc.

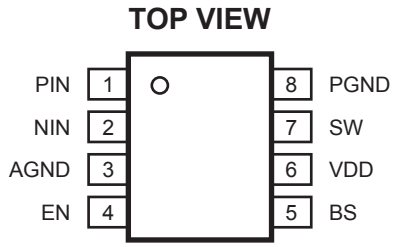
TYPICAL APPLICATION





MPS Proprietary Information. Unauthorized Photocopy and Duplication Prohibited.
© 2010 MPS. All Rights Reserved.

PACKAGE REFERENCE



Part Number*	Package	Temperature
MP7720DS	SOIC8	–40°C to +85°C
MP7720DP	PDIP8	–40°C to +85°C

* For Tape & Reel, add suffix –Z (eg. MP7720DS–Z)
For Lead Free, add suffix –LF (eg. MP7720DS–LF–Z)

ABSOLUTE MAXIMUM RATINGS (1)

Supply Voltage V_{DD} 26V
BS Voltage..... V_{SW} – 0.3V to V_{SW} + 6.5V
Enable Voltage V_{EN} ..... –0.3V to +6V
V_{SW}, V_{PIN}, V_{NIN} ..... –1V to V_{DD} + 1V
AGND to PGND ..... –0.3V to +0.3V
Junction Temperature..... 150°C
Lead Temperature ..... 260°C
Storage Temperature ..... –65°C to +150°C

Recommended Operating Conditions (2)

Supply Voltage V_{DD} ..... 9.5V to 24V
Operating Temperature T_A ..... –40°C to +85°C

Thermal Resistance (3)

	θ_{JA}	θ_{JC}	
SOIC8	105	40	°C/W
PDIP8	95	55	°C/W

Notes:
1) Exceeding these ratings may damage the device.
2) The device is not guaranteed to function outside of its operating conditions.
3) Measured on approximately 1" square of 1 oz copper.

ELECTRICAL CHARACTERISTICS

V_{DD} = 24V, V_{EN} = 5V, T_A = +25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Supply Current						
Standby Current		V_{EN} = 0V		1	5	µA
Quiescent Current				1.5	3.0	mA
Output Drivers						
SW On Resistance		Sourcing and Sinking		0.18		Ω
Short Circuit Current		Sourcing and Sinking		5.0		A
Inputs						
PIN, NIN Input Common Mode Voltage Range			0	$\frac{V_{DD}}{2}$	V_{DD} – 1.5	V
PIN, NIN Input Current		V_{PIN} = V_{NIN} = 12V		1	5	µA
EN Enable Threshold Voltage		V_{EN} Rising		1.4	2.0	V
		V_{EN} Falling	0.4	1.2		V
EN Enable Input Current		V_{EN} = 5V		1		µA
Thermal Shutdown						
Thermal Shutdown Trip Point		T_J Rising		150		°C
Thermal Shutdown Hysteresis				30		°C

MPS Proprietary Information. Unauthorized Photocopy and Duplication Prohibited.
© 2010 MPS. All Rights Reserved.

OPERATING SPECIFICATIONS

Circuit of Figure 1, V_{DD} = 24V, V_{EN} = 5V, T_A = +25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Standby Current		V_{EN} = 0V		130		μA
Quiescent Current				13		mA
Power Output		f = 1KHz, THD+N = 10%, 4Ω Load		20		W
		f = 1KHz, THD+N = 10%, 8Ω Load		10		W
THD+ Noise		P_{OUT} = 1W, f = 1KHz, 4Ω Load		0.08		%
		P_{OUT} = 1W, f = 1KHz, 8Ω Load		0.04		%
Efficiency		f = 1KHz, P_{OUT} = 1W, 4Ω Load		90		%
		f = 1KHz, P_{OUT} = 1W, 8Ω Load		95		%
Maximum Power Bandwidth				20		KHz
Dynamic Range				93		dB
Noise Floor		A-Weighted		190		μV
Power Supply Rejection		f = 1KHz		60		dB

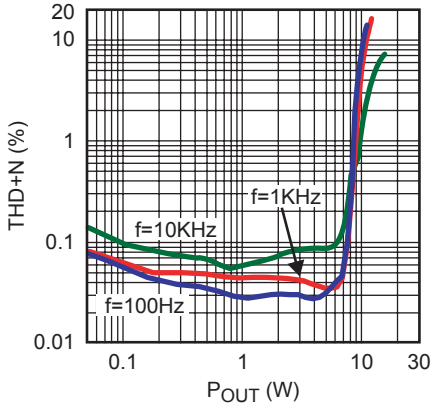
PIN FUNCTIONS

Pin #	Name	Description
1	PIN	Amplifier Positive Input. PIN is the positive side of the differential input to the amplifier. Use a resistive voltage divider to set the voltage at PIN to V_{DD}/2. See Figure 1.
2	NIN	Amplifier Negative Input. NIN is the negative side of the differential input to the amplifier. Drive the input signal and close the feedback loop at NIN. See Figure 1.
3	AGND	Analog Ground. Connect AGND to PGND at a single point.
4	EN	Enable Input. Drive EN high to turn on the amplifier, low to turn it off.
5	BS	High-Side MOSFET Bootstrap Input. A capacitor from BS to SW supplies the gate drive current to the internal high-side MOSFET. Connect a 0.1μF capacitor from SW to BS. Place a 6.2V zener diode from BS to SW to prevent overstressing of the internal circuitry.
6	VDD	Power Supply Input. VDD is the drain of the high-side MOSFET switch, and supplies the power to the output stage and the MP7720 internal control circuitry. In addition to the main bulk capacitor, bypass VDD to PGND with a 1μF X7R capacitor placed close to pins 6 and 8.
7	SW	Switched Power Output. SW is the output of the MP7720. Connect the LC filter between SW and the output coupling capacitor. See Figure 1.
8	PGND	Power Ground. Connect PGND to AGND at a single point.

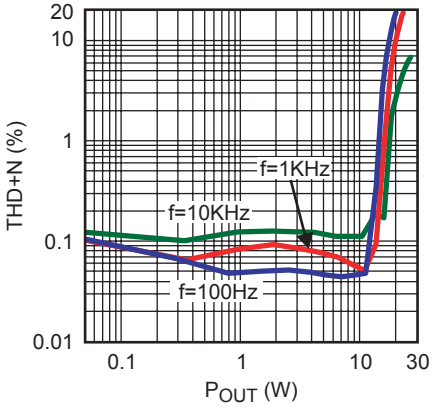
MPS Proprietary Information. Unauthorized Photocopy and Duplication Prohibited.
© 2010 MPS. All Rights Reserved.

TYPICAL PERFORMANCE CHARACTERISTICS

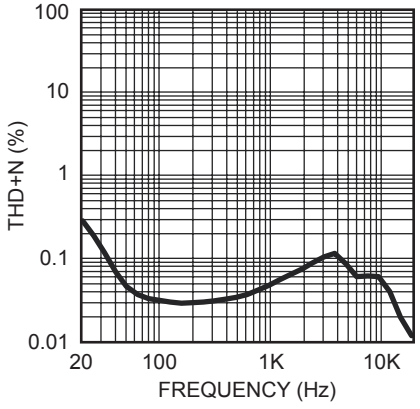
THD+N vs P_{OUT} (24V, 8Ω)



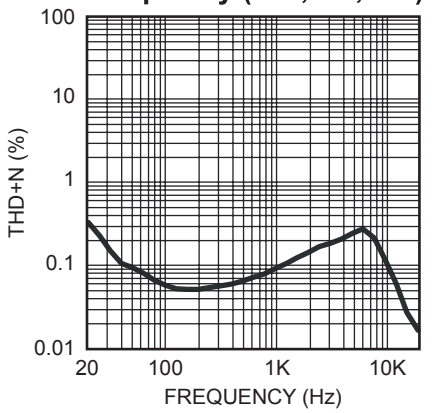
THD+N vs P_{OUT} (24V, 4Ω)



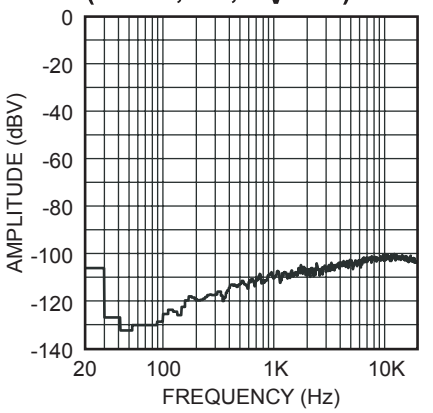
THD+N vs Frequency (24V, 8Ω, 1W)



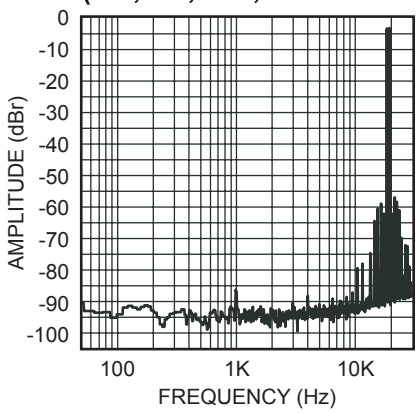
THD+N vs Frequency (24V, 4Ω, 1W)



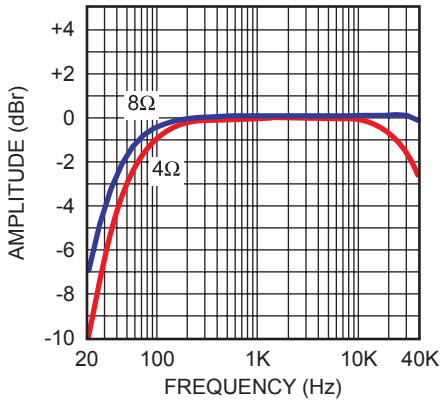
FFT Noise Floor (190μV) (A-wtd, 4Ω, A_V=8.2)



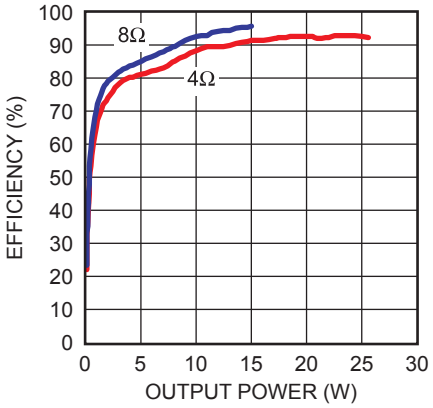
IHF-IMD (1W, 4Ω, 24V, BW=80KHz)



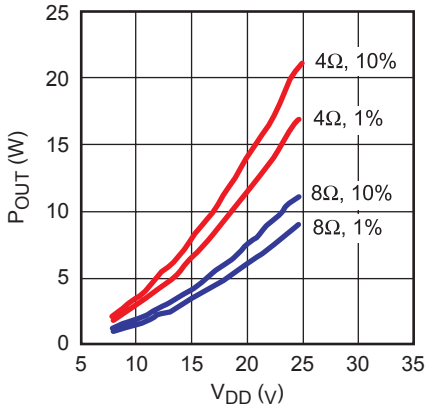
Frequency Response (Ref=2Vrms, A_V=8.2)



Efficiency vs P_{OUT}



P_{OUT} vs V_{DD}



MPS Proprietary Information. Unauthorized Photocopy and Duplication Prohibited.
© 2010 MPS. All Rights Reserved.

OPERATION

The MP7720 is a single-ended Class D audio amplifier. It uses the Monolithic Power Systems patented Analog Adaptive Modulation™ to convert the audio input signal into pulses. These pulses drive an internal high-current output stage and, when filtered through an external inductor-capacitor filter, reproduce the input signal across the load. Because of the switching Class D output stage, power dissipation in the amplifier is drastically reduced when compared to Class A, B or A/B amplifiers while maintaining high fidelity and low distortion.

The amplifier uses a differential input to the modulator. PIN is the positive input and NIN is the negative input. The common mode voltage of the input is set to half the DC power supply input voltage (V_{DD}/2) through the resistive voltage divider formed by R2 and R3. The input capacitor C1 couples the AC signal at the input.

The amplifier voltage gain is set by the combination of R1 and R4 and is calculated by the equation:

$$AV = \frac{-R4}{R1}$$

The output driver stage uses two 180mΩ N-Channel MOSFETs to deliver the pulses to the LC output filter which in turn drives the load. To fully enhance the high-side MOSFET, the gate is driven to a voltage higher than the source by the bootstrap capacitor between SW and BS. While the output is driven low, the bootstrap capacitor is charged from V_{DD} through an internal circuit on the MP7720. The gate of the high-side MOSFET is driven high from the voltage at BS, forcing the MOSFET gate to a voltage higher than V_{DD} and allowing the MOSFET to fully turn on, reducing power loss in the amplifier.

Pop Elimination

The capacitor C9 passes only AC currents to the load. To insure that the amplifier passes low frequency signals, the time constant of C9*R_{LOAD} needs to be long. However, when EN is asserted, the capacitor charges over a long period and in a normal amplifier can result in a turn on and/or turn off “pop.” The MP7720 includes integrated circuitry that eliminates the turn on and turn off pop associated with the charging of the AC coupling capacitor.

Short Circuit/Overload Protection

The MP7720 has internal overload and short circuit protection. The currents in both the high-side and low-side MOSFETs are measured and if the current exceeds the 5.0A short circuit current limit, both MOSFETs are turned off. The MP7720 then restarts with the same power up sequence that is used for normal starting to prevent a pop from occurring after a short circuit condition is removed.

Mute/Enable Function

The MP7720 EN input is an active high enable control. To enable the MP7720, drive EN with a 2.0V or greater voltage. To disable the amplifier, drive it below 0.4V. While the MP7720 is disabled, the VDD operating current is less than 5μA and the output driver MOSFETs are turned off. The MP7720 requires approximately 500ms from the time that EN is asserted (driven high) to when the amplifier begins normal operation.

MPS Proprietary Information. Unauthorized Photocopy and Duplication Prohibited.
© 2010 MPS. All Rights Reserved.

APPLICATION INFORMATION

COMPONENT SELECTION

The MP7720 uses a minimum number of external components to complete a Class D audio amplifier. The circuit of Figure 1 is optimized for a 24V power supply and a 1.5V RMS maximum input signal. This circuit should be suitable for most applications. However, if this circuit is not suitable, use the following sections to determine how to customize the amplifier for a particular application.

Setting the Voltage Gain

The maximum output voltage swing is limited by the power supply. To achieve the maximum power out of the MP7720 amplifier, set the gain such that the maximum input signal results in the maximum output voltage swing.

The maximum output voltage swing is $\pm V_{DD}/2$. For a given input signal voltage, where $V_{IN}(pk)$ is the peak input voltage, the maximum voltage gain is:

$$A_V(MAX) = \frac{V_{DD}}{2 \times V_{IN}(pk)}$$

This voltage gain setting results in the peak output voltage approaching it's maximum for the maximum input signal. In some cases the amplifier is allowed to overdrive slightly, allowing the THD to increase at high power levels, and so a higher gain than A_V (max) is required.

Setting the Switching Frequency

The idle switching frequency is a function of V_{DD}, the capacitor C3 and the feedback resistor R4. Lower switching frequencies result in more inductor ripple, causing more quiescent output voltage ripple and increasing the output noise and distortion. Higher switching frequencies result in more power loss. The optimum quiescent switching frequency is approximately 600KHz to 700KHz. Refer to the Operating Specifications for recommended values.

Table 1—Switching Frequency vs. Integrating Capacitor and Feedback Resistor (see Figure 1)

Gain (V/V)	Gain (dB)	R_4 (kΩ)	R_1 (kΩ)	C_3	F_{SW}	V_{DD} (V)
3.9	11.8	39	10	6.8nF	660KHz	12
8.2	18.3	82	10	3.3nF	660KHz	12
8.3	18.4	39	4.7	6.8nF	660KHz	12
12.0	21.6	120	10	2.2nF	610KHz	12
17.4	24.8	82	4.7	3.3nF	660KHz	12
25.5	28.1	120	4.7	2.2nF	610KHz	12
5.6	15.0	56	10	8.2nF	670KHz	24
8.2	18.3	82	10	5.6nF	720KHz	24
11.9	21.5	56	4.7	8.2nF	670KHz	24
12.0	21.6	120	10	4.7nF	620KHz	24
17.4	24.8	82	4.7	5.6nF	720KHz	24
25.5	28.1	120	4.7	4.7nF	620KHz	24
33.0	30.4	330	10	1.8nF	700KHz	24

Choosing the LC Filter

The Inductor-Capacitor (LC) filter converts the pulse train at SW to the output voltage that drives the speaker. Typical values for the LC filter are shown in Figure 1, 10µH inductor and 0.47µF capacitor.

The characteristic frequency of the LC filter needs to be high enough to allow high frequency audio to the output, yet needs to be low enough to filter out high frequency products of the pulses from SW. The characteristic frequency of the LC filter is:

$$f_0 = \frac{1}{2\pi(LC)^{\frac{1}{2}}}$$

The voltage ripple at the output is approximated by the equation:

$$V_{RIPPLE} \cong V_{DD} \times \left(\frac{f_0}{f_{SW}}\right)$$

MPS Proprietary Information. Unauthorized Photocopy and Duplication Prohibited.
© 2010 MPS. All Rights Reserved.

The quality factor (Q) of the LC filter is important. If this is too low, output noise will increase, if this is too high, then peaking may occur at high signal frequencies reducing the passband flatness. The circuit Q is set by the load resistance (speaker resistance, typically 4Ω or 8Ω). The Q is calculated as:

$$Q = \omega_0 \times \frac{L}{R} = 2\pi \times f_0 \times \frac{L}{R}$$

ω_0 is the characteristic frequency in radians per second and f_0 is in Hz. Use an LC filter with Q between 0.7 and 1.

The actual output ripple and noise is greatly affected by the type of inductor and capacitor used in the LC filter. Use a film capacitor and an inductor with sufficient power handling capability to supply the output current to the load. The inductor should exhibit soft saturation characteristics. If the inductor exhibits hard saturation, it should operate well below the saturation current. Gapped ferrite, MPP, Powdered Iron, or similar type toroidal cores are recommended. If open or shielded bobbin ferrite cores are used for multi-channel designs, make sure that the start windings of each inductor line up (all starts going toward SW pin, or all starts going toward the output) to prevent crosstalk or other channel-to-channel interference.

Output Coupling Capacitor

The output AC coupling capacitor C9 serves to block DC voltages and thus passes only the amplified AC signal from the LC filter to the load. The combination of the coupling capacitor, C9 and the load resistance results in a first-order high-pass filter. The value of C9 should be selected such that the required minimum frequency is still allowed to pass. The output corner frequency (-3dB point), f_{OUT}, can be calculated as:

$$f_{OUT} = \frac{1}{2 \times \pi \times R_{LOAD} \times C9}$$

Set the output corner frequency (f_{OUT}) at or below the minimum required frequency.

The output coupling capacitor carries the full load current, so a capacitor should be chosen such that its ripple current rating is greater than the maximum load current. Low ESR aluminum electrolytic capacitors are recommended.

Input Coupling Capacitor

The input coupling capacitor C1 is used to pass only the AC signal at the input. In a typical system application, the source input signal is typically centered around the circuit ground, while the MP7720 input is at half the power supply voltage (V_{DD}/2). The input coupling capacitor transmits the AC signal from the source to the MP7720 while blocking the DC voltage. Choose an input coupling capacitor such that the corner frequency (f_{IN}) is less than the passband frequency. The corner frequency is calculated as:

$$f_{IN} = \frac{1}{2 \times \pi \times R1 \times C1}$$

Power Source

For maximum output power, the amplifier circuit requires a regulated external power source to supply the power to the amplifier. The higher the power supply voltage, the more power can be delivered to a given load resistance, however if the power source voltage exceeds the maximum operating voltage of 24V, the MP7720 may sustain damage. The power supply rejection of the MP7720 is excellent (typically 60dB), however noise at the power supply can get to the output, so care must be taken to minimize power supply noise within the pass-band frequencies. Bypass the power supply with a large capacitor (typically aluminum electrolytic) along with a smaller 1µF ceramic capacitor at the MP7720 V_{DD} supply pins.

Circuit Layout

The circuit layout is critical for optimum performance and low output distortion and noise. Place the following components as close to the MP7720 as possible:

Power Supply Bypass, C5

C5 carries the transient current for the switching input stage. To prevent overstressing of the MP7720 and excessive noise at the output, place the power supply bypass capacitor as close to pins 6 (VDD) and 8 (PGND) as possible.

MPS Proprietary Information. Unauthorized Photocopy and Duplication Prohibited.
© 2010 MPS. All Rights Reserved.

Output Catch Diode, D1

D1 carries the current over the dead-time while both MOSFET switches are off. Place D1 between pins 7 (SW) and 8 (PGND) to prevent the voltage at SW from swinging excessively below ground.

Input Modulator Capacitor, C3

C3 is used to set the amplifier switching frequency and is typically on the order of a few nanofarads. Place C3 as close to the differential input pins (1 and 2) as possible to reduce distortion and noise.

Reference Bypass Capacitor, C2

C2 filters the ½ V_{DD} reference voltage at the PIN input (pin 1). Place C2 as close to PIN as possible to improve power supply rejection and reduce distortion and noise at the output.

Use two separate ground planes, analog ground (AGND) and power ground (PGND), and connect the two grounds together at a single point to prevent noise injection into the amplifier input to reduce distortion. Power components (C5, D1, C6 and C8) connect to the power ground. The quiet analog components (C2, C3, R2, and the input source ground) connect to the analog ground.

Place the input and feedback resistors R1 and R4 as close to the NIN input as possible. Make sure that any traces carrying the switching node (SW) voltage are separated far from any input signal traces. If multiple amplifiers are used on a single board, make sure that each channel is physically separated to prevent crosstalk. If it is required to run the SW trace near the input, shield the input with a ground plane between the traces. Make sure that all inductors used on a single circuit board have the same orientation.

If multiple channels are used on a single board, make sure that the power supply is routed from the source to each channel individually, not serially. This prevents channel-to-channel coupling through the power supply input.

High V_{DD} Operation

When operating at higher supply voltages, special care must be taken to ensure that the V_{DD} level does not exceed the absolute maximum supply rating of the IC. Power supply pumping is of significant concern when operating near the maximum supply voltage. Supply pumping is an effect where the V_{DD} voltage is “pumped up” to a higher potential when charge from the output DC blocking capacitor is transferred to the power supply rail during switch transitions. The simplest way to handle excess pumping is to increase the size of the V_{DD} main bulk capacitance such that the extra charge will be absorbed by the increased capacitance, with minimal supply increase. One way to eliminate supply pumping altogether is to use a different output configuration circuit. Figure 2 shows such an alternate configuration for connecting the speaker load. With this configuration, one side of the speaker load is connected directly to the output of the LC filter, while the other side is connected to the mid-point of a series capacitor-divider (C26, C28). Both the LC filter point and the mid point of the capacitor divider will be at a DC bias level of ½ V_{DD}, so the net DC across the speaker is $0V_{DC}$. With the speaker connected in this fashion, there is no series capacitor to cause supply pumping, and supply pumping is virtually eliminated. If the output is connected in this way, however, additional circuitry may be required to protect the speaker from damage in the event of a short circuit. Because both sides of the speaker will be typically biased at ½ V_{DD}, a short-circuit to GND on the negative side of the speaker load will result in a large DC current through the load. For example, if V_{DD}=24V and R_L=4Ω, there will be 12/4=3A of DC current through the load. This current will be sustained by the output FET stage of the IC as it will not trigger the internal over-current protection sense circuitry. A simple external sense circuit will be required for those applications which may experience an externally applied short circuit under normal use. An example of such a circuit is also shown in Figure 2.

MPS Proprietary Information. Unauthorized Photocopy and Duplication Prohibited.
© 2010 MPS. All Rights Reserved.

Electro-Magnetic Interference (EMI) Considerations

Due to the switching nature of the Class D amplifier, care must be taken to minimize the effects of electromagnetic interference from the amplifier. However, with proper component selection and careful attention to circuit layout, the effects of the EMI due to the amplifier switching can be minimized.

The power inductors are a potential source of radiated emissions. For the best EMI performance, use toroidal inductors, since the magnetic field is well contained inside the core. However toroidal inductors can be expensive to wind. For a more economical solution, use shielded gapped ferrite or shielded ferrite bobbin core inductors. These inductors typically do not contain the field as well toroidal inductors, but usually can achieve a better balance of good EMI performance with low cost.

The size of high-current loops that carry rapidly changing currents needs to be minimized. To do this, make sure that the V_{DD} bypass capacitor (C5) is as close to the MP7720 as possible.

Nodes that carry rapidly changing voltage, such as SW, need to be made as small as possible. If sensitive traces run near a trace connected to SW, place a ground shield between the traces.

MPS Proprietary Information. Unauthorized Photocopy and Duplication Prohibited.
© 2010 MPS. All Rights Reserved.

TYPICAL APPLICATION CIRCUITS

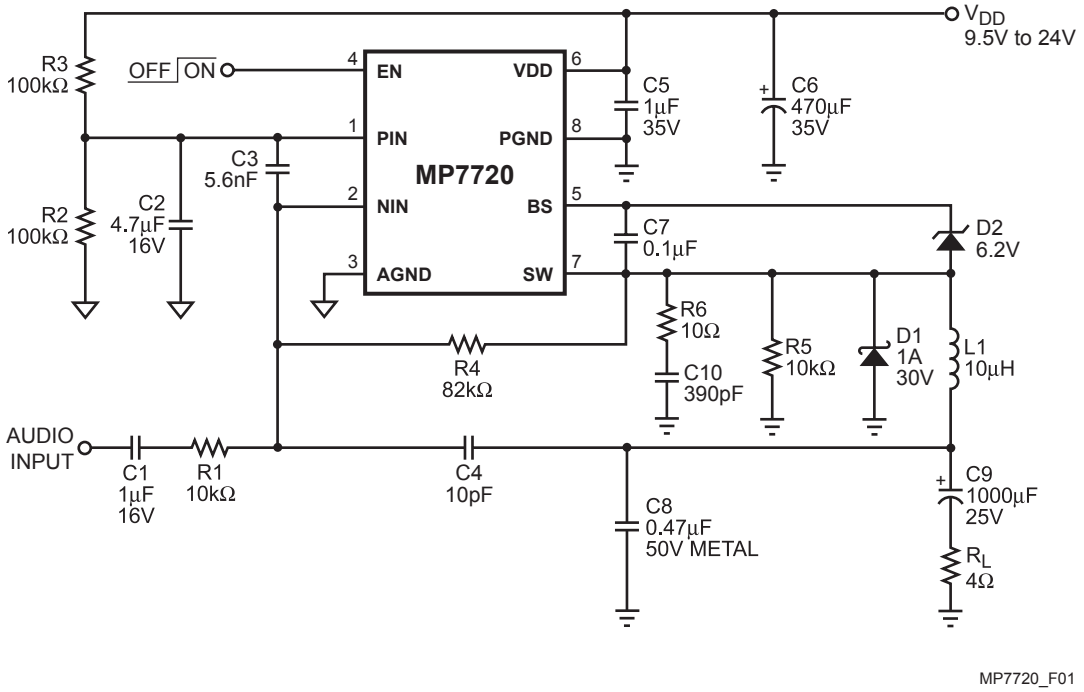


Figure 1—20W Mono Typical Application Circuit

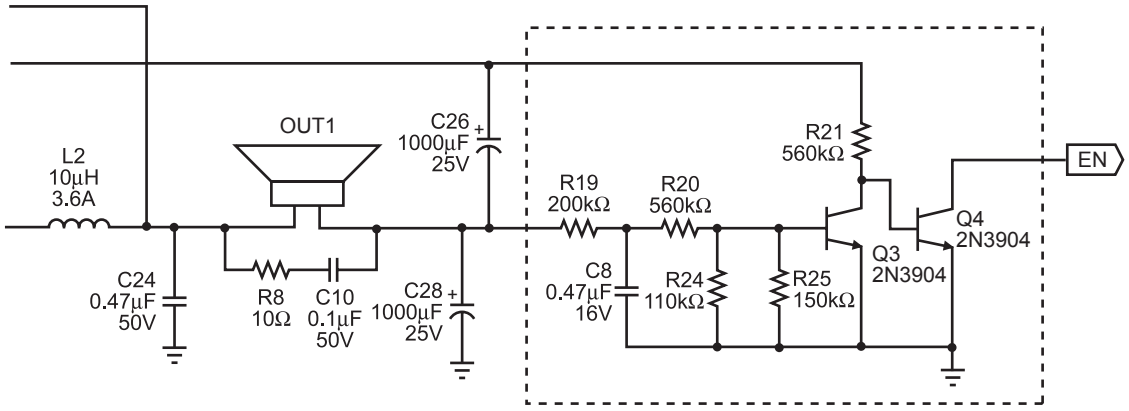
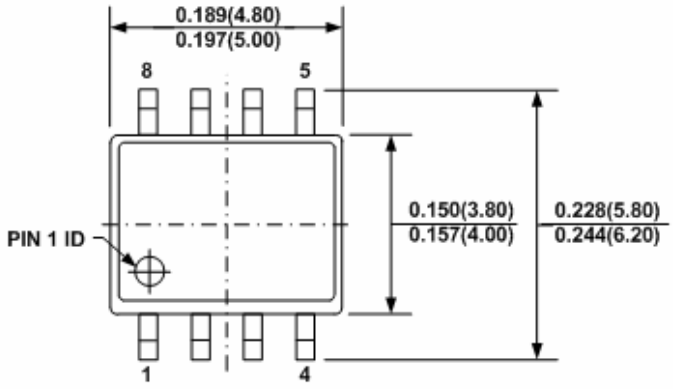


Figure 2—Alternate Configuration for high V_{DD} Applications

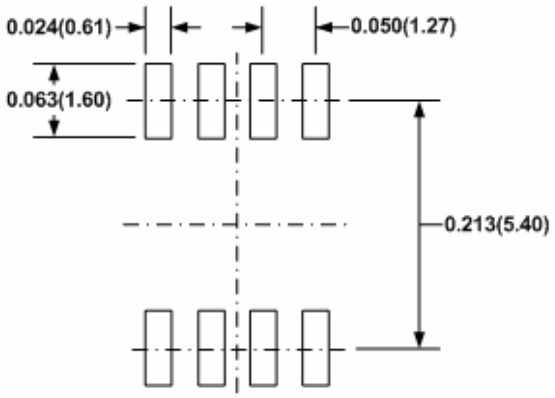
MPS Proprietary Information. Unauthorized Photocopy and Duplication Prohibited.
© 2010 MPS. All Rights Reserved.

PACKAGE INFORMATION

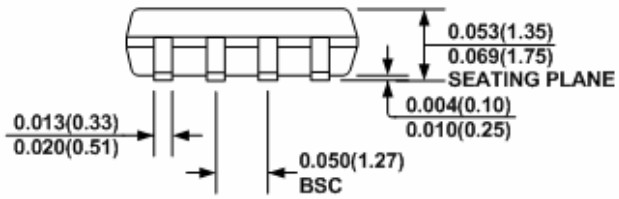
SOIC8



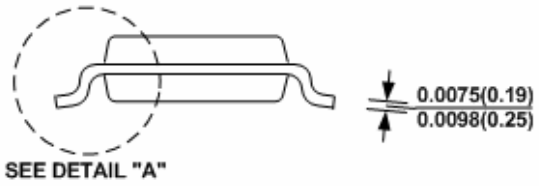
TOP VIEW



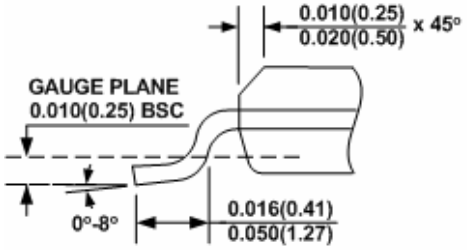
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW



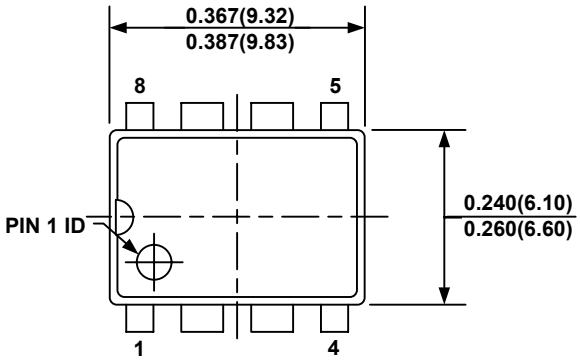
DETAIL "A"

NOTE:

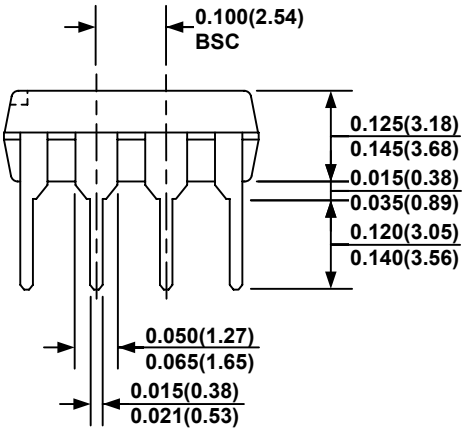
1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
5) DRAWING CONFORMS TO JEDEC MS-012, VARIATION AA.
6) DRAWING IS NOT TO SCALE.

MPS Proprietary Information. Unauthorized Photocopy and Duplication Prohibited.
© 2010 MPS. All Rights Reserved.

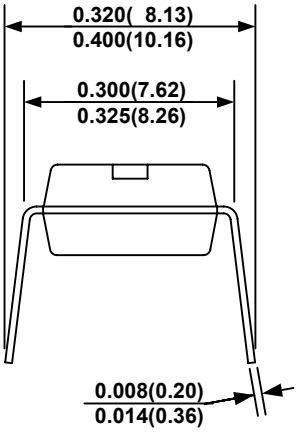
PDIP8



TOP VIEW



FRONT VIEW



SIDE VIEW

NOTE:

1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
2) PACKAGE LENGTH AND WIDTH DO NOT INCLUDE MOLD FLASH, OR PROTRUSIONS.
3) DRAWING CONFORMS TO JEDEC MS-001, VARIATION BA.
4) DRAWING IS NOT TO SCALE.

NOTICE: The information in this document is subject to change without notice. Users should warrant and guarantee that third party Intellectual Property rights are not infringed upon when integrating MPS products into any application. MPS will not assume any legal responsibility for any said applications.

MPS Proprietary Information. Unauthorized Photocopy and Duplication Prohibited.
© 2010 MPS. All Rights Reserved.