MP86884

Intelli-Phase™ Solution (Integrated HS/LS FETs and Driver) in 6x6mm TQFN

The Future of Analog IC Technology

DESCRIPTION

The MP86884 is a monolithic half-bridge with built-in internal power MOSFETs and gate drivers. It achieves 55A of continuous output current over a wide input supply range.

Integration of the driver and MOSFETS results in high efficiency due to optimal dead time control and parasitic inductance reduction.

The MP86884 is a Monolithic IC approach to drive up to 55A per phase. This very small 6mmx6mm TQFN device can operate from 100kHz to 1MHz.

This device works with tri-state output controllers. It also comes with a general-purpose current sense and temperature sense.

The MP86884 is ideal for server applications where efficiency and small size are a premium.

FEATURES

- Wide 4.5V to 14V Operating Input Range
- Simple Logic Interface
- 55A Output Current
- Accepts Tri-State PWM Signal
- Built-In Switch for bootstrap
- Current Sense
- Temperature Sense
- Current Limit Protection
- Used for Multi-Phase Operation
- Available in 6mm x 6mm TQFN Package
- ROHS6 Compliant

APPLICATIONS

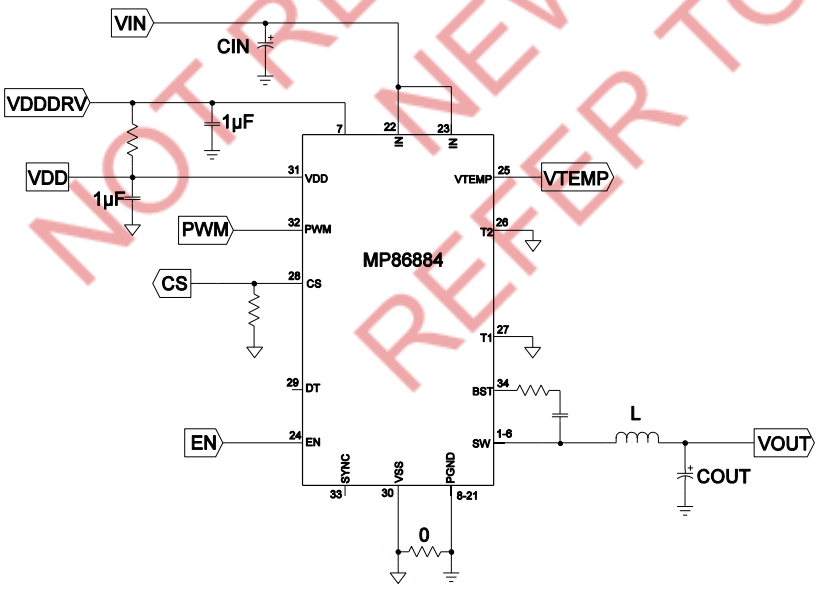
- Server Core Voltage
- Graphic Card Core Regulators
- Power Modules

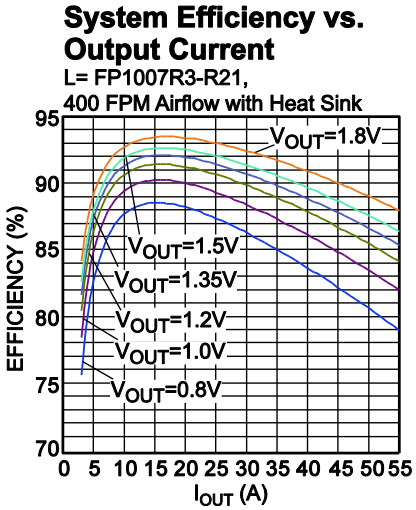
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TYPICAL APPLICATION





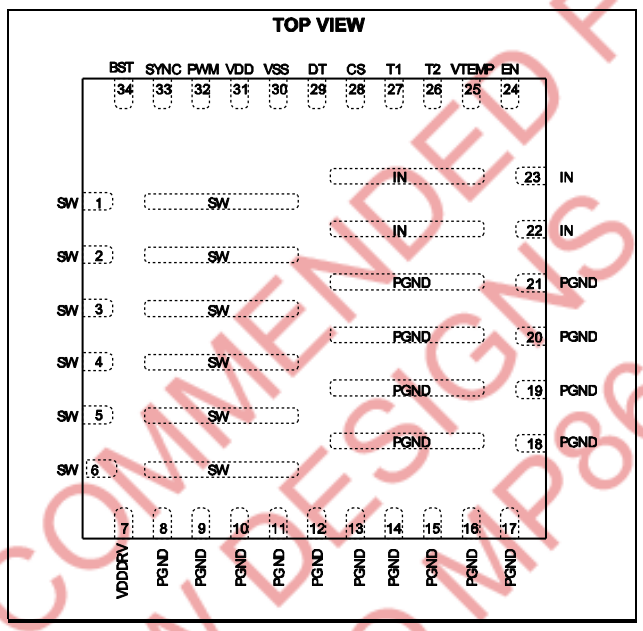
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ORDERING INFORMATION

Part Number*	Package	Top Marking
MP86884DQKT	6x6mm TQFN	MP86884

* For Tape & Reel, add suffix –Z (e.g. MP86884DQKT–Z)
For RoHS Compliant Packaging, add suffix –LF (e.g. MP86884DQKT–LF–Z)

PACKAGE REFERENCE



ABSOLUTE MAXIMUM RATINGS (1)

Supply Voltage V_{IN} 16V
$V_{SW\ (DC)}$ ..... -1 V to 15V
$V_{SW\ (25ns)}$ ..... -3V to 23V
V_{BST} ..... V_{SW} + 6V
All Other Pins..... -0.3V to +6V
Instantaneous Current 100A
Continuous Power Dissipation (T_A =+25°C)(2)
..... 4.3W
Junction Temperature..... 150°C
Lead Temperature ..... 260°C
Storage Temperature..... -65°C to +150°C

Recommended Operating Conditions (3)

Supply Voltage V_{IN} ..... 4.5V to 14V
Driver Voltage V_{DDDRV}..... 4.5V to 5.5V
Logic Voltage V_{DD} ..... 4.5V to 5.5V
Operating Junction Temp. (T_J). -40°C to +125°C

Thermal Resistance (4) θ_{JA} θ_{JC}

6x6mm TQFN..... 29 ..... 8.... °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

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ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, V_{DDDRV}=V_{DD}=5V, T_A = -40°C to 125°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
I_{IN} Shutdown	$I_{IN\ (Off)}$	V_{DDDRV}=V_{DD}=0V		55		μA
I_{IN} Standby	$I_{IN\ (Standby)}$	V_{DDDRV}=V_{DD}=5V, PWM=EN=Low		60		μA
V_{IN} Under Voltage Lockout Threshold Rising				4	4.4	V
V_{IN} Under Voltage Lockout Threshold Hysteresis				300		mV
I_{DDDRV} Quiescent Current	$I_{DDDRV\ (Quiescent)}$	PWM=Low			500	μA
I_{DDDRV} Shutdown Current	$I_{DDDRV\ Shutdown}$			250		μA
I_{DD} Quiescent Current	$I_{DD\ (Quiescent)}$	PWM=Low		2.4		mA
I_{DD} Shutdown Current	$I_{DD\ Shutdown}$			70		μA
VDD Voltage UVLO Rising				4	4.4	V
VDD Voltage UVLO Hysteresis				300		mV
High Side Current Limit (5)	I_{LIM}			80		A
Low Side Current Limit (5)				-30		A
EN Input Low Voltage					0.4	V
EN Input High Voltage			2			V
Dead-Time Rising (5)				3		ns
Dead-Time Falling (5)				8		ns
SYNC Current	I_{SYNC}	V_{SYNC}=0V		13		μA
SYNC Logic High Voltage			2			V
SYNC Logic Low Voltage					0.4	V
PWM High to SW Rising Delay(5)				35		ns
PWM Low to SW Falling Delay(5)				35		ns
PWM Tristate to SW Hi-Z Delay(5)	t_{LT}	I_{OUT}=10A		60		ns
	t_{TL}	I_{OUT}=10A		60		
	t_{HT}	I_{OUT}=10A		75		
	t_{TH}	I_{OUT}=10A		45		
Minimum PWM Pulse Width(5)				30		ns
Current Sense Accuracy(5)		I_{OUT}=30A		±4		%
Current Sense Gain				10		μA/A
Temperature Sense Gain(6)				10		mV/°C
Temperature Sense Offset(6)				-100		mV
PWM Input Current	I_{PWM}	V_{PWM}=5V, V_{EN}=5V		105		μA
		V_{PWM}=0V, V_{EN}=5V		-105		μA
PWM Logic High Voltage			4.00			V
PWM Tristate Region(5)			1.45		3.20	V
PWM Logic Low Voltage					0.50	V

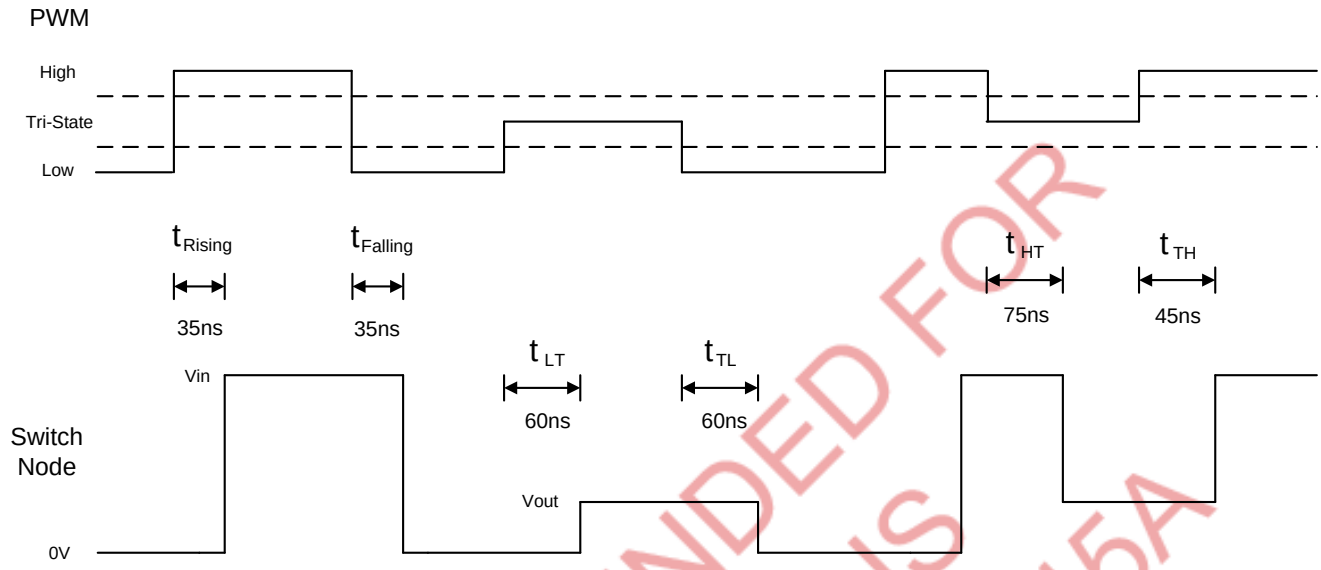
Notes:

5) Guaranteed by design.

6) See “Junction Temperature Sense” section for details.

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PIN FUNCTIONS

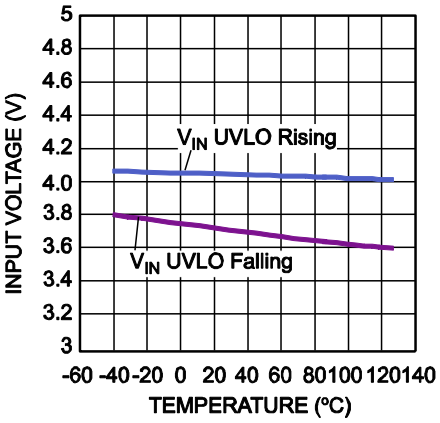
Pin #	Name	Description
1-6 Exposed Pad	SW	Switch Output.
7	VDDDRV	Driver Voltage. Connect to 5V supply and decouple with 1µF to 4.7µF ceramic capacitor.
8-21 Exposed Pad	PGND	Power Ground.
22-23 Exposed Pad	IN	Supply Voltage. Place C_{IN} close to the device to prevent large voltage spikes at the input.
24	EN	Enable. Pull low to place SW in a high impedance state.
25	VTEMP	Single pin temperature sense output.
26	T2	Test pin. Connect to ground.
27	T1	Test pin. Connect to ground.
28	CS	Current Sense Output. Requires an external resistor.
29	DT	Dead Time. It is recommended to float this pin to use default dead time setting.
30	VSS	Signal Ground.
31	VDD	Internal Circuitry Voltage. Connect to VDDDRV thru 2.2Ω resistor and decouple with 1µF capacitor to VSS. Connect VSS and PGND at this point.
32	PWM	Pulse Width Modulation. Leave PWM floating or drive to mid-state to put SW in high impedance state.
33	SYNC	Synchronous Low Switch. Leave open or pull high to enable. Pull low to enter diode emulation mode.
34	BST	Bootstrap. Requires a 0.22µF to 1µF capacitor to drive the power switch's gate above the supply voltage. Connects between SW and BST pins to form a floating supply across the power switch driver.

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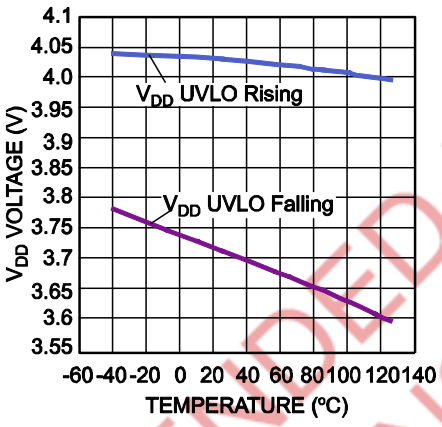
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TYPICAL CHARACTERISTICS

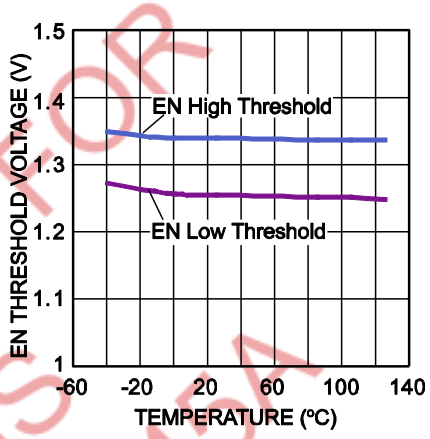
V_{IN} UVLO Threshold vs. Temperature



V_{DD} UVLO Threshold vs. Temperature

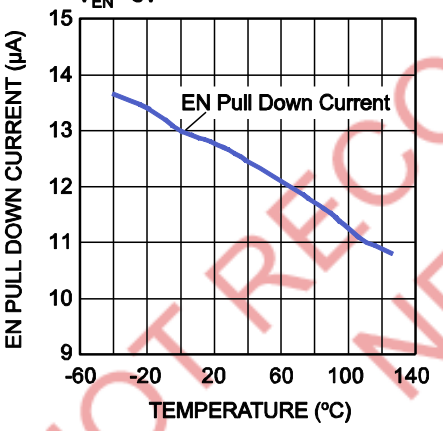


EN Threshold vs. Temperature

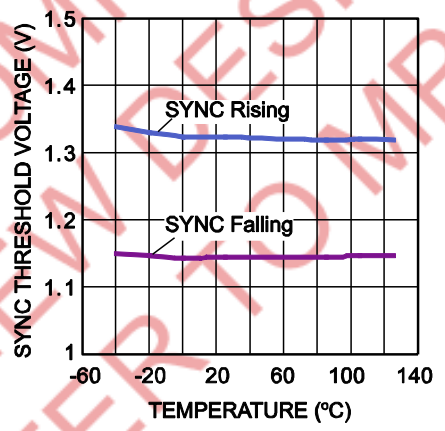


EN Pull Down Current vs. Temperature

V_{EN} =5V

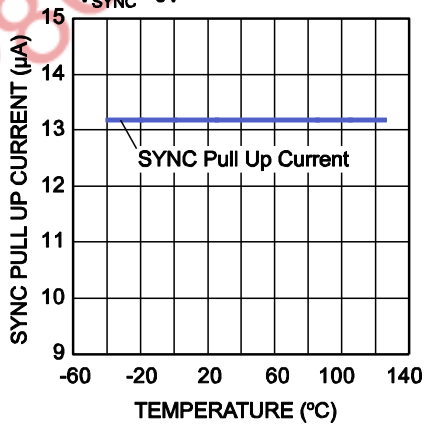


SYNC Threhold vs. Temperature

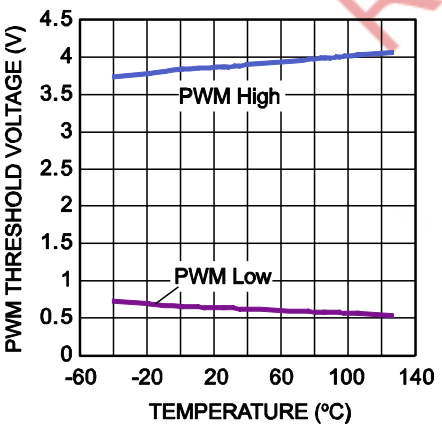


SYNC Pull Up Current vs. Temperature

V_{SYNC} =0V



PWM Threshold vs. Temperature



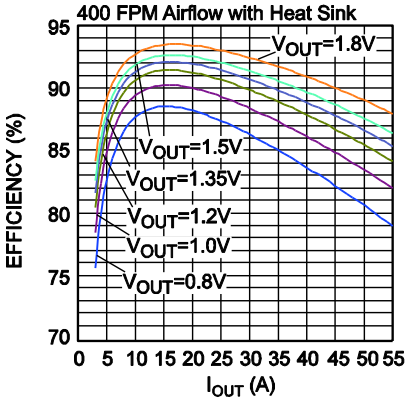
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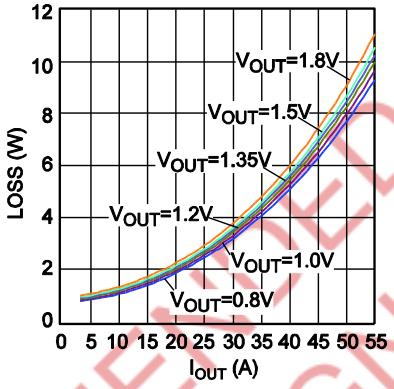
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN}=12V, V_{OUT}=1.2V, V_{DDDRV}= V_{DD}=5V, L=200nH, F_{SW}=600kHz, T_A=25°C, no droop, unless otherwise noted.

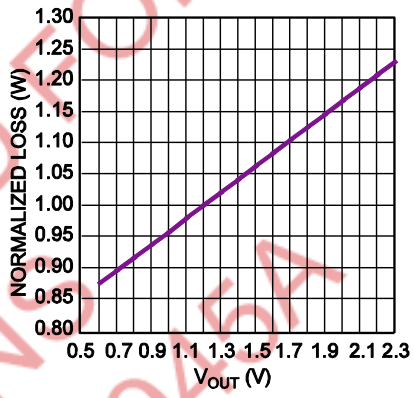
System Efficiency vs. Output Current
L= FP1007R3-R21,
400 FPM Airflow with Heat Sink



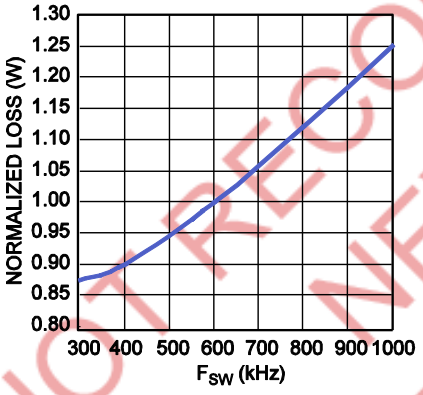
Device Loss vs. Output Current
400 FPM Airflow with Heat Sink



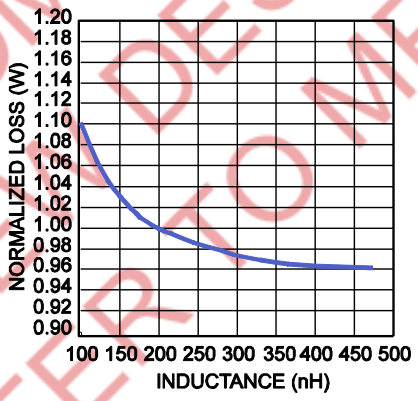
Normalized Power Loss vs. Output Voltage



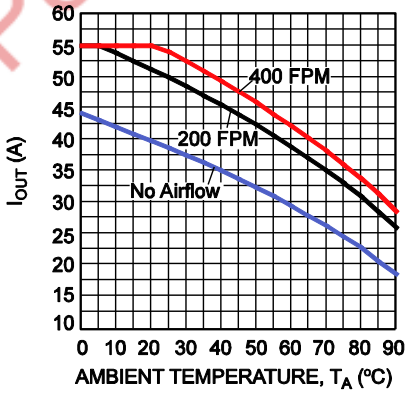
Normalized Power Loss vs. Switching Frequency



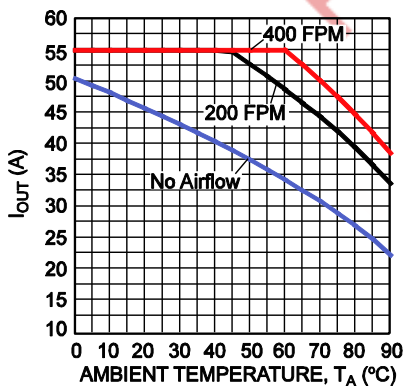
Normalized Power Loss vs. Inductance



Safe Operating Area
No Heat Sink



Safe Operating Area
With Heat Sink



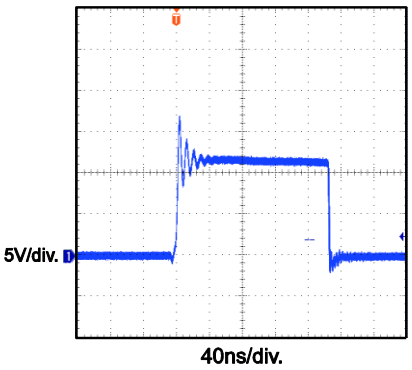
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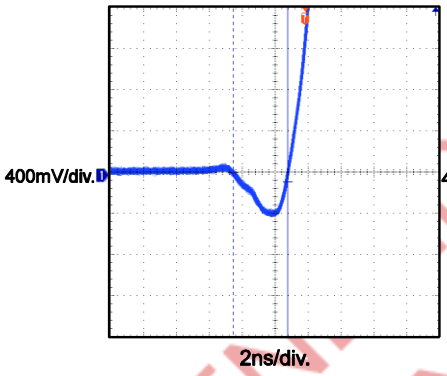
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

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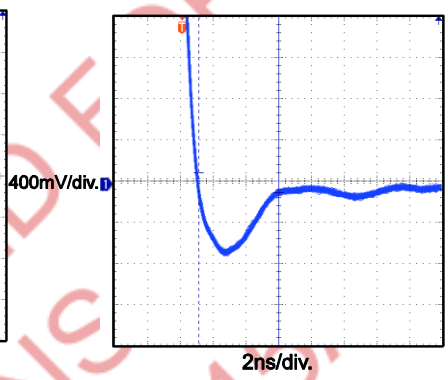
SW Output Waveform



SW Rising Edge Dead Time



SW Falling Edge Dead Time



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BLOCK DIAGRAM

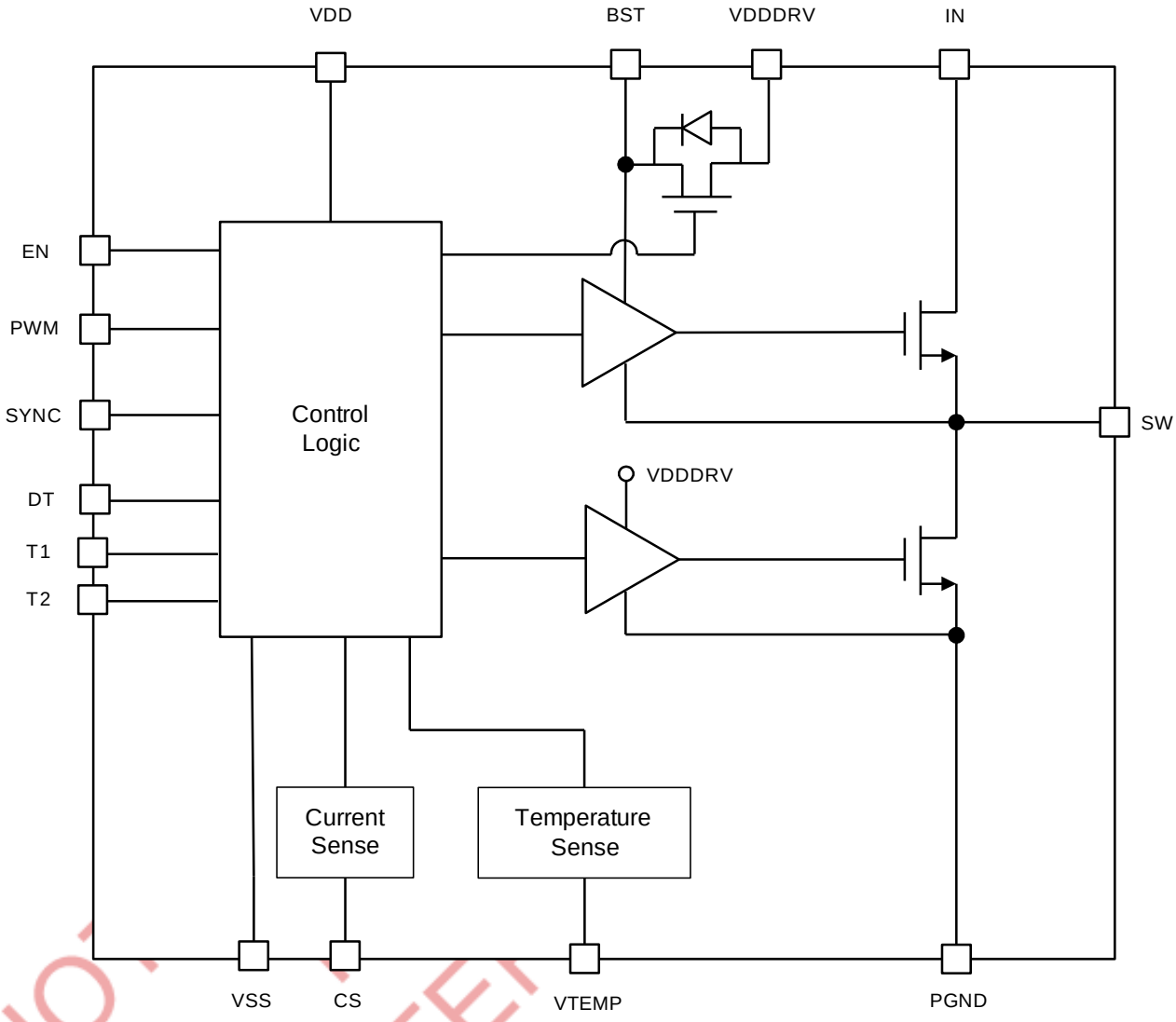


Figure 1: Functional Block Diagram

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OPERATION

The MP86884 is a 55A monolithic half-bridge driver with MOSFETs ideally suited for multi-phase buck regulators.

When the EN transitions from low to high and both V_{DD} and V_{BST} signals are sufficiently high, operation begins. It is recommended to use EN pin to startup and shutdown the Intelli-Phase.

To put SW node in a high impedance state, let PWM pin float or drive PWM pin to mid-state. Drive the SYNC pin low to enter diode emulation mode. In diode emulation mode, the LSFET is off after inductor current crossed zero current.

When HSFET over current is detected, the part will latch off. Recycling Vin/Vdd or toggling EN will release the latch and restart the device. When the LSFET detects a -30A current, the part will turn off the LSFET for that cycle.

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APPLICATION INFORMATION

Current Sense

The CS pin is a current source that generates 10μA per 1A of LSFET current. It will hold the valley current when LS turned off. Place a resistor between CS pin and ground to generate a voltage proportional to the output current. A capacitor is optional for noise immunity.

Intelli-Phase's current sense output can be used by controller to accurately monitor the output current. The cycle-by-cycle current information from CS pin can be used for phase current balancing, over current protection and active voltage positioning (output voltage droop). In multi-phase operation, the CS pins of every Intelli-Phase can be summed through resistors and connected to the current sense amplifier of the controller. This circuitry is shown in Figure 2. The reference voltage cannot be higher than 3.2V.

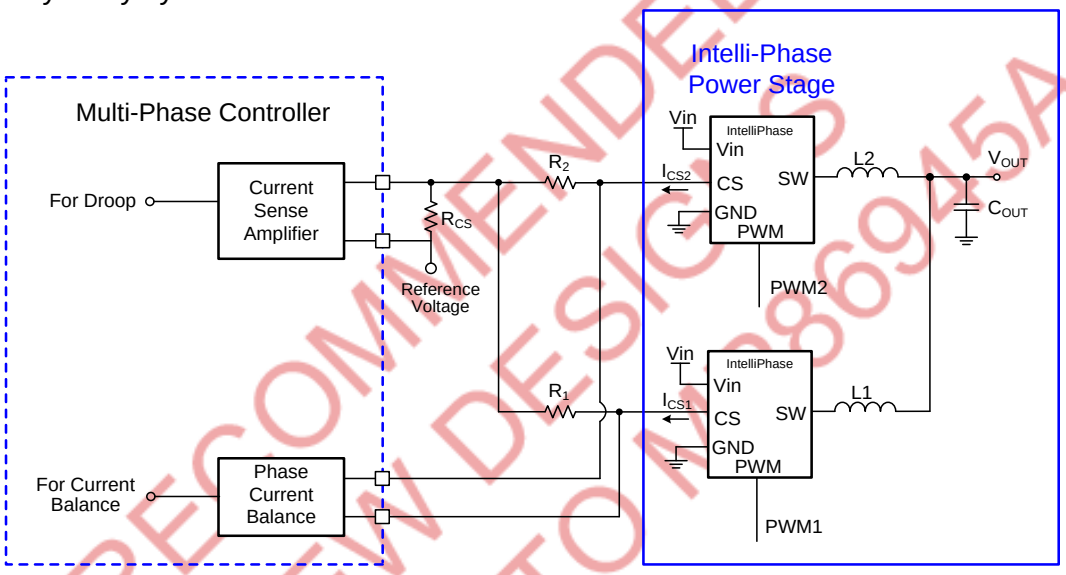


Figure 2: Multi-Phase Current Sense Utilization

Junction Temperature Sense

The VTEMP pin is a voltage output proportional to the junction temperature. The VTEMP pin output voltage is 10mV/°C with a 100mV offset.

VTEMP = Junction Temperature x 10mV/°C – 100mV.

For example, if the junction temperature is 80°C, then the VTEMP voltage is 700mV. Be sure to measure this voltage between VTEMP and VSS pins for the most accurate reading. In multi-phase operation, the VTEMP pins of every Intelli-Phase can be connected to the temperature monitor pin of the controller. A sample circuitry is shown in Figure 3. VTEMP signals can also be used for system thermal protection as shown in Figure 4.

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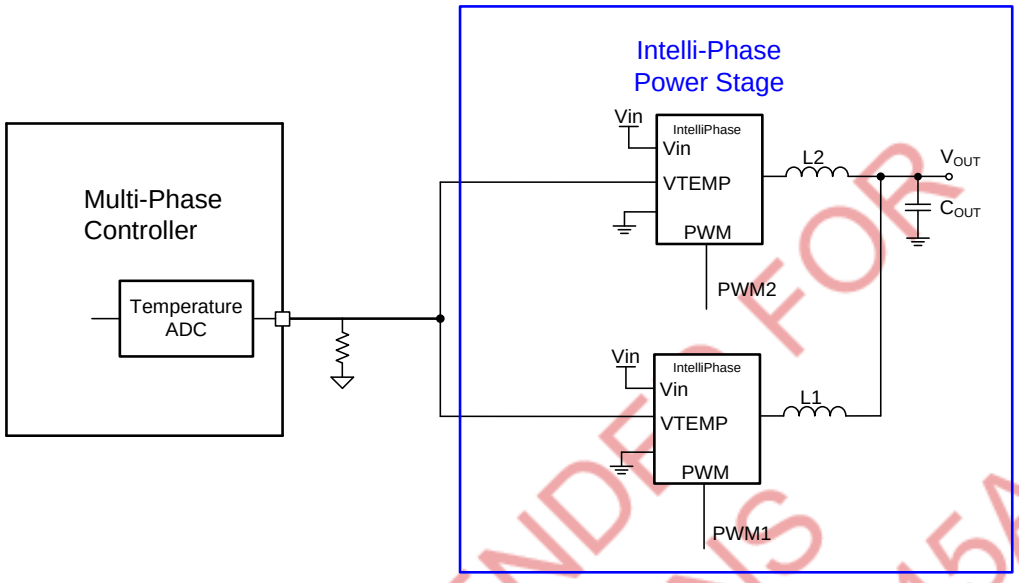


Figure 3: Multi-Phase Temperature Sense Utilization

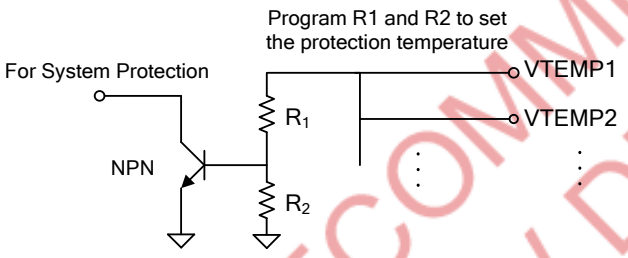
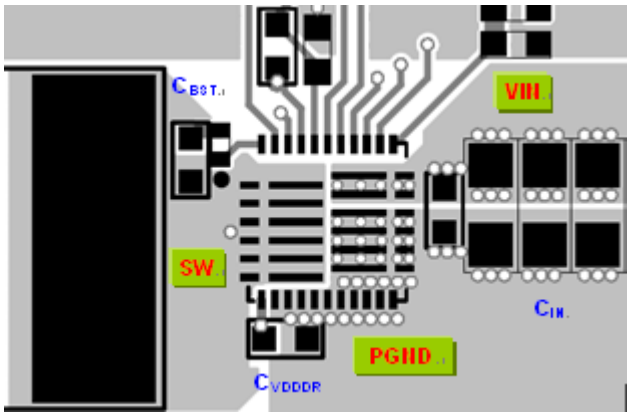


Figure 4: System Thermal Protection

PCB Layout Guide Line

PCB layout plays an important role to achieve stable operation. For optimal performance, follow these guidelines.

1. Always place some input bypass ceramic capacitors next to the device and on the same layer as the device. Do not put all of the input bypass capacitors on the back side of the device. Use as many via and input voltage planes as possible to reduce switching spikes. Place the BST capacitor and the VDDDRV capacitor as close to the device as possible.
2. Place the VDD decoupling capacitor close to the device. Connect VSS and PGND at the point of VDD capacitor's ground connection.
3. It is recommended to use 0.22µF to 1µF bootstrap capacitor and 3.3Ω bootstrap resistance. Do not use capacitance values below 100nF for the BST capacitor.
4. Connect IN, SW and PGND to large copper areas and use via to cool the chip to improve thermal performance and long-term reliability.
5. Keep the path of switching current short and minimize the loop area formed by the input capacitor. Keep the connection between the SW pin and the input power ground as short and wide as possible.



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TYPICAL APPLICATION CIRCUITS

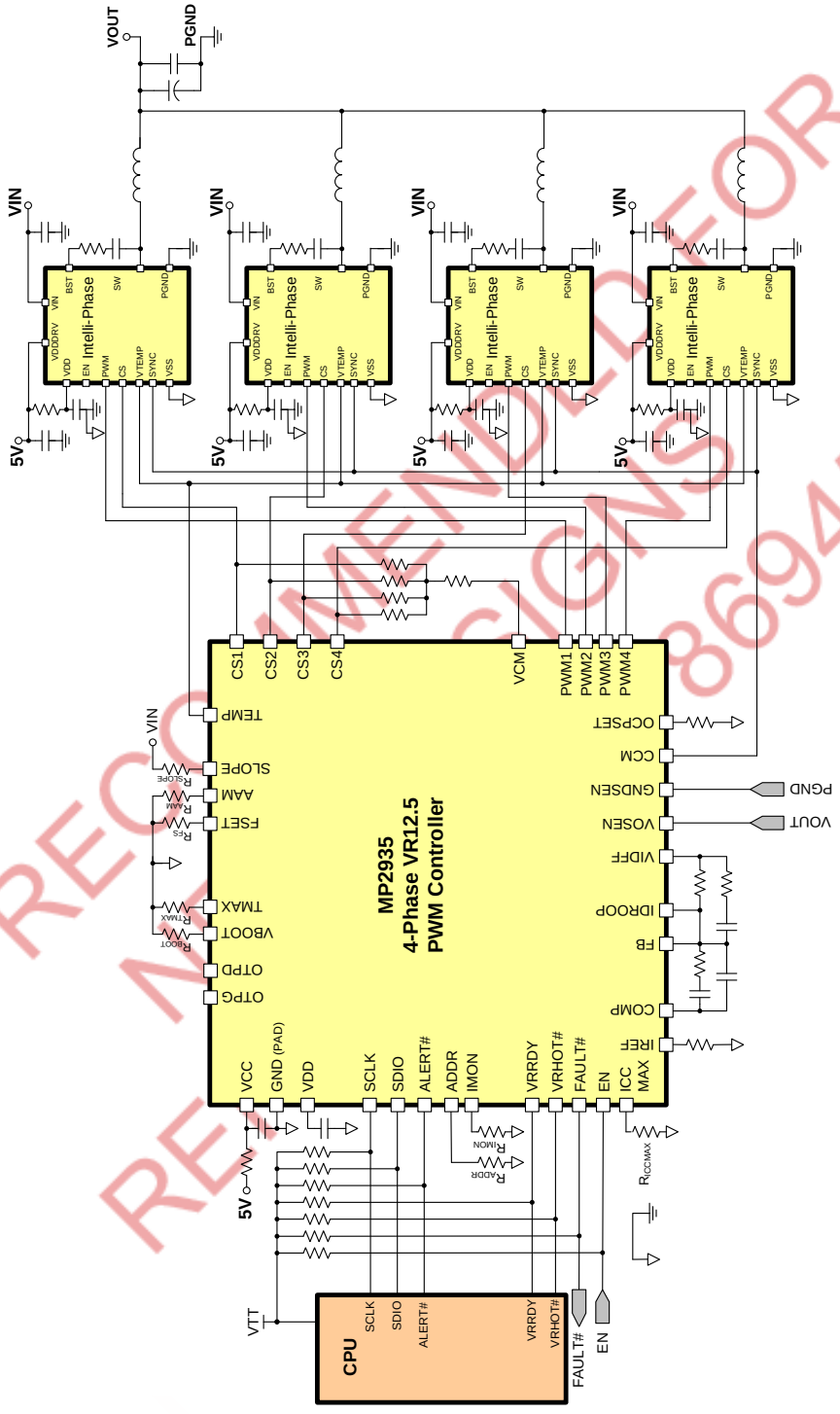


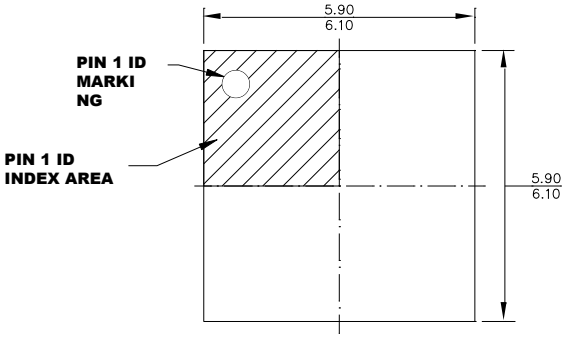
Figure 5: 4-Phase Intelli-Phase with MP2935 VR12.5 Controller

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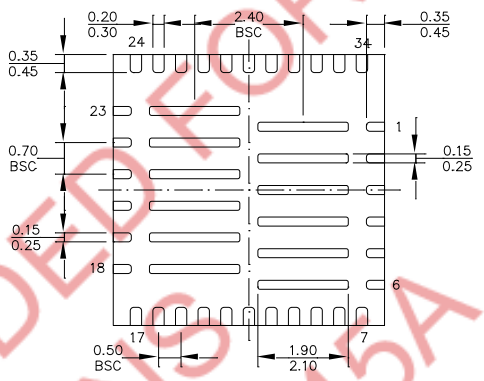
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PACKAGE INFORMATION

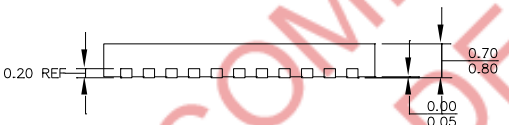
TQFN (6mm x 6mm)



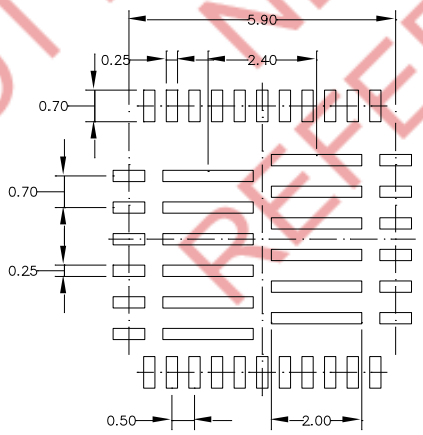
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

NOT RECOMMENDED FOR NEW DESIGNS REFER TO MP86945A

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