MP86945A

Intelli-Phase™ Solution with Integrated High-Side and Low-Side FETs and Driver

The Future of Analog IC Technology

DESCRIPTION

The MP86945A is a monolithic half-bridge with built-in, internal power MOSFETs and gate drivers. The MP86945A achieves 60A of continuous output current over a wide input supply range.

The MP86945A is a monolithic IC approach that drives up to 60A of current per phase. The integration of drivers and MOSFETs results in high efficiency due to optimal dead time and parasitic inductance reduction. The MP86945A can operate from 100kHz to 2MHz.

The MP86945A offers many features to simplify system design. The MP86945A works with controllers with tri-state PWM signal and comes with an accurate current sense to monitor inductor current and temperature sense to report junction temperature.

The MP86945A is ideal for server applications where efficiency and small size are a premium.

FEATURES

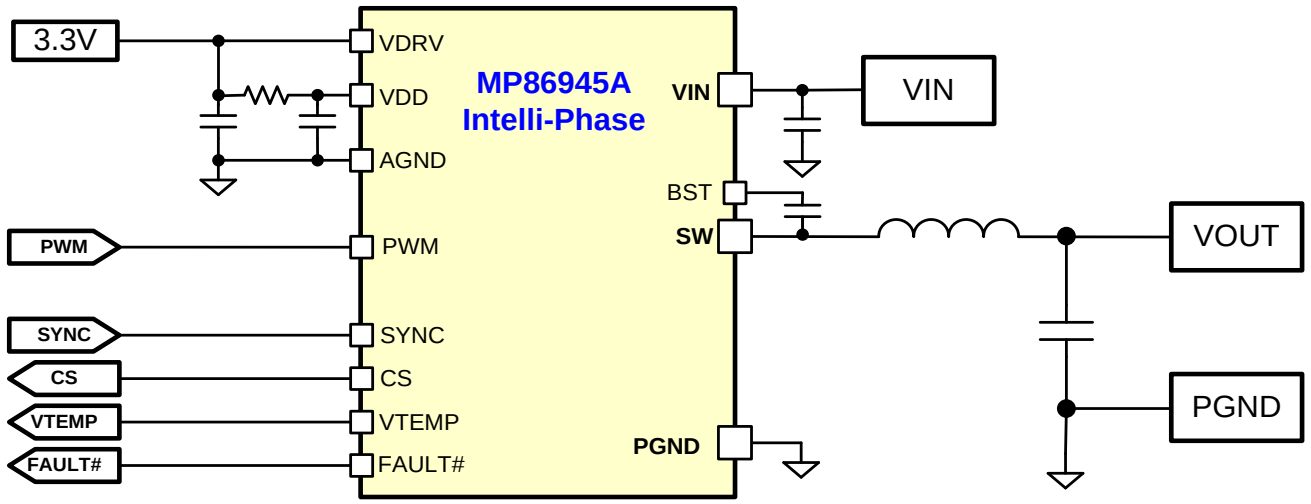
- Wide 4.5V to 16V Operating Input Range
- 60A Output Current
- Current Sense: Accu-Sense™
- Temperature Sense
- Accepts Tri-State PWM Signal
- Current-Limit Protection
- Over-Temperature Protection (OTP)
- Fault Reporting
- Available in TQFN (4mmx5mm) Package

APPLICATIONS

- Server Core Voltage
- Graphic Card Core Regulators
- Power Modules

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TYPICAL APPLICATION



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ORDERING INFORMATION

Part Number	Package	Top Marking
MP86945-AGVT*	TQFN-25 (4mmx5mm)	*See Below*

* For Tape & Reel, add suffix –Z (e.g. MP86945-AGVT–Z)

TOP MARKING (MP86945-AGVT)

MPSYWW

M86945

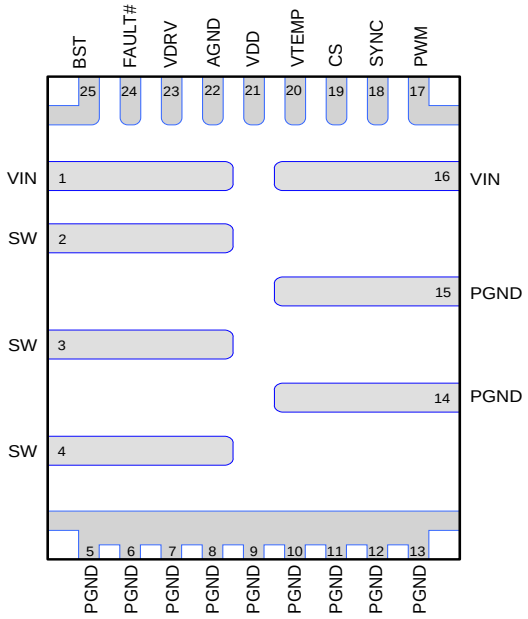
LLLLLL

A

MPS: MPS prefix
Y: Year code
WW: Week code
M86945: Part number
LLLLLL: Lot number
A: Part number

PACKAGE REFERENCE

TOP VIEW



TQFN-25 (4mmx5mm)

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ABSOLUTE MAXIMUM RATINGS (1)

Supply voltage (VIN) 18V
$V_{SW(DC)}$ ..... -0.3 V to V_{IN} + 0.3V
V_{SW} (25ns) ..... -3V to 25V
V_{IN}-V_{SW} (10ns) ..... -5V to 32V
V_{BST}-V_{SW} (25ns) 5V
V_{BST} ..... V_{SW} + 4V
VDD, VDRV ..... -0.3V to +4V
All other pins ..... -0.3V to VDD + 0.3V
Instantaneous current 95A
Junction temperature ..... 150°C
Lead temperature ..... 260°C
Storage temperature ..... -65°C to +150°C

Recommended Operating Conditions (2)

Supply voltage (VIN) ..... 4.5V to 16V
Driver voltage (VDRV) ..... 3.0V to 3.6V
Logic voltage (VDD) ..... 3.0V to 3.6V
Operating junction temp. (T_J) ..... -40°C to +125°C

Thermal Resistance (3) θ_{JB} θ_{JC_TOP}

	θ_{JB}	θ_{JC_TOP}	
TQFN-25 (4mmx5mm)	1.8	6.3	°C/W

NOTES:

1) Exceeding these ratings may damage the device.
2) The device is not guaranteed to function outside of its operating conditions.
3) θ_{JB} is the thermal resistance from the junction to the board around the PGND soldering point.
   θ_{JC_TOP} is the thermal resistance from the junction to the top of the package.

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ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, VDRV = VDD = SYNC = 3.3V, T_A = 25°C for typical value, T_J = -40°C to 125°C for max and min values, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
I_{IN} shutdown	$I_{IN\ Off}$	SYNC = Hi-Z			10	μA
VIN under-voltage lockout threshold rising				2.5	3.0	V
VIN under-voltage lockout threshold hysteresis			520	620	720	mV
I_{VDRV} quiescent current		SYNC = Hi-Z, V_{DRV} = 3.6V			20	μA
		PWM = low, V_{DRV} = 3.6V			85	μA
I_{VDD} quiescent current		SYNC = Hi-Z, V_{DD} = 3.6V			35	μA
		PWM = low, V_{DD} = 3.6V		4	5	mA
VDD voltage UVLO rising				2.8	2.9	V
VDD voltage UVLO hysteresis			200	250	300	mV
VDRV voltage UVLO rising				2.75	2.9	V
VDRV voltage UVLO hysteresis			380	430	480	mV
High-side current limit(4)	I_{LIM_FLT}	Cycle by cycle up to 3 cycles		90		A
Low-side current limit(4)		Negative current limit, cycle-by-cycle, no fault report		-30		A
Negative current limit low-side off time(4)				40		ns
High-side current limit shutdown counter(4)				3		times
Dead-time rising(4)				2		ns
Dead-time falling(4)		Positive inductor current		6		ns
		Negative inductor current		35		ns
SYNC logic high voltage			2.50			V
SYNC tri-state region			1.20		2.00	V
SYNC logic low voltage					0.70	V
PWM high to SW rising delay(4)	t_{Rising}			15		ns
PWM low to SW falling delay(4)	$t_{Falling}$			15		ns
PWM tri-state to SW Hi-Z delay(4)	t_{LT}			40		ns
	t_{TL}			20		ns
	t_{HT}			40		ns
	t_{TH}			20		ns

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ELECTRICAL CHARACTERISTICS *(continued)*

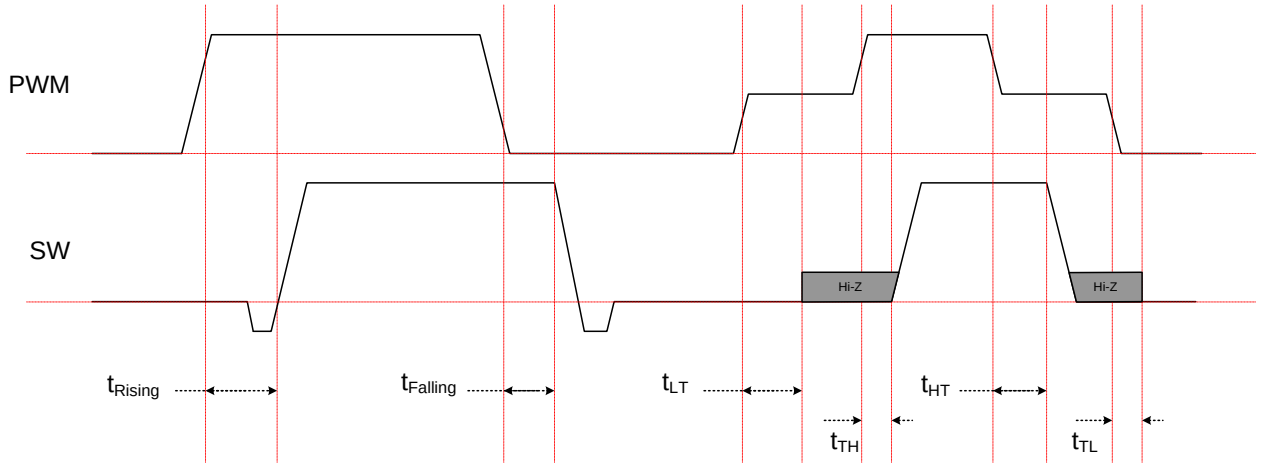
V_{IN} = 12V, VDRV = VDD = SYNC = 3.3V, T_A = 25°C for typical value, T_J = -40°C to 125°C for max and min values, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Minimum PWM pulse width(4)				20		ns
CS sense gain accuracy		15A ≤ I_{SW} ≤ 60A	-2	0	+2	%
CS sense gain				8.5		µA/A
CS voltage range	V_{CS}		0.7		2.1	V
Current sense offset		I_{SW} = 0A	-5		5	µA
Current sense offset at Hi-Z		SW = Hi-Z			2	µA
VTEMP sense gain(4)				10		mV/°C
VTEMP sense offset(4)		T_J = 25°C		-100		mV
Over-temperature shutdown and fault flag(4)				160		°C
Over-temperature threshold hysteresis(4)				30		°C
PWM input current	I_{PWM}	V_{PWM} = 3.0V		730	830	µA
		V_{PWM} = 0V, V_{DD} = 3.0V		-550	-500	µA
PWM logic high voltage			2.30			V
PWM tri-state region			1.10		1.90	V
PWM logic low voltage					0.80	V
FAULT# pull-down		Sink 5mA			0.3	V
Wake-up time(4)		SYNC = Hi-Z to Hi, PWM = 0V		30	50	µs

NOTE:

4) Guaranteed by design or characterization data, not tested in production.

PWM TIMING DIAGRAM



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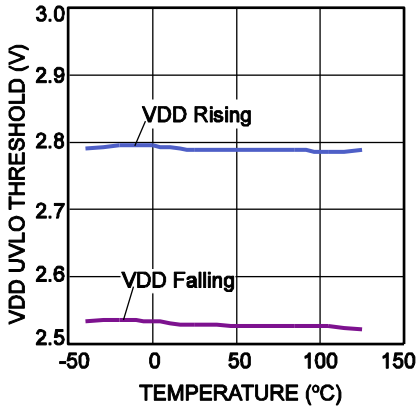
PIN FUNCTIONS

Pin #	Name	Description
1, 16	VIN	**Supply voltage.** Place the input capacitor (C_{IN}) close to the device to support the switching current reducing voltage spikes at the input.
2 - 4	SW	**Phase node.**
5 - 15	PGND	**Power ground.**
17	PWM	**Pulse width modulation input.** Leave PWM floating or drive PWM to mid-state to put SW in a high-impedance state.
18	SYNC	**Diode emulation mode and standby mode selection.** Leave SYNC floating or drive SYNC to mid-state to enter standby mode. Pull SYNC high for CCM operation. Pull SYNC low to enable diode emulation mode.
19	CS	**Current sense output.** Use an external resistor to adjust the voltage proportional to the inductor current.
20	VTEMP	**Single pin temperature sense.**
21	VDD	**Internal circuitry voltage.** Connect VDD to VDRV through a 2.2Ω resistor and decouple with a 1µF capacitor to AGND. Connect AGND and PGND at the VDD capacitor.
22	AGND	**Analog ground.**
23	VDRV	**Driver voltage.** Connect VDRV to a 3.3V supply and decouple with a 1µF to 4.7µF ceramic capacitor.
24	FAULT#	**Fault.** FAULT# is an open drain, active low. FAULT# pulls low when a fault occurs.
25	BST	**Bootstrap.** BST requires a 0.1µF to 1µF capacitor to drive the power switch's gate above the supply voltage. Connect a capacitor between SW and BST to form a floating supply across the power switch driver.

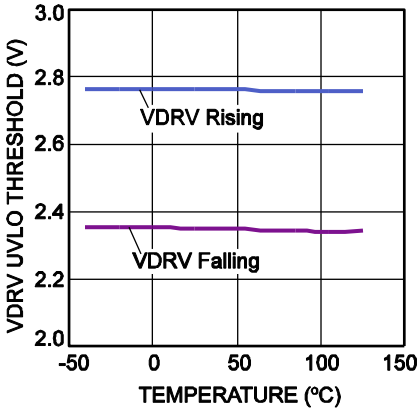
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TYPICAL CHARACTERISTICS

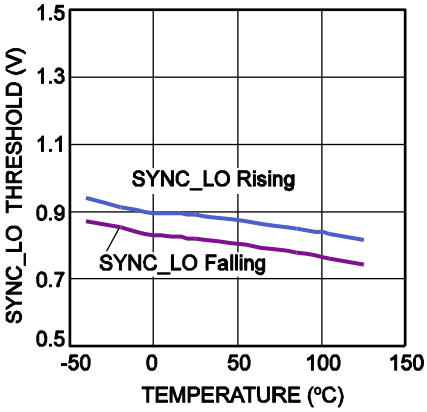
VDD UVLO



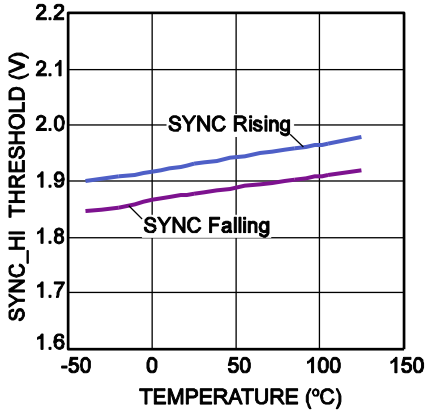
VDRV UVLO



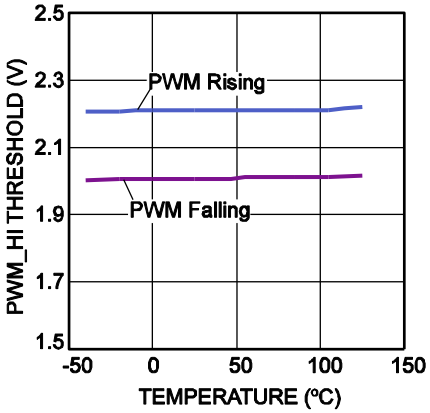
Sync_Lo



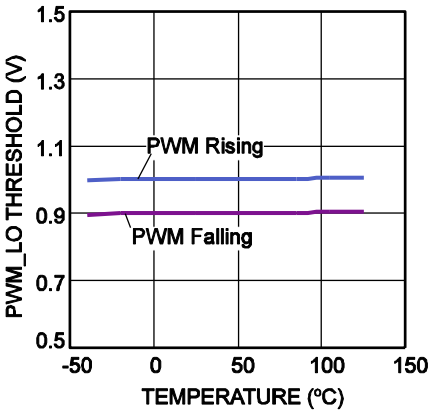
Sync_Hi



PWM Hi

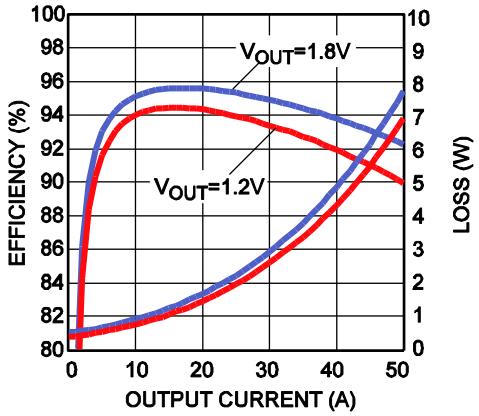


PWM Lo



Device Efficiency and Loss

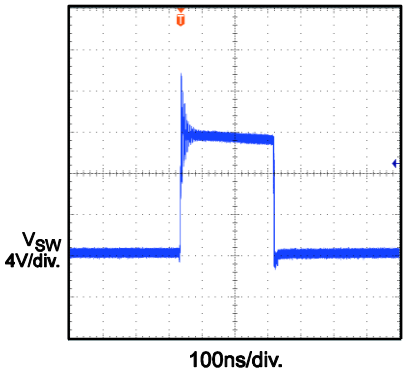
V_{IN}=12V, L=220nH, F_{SW}=500kHz



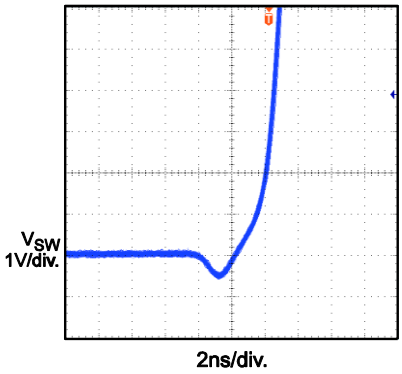
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TYPICAL PERFORMANCE CHARACTERISTICS

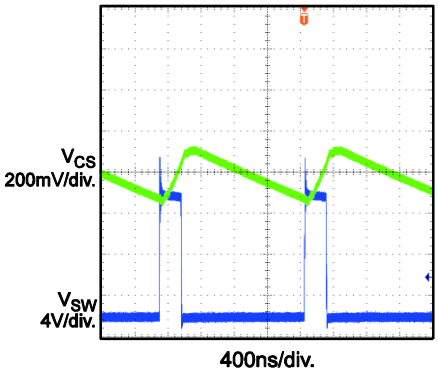
Switching Waveform
V_{IN} = 12V, L = 150nH, I_{OUT} = 30A



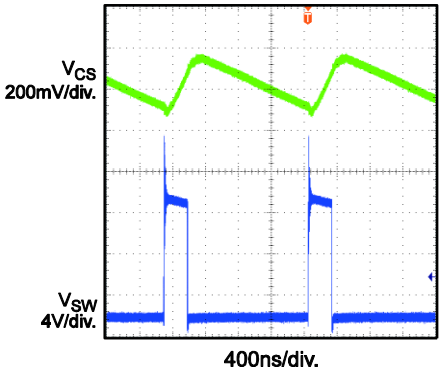
Dead Time @ SW Rising
I_{OUT} = 30A



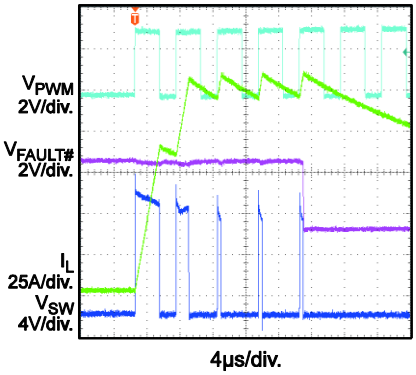
CS Output Waveform
I_{OUT} = 0A



CS Output Waveform
I_{OUT} = 30A



HS Current Limit



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BLOCK DIAGRAM

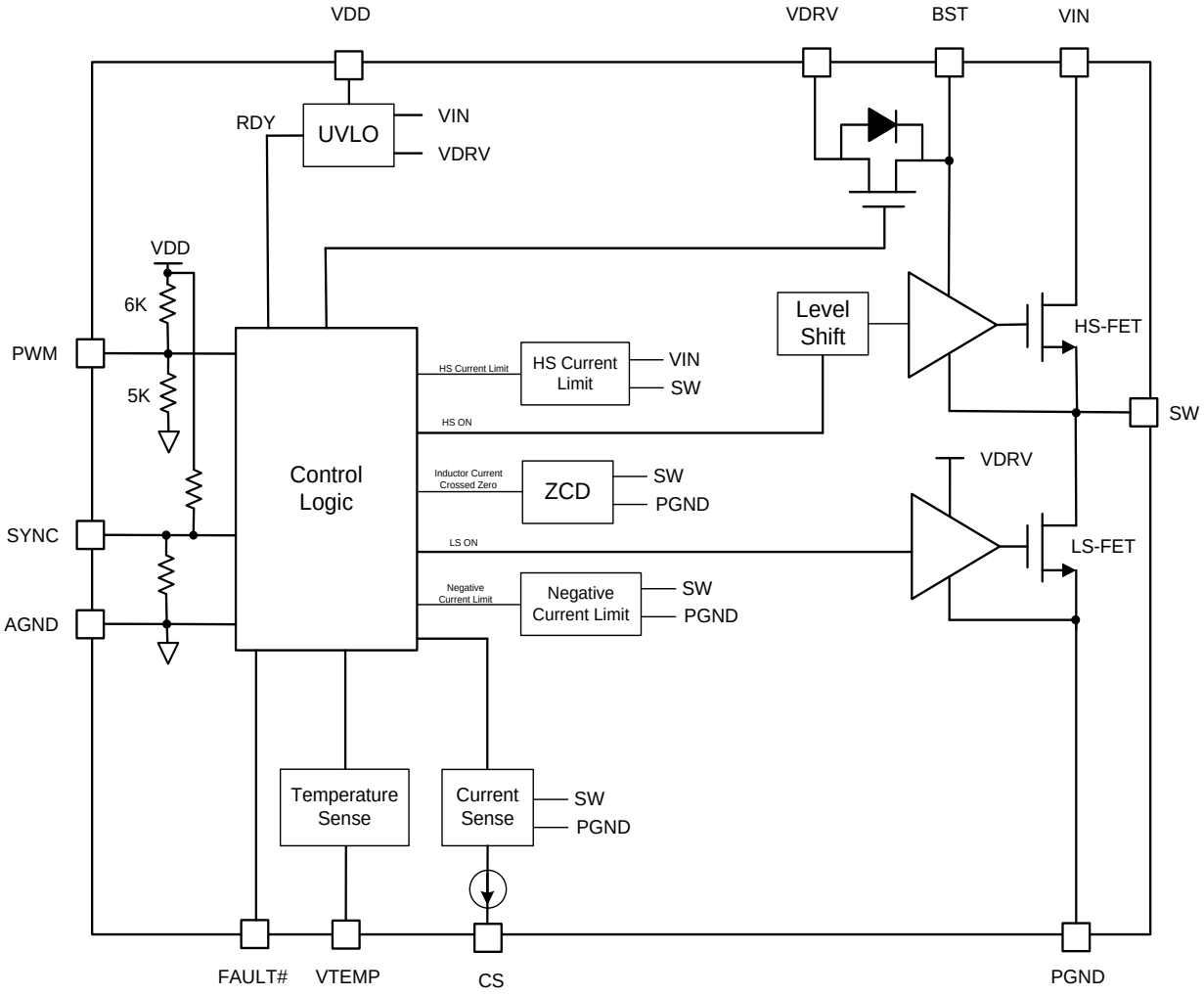


Figure 1: Functional Block Diagram

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OPERATION

The MP86945A is a 60A, monolithic, half-bridge driver with integrated MOSFETs and is ideally suited for multi-phase buck regulators. An external 3.3V supply is required to supply both VDD and VDRV. When the VIN, VDD, and VDRV signals are sufficiently high, operation begins.

APPLICATION INFORMATION

Pulse-Width Modulation (PWM)

The PWM input pin is capable of tri-state input. When the PWM input signal is within the tri-state threshold window for a typical 40ns (T_{HT} or T_{LT}), the HS-FET turns off immediately, and the LS-FET enters diode emulation mode and remains on until zero-current detection. The tri-state PWM input can come from a forced middle voltage PWM signal or be made by floating the PWM input. The internal current source charges the signal to a middle voltage. Please refer to the PWM timing diagram on page 6 for the propagation delay definition from PWM to the SW node.

Standby Mode

When SYNC is floating or is forced into a middle-state voltage for 2µs, the MP86945A enters standby mode. In standby mode, the MP86945A shuts down, and both the CS and VTEMP outputs are disabled. The FAULT# latch cannot be reset by entering standby mode.

Diode Emulation Mode

In diode emulation mode, when PWM is either low or in a tri-state input, the LS-FET is turned on whenever the inductor current is positive. The LS-FET turns off if the inductor current is negative or after the inductor current crosses the zero current. Diode emulation mode can be enabled by pulling SYNC low, driving PWM to middle state, or floating PWM.

Current Sense (CS)

CS is a bidirectional current source proportional to the inductor current. The current sense gain is 8.5µA/A. A resistor is used to program the voltage gain proportional to the inductor current if needed.

The CS output has two states (see Table 1). In standby mode, the CS circuit is disabled. It needs up to 50µs to wake up from standby mode to enter active mode.

Table 1: CS Output States

PWM	SYNC	CS
PWM	Hi	Active
PWM	Low	Active
x	Hi-Z (or middle)	Standby

The CS voltage range of 0.7V to 2.1V is required to achieve an accurate CS current output of up to +510µA/-255µA (i.e.: +60A/ -30A). Generally, there is a resistor (R_{CS}) connected from CS to an external voltage which is capable of sinking small currents to provide enough voltage level to meet the required operating voltage range. Determine a proper reference voltage, V_{CM}, and/or R_{CS} value with Equation (1) and Equation (2):

$$0.7V < I_{CS} \times R_{CS} + V_{CM} < 2.1V \quad (1)$$

$$I_{CS} = I_L \times G_{CS} \quad (2)$$

Where V_{CM} is a reference voltage connected to R_{CS}.

The Intelli-Phase's current sense output can be used by a controller to accurately monitor the output current. The cycle-by-cycle current information from CS can be used for phase-current balancing, over-current protection (OCP), and active-voltage positioning (output-voltage droop).

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Positive and Negative Inductor Current Limit

When HS-FET over-current is detected for three consecutive cycles, the HS-FET latches off, FAULT# is asserted low, and the LS-FET turns on until zero-current detection. Recycling VIN and VDD/VDRV releases the latch and restarts the device.

When the LS-FET detects a -30A current, the MP86945A turns off the LS-FET for 40ns to limit the negative current. The LS-FET's negative current limit will not trigger a fault report.

Over-Temperature Protection (OTP)

When the junction temperature reaches the over-temperature threshold, the HS-FET latches off, FAULT# is asserted low, and the LS-FET turns turn on until zero-current detection.

An OTP test mode can be entered by pulling VTEMP up to the VDD voltage. When VTEMP is higher than the internal OTP test mode threshold of 2.4V (typical), the MP86945A emulates the OTP shutdown mode. For normal operation, the VTEMP voltage must be lower than VDD - 0.9V (2.2V at VDD = 3.3V).

Temperature Sense Output (VTEMP)

VTEMP is used to report the junction temperature. VTEMP is a voltage output proportional to the junction temperature. The VTEMP output voltage is 10mV/°C with a -100mV offset. Calculate VTEMP with Equation (3):

$$V_{TEMP} = T_J \times 10^{mV/^oC} - 100mV \quad (3)$$

For example, if the junction temperature is 100°C, then VTEMP is 0.9V. VTEMP is 0V when the junction temperature is below 10°C. In multi-phase operation, the VTEMP pin of every Intelli-Phase can be connected to the temperature monitor pin of the controller (see Figure 2).

Fault Reporting (FAULT#)

FAULT# is an open-drain, active-low signal that reports faults from the Intelli-Phase. When any fault occurs, FAULT# is pulled low immediately. After 200ns, the PWM impedance represents the fault type. Table 2 shows the PWM status in regards to each fault event.

Table 2: PWM Resistance when Fault Occurs

Fault Type	PWM
Current-limit protection	10kΩ to AGND
Over-temperature protection	20kΩ to AGND
SW-PGND short protection	1kΩ to VDD

FAULT# is able to monitor four fault events (see Table 2). Each fault type manifests as an impedance between PWM and either AGND or VDD, which is read by the appropriate controller and logged as a fault.

FAULT# monitors the following fault events:

1. Over-current limit: To trip the over-current fault, the current limit must be exceeded four consecutive times. Once the fault occurs, the part latches off to turn off the HS-FET. The LS-FET turns off when the inductor current reaches zero.
2. Over-temperature fault at T_J > 160°C: Once the fault occurs, the MP86945A latches off to turn off the HS-FET. The LS-FET turns off when the inductor current reaches zero.
3. SW to PGND shorted: Once the fault occurs, the MP86945A latches off to turn off the HS-FET. PWM is pulled high to indicate the fault type.

The fault latch cannot be reset by entering standby mode. The fault latch can be released by recycling VIN or VDD.

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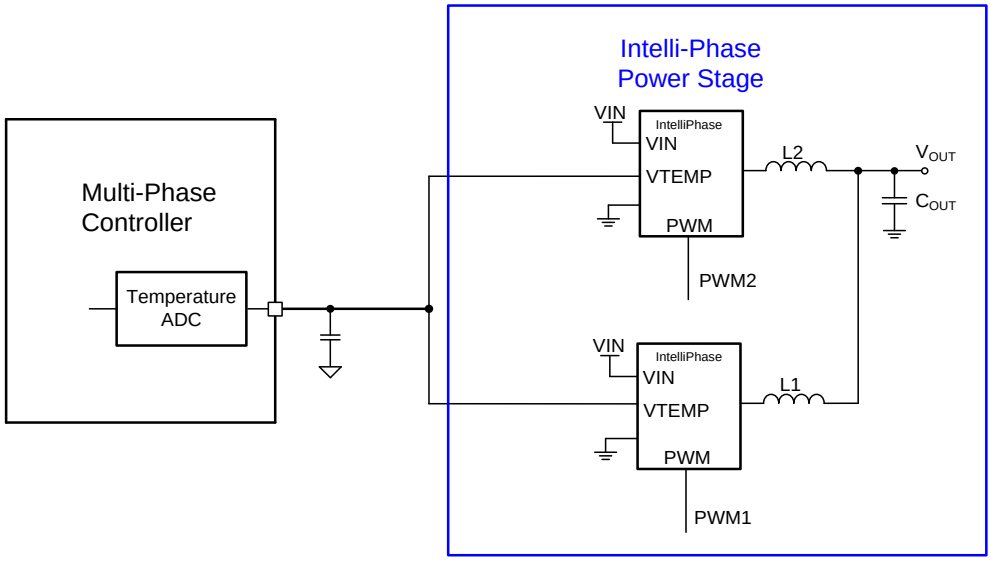


Figure 2: Multi-Phase Temperature Sense Utilization

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PCB Layout Guidelines

Efficient PCB layout is critical for stable operation. For best results, refer to Figure 3 and follow the guidelines below.

1. Place the input MLCC capacitors as close to VIN and PGND as possible.
2. Place the major MLCC capacitors on the same layer as the MP86945A.
3. Place as many VIN and PGND vias as possible underneath the package.
4. Place the vias between the VIN or PGND long pads.
5. Place a VIN copper plane on the second inner layer to form the PCB stacks as VIN on top, GND on the second layer, and VIN on the third layer to reduce parasitic impedance from the input MLCC cap to the MP86945A.
6. Ensure that the copper plane on the inner layer at least covers the VIN vias underneath the package and input MLCC capacitors.
7. Place more PGND vias close to the PGND pin/pad to minimize both parasitic resistance/impedance and thermal resistance.
8. Place a BST capacitor and a VDRV capacitor as close to the MP86945A's pins as possible.
9. Use a trace width 20 mils or higher to route the path.
10. Avoid the via for the BST driving path. It is recommended to use a bootstrap capacitor 0.1µF to 1µF.
11. Place the VDD decoupling capacitor close to the device.
12. Connect AGND and PGND at the point of the VDD capacitor's ground connection.
13. Keep the CS signal trace away from high current paths such as SW and PWM.

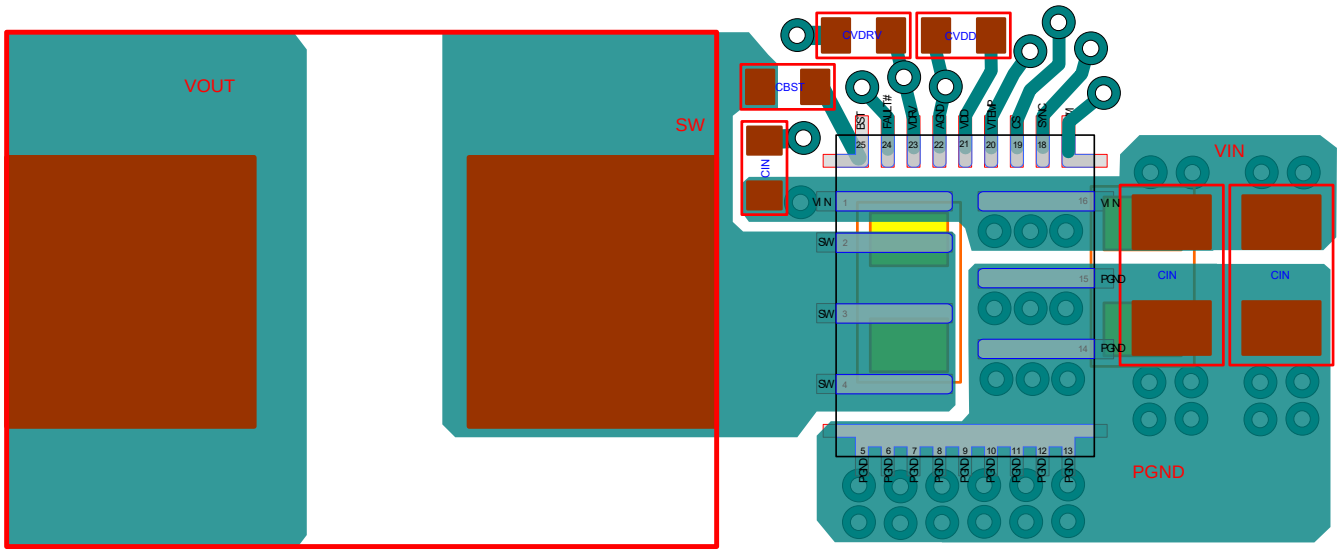


Figure 3: Example of PCB Layout (Placement and Top Layer PCB)

Input capacitor: 0805 package (top and bottom sides) and 0402 package (top side)

Inductor: 11x8 package

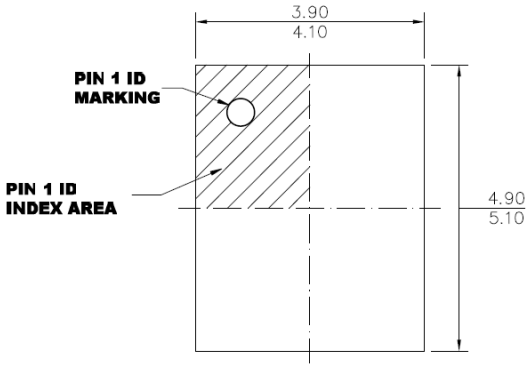
VDD/BST/VDRV capacitor: 0402 package

Via size: 20/10 mils

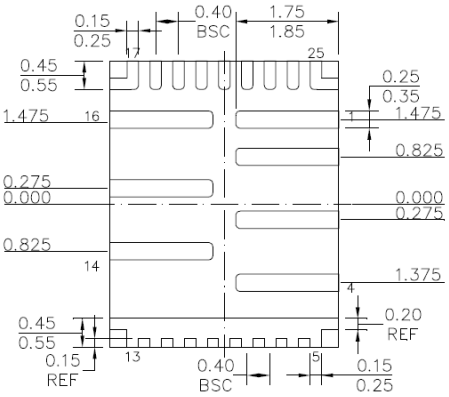
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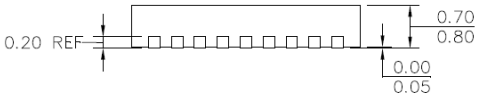
TQFN-25 (4mmx5mm)



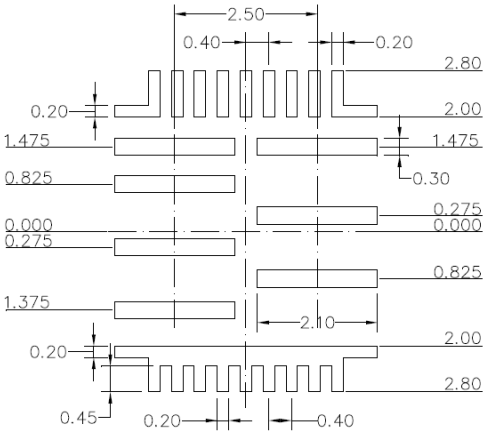
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) LAND PATTERNS OF PIN1,2,3,4,14,15 AND 16 HAVE THE SAME LENGTH AND WIDTH.
3)ALL DIMENSIONS ARE IN MILLIMETERS.
4) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
5) JEDEC REFERENCE IS MO-220.
6) DRAWING IS NOT TO SCALE.

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Revision History

Revision #	Revision Date	Description	Pages Updated
r1.2	5/19/2020	Correct/add the “Vin-Vsw (10ns) ……. -5V to 32V” on absMax rating.	Page 3

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