MP86957

Intelli-Phase™ Solution (Integrated HS/LS-FETs and Driver) in 5mmx6mm LGA

DESCRIPTION

The MP86957 is a monolithic half-bridge with built-in internal power MOSFETs and gate drivers. It achieves 70A of continuous output current over a wide input supply range.

The MP86957 is a monolithic IC approach that can drive up to 70A per phase. Integration of drivers and MOSFETs results in high efficiency due to optimal dead time and parasitic inductance reduction. This small 5mmx6mm LGA device can operate from 100kHz to 3MHz.

The MP86957 offers many features to simplify system design. This device works through controllers with a tri-state PWM signal. It also comes with Accu-Sense™ current sense to monitor the inductor current, and temperature sense to report junction temperature.

The MP86957 is ideal for server applications where efficiency and small size are at a premium.

FEATURES

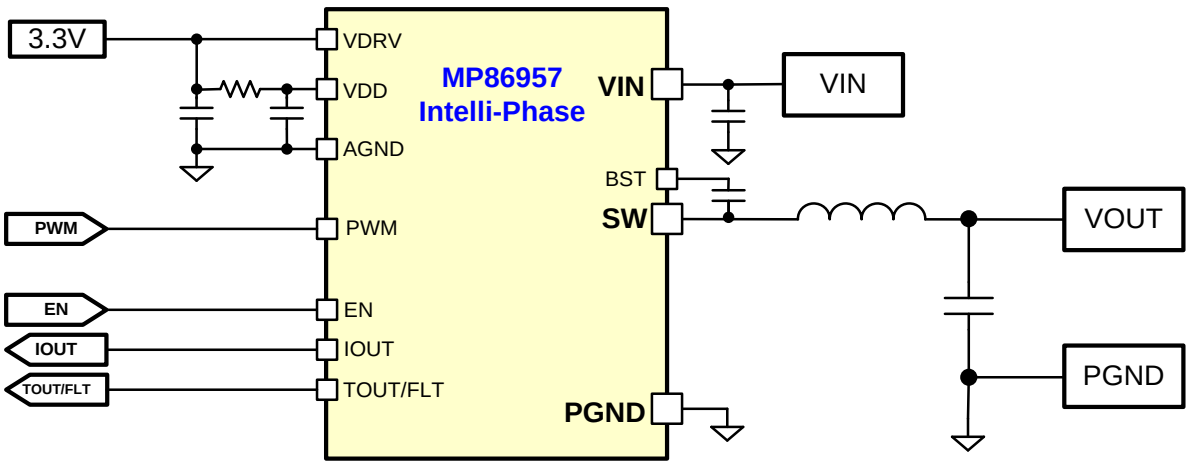
- Wide 3V to 16V Operating Input Range
- 70A Output Current
- Current Sense: Accu-Sense™
- Temperature Sense
- Accepts Tri-State PWM Signal
- Current Limit Fault Flag
- Over-Temperature Fault Flag
- Low-Side Catastrophic Fault Flag and Protection
- Available in a 5mmx6mm LGA Package

APPLICATIONS

- Server Core Voltage
- Graphic Card Core Regulators
- Power Modules

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TYPICAL APPLICATION



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ORDERING INFORMATION

Part Number*	Package	Top Marking
MP86957GMJ	LGA-41 (5mmx6mm)	*See Below*

* For Tape & Reel, add suffix –Z (e.g. MP86957GMJ–Z).

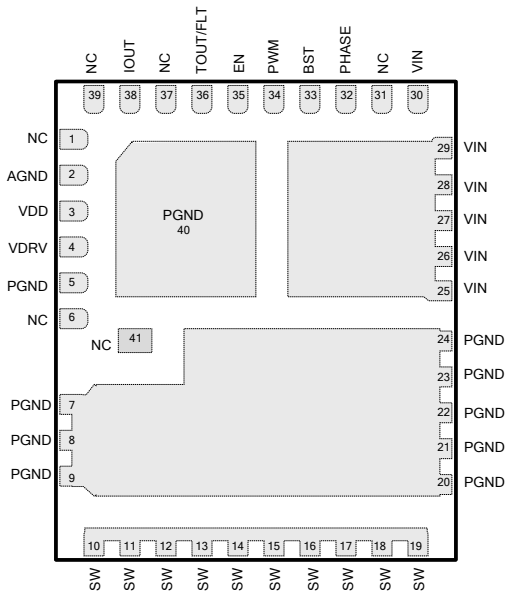
TOP MARKING

MPSYYWW
MP86957
LLLLLLL

MPS: MPS prefix
YY: Year code
WW: Week code
MP86957: Part number
LLLLLLL: Lot number

PACKAGE REFERENCE

TOP VIEW



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PIN FUNCTIONS

Pin #	Name	Description
1, 6, 31, 37, 39, 41	NC	**No connection.**
2	AGND	**Analog ground.**
3	VDD	**Supply voltage for internal circuitry.** Connect to the VDRV pin through a 2.2Ω resistor and decouple with a 1µF capacitor to AGND. Connect AGND and PGND at the VDD capacitor.
4	VDRV	**Driver voltage.** Connect to 3.3V supply and decouple with a 1µF to 4.7µF ceramic capacitor.
5, 7, 8, 9, 20, 21, 22, 23, 24, 40	PGND	**Power ground.**
10, 11, 12, 13, 14, 15, 16, 17, 18, 19	SW	**Phase node.**
25, 26, 27, 28, 29, 30	VIN	**Input supply voltage.** Place input ceramic capacitors (C_{IN}) close to the device to support the switching current with minimal parasitic inductance.
32	PHASE	**Switching node for bootstrap capacitor connection.** PHASE pin is connected to SW internally.
33	BST	**Bootstrap.** Requires a 0.1µF to 0.22µF capacitor to drive the power switch's gate above the supply voltage. Connect the capacitor between PHASE and BST to form a floating supply across the power switch driver.
34	PWM	**Pulse-width modulation input.** Leave PWM floating or drive to mid-state to put SW in high-impedance state.
35	EN	**Enable.** Pull low to disable the device and place SW in a high-impedance state.
36	TOUT/FLT	**Single-pin temperature sense and fault reporting.** When a fault occurs, the pin is pulled up to the VDD voltage.
38	IOUT	**Current sense output.** Use an external resistor to adjust the voltage proportional to the inductor current.

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ABSOLUTE MAXIMUM RATINGS (1)

Supply voltage (V_{IN}) 18V
V_{IN} to $V_{PHASE\ (DC)}$..... -0.3V to 25V
V_{IN} to $V_{PHASE\ (10ns)}$..... -5V to 32V
V_{SW} to $PGND_{(DC)}$.....-0.3 V to V_{IN} + 0.3V
V_{SW} to $PGND_{(25ns)}$ .....-5V to 25V
V_{BST} ..... V_{PHASE} + 4V
V_{DD}, V_{DRV} ..... -0.3V to +4V
All other pins .....-0.3V to V_{DD} + 0.3V
Instantaneous current 95A
Junction temperature .....150°C
Lead temperature .....260°C
Storage temperature..... -65°C to +150°C

Recommended Operating Conditions (2)

Supply voltage (V_{IN}) .....3.0V to 16V
Driver voltage (V_{DRV}) .....3.0V to 3.6V
Logic voltage (V_{DD}).....3.0V to 3.6V
Operating junction temp (T_J)... -40°C to +125°C

Thermal Resistance (3) θ_{JB} θ_{JC_TOP}

LGA- 41 (5mmx6mm) .....2.2 ..... 8.7...°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The device is not guaranteed to function outside of its operating conditions.
3) θ_{JB}: Thermal resistance from junction to board around PGND soldering point.
   θ_{JC_TOP}: Thermal resistance from junction to top of package.

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ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, VDRV = VDD = EN = 3.3V; T_A = 25°C for typical value and T_J = -40°C to +125°C for max and min values, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
I_{IN} shutdown		EN = low		90	180	μA
VIN under-voltage lockout threshold rising				2.5	3.0	V
VIN under-voltage lockout threshold hysteresis				450		mV
I_{VDRV} quiescent current		PWM = low		250	350	μA
I_{VDD} quiescent current		PWM = low		3		mA
VDD voltage UVLO rising				2.75	2.95	V
VDD voltage UVLO hysteresis				300		mV
High-side current limit (4)	I_{LIM_FLT}	Cycle-by-cycle up to 8 cycles		95		A
High-side current limit tolerance (4)			-15%		+15%	
Low-side current limit (4)		Negative current limit, cycle-by-cycle, no fault report		-40		A
Low-side current limit tolerance (4)			-15%		+15%	
Negative current limit low-side off time (4)				200		ns
High-side current limit fault flag counter (4)				8		times
High-side current limit fault flag clear counter (4)				4		times
Dead time at SW rising (4)				2		ns
Dead time at SW falling (4)		Positive inductor current		6		ns
		Negative inductor current		28		ns
EN input high threshold voltage			2.30			V
EN input low threshold voltage					0.8	V
PWM high to SW rising delay (4)	t_{Rising}			20		ns
PWM low to SW falling delay (4)	$t_{Falling}$			20		ns
PWM tri-state to SW Hi-Z delay (4)	t_{LT}			40		ns
	t_{TL}			30		ns
	t_{HT}			40		ns
	t_{TH}			30		ns
Minimum PWM pulse width (4)				30		ns
IOUT sense gain accuracy (4)		20A ≤ ISW ≤ 70A	-2	0	+2	%
IOUT sense gain	G_{IOUT}			5		μA/A

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ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, VDRV = VDD = EN = 3.3V; T_A = 25°C for typical value and T_J = -40°C to +125°C for max and min values, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
IOUT sense offset		I_{SW} = 0A, V_{IOUT} = 1.2V, T_J = 25°C	-2	0	2	µA
		EN = low, V_{IOUT} = 1.2V	-1	0	1	µA
IOUT pin voltage range (4)	V_{IOUT}		0.7		2.1	V
TOUT/FLT sense gain (4)				8		mV/°C
TOUT/FLT sense offset (4)		T_J = 25°C		800		mV
Over-temperature fault flag (4)				145		°C
Over-temperature fault tolerance (4)			-10%		+10%	
Over-temperature fault hysteresis (4)				12		°C
TOUT/FLT when fault (4)			3.0	3.3		V
PWM resistor		Pull up, EN = high		6		kΩ
		Pull down, EN = high		5		kΩ
PWM logic high voltage			2.30			V
PWM tri-state region			1.10		1.80	V
PWM logic low voltage					0.80	V

Note:

4) Guaranteed by design or characterization data, not tested in production.

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PWM TIMING DIAGRAM

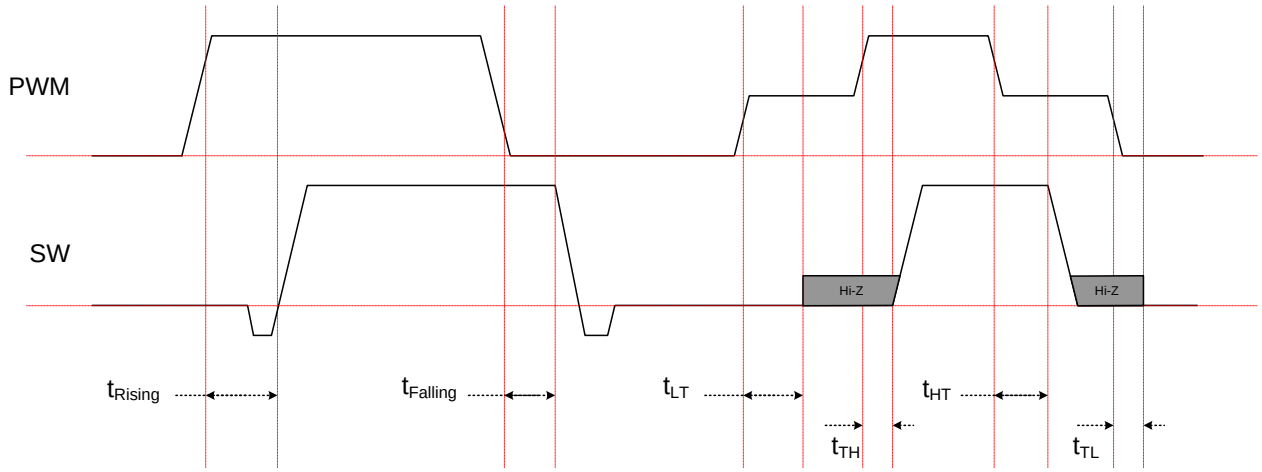


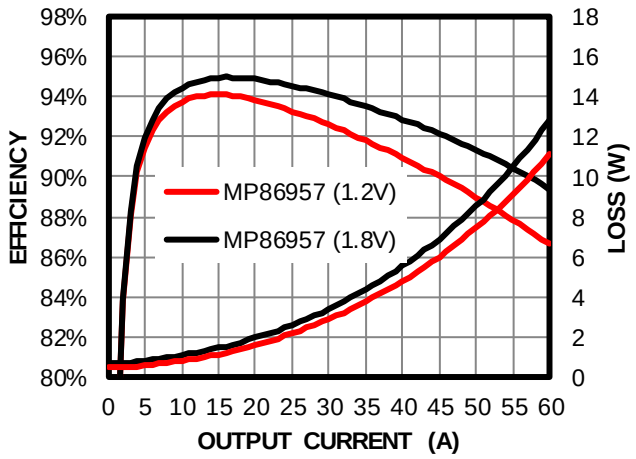
Figure 1: PWM Timing Diagram

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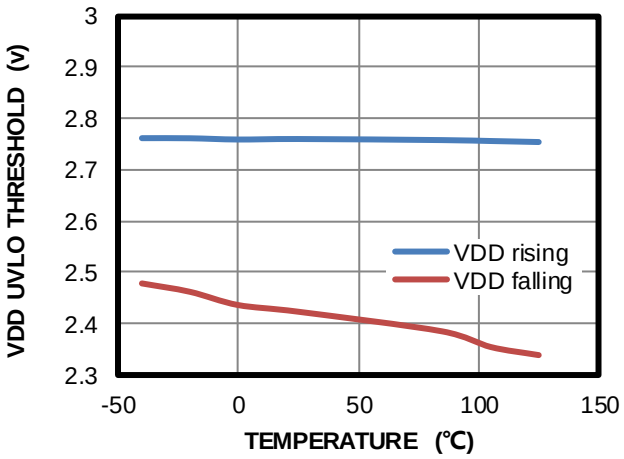
TYPICAL CHARACTERISTICS

Efficiency and Loss

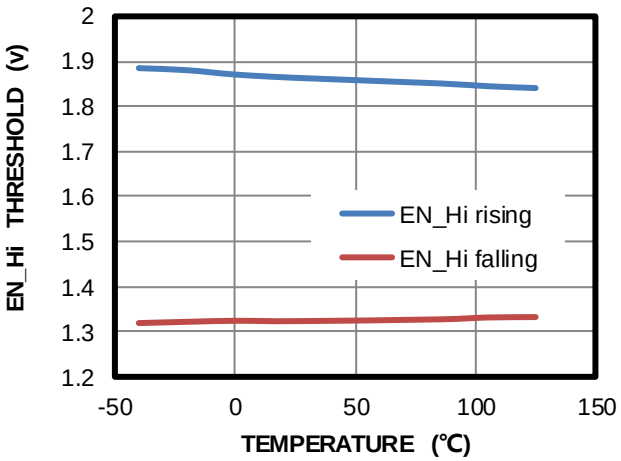
V_{IN} = 12V, L = 150nH, f_{SW} = 500kHz



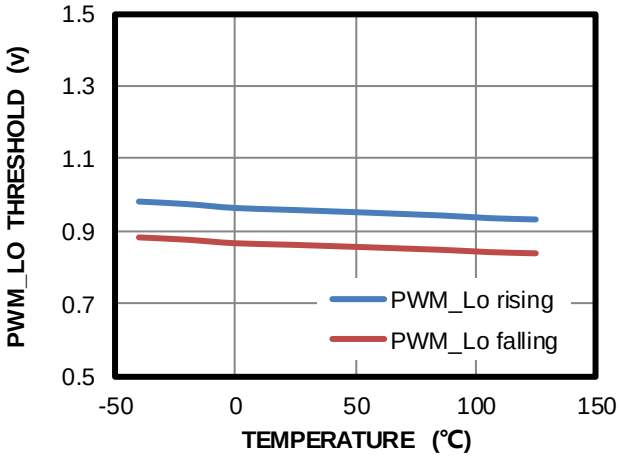
VDD UVLO



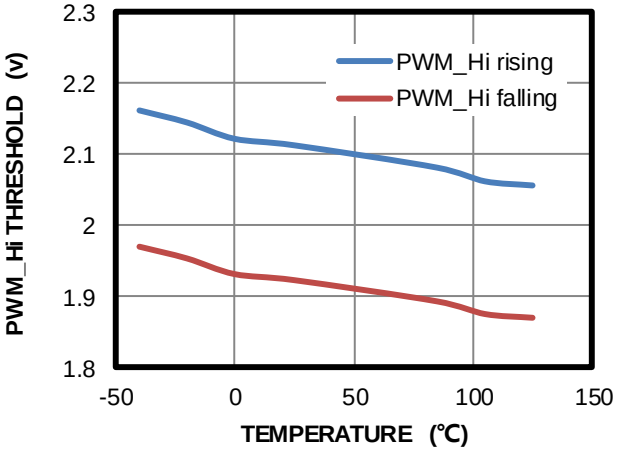
EN_HI



PWM_LO



PWM_HI

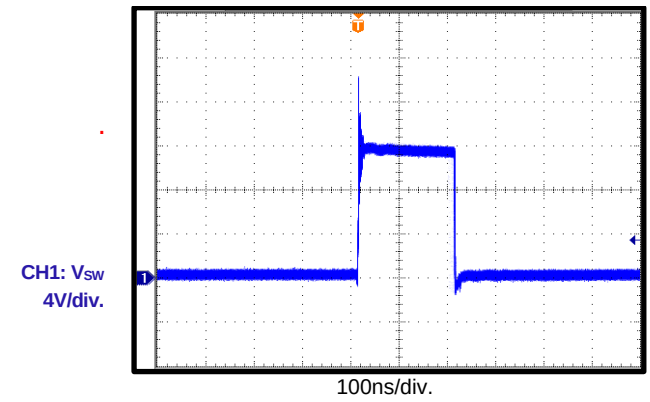


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TYPICAL PERFORMANCE CHARACTERISTICS

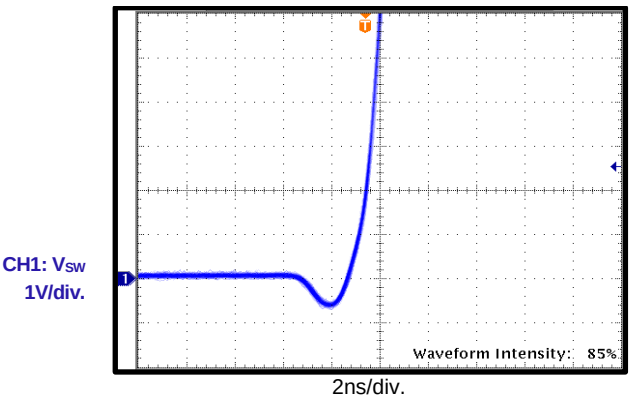
Switching

V_{IN}=12V, V_{OUT}=1.8V, L=100nH, f_{SW}=800kHz, Load=30A



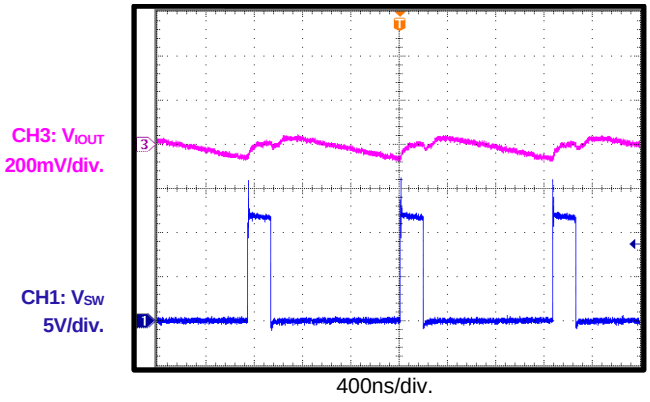
Dead Time @ SW Ringing

Load = 30A



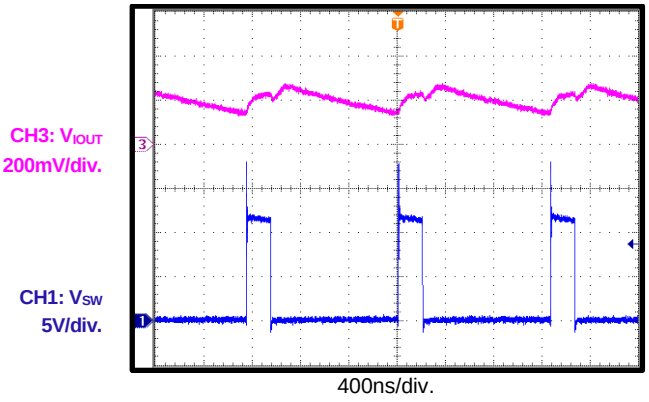
IOUT Output

Load = 0A



IOUT Output

Load = 30A



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FUNCTIONAL BLOCK DIAGRAM

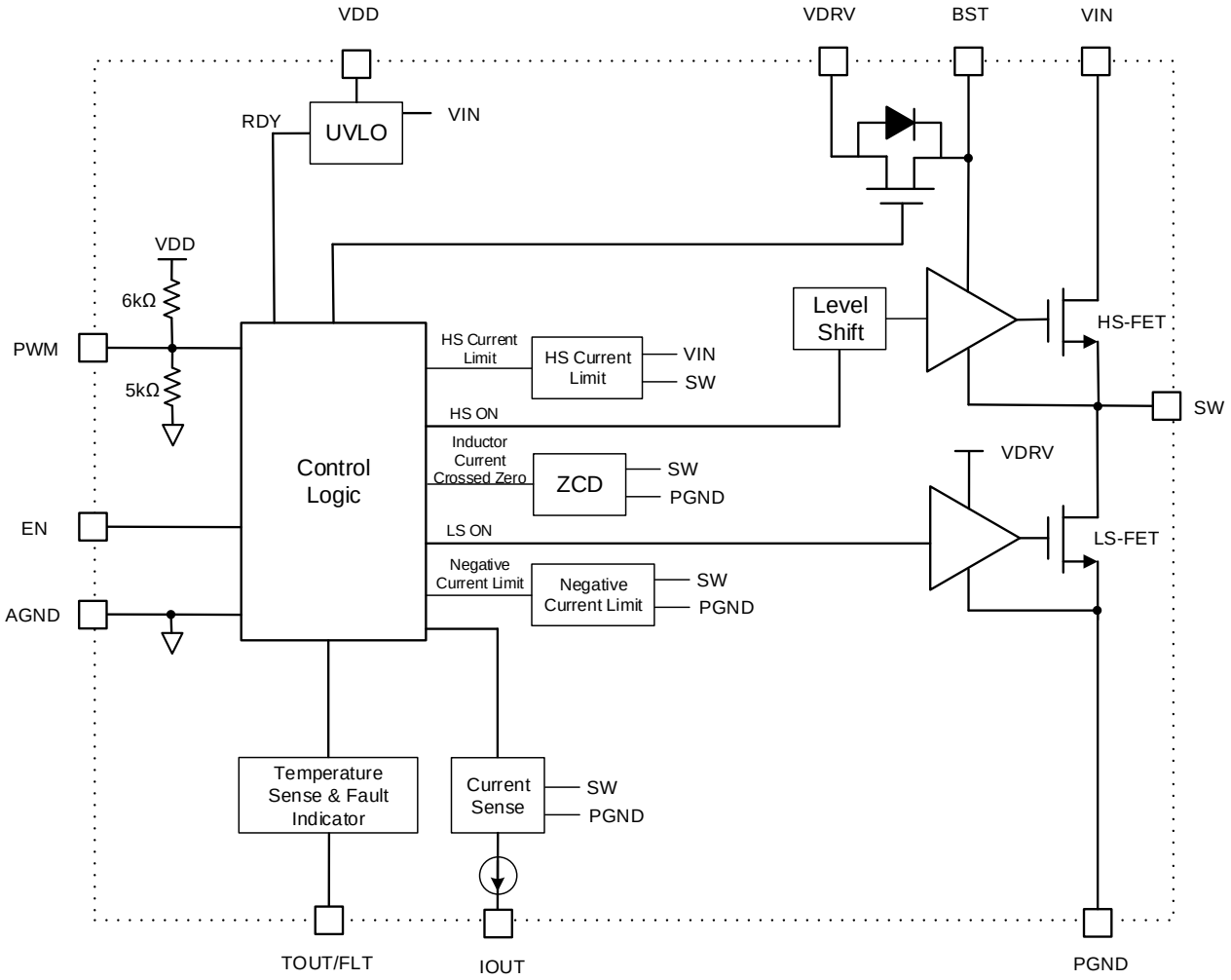


Figure 2: Functional Block Diagram

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OPERATION

The MP86957 is a 70A, monolithic half-bridge driver with MOSFETs ideally suited for multiphase buck regulators.

An external 3.3V is required to supply both VDD and VDRV.

When EN transitions from low to high and the VDD and VDRV signals are sufficiently high, operation begins.

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APPLICATION INFORMATION

PWM

The PWM input pin is capable of tri-state input. When the PWM input signal is within the tri-state threshold window for 40ns (typical), THT or TLT, the high-side MOSFET (HS-FET) turns off immediately and the low-side MOSFET (LS-FET) remains in diode emulation mode until zero current detection. The tri-state PWM input can be from a forced middle voltage PWM signal. Alternately, the PWM input can be floated and the internal current source will charge the signal to a middle voltage. The PWM timing diagram shows the propagation delay definition from PWM to the SW node (see Figure 1).

Place a resistor divider (e.g. 1.2kΩ to VDD and 1kΩ to GND) at the PWM pin to anticipate when the controller's PWM tri-state enters Hi-Z (High impedance) mode. This function prevents the LS-FET from turning on if the TOUT/FLT signal is pulled up after a fault occurs and the controller responds the fault and shuts down by placing PWM to HiZ mode. The PWM pin does not require a resistor divider if the controller's PWM tri-state is at a middle voltage.

Diode Emulation Mode

In diode emulation mode, when PWM is at either low or tri-state input, the LS-FET turns on whenever the inductor current is positive. The LS-FET is off if the inductor current is negative or after it has crossed zero current. Diode emulation mode can be enabled by:

1. Driving PWM to middle state
2. Floating the PWM pin

Current Sense

The IOUT pin is a bi-directional current source proportional to the inductor current. The current sensing gain is 5μA/A, and a resistor is used to program the voltage gain proportional to the inductor current if needed.

The IOUT pin output has two states (see Table 1). In disable mode (EN = low), the current sense circuit is disabled and IOUT is in Hi-Z (high-impedance) state.

Table 1: IOUT Output States

PWM	EN	IOUT
PWM	High	Active
x	Low	Hi-Z

The IOUT pin voltage range of 0.7V to 2.1V is required to get IOUT's accurate current output. In general, there is a resistor (R_{IOUT}) connected from IOUT to an external voltage, which is capable of sinking a small current to provide enough voltage to meet the required operating voltage range. Determine a proper reference voltage (V_{CM}) and/or R_{IOUT} value using Equation (1) and Equation (2):

$$0.7V < I_{IOUT} \times R_{IOUT} + V_{CM} < 2.1V \quad (1)$$

$$I_{IOUT} = I_{SW} \times G_{IOUT} \quad (2)$$

Where V_{CM} is a reference voltage connected to R_{IOUT}.

The Intelli-Phase™ current sense output can be used to accurately monitor the output current. The cycle-by-cycle current information from IOUT can be used for phase current balancing, over-current protection, and active voltage positioning (output voltage droop).

Positive and Negative Inductor Current Limit

When HS-FET over-current is detected, the HS-FET on-pulse is truncated for that PWM cycle. If an HS current limit event is detected for eight consecutive cycles, the TOUT/FLT pin is pulled high to VDD, during which time the driver continues responding to PWM. Once four consecutive normal cycles are detected, TOUT/FLT is cleared.

When the LS-FET detects a -40A valley current, the part turns off the LS-FET and turns on the HS-FET for 200ns to limit the negative current. The LS-FET negative current limit will not trigger a fault report.

Over-Temperature Fault Flag

If the junction temperature rises above 145°C, TOUT/FLT is pulled to VDD, during which time the driver continues responding to PWM. Once the junction temperature falls below 133°C, the fault flag clears.

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Low-Side Catastrophic Failure Protection

If the HS-FET V_{DS} is greater than 0.7V when the HS-FET is on, the low-side catastrophic failure protection is triggered. The MP86957 stops responding to PWM and latches, and TOUT/FLT is pulled high immediately. After 200ns, the PWM impedance becomes 10k to GND. The MPS multiphase controller can detect this impedance and record which phase experiences this failure.

This fault latch can be released by toggling EN or recycling VDD/VIN.

Temperature Sense Output with Fault Indicator (TOUT/FLT)

TOUT/FLT reports junction temperature. It sources a voltage proportional to the junction temperature when V_{DD} is higher than the UVLO threshold. The gain is 8mV/°C, and the offset is +800mV at 25°C. TOUT pins from multi-phase topologies can be tied together to report the highest TMON signals to the controller.

TOUT/FLT are pulled to VDD when a fault event is detected. It reports three fault events: HS-FET over-current limit, over-temperature, low-side catastrophic failure.

For multiphase operation, connect TOUT/FLT of each Intelli-Phase™ together (see Figure 3).

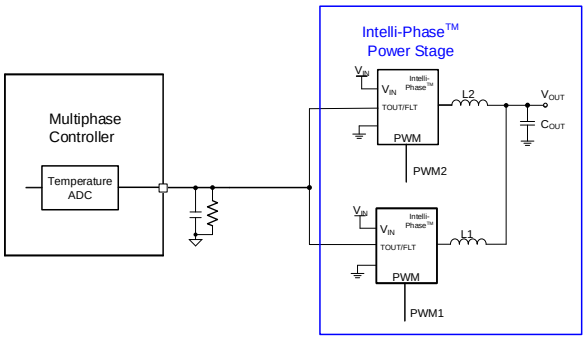


Figure 3: Multiphase Temperature Sense Utilization

PCB Layout Guidelines

PCB layout plays an important role in achieving stable operation. For optimal performance, refer to Figure 4 and follow the guidelines below:

1. Place the input MLCC capacitors as close to VIN and PGND as possible. The major MLCC capacitors should be placed on the same layer as the MP86957.
2. Place as many VIN and PGND vias underneath the package as possible, in-between VIN or PGND long pads.
3. Place a VIN copper plane on the second inner layer to form the PCB stacking in a +/-/+ pattern to reduce the parasitic impedance from the input MLCC cap to the MP86957. The copper plane on inner layer must at least cover the VIN vias underneath the package and the input MLCC capacitors.
4. Place more PGND vias close to the PGND pin/pad to minimize parasitic resistance and impedance, as well as thermal resistance.
5. Place the BST and VDRV capacitors as close to the device's pins as possible. Use a ≥20 mil width trace to route the path. Avoid the via for the BST driving path. It is recommended to use 0.1µF to 0.22µF for the bootstrap capacitor.
6. Place the VDD decoupling capacitor close to the device. Connect AGND and PGND at the point of the VDD capacitor's ground connection.
7. Keep the IOUT signal trace away from high-current paths, such as SW and PWM.

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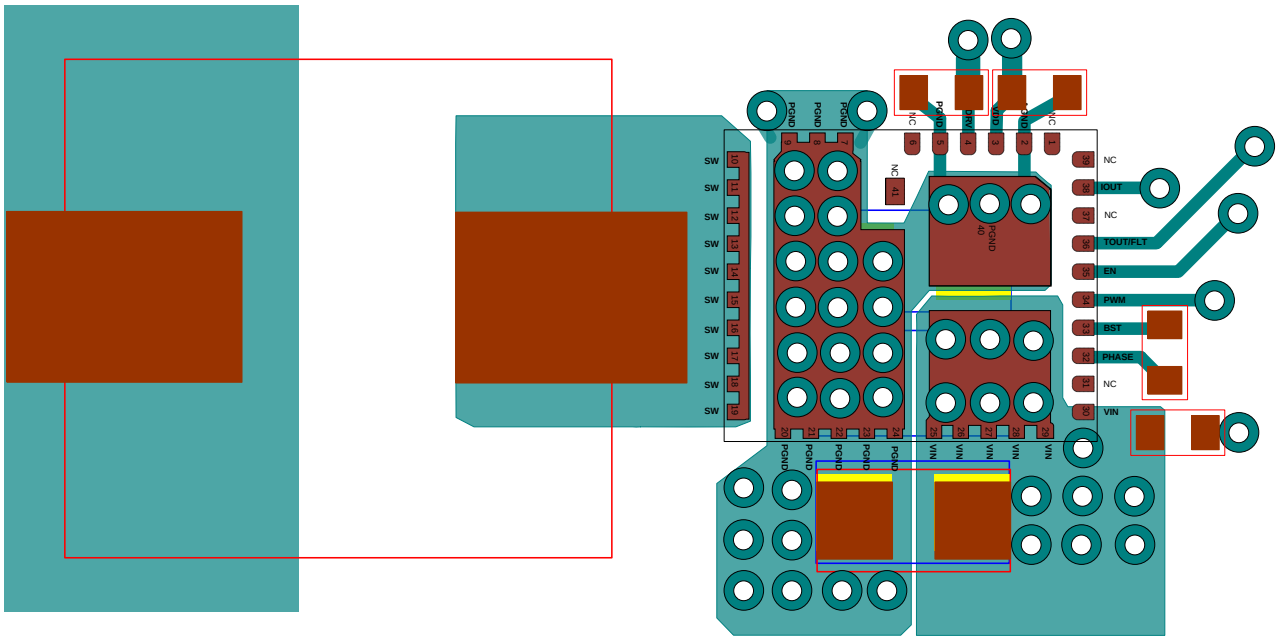


Figure 4: Example of PCB Layout (Placement & Top layer PCB)

Input Capacitor: 0805 package (top side & bottom side) & 0402 package (Top side)

Inductor: 11x8 package

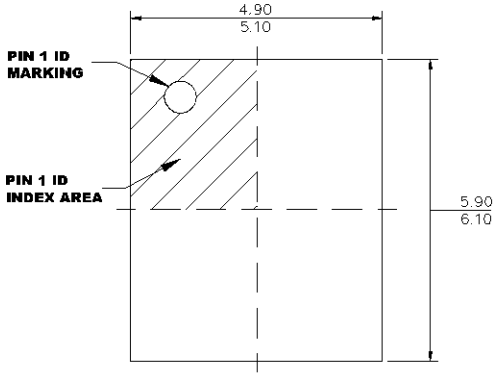
VDD/BST/VDRV Capacitor: 0402 package

Via Size: 20/10 mils

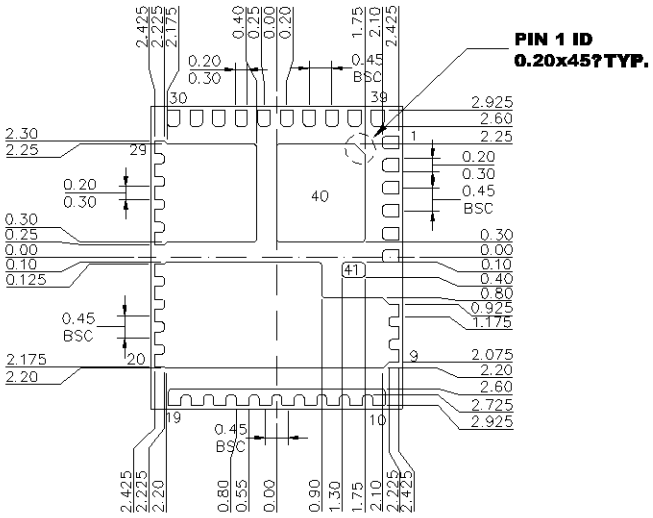
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PACKAGE INFORMATION

LGA-41 (5mmx6mm)



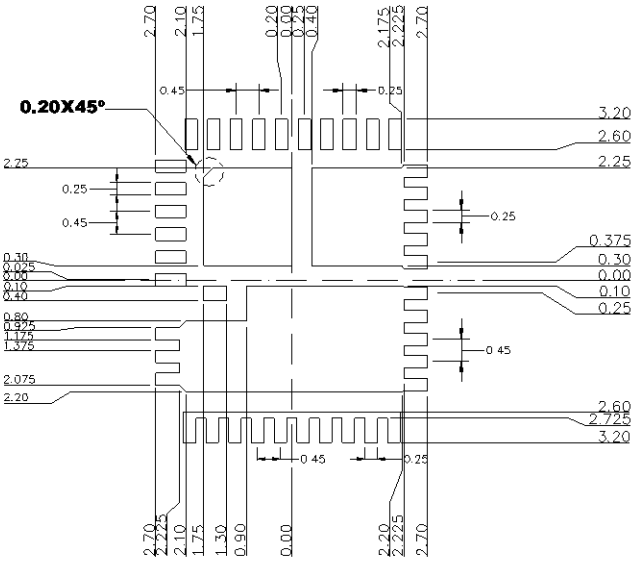
TOP VIEW



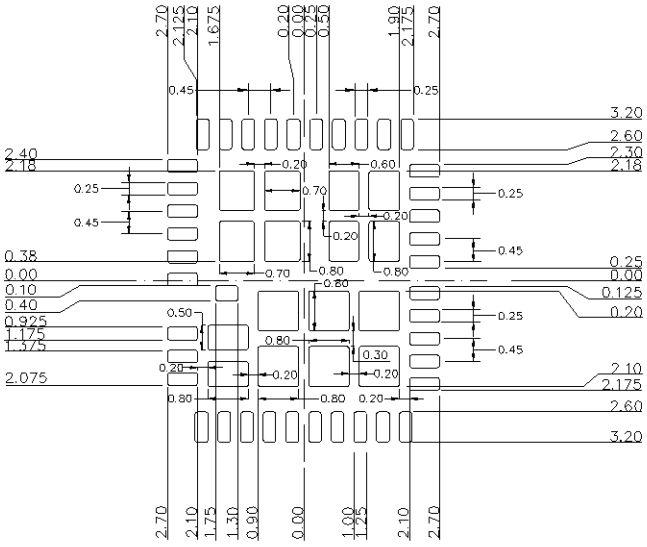
BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN



RECOMMENDED STENCIL DESIGN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
3) JEDEC REFERENCE IS MO-303.
4) DRAWING IS NOT TO SCALE.

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Revision History

Revision #	Revision Date	Description	Pages Updated
1.0	05/08/2019	Initial Release	-
1.1	07/08/2020	Update the descriptions for pin 32.	3
		Add (V_{IN} to V_{PHASE}) to Absolute Maximum Ratings	4
		Update recommended operating conditions for V_{IN} from 3.0V to 16V	4
		Update the typical dead-time for negative inductor current at SW falling edge to 28ns	5
		Update the typical propagation delay from PWM to SW	5
		Update the typical minimum PWM pulse width to 30ns	5
		Add Typical Characteristics for threshold of EN, PWM and VDD UVLO	8
		Update typical performance characteristics	9
		Update the application information for PWM section	12
		Update Figure 3	13
		Correct the BST capacitor's capacitance to 0.22µF	13
		Update the recommended Land Pattern and Stencil Design	15
		Add revision history page	16

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