MP9485

100V Input, 500mA, Step-Down Converter

The Future of Analog IC Technology

DESCRIPTION

The MP9485 is a high-voltage, step-down, switching regulator that delivers up to 0.5A of current to the load. It integrates a high-side, high-voltage power MOSFET with a current limit of 1.0A, typically. The wide 4.5V to 100V input range accommodates a variety of step-down applications, making it ideal for automotive, industry, and lighting applications. Hysteretic voltage-mode control is employed for very fast response. MPS's proprietary feedback control scheme minimizes the number of required external components.

The switching frequency can be up to 2MHz, allowing for small component size. Thermal shutdown and short-circuit protection (SCP) provide reliable and fault-tolerant operations. A 170µA quiescent current allows the MP9485 to be used in battery-powered applications.

The MP9485 is available in a SOIC-8 package with an exposed pad.

FEATURES

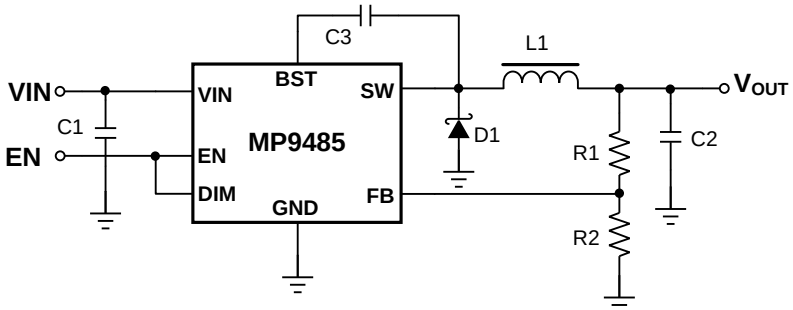
- Wide 4.5V to 100V Input Range
- Hysteretic Control: No Compensation
- Up to 2MHz Switching Frequency
- PWM Dimming Control Input for LED Application
- Short-Circuit Protection (SCP) with Integrated High-Side MOSFET
- 170µA Quiescent Current
- Thermal Shutdown
- Available in a SOIC-8 Package with an Exposed Pad

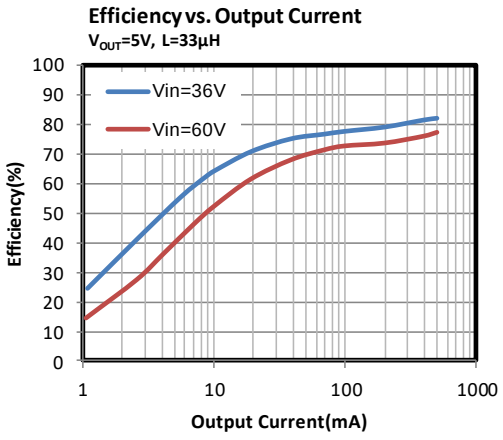
APPLICATIONS

- E-Bike Control Power Supplies
- Solar Energy Systems
- Automotive System Power
- Industrial Power Supplies
- High-Power LED Drivers

All MPS parts are lead-free, halogen-free, and adhere to the RoHS directive. For MPS green status, please visit the MPS website under Quality Assurance. "MPS" and "The Future of Analog IC Technology" are registered trademarks of Monolithic Power Systems, Inc.

TYPICAL APPLICATION





MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2019 MPS. All Rights Reserved.

ORDERING INFORMATION

Part Number*	Package	Top Marking
MP9485GN	SOIC-8 EP	*See Below*

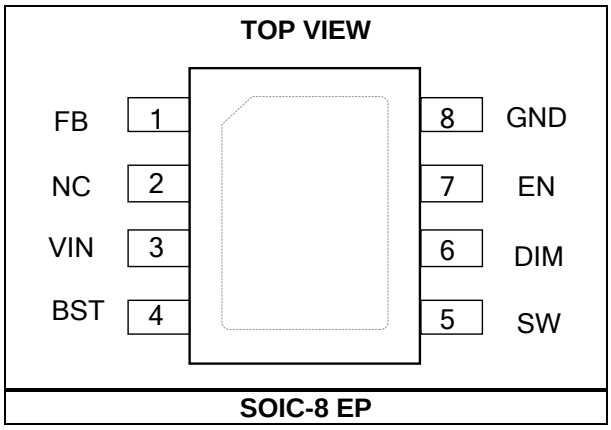
***** For Tape & Reel, add suffix –Z (e.g. MP9485GN–Z)

TOP MARKING

MP9485
LLLLLLLL
MPSYWW

MP9485: Product code of MP9485GN
LLLLLLLL: Lot number
MPS: MPS prefix
Y: Year code
WW: Week code

PACKAGE REFERENCE



MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2019 MPS. All Rights Reserved.

ABSOLUTE MAXIMUM RATINGS (1)

Supply voltage (VIN) ..... -0.3V to +100V
Switch voltage (V_{SW}) ..... -0.5V (-4V for <10ns) to V_{IN} + 0.5V
BST to SW ..... -0.3V to +6V
All other pins ..... -0.3V to +6V
Junction temperature ..... 150°C
Continuous power dissipation (T_A = +25°C) (2) 2.5W
Lead temperature ..... 260°C
Storage temperature ..... -65°C to +150°C

Recommended Operating Conditions (3)

Supply voltage (VIN) ..... 4.5V to 95V
EN and DIM voltages ..... 0V to 5V
Max switching frequency 2MHz
Operating junction temp. ..... -40°C to +125°C

Thermal Resistance (4)	θ_{JA}	θ_{JC}	
SOIC-8 EP	50	10	°C/W

NOTES:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J(MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by $P_D(MAX)=(T_J(MAX)-T_A)/\theta_{JA}$. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7 4-layer board.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2019 MPS. All Rights Reserved.

ELECTRICAL CHARACTERISTICS

V_{IN} = 60V, T_A = +25°C, unless otherwise noted. Specifications over temperature are guaranteed by design and characterization.

Parameter	Symbol	Condition	Min	Typ	Max	Units
VIN UVLO threshold			3.6	4.0	4.4	V
VIN UVLO hysteresis				0.4		V
Shutdown supply current		V_{EN} = 0V		2	5	µA
Quiescent supply current		No load, V_{FB} = 250mV		170	220	µA
Upper switch on resistance (5)	$R_{DS(ON)}$	V_{BST} - V_{SW} = 5V		500		mΩ
Upper switch leakage current	I_{SWLK}	V_{EN} = 0V, V_{SW} = 0V		0.01	1	µA
Current limit	I_{PK}	V_{FB} = 0.15V	0.75			A
EN up threshold	V_{ENH}		1.4	1.55	1.7	V
EN threshold hysteresis	V_{ENHY}			320		mV
EN input current	I_{ENI}	V_{EN} = 5V		0.01	1	µA
EN sinking current	I_{ENS}	V_{EN} = 2V		2	3	µA
DIM up threshold	V_{DIMH}		0.8	1.15	1.5	V
DIM threshold hysteresis	V_{DIMHY}			300		mV
DIM input current	I_{DIM}	V_{DIM} = 5V or 0V	-1		1	µA
DIM on propagation delay	T_{DIMDH}	V_{FB} = 0V, V_{DIM} rising edge to V_{SW} rising edge		50		ns
DIM off propagation delay	T_{DIMDL}	V_{FB} = 0V, V_{DIM} falling edge to V_{SW} falling edge		50		ns
FB voltage threshold high (5)	V_{FBH}	4.5V < VIN < 95V, V_{FB} rising from 0V until V_{SW} < 30V	209	215	221	mV
FB voltage threshold low (5)	V_{FBL}	4.5V < VIN < 95V, V_{FB} falling from 0.25V until V_{SW} > 30V	179	185	191	mV
FB input current	I_{FB}	V_{FB} = 5V or 0V	-300		300	nA
FB propagation delay to output high	T_{FBDH}	Falling edge of V_{FB} from 0.25V to 0V to V_{SW} rising edge		100		ns
FB propagation delay to output high	T_{FBDL}	Rising edge of V_{FB} from 0V to 0.25V to V_{SW} falling edge		100		ns
Thermal shutdown (6)		Hysteresis = 20°C		150		°C

NOTES:

5) Guaranteed by design, not tested.
6) Guaranteed by characterization, not production tested.

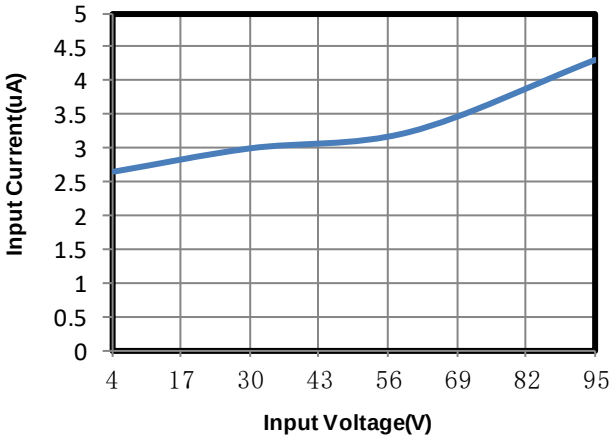
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2019 MPS. All Rights Reserved.

TYPICAL ELECTRICAL CHARACTERISTICS

V_{IN} = 60V, T_A= +25°C, unless otherwise noted.

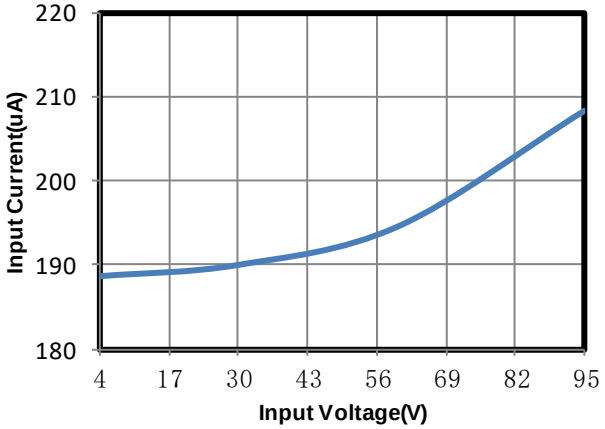
Shutdown Current vs. Input Voltage

EN=LOW



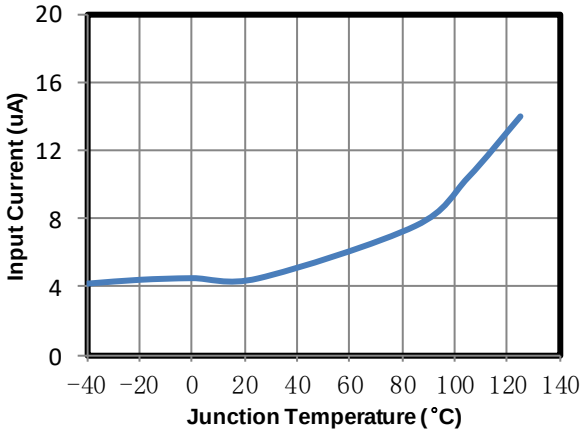
Quiesvent Current vs. Input Voltage

EN=HIGH, DIM=LOW, V_{FB}=250mV



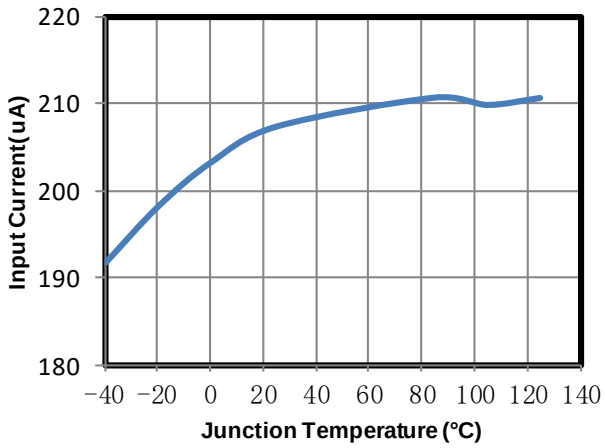
Shutdown Current vs. Temperature

V_{IN}=95V, EN=LOW

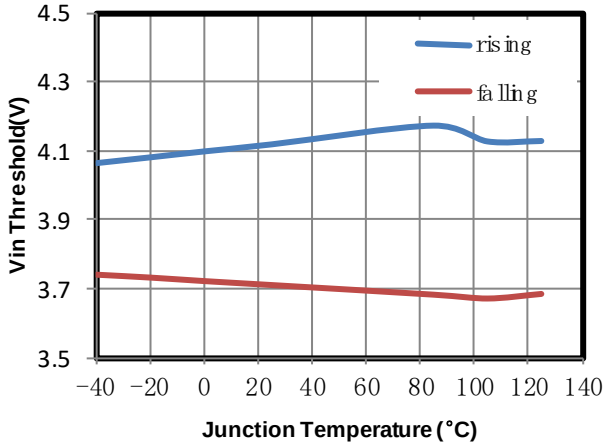


Quiescent Current vs. Temperature

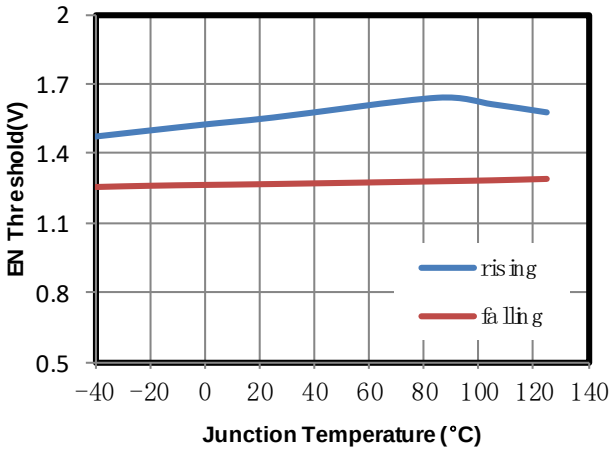
V_{IN}=95V, DIM=LOW,EN=HIGH,V_{FB}=250mV



UVLO Threshold vs. Temperature



EN Threshold vs. Temperature

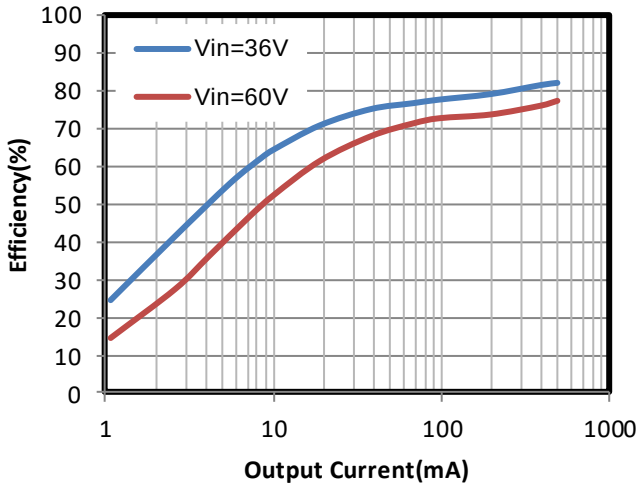


MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2019 MPS. All Rights Reserved.

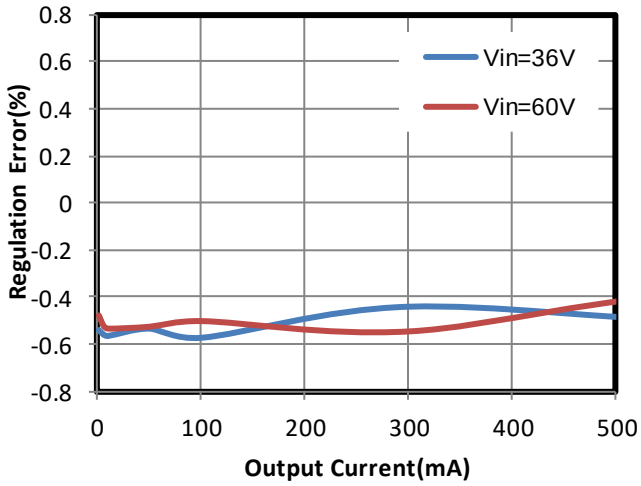
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 60V, V_{OUT} = 5V, I_{OUT} = 1A, L=33µH, C_{OUT} = 100µF, T_A= +25°C, unless otherwise noted.

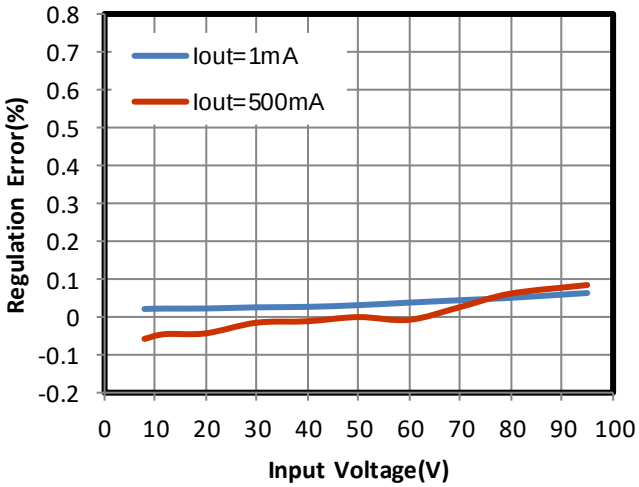
Efficiency vs. Output Current



Load Regulation



Line Regulation



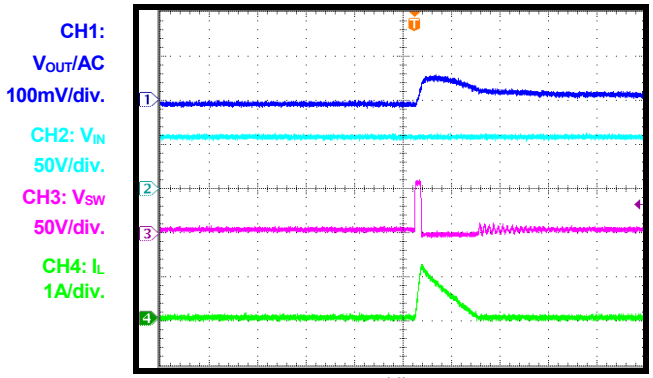
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2019 MPS. All Rights Reserved.

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 60V, V_{OUT} = 5V, I_{OUT} = 1A, L=33µH, C_{OUT} = 100µF, T_A= +25°C, unless otherwise noted.

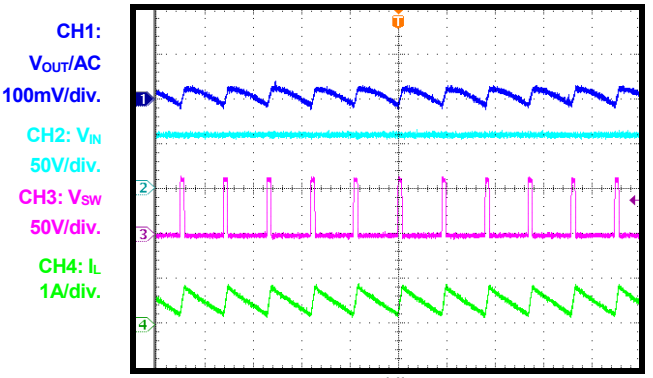
Steady State

I_{OUT}=0A



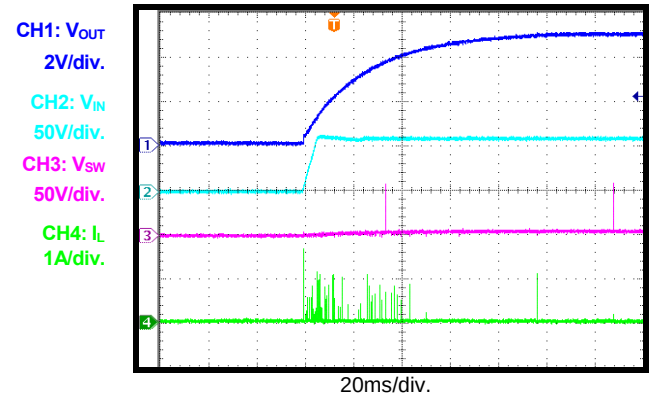
Steady State

I_{OUT}=0.5A



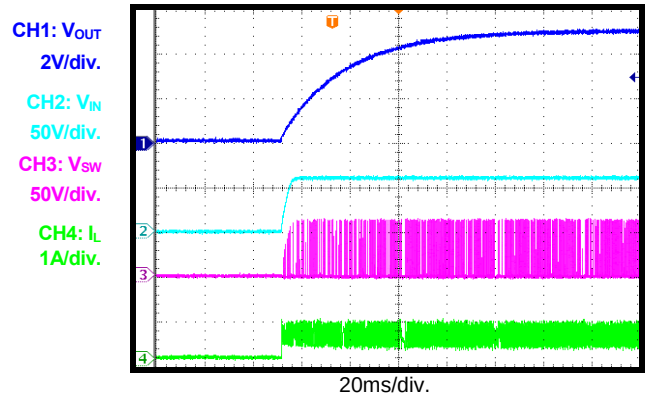
Power On

I_{OUT}=0A



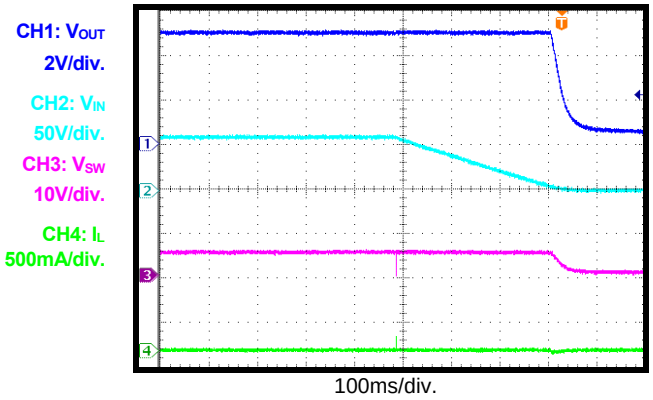
Power On

I_{OUT}=0.5A



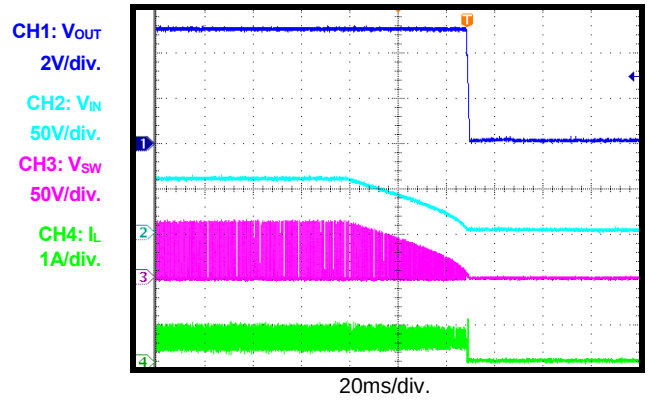
Power Off

I_{OUT}=0A



Power Off

I_{OUT}=0.5A



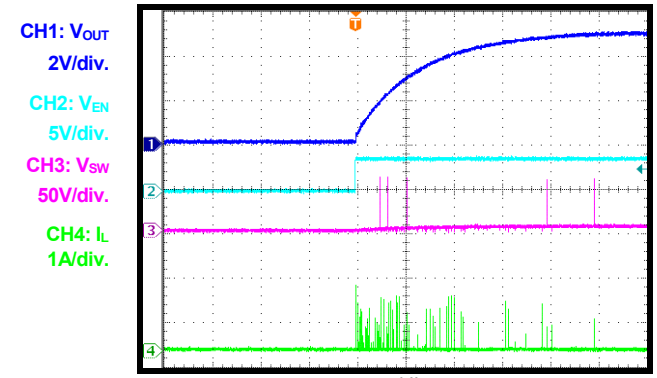
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2019 MPS. All Rights Reserved.

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 60V, V_{OUT} = 5V, I_{OUT} = 1A, L=33µH, C_{OUT} = 100µF, T_A= +25°C, unless otherwise noted.

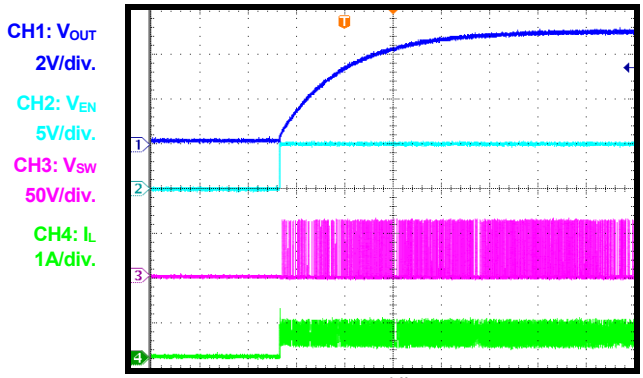
EN Start-Up

I_{OUT}=0A



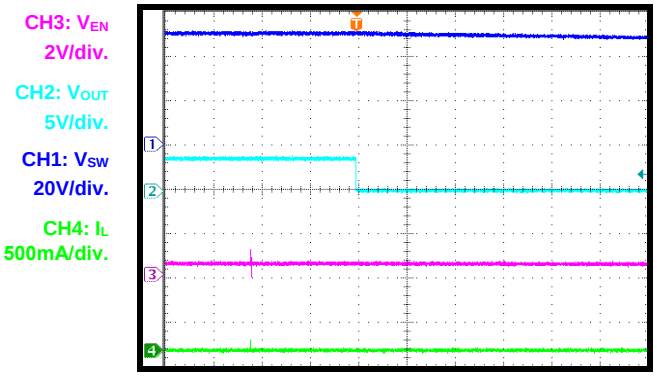
EN Start-Up

I_{OUT}=0.5A



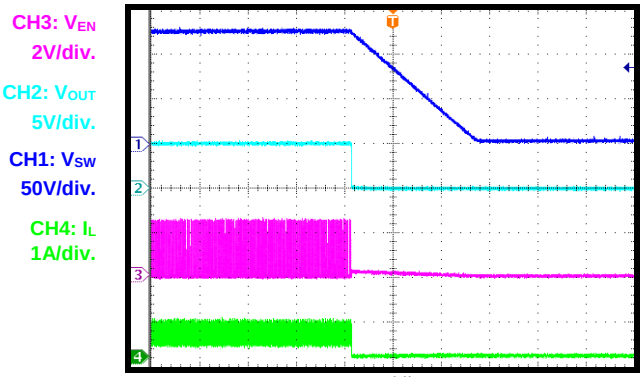
EN Shutdown

I_{OUT}=0A



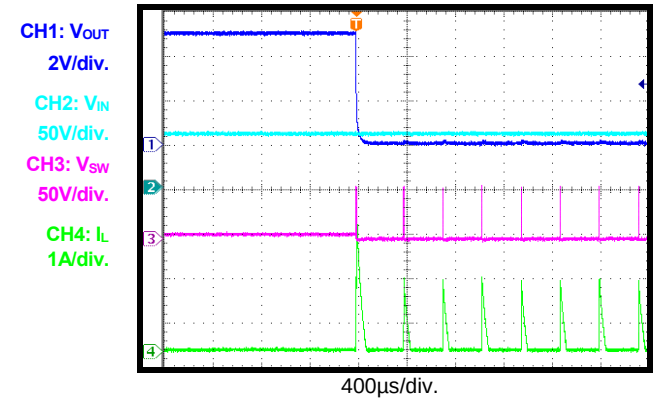
EN Shutdown

I_{OUT}=0.5A



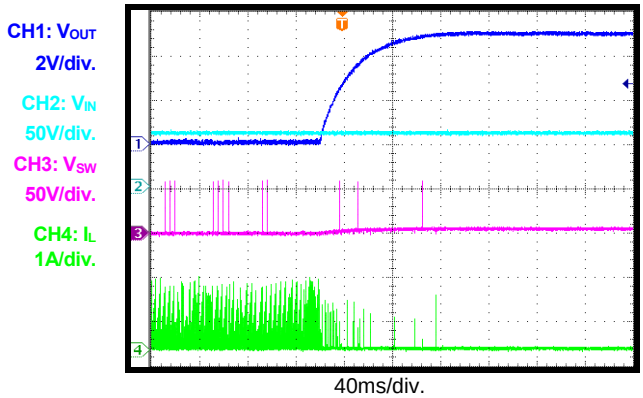
SCP Entry

I_{OUT}=0A



SCP Recovery

I_{OUT}=0A



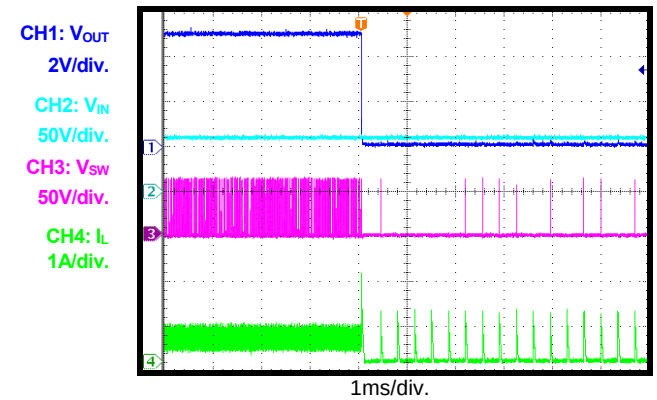
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2019 MPS. All Rights Reserved.

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 60V, V_{OUT} = 5V, I_{OUT} = 1A, L=33µH, C_{OUT} = 100µF, T_A= +25°C, unless otherwise noted.

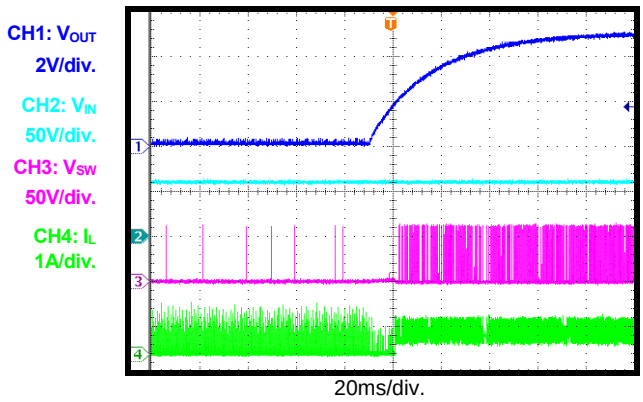
SCP Entry

I_{OUT}=0.5A



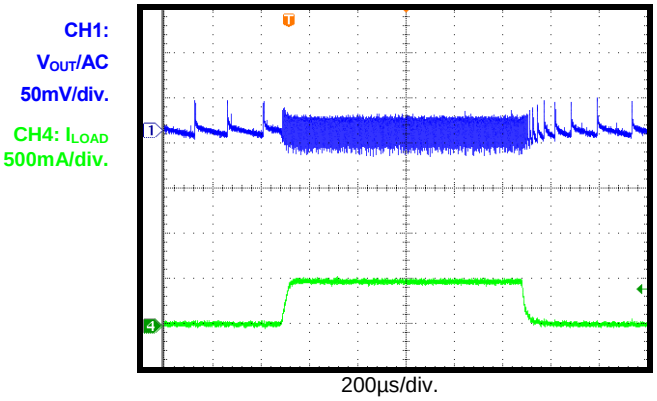
SCP Recovery

I_{OUT}=0.5A, E-load turn-on Threshold=0.32V



Load Transient

I_{OUT}=0A-->0.5A



MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2019 MPS. All Rights Reserved.

PIN FUNCTIONS

SOIC-8 EP Pin #	Name	Description
1	FB	**Feedback.** FB is the input to the voltage feedback hysteretic comparator.
2	NC	**No connection.** NC is not connected.
3	VIN	**Input supply.** VIN supplies power to all of the internal control circuitries, both BST regulators, and the high-side switch. A decoupling capacitor to ground must be placed close to VIN to minimize switching spikes.
4	BST	**Bootstrap.** BST is the positive power supply for the internal, floating, high-side MOSFET driver. Connect a bypass capacitor between BST and SW.
5	SW	**Switch node.** SW is the output from the high-side switch. A low forward voltage (V_F) Schottky rectifier to ground is required. The rectifier must be placed close to SW to reduce switching spikes.
6	DIM	**PWM dimming input.** DIM is useful in LED driver applications. Pull DIM below the specified threshold for dimming off; pull DIM above the specified threshold for dimming on. If there is no need for a dimming function, such as in common buck applications, then connect DIM and EN together.
7	EN	**Enable input.** Pull EN below the specified threshold to shut down the MP9485; pull EN above the specified threshold or leave EN floating to enable the MP9485.
8	GND	**Ground.** GND should be placed as close to the output capacitor as possible to avoid the high-current switch paths. Connect the exposed pad to the GND plane for optimal thermal performance.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2019 MPS. All Rights Reserved.

BLOCK DIAGRAM

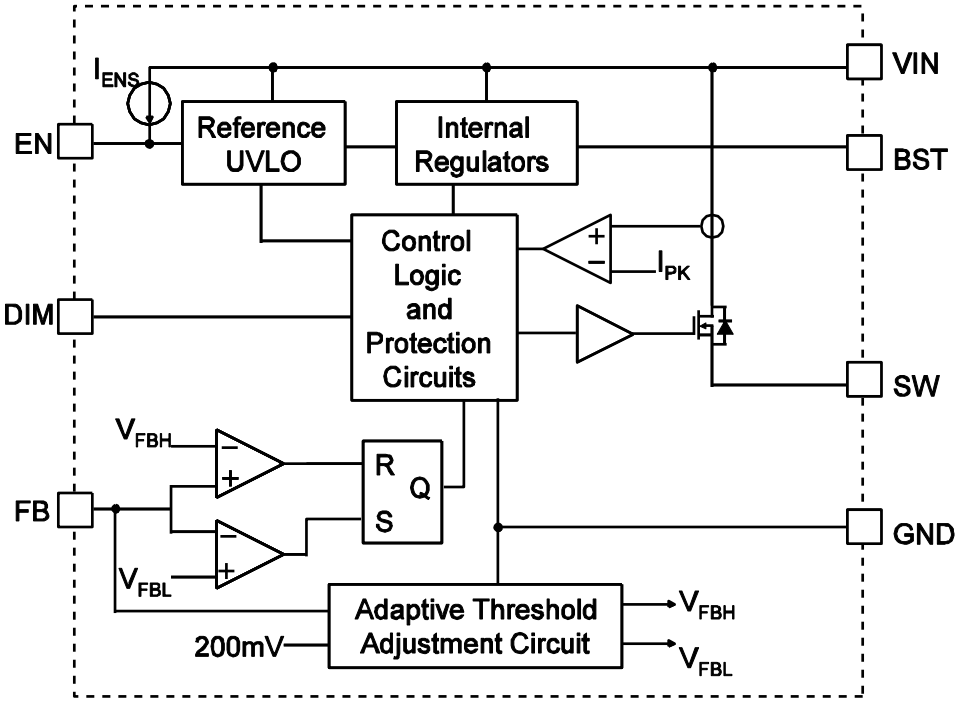


Figure 1: Functional Block Diagram

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2019 MPS. All Rights Reserved.

OPERATION

Hysteresis Current Control with Adaptive Threshold Adjustment

The MP9485 operates in a hysteretic voltage-mode control to regulate the output voltage. FB is connected to the tap of a resistor divider, which determines the output voltage. The power MOSFET is turned on and remains on until FB rises to 215mV. The power MOSFET is turned off and remains off until FB falls to 185mV. The two thresholds of 215mV and 185mV are adaptively adjusted to compensate for all the circuit delays so that the output voltage is regulated with an average 200mV value at FB.

Enable (EN) Control

The MP9485 has a dedicated enable control pin (EN) with positive logic. Its falling threshold is 1.23V, and its rising threshold is 1.55V (320mV higher).

When floating, EN is pulled up to about 3.0V by an internal 2μA current source, so it is enabled. A current capability over 2μA is needed to pull EN down.

Floating Driver and Bootstrap Charging

The floating power MOSFET driver is powered by an external bootstrap capacitor. This floating driver has its own UVLO protection. This UVLO's rising threshold is 2.2V with a threshold of 150mV.

The bootstrap capacitor is charged and regulated at about 5V by the dedicated internal bootstrap regulator.

If the internal circuit does not have sufficient voltage, and the bootstrap capacitor is not sufficiently charged, extra external circuitry can be used to ensure that the bootstrap voltage is in the normal operating region. Refer to the External Bootstrap Diode section on page 12 for more detail.

Under-Voltage Lockout (UVLO)

Under-voltage lockout (UVLO) is implemented to protect the chip from operating at an insufficient supply voltage. The UVLO rising threshold is about 4.0V, while its falling threshold is a consistent 3.6V.

Dimming Function for LED Applications

Because the FB reference of the MP9485 is very low, it is a good idea for the LED driver to have the LED current sense resistor connected between FB and GND. In such applications, the MP9485 uses DIM for dimming. To achieve dimming, apply a pulse on DIM. The high level of the pulse should be >1.5V, and the low level should be <0.5V. The frequency can be as high as 20kHz.

Thermal Shutdown

Thermal shutdown is implemented to prevent the chip from operating at exceedingly high temperatures. When the silicon die temperature is higher than its upper threshold, the entire chip shuts down. When the temperature is lower than its lower threshold, the chip is enabled again.

Output Short Protection

The output voltage is well-regulated when the FB voltage is around 200mV. If the output is pulled low in over-current protection (OCP) or is shorted to GND directly, the FB voltage is low, even though the power MOSFET is turned on. The power MOSFET is shut off if the failure time is longer than 10μs. The MP9485 attempts the operation again after a delay of about 300μs.

The power MOSFET current is also accurately sensed via a current sense MOSFET. If the current is over the current limit, the IC is shut down. This offers extra protection under output-short conditions.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2019 MPS. All Rights Reserved.

APPLICATION INFORMATION

Setting the Output Voltage

The output voltage (V_{OUT}) is set by a divider resistor (R1 and R2) (see the Typical Application on page 1). To achieve good noise immunity and low power loss, R2 is recommended to be in the range of 5kΩ to 50kΩ. R1 can then be determined with Equation (1):

$$R1 = \frac{V_{OUT} - V_{FB}}{V_{FB}} \times R2 \quad (1)$$

Where V_{FB} = 0.2V, typically.

Output Capacitor and Frequency Setting

The output capacitor (C_{OUT}) is necessary to achieve a smooth output voltage. The ESR of the capacitor should be sufficiently large compared to the capacitance; otherwise, the system may behave in an unexpected way, and the current ripple may be very high. V_{FB} changes from 185mV to 215mV when the power MOSFET switches from on to off. To charge the capacitor and generate 215mV at FB, the system needs ESR and some inductor current. For example, for a 5V V_{OUT}, if the forward capacitor is 0.1μF, the suggested ESR range of the output capacitor is 100mΩ to 250mΩ. Tantalum or aluminum electrolytic capacitors with a small ceramic capacitor are recommended.

A forward capacitor across R1 is recommended when the output capacitor is tantalum or aluminum electrolytic, which can set the wanted frequency if the output capacitor and ESR cannot be changed. The forward capacitor can reduce the output voltage ripple.

Selecting the Inductor

An inductor (L_O) is required to convert the switching voltage to a smooth current to the load. Although the output current is low, it is recommended that the inductor current be continuous in each switching period to prevent reaching the current limit. Calculate the inductor value with Equation (2):

$$L = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{F_{SW} \times I_{OUT} \times V_{IN} \times K} \quad (2)$$

Where K is a coefficient of about 0.15 ~ 0.85.

Output Rectifier Diode

The output rectifier diode supplies current to the inductor when the high-side switch is off. To reduce losses due to the diode forward voltage and recovery times, use a Schottky diode.

Choose a diode with a maximum reverse voltage rating greater than the maximum input voltage and a current rating greater than the average diode current.

Input Capacitor (C_{IN})

The input current to the step-down converter is discontinuous and therefore requires a capacitor to supply AC current to the step-down converter while maintaining the DC input voltage. Use low ESR capacitors for the best performance, especially under high switching frequency applications.

The RMS current through the input capacitor can be calculated with Equation (3):

$$I_{C1} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}})} \quad (3)$$

With low ESR capacitors, the input voltage ripple can be estimated with Equation (4):

$$\Delta V_{IN} = \frac{I_{OUT} \times V_{OUT}}{F_{SW} \times C_{IN} \times V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (4)$$

Choose an input capacitor with enough RMS current rating and enough capacitance for small input voltage ripples.

When electrolytic or tantalum capacitors are applied, a small, high-quality ceramic capacitor (i.e.: 0.1μF) should be placed as close to the IC as possible.

External Bootstrap Diode

An external bootstrap diode may enhance the efficiency of the converter (see Figure 2). An external BST diode is recommended from the 5V supply to BST in the following cases:

- There is a 5V rail available in the system
- VIN is no greater than 5V
- V_{OUT} is between 3.3V and 5V

This diode is also recommended for high duty cycle operation (when V_{OUT}/V_{IN} > 65%) and very high frequency (over 1.5MHz) applications.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2019 MPS. All Rights Reserved.

The bootstrap diode can be a low-cost one, such as IN4148 or BAT54.

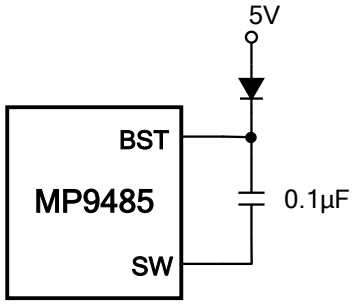


Figure 2: External Bootstrap Diode

PCB Layout Guidelines

Efficient PCB layout is critical for stable operation. Refer to Figure 3 and follow the guidelines below.

1, Place the input decoupling capacitor, catch diode, and MP9485 (VIN, SW, and PGND pin) as close to each other as possible.

2, Power traces should be short and wide to reduce voltage spikes on the SW node and lower EMI noise level.

3, Run the feedback trace as far from the inductor and noisy power traces as possible.

4, Thermal vias with 15mil barrel diameter and 40mil pitch (instance between the centers) are suggested under the exposed pad to improve thermal conduction.

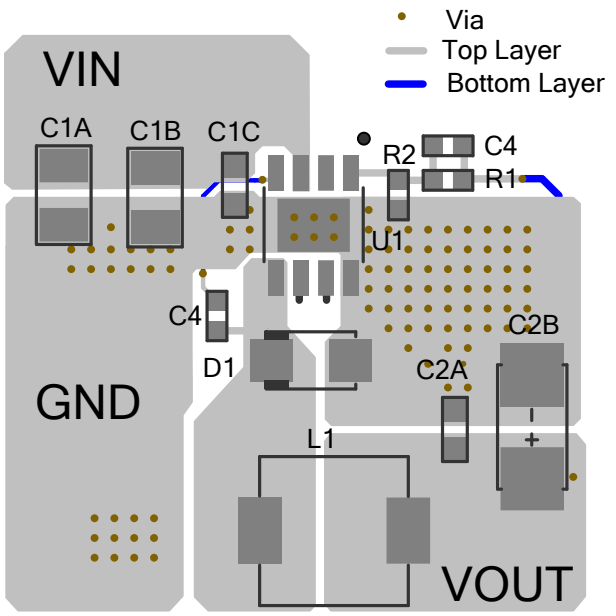


Figure 3: Layout Recommendation

Design Example

Table 1 is a design example following the application guidelines for the specifications below.

Table 1: Design Example

VIN	8V to 95V
V_{OUT}	5V
I_{OUT}	0A to 0.5A

The typical application circuit for V_{OUT} = 5V in Figure 4 shows the detailed application schematic and is the basis for the typical performance waveforms. This circuit can work down to 4.5V after start-up, but V_{OUT} may drop when VIN is low due to the maximum duty cycle limit. For more detailed device applications, please refer to the related evaluation board datasheet.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2019 MPS. All Rights Reserved.

TYPICAL APPLICATION CIRCUIT

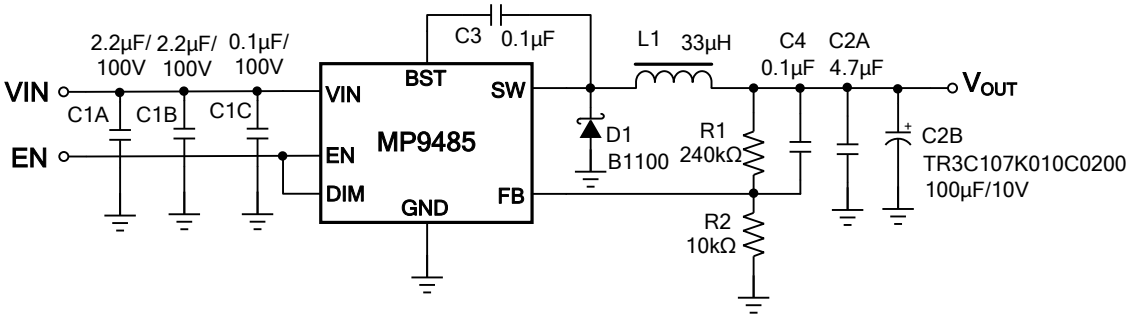
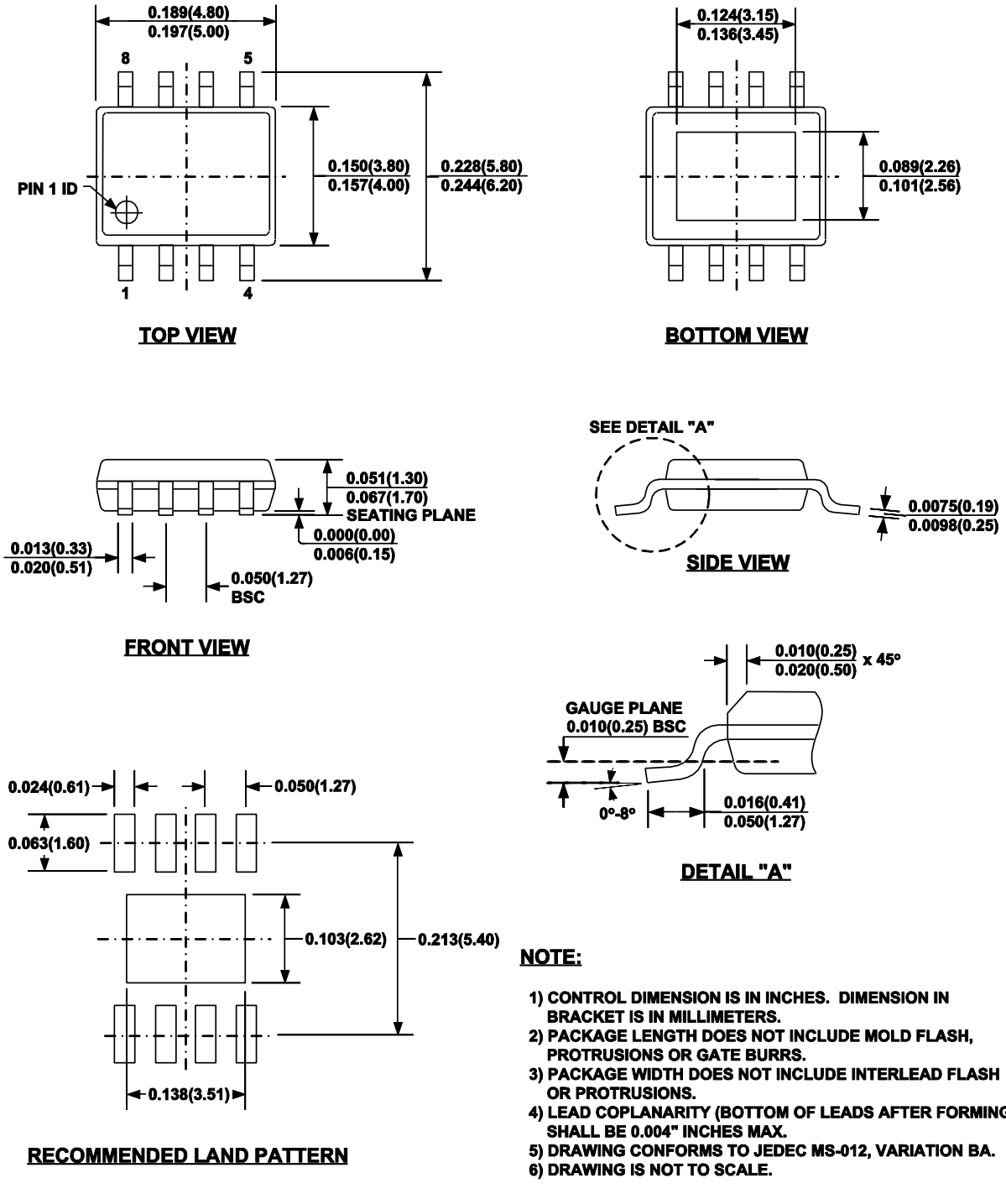


Figure 4: VIN = 60V, V_{OUT} = 5V, I_{OUT} = 0.5A

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2019 MPS. All Rights Reserved.

PACKAGE INFORMATION

SOIC-8 EP



NOTE:

1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
5) DRAWING CONFORMS TO JEDEC MS-012, VARIATION BA.
6) DRAWING IS NOT TO SCALE.

NOTICE: The information in this document is subject to change without notice. Users should warrant and guarantee that third party Intellectual Property rights are not infringed upon when integrating MPS products into any application. MPS will not assume any legal responsibility for any said applications.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2019 MPS. All Rights Reserved.