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The MPC9608 is a 3.3 V compatible, 1:10 PLL based zero-delay buffer. With a very wide frequency range and low output skews the MPC9608 is targeted for high performance and mid-range clock tree designs.

MPC9608

LOW VOLTAGE 3.3 V LVCMOS 1:10 ZERO-DELAY CLOCK BUFFER

FA SUFFIX
32-LEAD LQFP PACKAGE
CASE 873A-03

AC SUFFIX
32-LEAD LQFP PACKAGE
Pb-FREE PACKAGE
CASE 873A-03

Features

- 1:10 outputs LVCMOS zero-delay buffer
- Single 3.3 V supply
- Supports a clock I/O frequency range of 12.5 to 200 MHz
- Selectable divide-by-two for one output bank
- Synchronous output enable control (CLK_STOP)
- Output tristate control (output high impedance)
- PLL bypass mode for low frequency system test purpose
- Supports networking, telecommunications and computer applications
- Supports a variety of microprocessors and controllers
- Compatible to PowerQuicc I and II
- Ambient Temperature Range -40°C to +85°C
- 32-lead Pb-free Package Available
- **For functional replacement use 2308-2HDCG**

The MPC9608 uses an internal PLL and an external feedback path to lock its low-skew clock output phase to the reference clock phase, providing virtually zero propagation delay. This enables nested clock designs with near-zero insertion delay. Designs using the MPC9608 as PLL fanout buffer will show significantly lower clock skew than clock distributions developed from traditional fanout buffers. The device offers one reference clock input and two banks of 5 outputs for clock fanout. The input frequency and phase is reproduced by the PLL and provided at the outputs. A selectable frequency divider sets the bank B outputs to generate either an identical copy of the bank A clocks or one half of the bank A clock frequency. Both output banks remain synchronized to the input reference for both bank B configurations.

Outputs are only disabled or enabled when the outputs are already in logic low state (CLK_STOP). For system test and diagnosis, the MPC9608 outputs can also be set to high-impedance state by connecting $\overline{OE}$ to logic high level. Additionally, the device provides a PLL bypass mode for low frequency test purpose. In PLL bypass mode, the minimum frequency and static phase offset specification do not apply.

CLK_STOP and $\overline{OE}$ do not affect the PLL feedback output (QFB) and down stream clocks can be disabled without the internal PLL losing lock.

The MPC9608 is fully 3.3 V compatible and requires no external components for the internal PLL. All inputs accept LVCMOS signals while the outputs provide LVCMOS compatible levels with the capability to drive terminated 50 Ω transmission lines on the incident edge. For series terminated transmission lines, each of the MPC9608 outputs can drive one or two traces giving the devices an effective fanout of 1:20. The device is packaged in a 7x7 mm^2 32-lead LQFP package.

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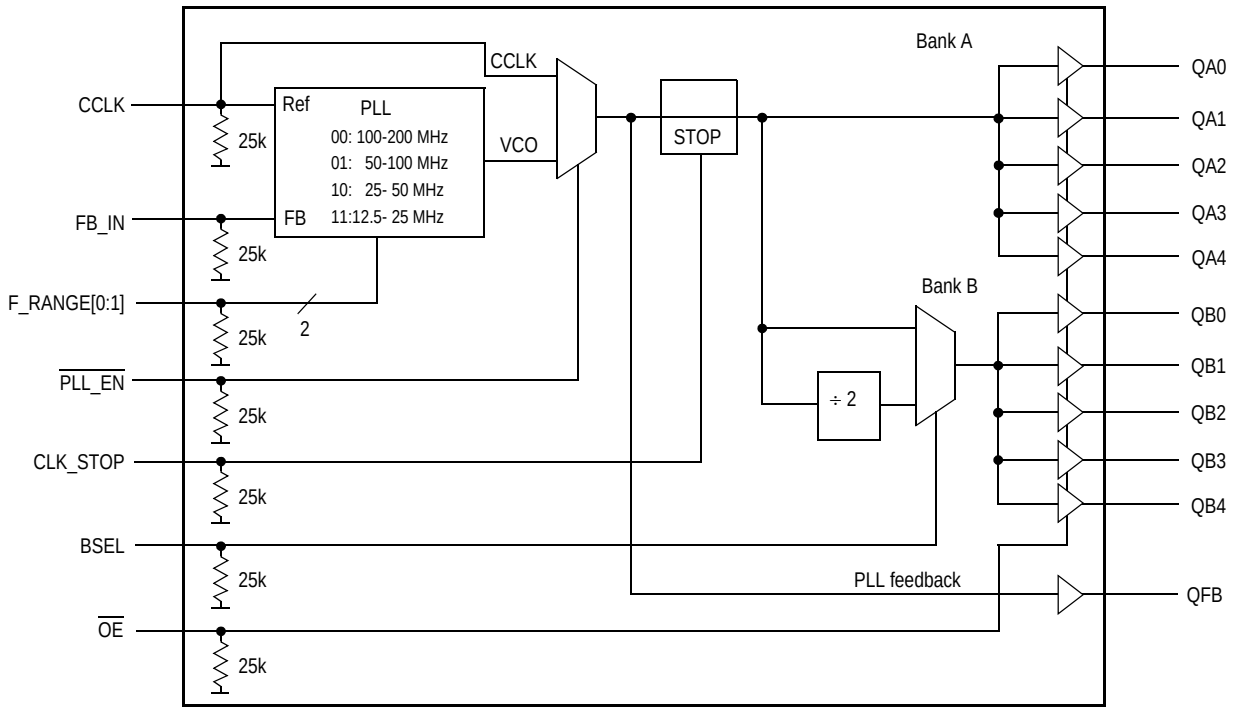

Figure 1. MPC9608 Logic Diagram

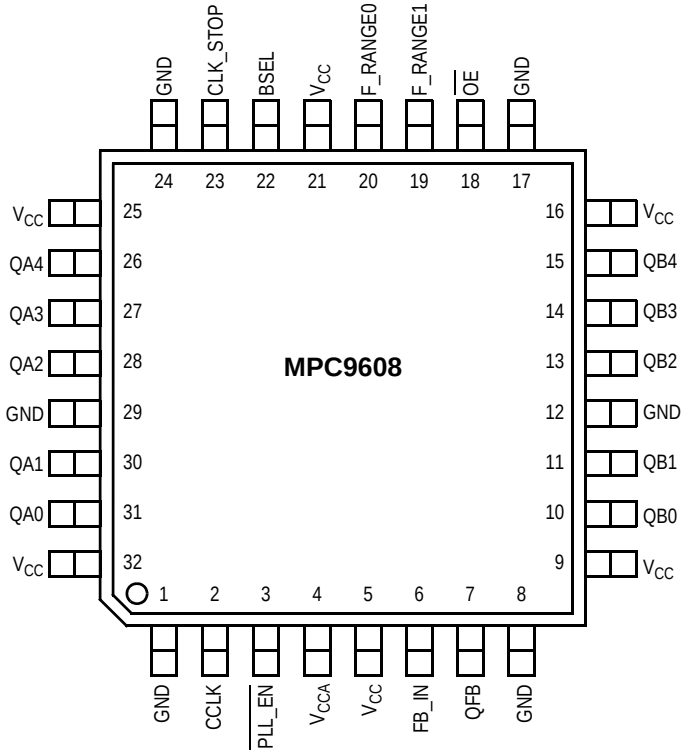

Figure 2. MPC9608 32-Lead Package Pinout (Top View)

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Table 1. Pin Configuration

Pin	I/O	Type	Function
CCLK	Input	LVCMOS	PLL reference clock signal
FB_IN	Input	LVCMOS	PLL feedback signal input, connect to a QFB output
F_RANGE[0:1]	Input	LVCMOS	PLL frequency range select
BSEL	Input	LVCMOS	Frequency divider select for bank B outputs
PLL_EN	Input	LVCMOS	PLL enable/disable
OE	Input	LVCMOS	Output enable/disable (high-impedance tristate)
CLK_STOP	Input	LVCMOS	Synchronous clock enable/stop
QA0-4, QB0-4	Output	LVCMOS	Clock outputs
QFB	Output	LVCMOS	PLL feedback signal output. Connect to FB_IN
GND	Supply	Ground	Negative power supply
V_{CCA}	Supply	V_{CC}	PLL positive power supply (analog power supply). The MPC9608 requires an external RC filter for the analog power supply pin $V_{CCA.}$ Refer to the Applications Information section for details.
V_{CC}	Supply	V_{CC}	Positive power supply for I/O and core

Table 2. Function Table

Control	Default	0	1
F_RANGE[0:1]	00	PLL frequency range. Refer to Table 3. Clock Frequency Configuration for QFB Connected to FB_INT	
BSEL	0	$f_{QB0-4} = f_{QA0-4}$	$f_{QB0-4} = f_{QA0-4} \div 2$
CLK_STOP	0	Outputs enabled	Outputs synchronously stopped in logic low state
OE	0	Outputs enabled (active)	Outputs disabled (high-impedance state), independent on CLK_STOP. Applying $\overline{OE}$ = 1 and $\overline{PLL_EN}$ = 1 resets the device. The PLL feedback output QFB is not affected by $\overline{OE}$.
PLL_EN	0	Normal operation mode with PLL enabled.	Test mode with PLL disabled. CCLK is substituted for the internal VCO output. MPC9608 is fully static and no minimum frequency limit applies. All PLL related AC characteristics are not applicable. Applying $\overline{OE}$ = 1 and $\overline{PLL_EN}$ = 1 resets the device.

Table 3. Clock Frequency Configuration for QFB Connected to FB_IN

F_RANGE[0]	F_RANGE[1]	BSEL	f_{REF} (CCLK) range [MHz]	QA0-QA4		QB0-B4		QFB
				Ratio	f_{QA0-4} [MHz]	Ratio	f_{QB0-4} [MHz]	
0	0	0	100.0 – 200.0	f_{REF}	100.0 – 200.0	f_{REF}	100.0 – 200.0	f_{REF}
0	0	1				$f_{REF} \div 2$	50.0 – 25.0	f_{REF}
0	1	0	50.0 – 100.0	f_{REF}	50.0 – 100.0	f_{REF}	50.0 – 100.0	f_{REF}
0	1	1				$f_{REF} \div 2$	25.0 – 50.0	f_{REF}
1	0	0	25.0 – 50.0	f_{REF}	25.0 – 50.0	f_{REF}	25.0 – 50.0	f_{REF}
1	0	1				$f_{REF} \div 2$	12.5 – 25.0	f_{REF}
1	1	0	12.5 – 25.0	f_{REF}	12.5 – 25	f_{REF}	12.5 – 25.0	f_{REF}
1	1	1				$f_{REF} \div 2$	6.25 – 12.5	f_{REF}

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Table 4. General Specifications

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V_{TT}	Output termination voltage		$V_{CC} \div 2$		V	
MM	ESD protection (Machine model)	200			V	
HBM	ESD protection (Human body model)	2000			V	
LU	Latch-up immunity	200			mA	
C_{PD}	Power dissipation capacitance		10		pF	Per output
C_{IN}	Input capacitance		4.0		pF	Inputs

Table 5. Absolute Maximum Ratings(1)

Symbol	Characteristics	Min	Max	Unit	Condition
V_{CC}	Supply Voltage	-0.3	3.6	V	
V_{IN}	DC Input Voltage	-0.3	V_{CC} + 0.3	V	
V_{OUT}	DC Output Voltage	-0.3	V_{CC} + 0.3	V	
I_{IN}	DC Input Current		±20	mA	
I_{OUT}	DC Output Current		±50	mA	
T_S	Storage temperature	-65	125	°C	

1. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute-maximum-rated conditions is not implied.

Table 6. DC Characteristics (V_{CC} = 3.3 V ± 5%, T_A = -40° to 85°C)

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V_{IH}	Input High Voltage	2.0		V_{CC} + 0.3	V	LVCMOS
V_{IL}	Input Low Voltage			0.8	V	LVCMOS
V_{OH}	Output High Voltage	2.4			V	I_{OH} = -24 mA(1)
V_{OL}	Output Low Voltage			0.55 0.30	V V	I_{OL} = 24 mA I_{OL} = 12 mA
Z_{OUT}	Output Impedance		14 – 17		Ω	
I_{IN}	Input Current(2)			±200	µA	V_{IN} = V_{CC} or GND
I_{CCA}	Maximum PLL Supply Current		4.0	8.0	mA	V_{CCA} Pin
I_{CCQ}	Maximum Quiescent Supply Current		1.0	4.0	mA	All V_{CC} Pins

1. The MPC9608 is capable of driving 50 Ω transmission lines on the incident edge. Each output drives one 50 Ω parallel terminated transmission line to a termination voltage of V_{TT}. Alternatively, the device drives up to two 50 Ω series terminated transmission lines.
2. Inputs have pull-down resistors affecting the input current.

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Table 7. AC Characteristics (V_{CC} = 3.3 V ± 5%, T_A = -40° to 85°C)[1]

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
f_{REF}	Input reference frequency in PLL mode[2]					
	F_RANGE = 00	100		200	MHz	
	F_RANGE = 01	50		100	MHz	
	F_RANGE = 10	25		50	MHz	
	F_RANGE = 11	12.5		25	MHz	
	Input reference frequency in PLL bypass mode[3]	0		200	MHz	
f_{max}	Output Frequency[4] F_RANGE = 00	100		200	MHz	BSEL = 0
	F_RANGE = 01	50		100	MHz	BSEL = 0
	F_RANGE = 10	25		50	MHz	BSEL = 0
	F_RANGE = 11	12.5		25	MHz	BSEL = 0
$t_{PW, MIN}$	Reference Input Pulse Width[5]	2.0			ns	
t_r, t_f	CCLK Input Rise/Fall Time			1.0	ns	0.8 V to 2.0 V
$t_{(\varnothing)}$	Propagation Delay (SPO) CCLK to FB_IN					
	f_{REF} = 100 MHz and above	-175		+175	ps	PLL Locked
	f_{REF} = 12.5 MHz to 100 MHz	-1.75% of t_{PER}		+1.75% of t_{PER}	ps	
$t_{SK(o)}$	Output-to-Output Skew				ps	
	Within a bank			80		
	Bank-to-bank			100		
	All outputs, including QFB			150		
DC	Output Duty Cycle	45	50	55	%	
t_r, t_f	Output Rise/Fall Time	0.1		1.0	ns	0.55 V to 2.4 V
$t_{PLZ, HZ}$	Output Disable Time			10	ns	
$t_{PZL, LZ}$	Output Enable Time			10	ns	
$t_{JIT(CC)}$	Cycle-to-cycle Jitter			150	ps	BSEL = 0
$t_{JIT(PER)}$	Period Jitter			150	ps	BSEL = 0
$t_{JIT(\varnothing)}$	I/O Phase Jitter RMS (1 σ)			125	ps	BSEL = 0
BW	PLL closed loop bandwidth[6] F_RANGE = 00		7 – 15		MHz	
	F_RANGE = 01		2 – 7		MHz	
	F_RANGE = 10		1 – 3		MHz	
	F_RANGE = 11		0.5 – 1.3		MHz	
t_{LOCK}	Maximum PLL Lock Time		10		ms	

1. AC characteristics apply for parallel output termination of 50 Ω to V_{TT}.
2. PLL mode requires PLL_EN = 0 to enable the PLL and zero-delay operation.
3. In bypass mode, the MPC9608 divides the input reference clock.
4. Applies for bank A and for bank B if BSEL = 0. If BSEL = 1, the minimum and maximum output frequency of bank B is divided by two.
5. Calculation of reference duty cycle limits: $DC_{REF, MIN} = t_{PW,MIN} * f_{REF}$ *100% and $DC_{REF,MAX}$ = 100% – $DC_{REF,MIN}$. For example, at f_{REF} = 100 MHz the input duty cycle range is 20% < DC < 80%.
6. -3 dB point of PLL transfer characteristics.

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APPLICATIONS INFORMATION

Power Supply Filtering

The MPC9608 is a mixed analog/digital product. Its analog circuitry is naturally susceptible to random noise, especially if this noise is seen on the power supply pins. Random noise on the V_{CCA} (PLL) power supply impacts the device characteristics, for instance I/O jitter. The MPC9608 provides separate power supplies for the output buffers (V_{CC}) and the phase-locked loop (V_{CCA}) of the device. The purpose of this design technique is to isolate the high switching noise digital outputs from the relatively sensitive internal analog phase-locked loop. In a digital system environment where it is more difficult to minimize noise on the power supplies a second level of isolation may be required. The simple but effective form of isolation is a power supply filter on the V_{CCA} pin for the MPC9608. Figure 3 illustrates a typical power supply filter scheme. The MPC9608 frequency and phase stability is most susceptible to noise with spectral content in the 100 kHz to 20 MHz range. Therefore the filter should be designed to target this range. The key parameter that needs to be met in the final filter design is the DC voltage drop across the series filter resistor R_F. From the data sheet the I_{CCA} current (the current sourced through the V_{CCA} pin) is typically 4 mA (8 mA maximum), assuming that a minimum of 3.125 V must be maintained on the V_{CCA} pin. The resistor R_F shown in Figure 3 must have a resistance of 9 – 10 Ω (V_{CC} = 3.3 V) to meet the voltage drop criteria.

R_F = 9-10 Ω for V_{CC} = 3.3 V C_F = 1 µF for V_{CC} = 3.3 V

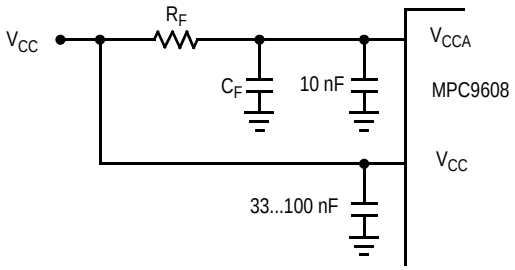

Figure 3. V_{CCA} Power Supply Filter

The minimum values for R_F and the filter capacitor C_F are defined by the required filter characteristics: the RC filter should provide an attenuation greater than 40 dB for noise whose spectral content is above 100 kHz. In the example RC filter shown in Figure 3, the filter cut-off frequency is around 3-5 kHz and the noise attenuation at 100 kHz is better than 42 dB.

As the noise frequency crosses the series resonant point of an individual capacitor, its overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the bandwidth of the PLL. Although the MPC9608 has several design features to minimize the susceptibility to power supply noise (isolated power and grounds and fully differential PLL), there still may be applications in which overall performance is being degraded due to system power supply noise. The power supply filter schemes discussed in this section should be adequate to eliminate power supply noise related problems in most designs.

Using the MPC9608 in Zero-Delay Applications

Nested clock trees are typical applications for the MPC9608. Designs using the MPC9608, as LVCMOS PLL fanout buffer with zero insertion delay, will show significantly lower clock skew than clock distributions developed from CMOS fanout buffers. The external feedback option of the MPC9608 clock driver allows for its use as a zero delay buffer. By using the QFB output as a feedback to the PLL the propagation delay through the device is virtually eliminated. The PLL aligns the feedback clock output edge with the clock input reference edge resulting in a near zero delay through the device. The maximum insertion delay of the device in zero-delay applications is measured between the reference clock input and any output. This effective delay consists of the static phase offset, I/O jitter (phase or long-term jitter), feedback path delay and the output-to-output skew error relative to the feedback output.

Calculation of Part-to-Part Skew

The MPC9608 zero delay buffer supports applications where critical clock signal timing can be maintained across several devices. If the reference clock inputs of two or more MPC9608 are connected together, the maximum overall timing uncertainty from the common CCLK input to any output is:

$$t_{SK(PP)} = t_{(\varnothing)} + t_{SK(O)} + t_{PD,\ LINE(FB)} + t_{JIT(\varnothing)} \cdot CF$$

This maximum timing uncertainty consists of 4 components: static phase offset, output skew, feedback board trace delay, and I/O (phase) jitter:

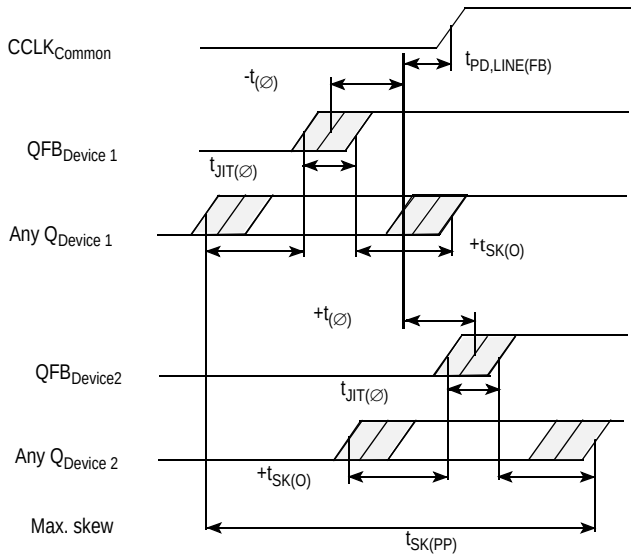

Figure 4. MPC9608 Maximum Device-to-Device Skew

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Due to the statistical nature of I/O jitter, an RMS value (1 σ) is specified. I/O jitter numbers for other confidence factors (CF) can be derived from Table 8.

Table 8. Confidence Factor CF

CF	Probability of clock edge within the distribution
± 1σ	0.68268948
± 2σ	0.95449988
± 3σ	0.99730007
± 4σ	0.99993663
± 5σ	0.99999943
± 6σ	0.99999999

The feedback trace delay is determined by the board layout and can be used to fine-tune the effective delay through each device. In the following example calculation a I/O jitter confidence factor of 99.7% (± 3σ) is assumed, resulting in a worst case timing uncertainty from input to any output of -295 ps to 295 ps[1] relative to CCLK:

$$t_{SK(PP)} = [-100\ ps...100\ ps] + [-150\ ps...150\ ps] + [(15\ ps \cdot -3)...(15\ ps \cdot 3)] + t_{PD,\ LINE(FB)}$$

$$t_{SK(PP)} = [-295\ ps...295\ ps] + t_{PD,\ LINE(FB)}$$

Driving Transmission Lines

The MPC9608 clock driver was designed to drive high speed signals in a terminated transmission line environment. To provide the optimum flexibility to the user the output drivers were designed to exhibit the lowest impedance possible. With an output impedance of less than 20 Ω the drivers can drive either parallel or series terminated transmission lines. For more information on transmission lines the reader is referred to Freescale Semiconductor application note AN1091. In most high performance clock networks point-to-point distribution of signals is the method of choice. In a point-to-point scheme either series terminated or parallel terminated transmission lines can be used. The parallel technique terminates the signal at the end of the line with a 50 Ω resistance to $V_{CC} \div 2$.

This technique draws a fairly high level of DC current and thus only a single terminated line can be driven by each output of the MPC9608 clock driver. For the series terminated case however there is no DC current draw, thus the outputs can drive multiple series terminated lines. Figure 5 illustrates an output driving a single series terminated line versus two series terminated lines in parallel. When taken to its extreme, the fanout of the MPC9608 clock driver is effectively doubled due to its capability to drive multiple lines.

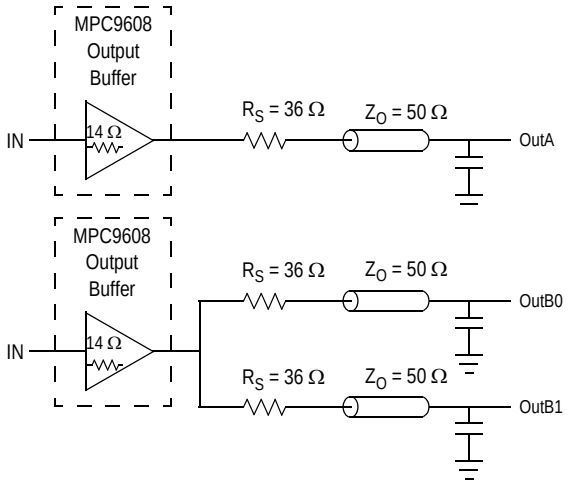

Figure 5. Single versus Dual Transmission Lines

The waveform plots in Figure 6. Single versus Dual Waveforms show the simulation results of an output driving a single line versus two lines. In both cases the drive capability of the MPC9608 output buffer is more than sufficient to drive 50 Ω transmission lines on the incident edge. From the delay measurements in the simulations a delta of only 43 ps exists between the two differently loaded outputs. This suggests that the dual line driving need not be used exclusively to maintain the tight output-to-output skew of the MPC9608. The output waveform in Figure 6. Single versus Dual Waveforms shows a step in the waveform. This step is caused by the impedance mismatch seen looking into the driver. The parallel combination of the 36 Ω series resistor plus the output impedance does not match the parallel combination of the line impedances. The voltage wave launched down the two lines will equal:

$$V_L = V_S (Z_0 \div (R_S + R_0 + Z_0))$$
$$Z_0 = 50\ \Omega \parallel 50\ \Omega$$
$$R_S = 36\ \Omega \parallel 36\ \Omega$$
$$R_0 = 14\ \Omega$$
$$V_L = 3.0\ (25 \div (18 + 17 + 25))$$
$$= 1.31\ V$$

At the load end the voltage will double to 2.6 V due to the near unity reflection coefficient. It will then increment towards the quiescent 3.0 V in steps separated by one round trip delay (in this case 4.0 ns).

1. Skew data are designed targets and pending device specifications.

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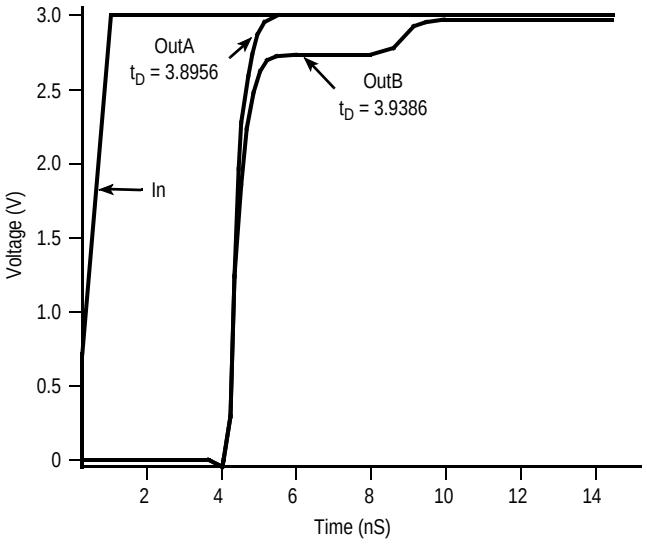
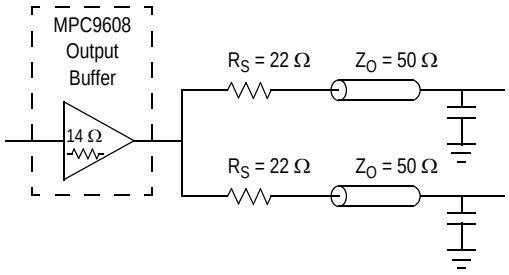


Figure 6. Single versus Dual Waveforms

Since this step is well above the threshold region, it will not cause any false clock triggering; however, designers may be uncomfortable with unwanted reflections on the line. To better match the impedances when driving multiple lines the situation in Figure 7. Optimized Dual Line Termination should be used. In this case the series terminating resistors are reduced such that when the parallel combination is added to the output buffer impedance the line impedance is perfectly matched.



14 Ω + 22 Ω || 22 Ω = 50 Ω || 50 Ω
25 Ω = 25 Ω

Figure 7. Optimized Dual Line Termination

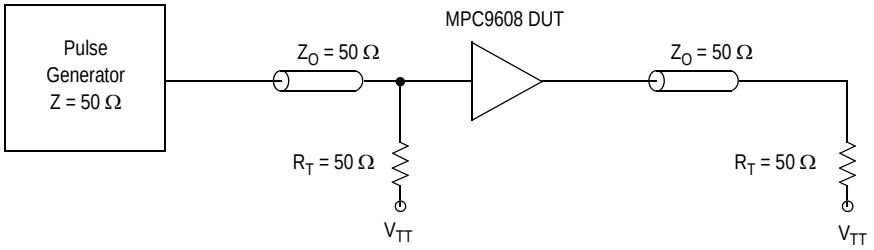


Figure 8. CCLK MPC9608 AC Test Reference for V_{CC} = 3.3 V

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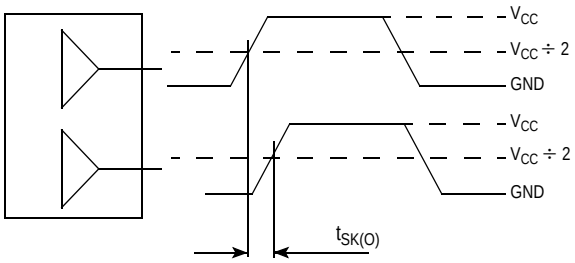


The pin-to-pin skew is defined as the worst case difference in propagation delay between any similar delay path within a single device.

Figure 9. Output-to-Output Skew $t_{SK(O)}$

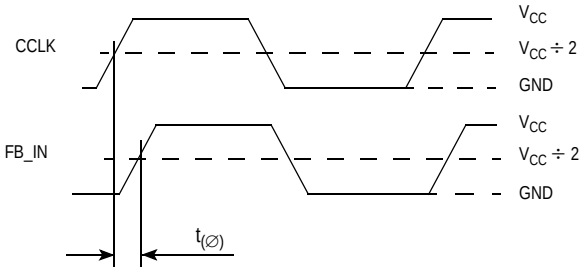
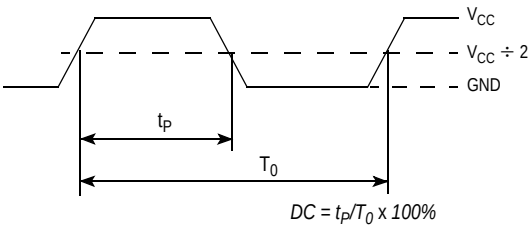
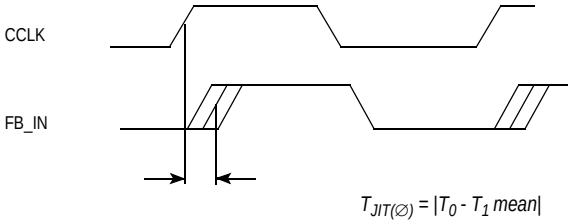


Figure 10. Propagation Delay (t_{PD}, static phase offset) Test Reference



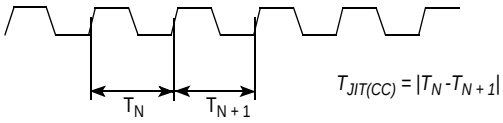
The time from the PLL controlled edge to the non controlled edge, divided by the time between PLL controlled edges, expressed as a percentage.

Figure 11. Output Duty Cycle (DC)



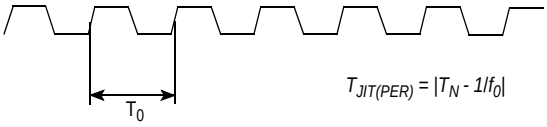
The deviation in t_0 for a controlled edge with respect to a t_0 mean in a random sample of cycles.

Figure 12. I/O Jitter



The variation in cycle time of a signal between adjacent cycles, over a random sample of adjacent cycle pairs.

Figure 13. Cycle-to-Cycle Jitter



The deviation in cycle time of a signal with respect to the ideal period over a random sample of cycles.

Figure 14. Period Jitter

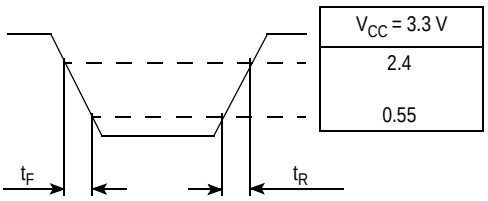


Figure 15. Output Transition Time Test Reference

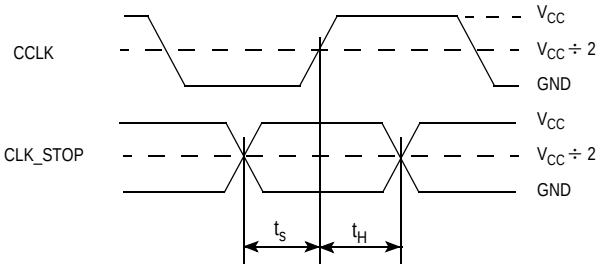


Figure 16. Setup and Hold Time (t_S, t_H) Test Reference

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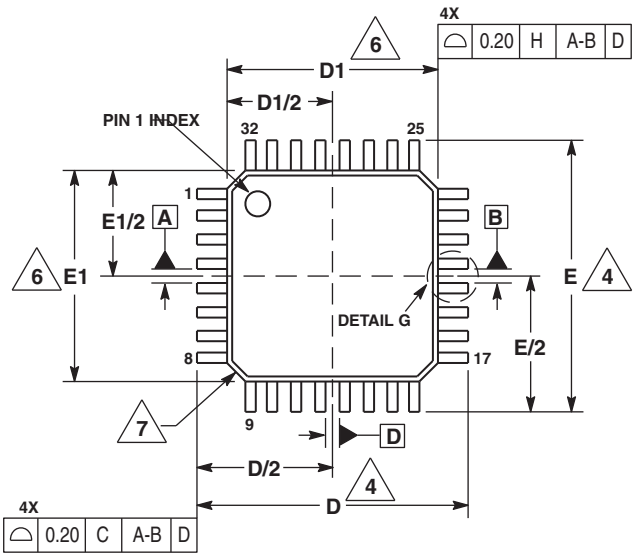
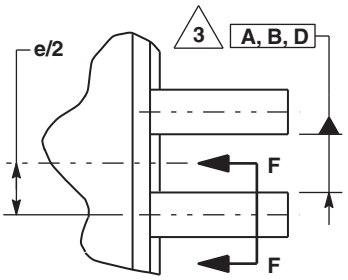
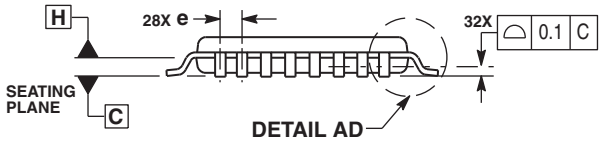
PACKAGE DIMENSIONS

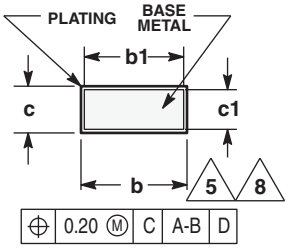




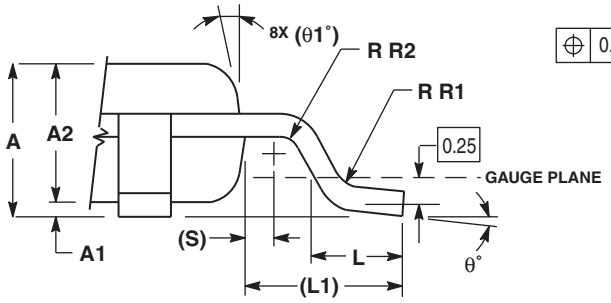
DETAIL G

NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DATUMS A, B, AND D TO BE DETERMINED AT DATUM PLANE H.
4. DIMENSIONS D AND E TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08-mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD OR PROTRUSION: 0.07-mm.
6. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25-mm PER SIDE. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
7. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
8. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.1-mm AND 0.25-mm FROM THE LEAD TIP.





SECTION F-F



DETAIL AD

	MILLIMETERS	
DIM	MIN	MAX
A	1.40	1.60
A1	0.05	0.15
A2	1.35	1.45
b	0.30	0.45
b1	0.30	0.40
c	0.09	0.20
c1	0.09	0.16
D	9.00 BSC	
D1	7.00 BSC	
e	0.80 BSC	
E	9.00 BSC	
E1	7.00 BSC	
L	0.50	0.70
L1	1.00 REF	
q	0°	7°
q1	12 REF	
R1	0.08	0.20
R2	0.08	---
S	0.20 REF	

CASE 873A-03
ISSUE B
32-LEAD LQFP PACKAGE

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NOTES

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Revision History Sheet

Rev	Table	Page	Description of Change	Date
4		1	NRND – Not Recommend for New Designs	1/7/13
4		1	Product Discontinuation Notice - Last time buy expires September 7, 2016. PDN N-16-02	3/15/16

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