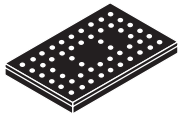
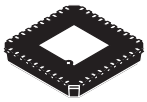
1.8 V PLL 1:10 Differential SDRAM Clock Driver

MPC96877

DDR II MEMORY
CLOCK / ZERO DELAY BUFFER



VK SUFFIX
52-BALL FP-MAPBGA PACKAGE
CASE 1544-01



EP SUFFIX
40-PIN MLF/QFN PACKAGE
CASE 1545-01

Recommended Applications

- DDR II Memory Modules
- Zero Delay Board fan-out

Features

- 1.8 V Phase Lock Loop Clock Driver for (DDR II) Applications
- Spread Spectrum Clock Compatible
- Operating Frequency: 100 MHz to 340 MHz
- 1 to 10 differential clock distribution (SSTL_18)
- 52-Ball VF-BGA (FP-MAPBGA 0.65-mm pitch) and 40-Pin MLF (QFN)
- 52-lead Pb-free Package Available
- External Feedback Pins (FBIN, $\overline{\text{FBIN}}$) are used to synchronize the Outputs to the Input Clocks
- Single-Ended Input and Single-Ended Output Modes
- Meets or Exceeds JESD82-8 PLL Standard for PC2-3200/4300
- Auto Power Down detect logic

Switching Characteristics

- Cycle-to-Cycle Jitter (>165 Mhz): 40 ps max.
- Output-to-Output Skew: 40 ps max.

AVAILABLE ORDERING OPTIONS

T_A	52-Ball BGA	40-Pin QFN
0°C to 70°C	MPC96877VK (Pb-Free)	MPC96877EP (Pb-Free)

Functional Description

The MPC96877 is a high-performance, low-jitter, low-skew, zero-delay buffer that distributes a differential clock input pair (CK, $\overline{\text{CK}}$) to ten differential pairs of clock outputs (Yn, $\overline{\text{Yn}}$) and to one differential pair of feedback clock outputs (FBOUT, $\overline{\text{FBOUT}}$). The clock outputs are controlled by the input clocks (CK, $\overline{\text{CK}}$), the feedback clocks (FBIN, $\overline{\text{FBIN}}$), the LVCMOS control pins (OE, OS), and the analog power input (AV_{DD}). When OE is low, the clock outputs, except FBOUT/$\overline{\text{FBOUT}}$, are disabled while the internal PLL continues to maintain its locked-in frequency. OS (output select) is a program pin that must be tied to GND or V_{DD}. When OS is high, OE functions as previously described. When OS and OE are both low, OE has no affect on Y7/$\overline{\text{Y7}}$, they are free running. When AV_{DD} is grounded, the PLL is turned off and bypassed for test purposes. When both clock inputs (CK, $\overline{\text{CK}}$) are logic low, the device enters in a low power mode. An input logic detection circuit on the differential inputs, independent from input buffers, detects the logic low level and performs in a low power state where all outputs, the feedback, and the PLL are off. When the clock inputs transition from being logic low to being differential signals, the PLL turns back on, the inputs and the outputs are enabled, and the PLL obtains phase lock between the feedback clock pair (FBIN, $\overline{\text{FBIN}}$) and the clock input pair (CK, $\overline{\text{CK}}$) within the specified stabilization time.

The MPC96877 is able to track spread spectrum clocking (SSC) for reduced EMI. This device operates from 0°C to 70°C.

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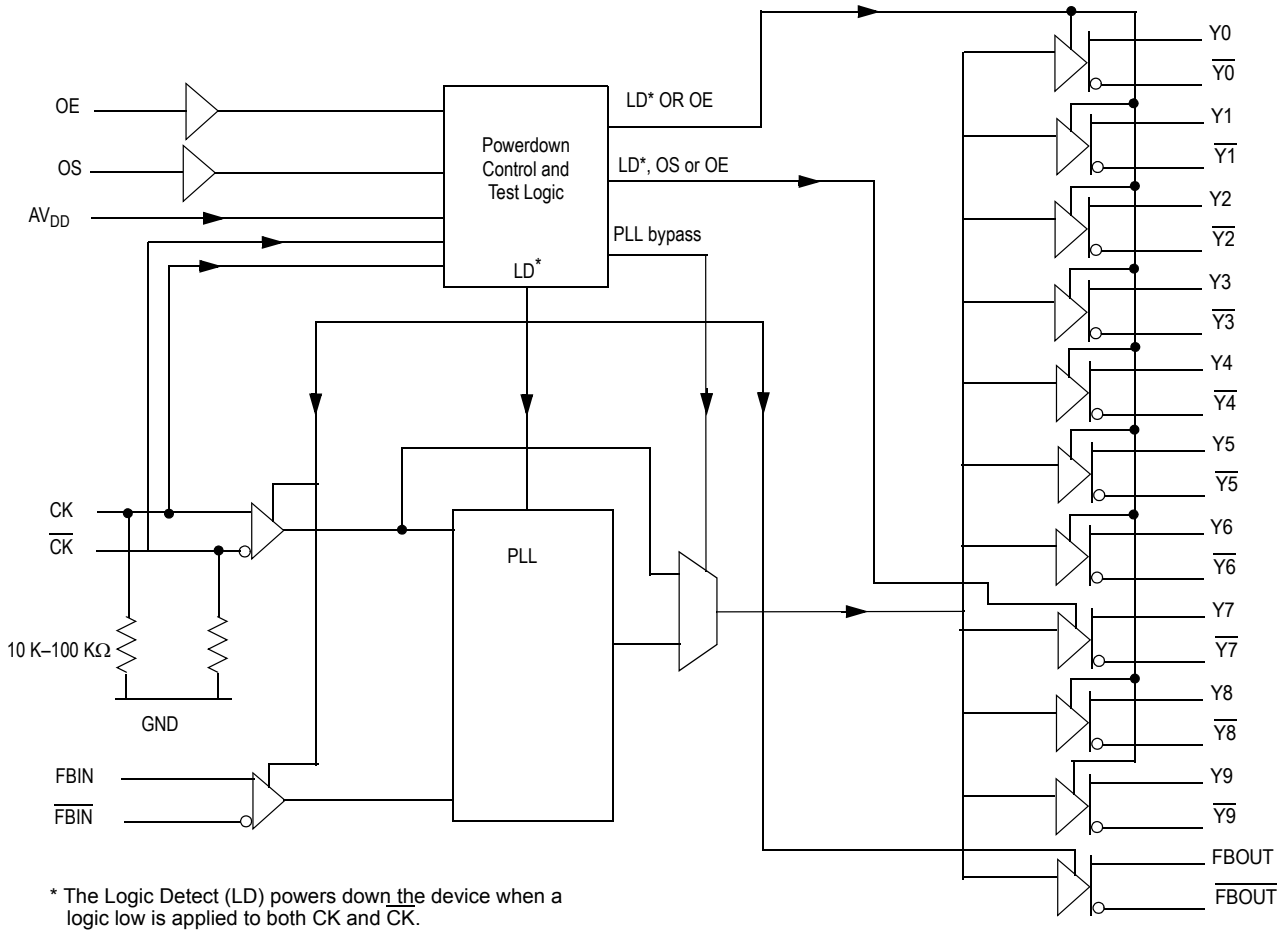
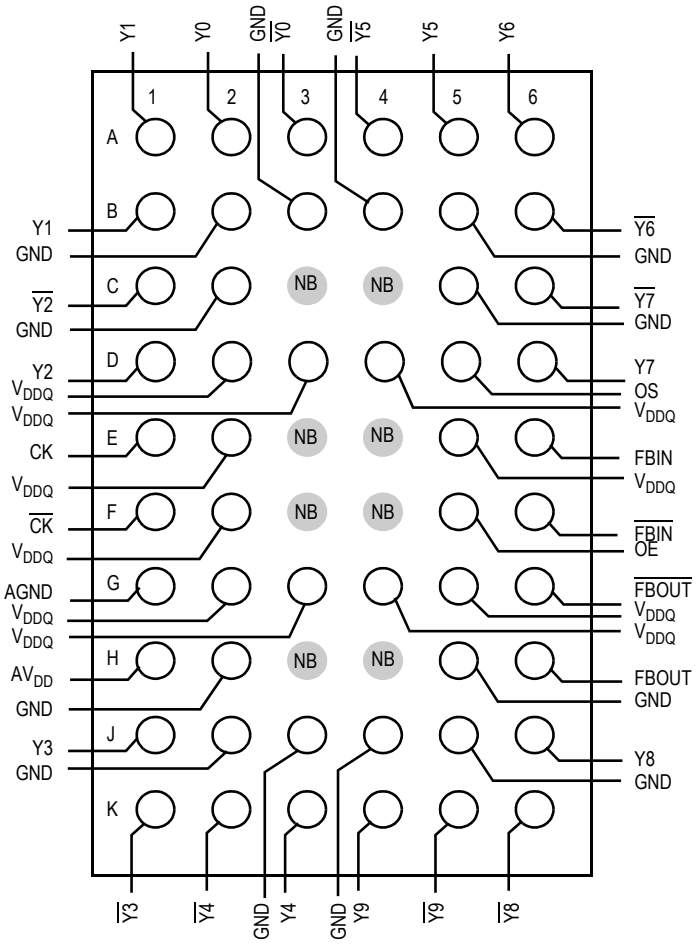


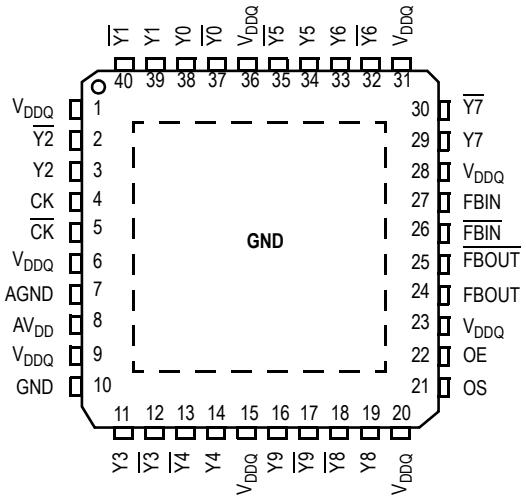
Figure 1. MPC96877 Logic Diagram

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VF-MAPBGA (VK) PACKAGE



EP PACKAGE
(TOP VIEW)



40-Pin TE-QFN(6.0 x 6.0 mm Body Size,
0.5 mm Pitch, M0#220, Variation VJJD-2,
E2 = D2 = 2.9 mm ±0.15 mm) Package Pinouts

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Table 1. Pin Configuration

Pin	BGA	MLF	I/O	Function
AGND	G1	7		Analog ground
AV_{DD}	H1	8		Analog power
CK	E1	4	Input	Clock input with a (10k to 100k) pulldown resistor
$\overline{CK}$	E6	5	Input	Complimentary clock input with a (10k to 100k) pulldown resistor
FBIN	F6	27	Input	Feedback clock input
$\overline{FBIN}$		26	Input	Complimentary Feedback clock input
FBOUT	H6	24	Output	Feedback clock output
$\overline{FBOUT}$	G6	25	Output	Complimentary feeback clock output
OE	F5	22	Input	Output Enable (asynchronous)
OS	D5	21	Input	Output Select (tied to GND or V_{DD})
GND	B2, B3, B4, B5, C2,C5,H2,H5, J2, J3, J4, J5	10		Ground
V_{DDQ}	D2, D3, D4, E2, E5, F2, G2, G3, G4, G5	1, 6, 9, 15, 20, 23, 28, 31, 36		Logic and output power
Y[0:9]	A2, A1, D1, J1, K3, A5, A6, D6, J6, K4	38, 39, 3, 11, 14, 34, 33, 29,19, 16	Output	Clock outputs
Y[0:9]	A3, B1, C1, K1, K2, A4, B6, C6, K6, K5	37, 40, 2, 12, 13, 35, 32, 30, 18, 17	Output	Complimentary clock outputs

Table 2. Function Table

Inputs					Outputs				PLL
AV_{DD}	OE	OS	CK	$\overline{CK}$	Y	Y	FBOUT	$\overline{FBOUT}$	
GND	H	X	L	H	L	H	L	H	Bypassed / OFF
GND	H	X	H	L	H	L	H	L	Bypassed / OFF
GND	L	H	L	H	L_Z	L_Z	L	H	Bypassed / OFF
GND	L	L	H	L	L_Z[1] Y7 Active	L_Z[1] $\overline{Y7}$ Active	H	L	Bypassed / OFF
1.8 V Nominal	L	H	L	H	L_Z[1]	L_Z[1]	L	H	ON
1.8 V Nominal	L	L	H	L	L_Z[1] Y7 Active	L_Z[1] $\overline{Y7}$ Active	H	L	ON
1.8 V Nominal	H	X	L	H	L	H	L	H	ON
1.8 V Nominal	H	X	H	L	H	L	H	L	ON
1.8 V Nominal	X	X	L	L	L_Z[1]	L_Z[1]	L_Z[1]	L_Z[1]	OFF
X	X	X	H	H	RESERVED				

1. $L_{(Z)}$ means the outputs are disabled to a low state meeting the I_{ODL} limit in Table 5.

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Table 3. Absolute Maximum Ratings Over Free-Air Operating Range[1]

Parameter	Value
Supply voltage range, V_{DDQ} or AV_{DD}	–0.5 V to 2.5 V
Input voltage range, V_I[2, 3]	–0.5 V to V_{DDQ} + 0.5 V
Output voltage range, V_O[1, 2]	–0.5 V to V_{DDQ} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{DDQ})	±50 mA
Output clamp voltage, I_{OK} (V_O < 0 or V_O > V_{DDQ})	±50 mA
Continuous output current, IO (V_O = 0 to V_{DDQ})	±50 mA
Continuous current through each V_{DDQ} or GND	±100 mA
Storage temperature range, T_{STG}	–65°C to 150°C

1. Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
3. This value is limited to 2.5 V maximum.

Table 4. Recommended Operating Conditions

Rating	Parameter	Affected Pins	Min	Nom	Max	Unit
Output supply voltage	V_{DDQ}		1.7	1.8	1.9	V
Supply voltage[1]	AV_{DD}			V_{DDQ}		
Low-level input voltage[2]	V_{IL}	OE, OS, CK, $\overline{CK}$			0.35 x V_{DDQ}	V
High-level input voltage[2]	V_{IH}	OE, OS, CK, $\overline{CK}$	0.65 x V_{DDQ}			
High-level output current	I_{OH}				–9	mA
Low-level output current	I_{OL}				9	mA
Input differential-pair cross voltage	V_{IX}		(V_{DDQ}/2) –0.15		(V_{DDQ}/2) +0.15	V
Input voltage level	V_{IN}		–0.3		V_{DDQ} +0.3	
Input differential-pair voltage[2] (see Figure 9. Half-Period Jitter)	V_{ID}	DC	0.3		V_{DDQ} +0.4	
		AC	0.6		V_{DDQ} +0.4	
Operating free-air temperature			0		70	°C

1. The PLL is turned off and bypassed for test purposes when AV_{DD} is grounded. During this test mode, V_{DDQ} remains within the recommended operating conditions and not timing parameters are guaranteed.
2. V_{ID} is the magnitude of the difference between the input level on CK and the input level on $\overline{CK}$, see Figure 12. Time Delay between OE and Clock Output for definition. For CK and $\overline{CK}$ the V_{IH} and V_{IL} limits are used to define the DC low and high levels for the logic detect state.

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Table 5. Electrical Characteristics Over Recommended Free-Air Operating Temperature Range

Description	Parameter	Affected Pins	Test Conditions	AV_{DD}, V_{DDQ}	Min	Max	Unit
All inputs	V_{IK}		I_I = –18mA	1.7 V		–1.2	V
High output voltage	V_{OH}		I_{OH} = –100 μA	1.7 to 1.9 V	V_{DDQ} –0.2		V
			I_{OH} = –9 mA	1.7 V	1.1		
Low output voltage	V_{OL}		I_{OL} = 100 μA	1.7 to 1.9 V		0.1	V
			I_{OL} = 9 mA	1.7 V		0.6	
Output disable current	I_{ODL}		OE = L, V_{ODL} = 100 mV	1.7 V	100		μA
Output differential voltage	V_{OD}			1.7 V	0.5		V
Input leakage current	I_I	CK, $\overline{CK}$	V_I = V_{DDQ} or GND	1.9 V		± 250	μA
		OE, OS, FBIN, $\overline{FBIN}$	V_I = V_{DDQ} or GND	1.9 V		± 10	
Static supply current I_{DDQ} + I_{ADD}	I_{DDLD}		CK and $\overline{CK}$ = L	1.9 V		500	μA
Dynamic Supply current I_{DDQ} + I_{ADD}, see Note 1 for CPD calculation	I_{DD}		CK and $\overline{CK}$ = 270 MHz all outputs open	1.9 V		300	mA

1. Total I_{DD} = I_{DDQ} + I_{ADD} = F_{CK}* C_{PD} * V_{DDQ}, solving for C_{PD} = (I_{DDQ} + I_{ADD})/(F_{CK} * V_{DDQ}) where F_{CK} is the input Frequency, V_{DDQ} is the power supply and C_{PD} is the Power Dissipation Capacitance.

Table 6. Timing Requirements Over Recommended Free-Air Operating Temperature Range

Timing Requirements	AV_{DD}, V_{DDQ} = 1.8 V ± 0.1 V		Unit
	Min	Max	
Operating clock frequency[1, 2]	125	340	MHz
Application clock frequency[1, 3]	160	340	MHz
Input clock duty cycle	40	60	%
Stabilization time[4]		15	μs

1. The PLL must be able to handle spread spectrum induced skew.
2. Operating clock frequency indicates a range over which the PLL must be able to lock, but in which it is not required to meet the other timing parameters. (Used for low speed system debug.)
3. Application clock frequency indicates a range over which the PLL must meet all timing parameters.
4. Stabilization time is the time required for the integrated PLL circuit to obtain phase lock of its feedback signal to its reference signal after power up. During normal operation, the stabilization time is also the time required for the integrated PLL circuit to obtain phase lock of its feedback signal to its reference signal when CK and $\overline{CK}$ go to a logic low state, enter the power-down mode and later return to active operation. CK and $\overline{CK}$ may be left floating after they have been driven low for one complete clock cycle.

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Table 7. Switching Characteristics over Recommended Free-Air Operating Temperature Range Unless Otherwise Noted (see Notes)

Description	Parameter	Diagram	AV_{DD}, V_{DDQ} = 1.8 V ± 0.1 V			Unit
			Min	Nom	Max	
OE to any Y/$\overline{Y}$	ten	see Figure 11			8	ns
OE to any Y/$\overline{Y}$	tdis	see Figure 11			8	ns
Cycle-to-Cycle period jitter	tjit(cc+)	see Figure 4	0		40	ps
	tjit(cc–)		0		–40	ps
Static phase offset	t(φ)	see Figure 5	–50		50	ps
Dynamic phase offset	t(φ)dyn	see Figure 10	–50		50	ps
Output clock skew	tsk(o)	see Figure 6			40	ps
Period Jitter	tjit(per)	see Figure 7	–40		40	ps
Half -period jitter	tjit(hper)	see Figure 8	–75		75	ps
Output Enable	slr(i)	see Figure 3 and Figure 9	0.5			V/ns
Input clock slew rate, measured single ended			1	2.5	4	
Output clock slew rate, measured single ended	slr(o)	see Figure 3 and Figure 9	1.5	2.5	3	V/ns
Output differential-pair cross voltage	V_{OX}	see Figure 2	(V_{DDQ}/2) – 0.1		(V_{DDQ}/2) + 0.1	V
SSC modulation frequency			30		33	kHz
SSC clock input frequency deviation			0.0		–0.5	
PLL Loop bandwidth (–3dB from unity gain)			2.0			MHz

NOTES:

1. There are two different terminations that are used with the following tests. The loadboard in Figure 2. IBIS Model Output Load is used to measure the input and output differential-pair cross voltage only. The loadboard in Figure 3. Output Load Test Circuit 1 is used to measure all other tests. For consistency, equal length cables must be used.
2. Static Phase offset does not include Jitter.
3. Period Jitter and Half-Period Jitter specifications are separate specifications that must be met independently of each other.
4. The Output Slew Rate is determined form the IBIS model into the load shown in Figure 4. Output Load Test Circuit 2. It is measured single ended.
5. To eliminate the impact of input slew rates on static phase offset, the input slew rates of Reference Clock Input CK, $\overline{CK}$ and Feedback Clock Input FBIN, $\overline{FBIN}$ are recommended to be nearly equal. The 2.5 V/ns slew rates are shown as a recommended target. Compliance with these Nom values is not mandatory if it can be adequately demonstrated that alternative characteristics meet the requirements of the registered DDR2 DIMM application.

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TEST CIRCUIT AND SWITCHING WAVEFORMS

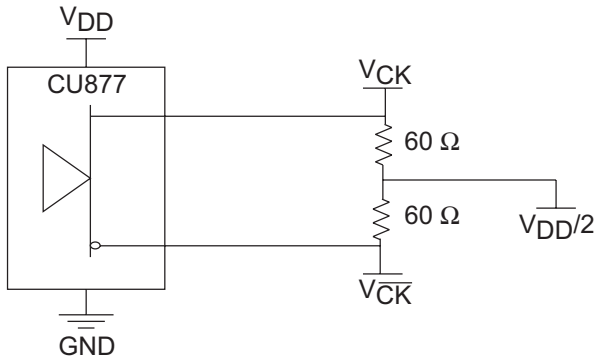


Figure 2. IBIS Model Output Load

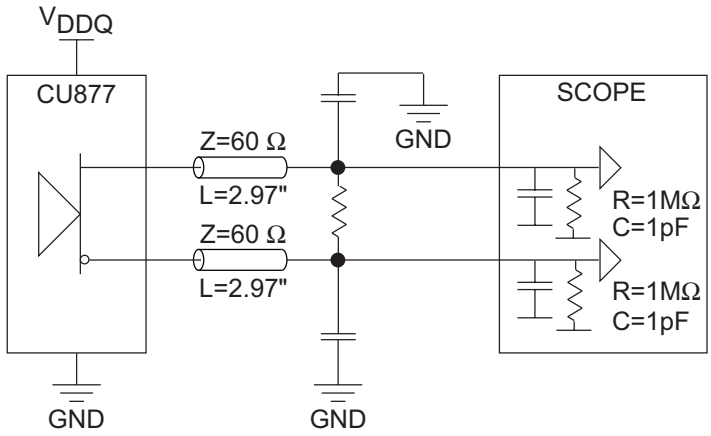


Figure 3. Output Load Test Circuit 1

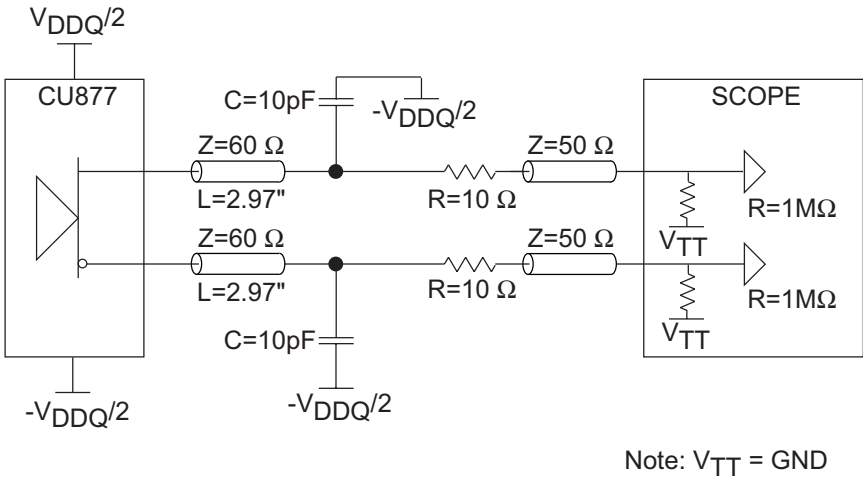
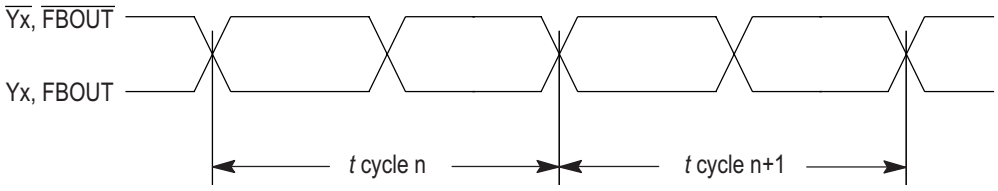


Figure 4. Output Load Test Circuit 2

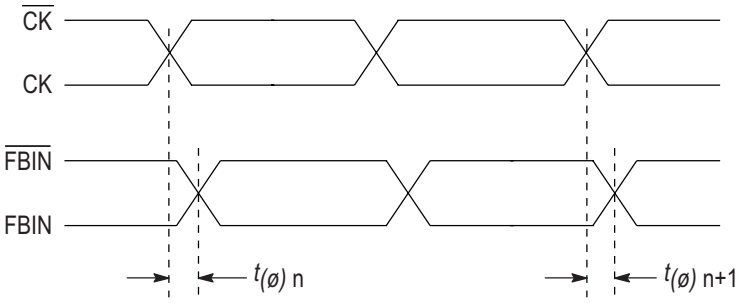
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TEST CIRCUIT AND SWITCHING WAVEFORMS (Continued)



$$t_{jit(cc)} = t \text{ cycle n} - t \text{ cycle n+1}$$

Figure 5. Cycle-to-Cycle Period Jitter



$$t_{(ø)} = \frac{\sum_{1}^{n=N} t_{(ø)\,n}}{N}$$ (N is a large number of samples)

Figure 6. Static Phase Offset

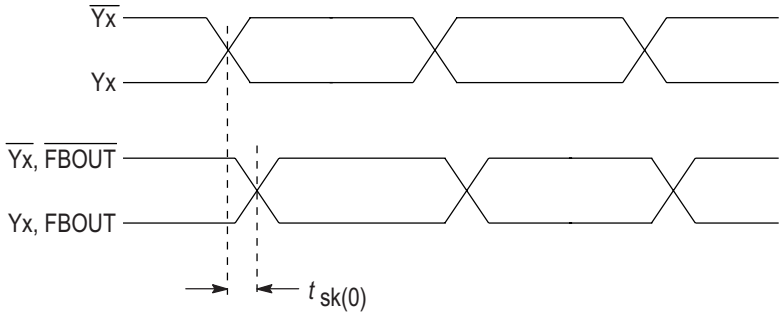


Figure 7. Output Skew

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TEST CIRCUIT AND SWITCHING WAVEFORMS (Continued)

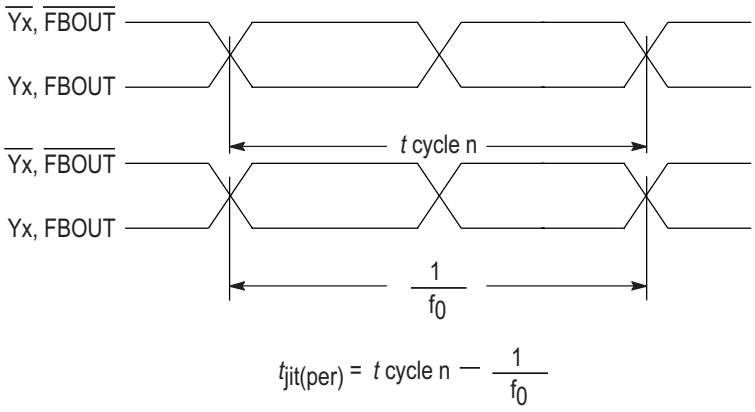


Figure 8. Period Jitter

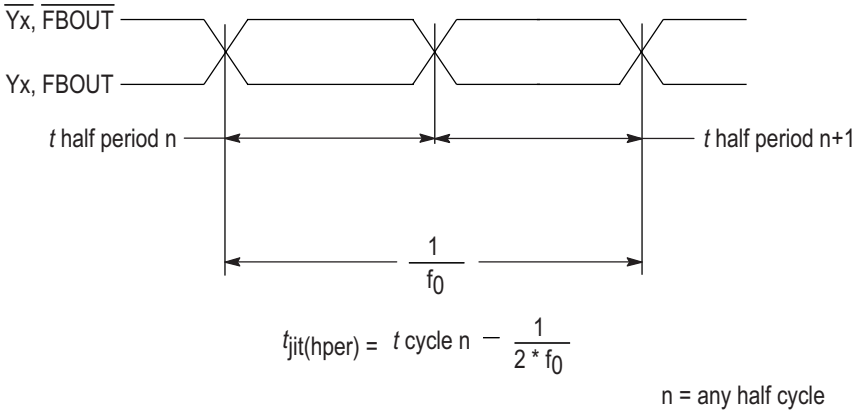


Figure 9. Half-Period Jitter

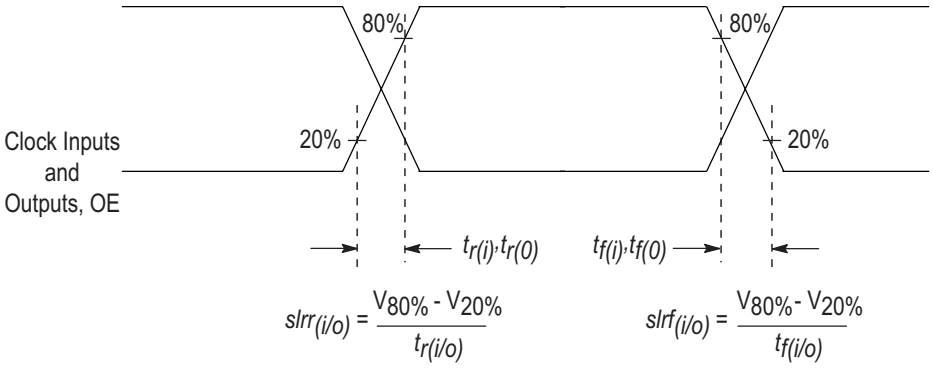


Figure 10. Input and Output Slew Rates

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TEST CIRCUIT AND SWITCHING WAVEFORMS (Continued)

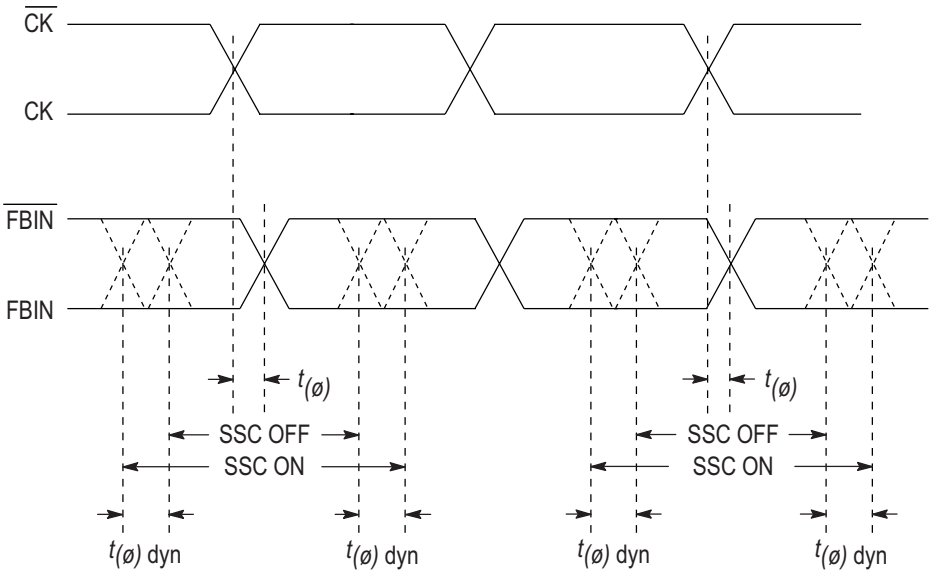


Figure 11. Dynamic Phase Offset

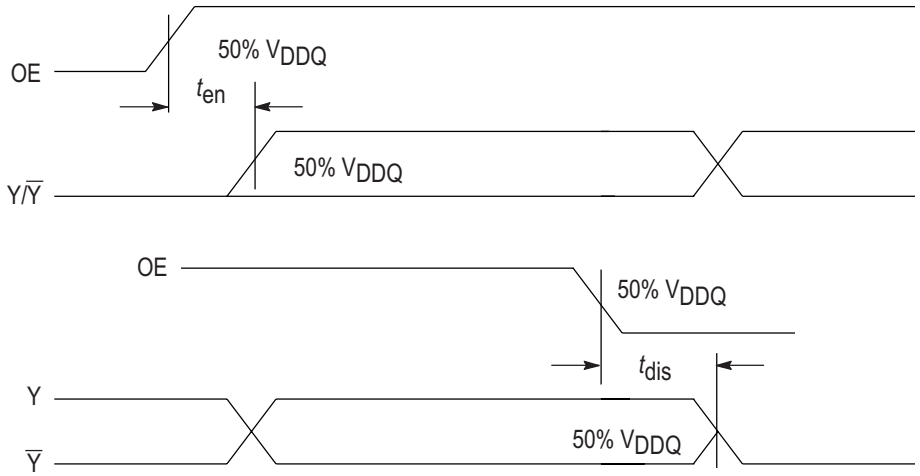
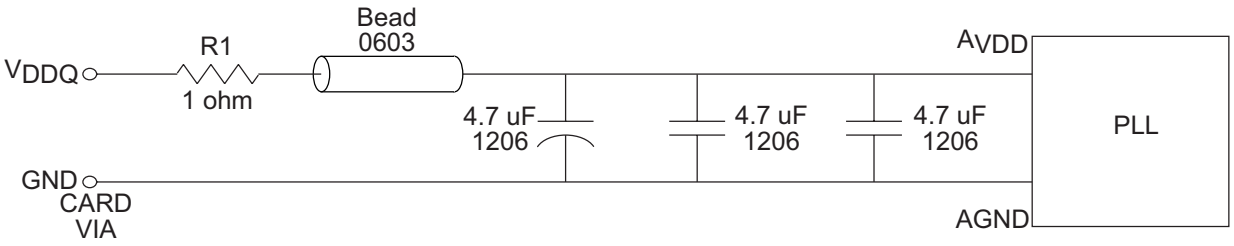


Figure 12. Time Delay between OE and Clock Output

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RECOMMENDED FILTERING FOR THE ANALOG POWER SUPPLY (AV_{DD})



NOTES:

1. Place the 2200pF capacitor close to the PLL
2. Use a wide trace for the PLL analog power and ground. Connect PLL and caps to AGND to AGND trace & connect trace to one GND via (farthest from PLL).
3. Recommended bead: Fair Rite P/N 2506036017Y0 or equivalent (0.8 Ohm DC max, 600 Ohms @ 100 MHz)

Figure 13. AV_{DD} Filtering

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