MPQ2166

6V, Dual 2A/2A or 3A/1A, Low Quiescent Current, Synchronous Buck with PG and SS AEC-Q100 Qualified

The Future of Analog IC Technology

DESCRIPTION

The MPQ2166 is an internally compensated, dual, PWM, synchronous, step-down regulator that operates from a 2.7V to 6V input and generates an output voltage as low as 0.6V. The MPQ2166 can be configured as a 2A/2A or 3A/1A output current regulator and is ideal for powering portable equipment that runs on a single-cell lithium-ion (Li+) battery due to a low 60µA quiescent current.

The MPQ2166 integrates dual, 55mΩ, high-side switches and 20mΩ synchronous rectifiers for high efficiency without an external Schottky diode. The MPQ2166 has peak-current-mode control and internal compensation and is capable of low dropout configurations. Both channels can operate at 100% duty cycle.

Full protection features include cycle-by-cycle current limit and thermal shutdown.

The MPQ2166 requires a minimum number of readily available, standard, external components and is available in QFN-18 (2mmx3mm) and QFN-18 (2.5mmx3.5mm) packages.

FEATURES

- 2.7V to 6V Operating Input Range
- 2A/2A or 3A/1A Continuous Current
- 55mΩ/20mΩ $R_{DS(ON)}$
- Programmed Frequency up to 3MHz
- External Sync Clock Up to 3MHz
- 180° Phase Shifted Operation
- Power Good (PG) Indicators
- External Soft Start (SS) and Track
- Adjustable Advanced Asynchronous Mode (AAM) or Forced Continuous Conduction Mode (FCCM)
- Peak Efficiency >90%
- Output Adjustable from 0.6V to 5.5V
- 100% Duty Cycle Operation
- 60µA Quiescent Current
- Cycle-by-Cycle Over-Current Protection (OCP)
- Short-Circuit Protection (SCP) with Hiccup Mode and Valley Current Detection
- Thermal Shutdown
- Available in QFN-18 (2mmx3mm) and QFN-18 (2.5mmx3.5mm) Packages
- Available in a Wettable Flank Package
- Available in AEC-Q100 Grade-1

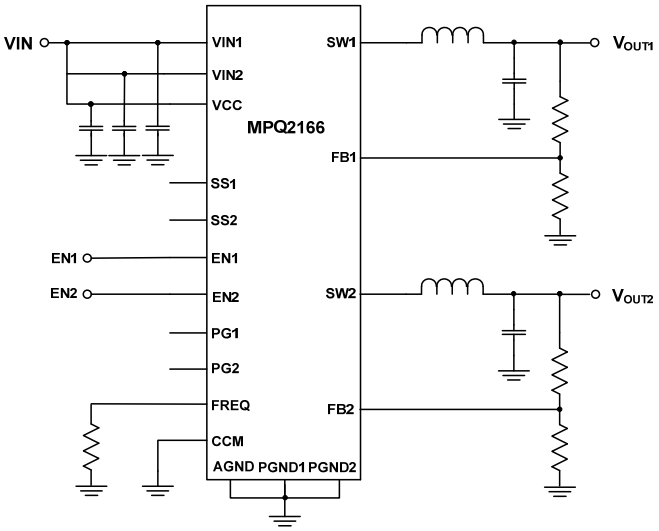
APPLICATIONS

- Automotive Infotainment
- Automotive Clusters
- Automotive Telematics
- Battery-Powered Devices
- Portable Instruments

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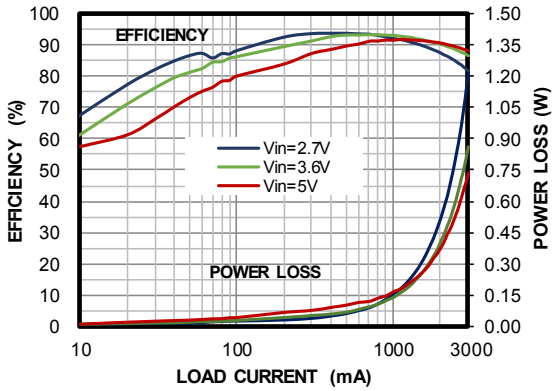
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TYPICAL APPLICATION



Efficiency vs. Load Current

V_{OUT1} = 1.8V, L1 = 0.68µH, f_{SW} = 2.25MHz, AAM, one channel on



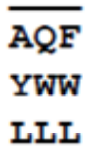
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ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating**
MPQ2166GD	QFN-18 (2mmx3mm)	*See Below*	1
MPQ2166GD-AEC1			
MPQ2166GDE-AEC1***			
MPQ2166GRH	QFN-18 (2.5mmx3.5mm)		1
MPQ2166GRH-AEC1			
MPQ2166GRHE-AEC1***			

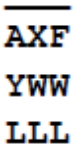
* For Tape & Reel, add suffix –Z (e.g. MPQ2166GD–Z)
** Moisture Sensitivity Level Rating
*** Wettable flank

TOP MARKING (MPQ2166GD & MPQ2166GD-AEC1)



AQF: Product code of MPQ2166GD and MPQ2166GD-AEC1
Y: Year code
WW: Week code
LLL: Lot number

TOP MARKING (MPQ2166GDE-AEC1)



AXF: Product code of MPQ2166GDE-AEC1
Y: Year code
WW: Week code
LLL: Lot number

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TOP MARKING (MPQ2166GRH&MPQ2166GRH-AEC1)

AVP
YWW
LLL

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Y: Year code
WW: Week code
LLL: Lot number

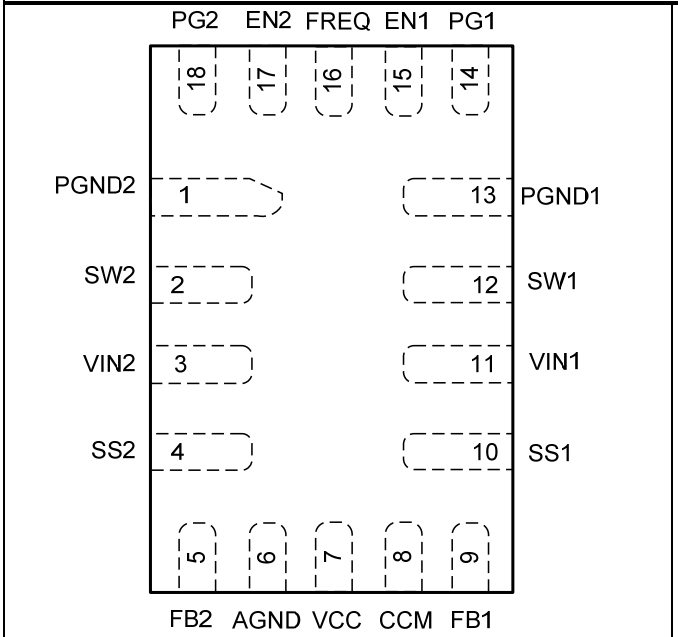
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BKG
YWW
LLL

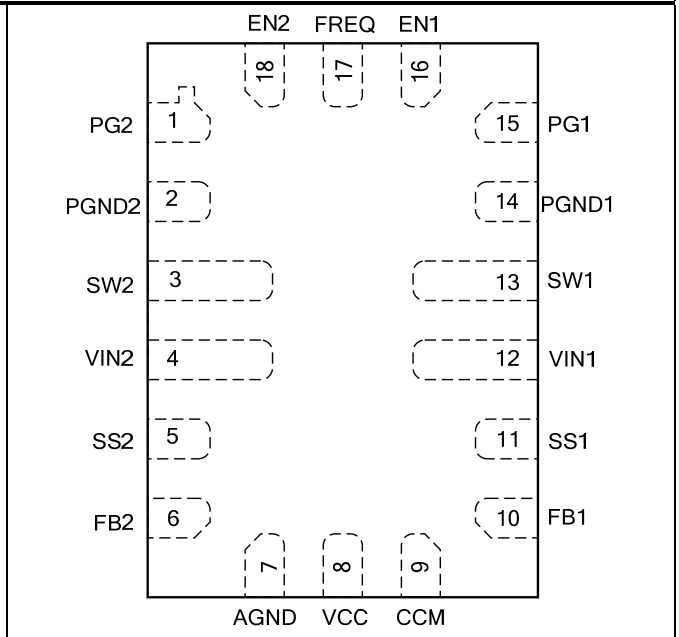
BKG: Product code of MPQ2166GRHE-AEC1
Y: Year code
WW: Week code
LLL: Lot number

PACKAGE REFERENCE

TOP VIEW



QFN-18 (2mmx3mm)



QFN-18 (2.5mmx3.5mm)

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ABSOLUTE MAXIMUM RATINGS (1)

Supply voltage (V_{IN}) 6.5V
V_{SW} ..... -0.3V to V_{IN} + 0.3V
All other pins ..... -0.3V to +6.5V
Junction temperature ..... 150°C
Lead temperature ..... 260°C
Storage temperature ..... -65°C to 150°C
Continuous power dissipation (T_A = +25°C) (2)
QFN-18 (2mmx3mm) 1.78W
QFN-18 (2.5mmx3.5mm) 2.5W

ESD Rating

Human-body model (HBM) ..... ±2kV
Charged-device model (CDM) ..... ±750V

Recommended Operating Conditions

Supply voltage (V_{IN}) ..... 2.7V to 6V
Output voltage (V_{OUT}) ..... 0.6V to 5.5V
Operating junction temp. ..... -40°C to +125°C (3)

Thermal Resistance θ_{JA} θ_{JC}

QFN-18 (2mmx3mm)		
JESD51-7 (4)	70	15 °C/W
QFN-18 (2.5mmx3.5mm)		
JESD51-7 (4)	50	12 °C/W
EV2166-RH-00A (5)	34.8	2.7 °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) Operating devices at junction temperatures greater than 125°C is possible, please contact MPS for details.
4) Measured on JESD51-7, 4-layer PCB.
5) Measured on MPS standard EVB, 6.35cm*6.35cm, 2oz cooper thick, 4-Layer PCB.

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ELECTRICAL CHARACTERISTICS

V_{IN} = 5V, T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_J = 25°C.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Supply current (quiescent)	I_Q	V_{IN} = 5V, V_{EN} = 2V, V_{FB} = 0.65V, no switching		60	80	μA
Shutdown current	I_{SHDN}	V_{EN} = 0V, CCM=GND, T_J = +25°C		0	0.2	μA
		V_{EN} = 0V, CCM=GND T_J = -40°C to +85°C(6)		0	1.5	μA
		V_{EN} = 0V, CCM=GND T_J = +85°C to +125°C			5	μA
VIN under-voltage lockout threshold	IN_{UVLO}	Rising edge		2.4	2.55	V
VIN under-voltage lockout hysteresis	IN_{UVLO_HYS}			230		mV
Regulated FB voltage	V_{FB}	T_J = +25°C	0.593	0.600	0.607	V
		T_J = -40°C to +125°C	0.588	0.600	0.612	V
FB input current	I_{FB}	V_{FB} = 0.65V		0	50	nA
EN high threshold	V_{EN_H}		1.6			V
EN low threshold	V_{EN_L}				0.4	V
EN input current	I_{EN}	V_{EN} = 2V		0	0.1	μA
		V_{EN} = 0V		0	0.1	
HS switch on resistance	R_{DSON_P}	V_{IN} = 5V		55	90	mΩ
LS switch on resistance	R_{DSON_N}	V_{IN} = 5V		20	45	mΩ
SW leakage current	I_{SW_LK}	V_{EN} = 0V, V_{IN} = 6V, V_{SW} = 0V and 6V, T_J = 25°C	-1	0	1	μA
HS switch current limit(6)	I_{HS_LIMIT}	Sourcing	3.4	4.5	5.6	A
LS valley current limit(6)	I_{VALLEY}			3.9		A
LS switch current limit	I_{LS_LIMIT}	Sinking, CCM	1			A
Oscillator frequency accuracy	f_{SW}	R_{FREQ} = 665k	298	350	402	kHz
		R_{FREQ} = 200k	850	1000	1150	kHz
		R_{FREQ} = 51k	2700	3000	3300	kHz
Sync frequency range	f_{SYNC}		0.35		3	MHz
Phase shift				180		degree
Minimum on time(6)	T_{ON_MIN}			55		ns
Minimum off time(6)	T_{OFF_MIN}			50		ns
Maximum duty cycle	D_{MAX}			100		%
Thermal shutdown threshold(6)	T_D			175		°C
Thermal shutdown hysteresis(6)	T_{D_HYS}			40		°C
Soft-start charging current	I_{SS}	V_{SS} = 0V	2	3.2	5	μA
Power good rising threshold	$PGOOD_{Vth-Hi}$		0.85	0.9	0.95	V_{FB}
Power good falling threshold	$PGOOD_{Vth-Lo}$		0.77	0.82	0.87	V_{FB}
Power good rising delay	T_{PGOOD_R}			30		μs
Power good falling delay	T_{PGOOD_F}			40		μs
CCM on threshold			1.6			V
CCM off threshold					0.4	V

NOTE:

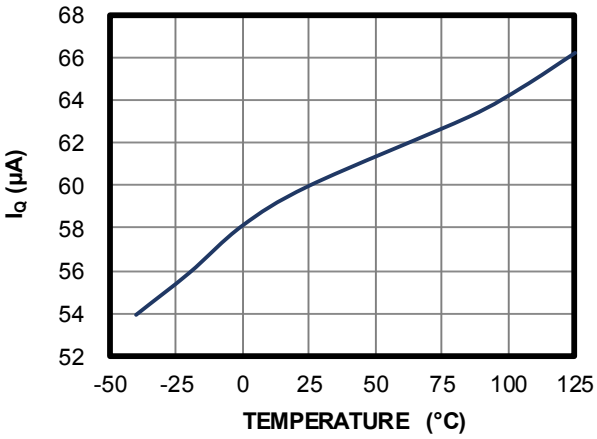
6) Guaranteed by design and characterization, not test in production.

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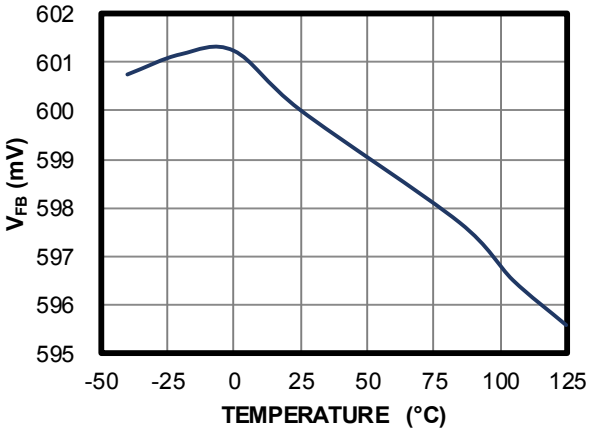
TYPICAL CHARACTERISTICS

V_{IN} = 5V, T_J = -40°C to +125°C, unless otherwise noted.

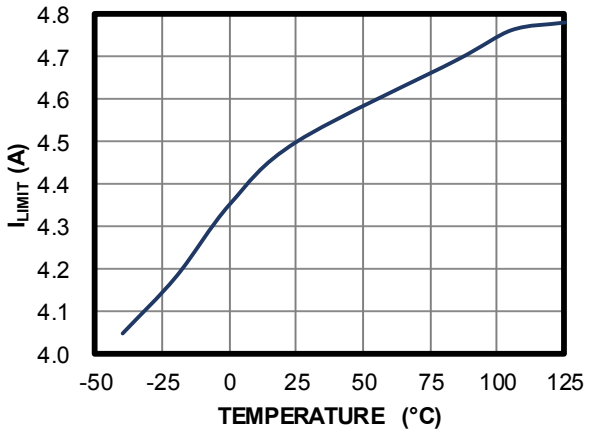
I_Q vs. Temperature



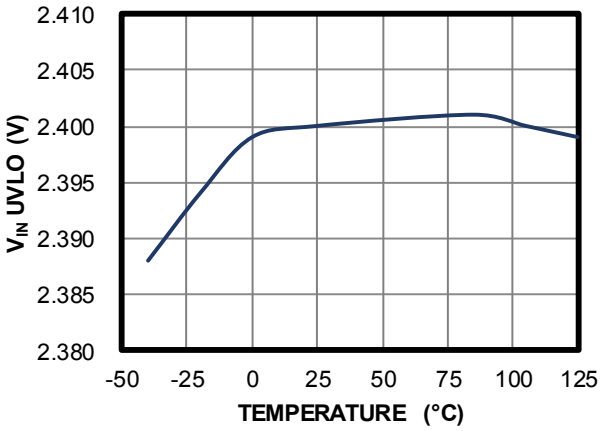
V_{FB} vs. Temperature



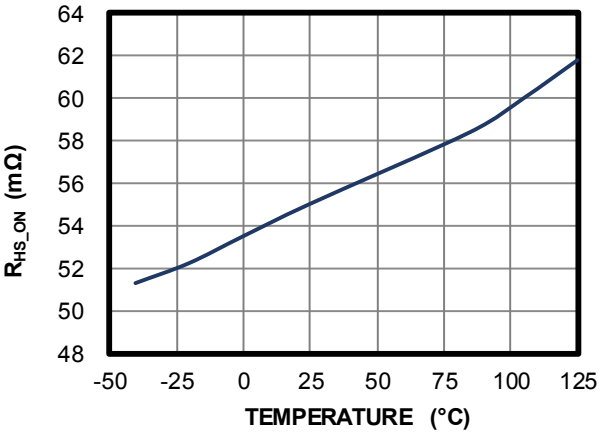
I_{LIMIT} vs. Temperature



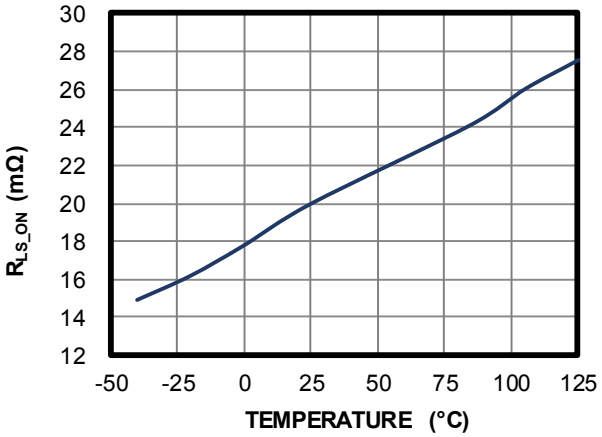
V_{IN} UVLO Rising Threshold vs. Temperature



R_{HS_ON} vs. Temperature



R_{LS_ON} vs. Temperature

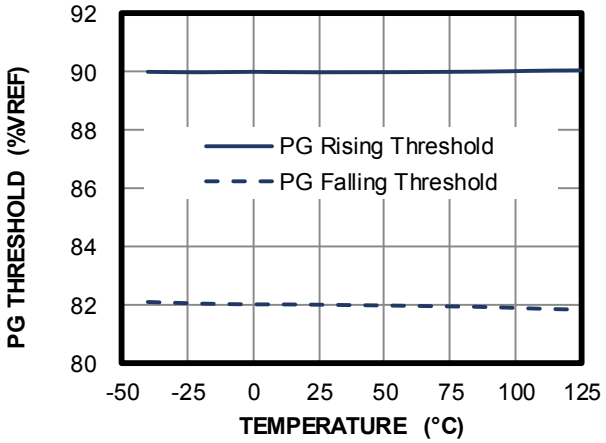


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TYPICAL CHARACTERISTICS *(continued)*

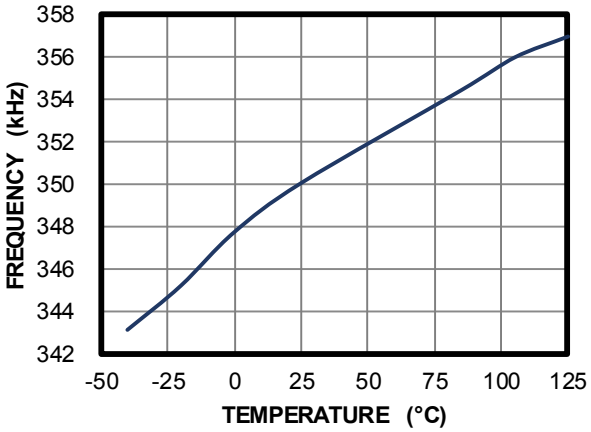
V_{IN} = 5V, T_J = -40°C to +125°C, unless otherwise noted.

PG Rising/Falling Threshold vs. Temperature



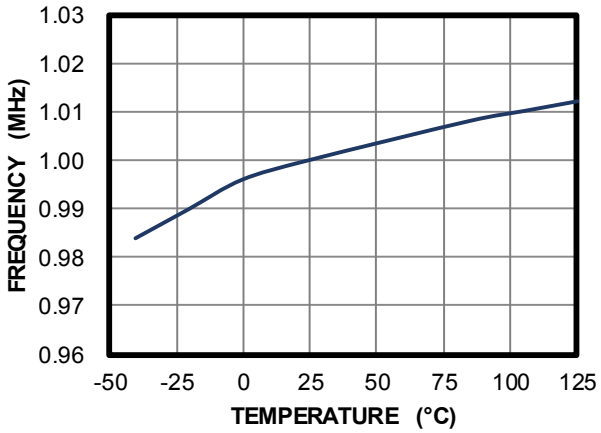
Frequency vs. Temperature

f_{SW} = 350kHz



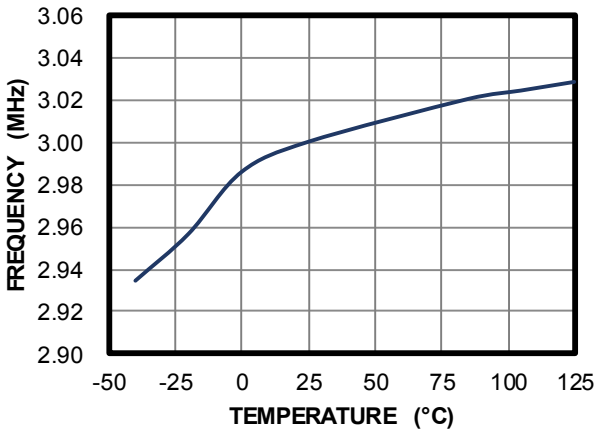
Frequency vs. Temperature

f_{SW} = 1MHz



Frequency vs. Temperature

f_{SW} = 3MHz



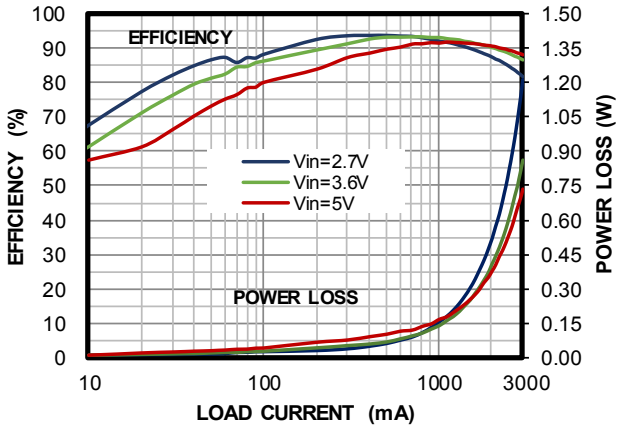
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TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 5V, V_{OUT1} = 1.8V, V_{OUT2} = 1.2V, L1 = L2 = 1.5µH, f_{SW} = 2.25MHz, T_A = 25°C, unless otherwise noted.

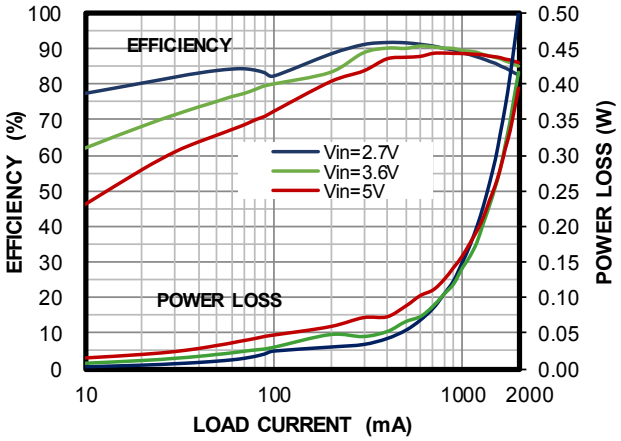
Efficiency vs. Load Current

V_{OUT1} = 1.8V, L1 = 0.68µH, AAM, one channel on



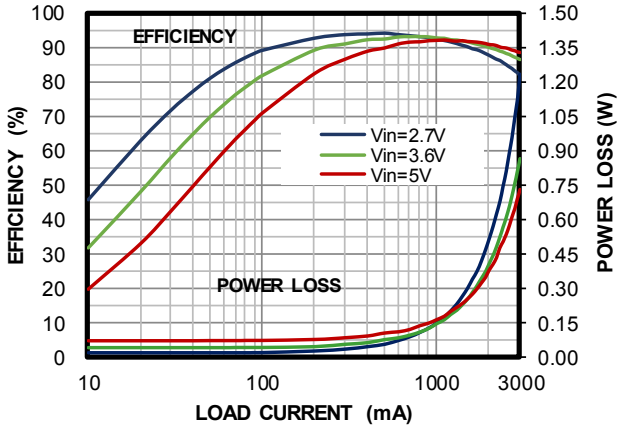
Efficiency vs. Load Current

V_{OUT2} = 1.2V, AAM, one channel on



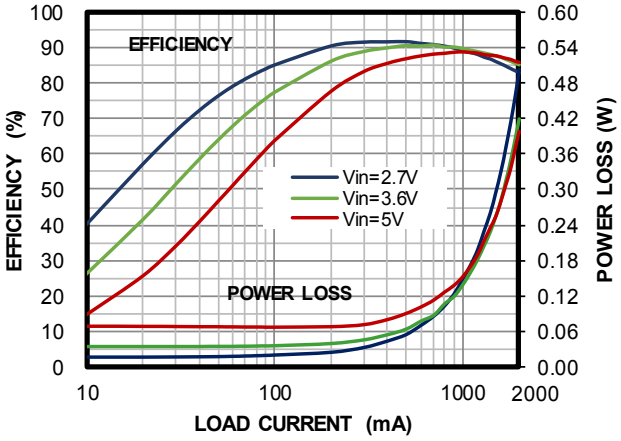
Efficiency vs. Load Current

V_{OUT1} = 1.8V, L1 = 0.68µH, FCCM, one channel on



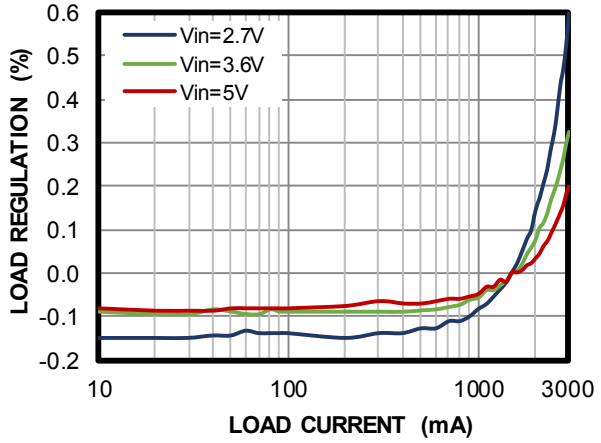
Efficiency vs. Load Current

V_{OUT2} = 1.2V, FCCM, one channel on



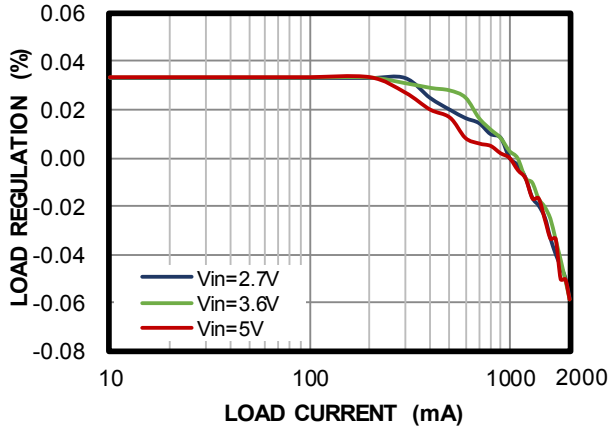
Load Regulation

V_{OUT1} = 1.8V, L1 = 0.68µH, AAM, one channel on



Load Regulation

V_{OUT2} = 1.2V, AAM, one channel on



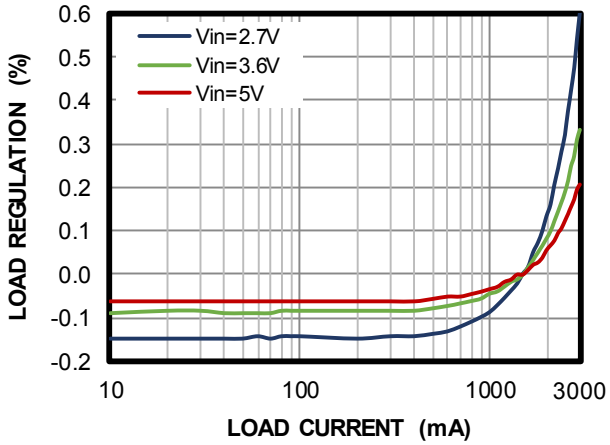
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TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT1} = 1.8V, V_{OUT2} = 1.2V, L1 = L2 = 1.5µH, f_{SW} = 2.25MHz, T_A = 25°C, unless otherwise noted.

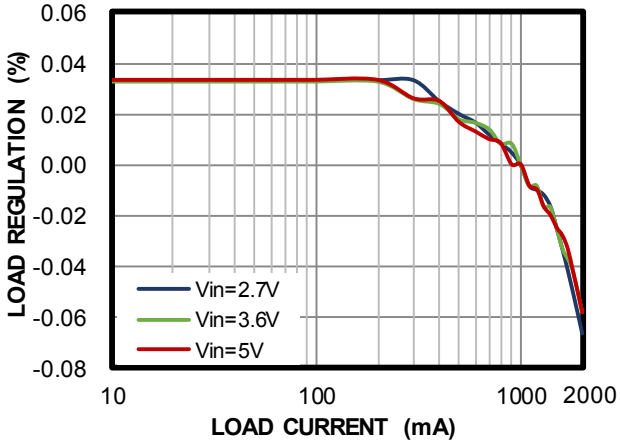
Load Regulation

V_{OUT1} = 1.8V, L1 = 0.68µH, FCCM, one channel on



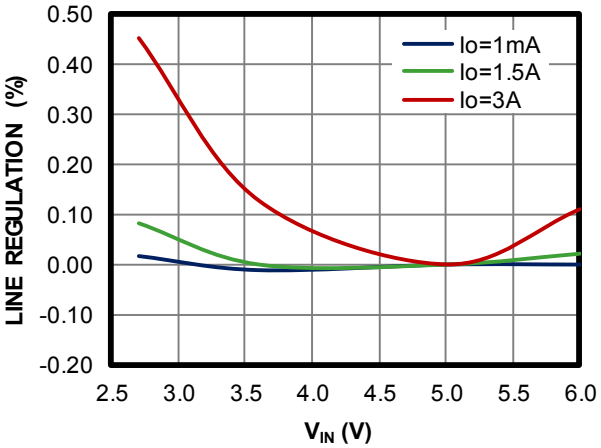
Load Regulation

V_{OUT2} = 1.2V, FCCM, one channel on



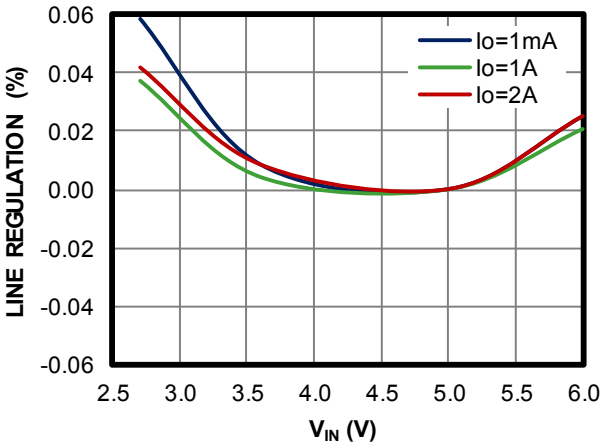
Line Regulation

V_{OUT1} = 1.8V, L = 0.68µH, AAM, one channel on



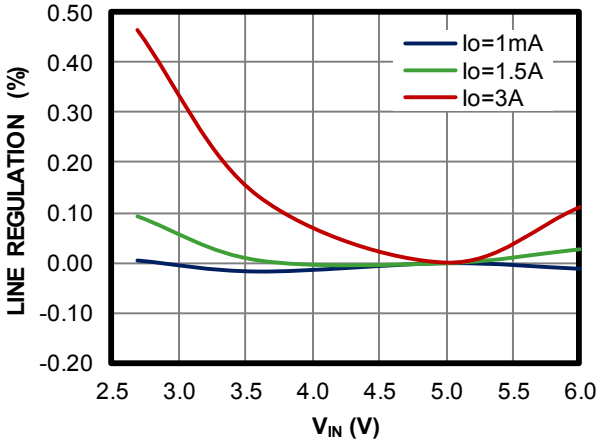
Line Regulation

V_{OUT2} = 1.2V, AAM, one channel on



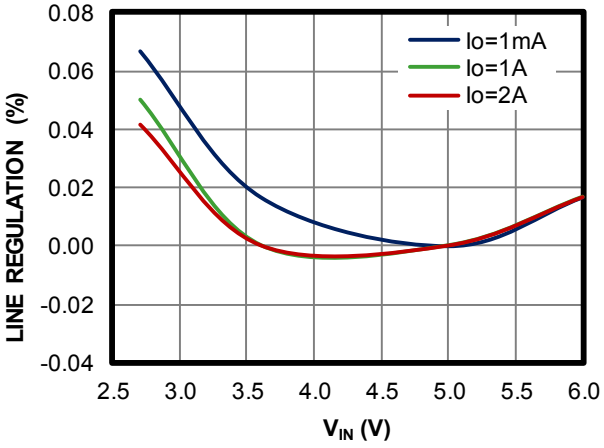
Line Regulation

V_{OUT1} = 1.8V, L = 0.68µH, FCCM, one channel on



Line Regulation

V_{OUT2} = 1.2V, FCCM, one channel on



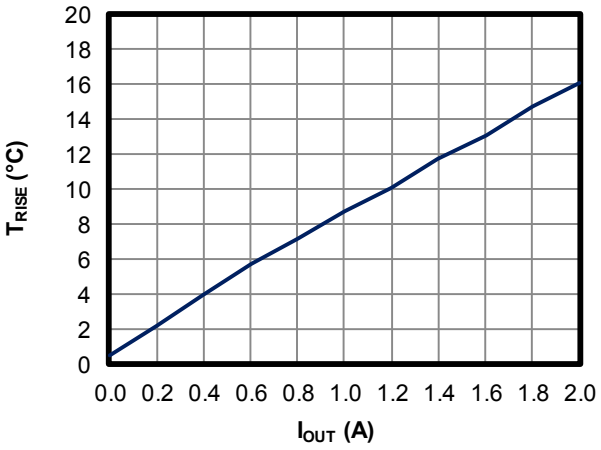
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TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT1} = 1.8V, V_{OUT2} = 1.2V, L1 = L2 = 1.5µH, f_{SW} = 2.25MHz, T_A = 25°C, unless otherwise noted.

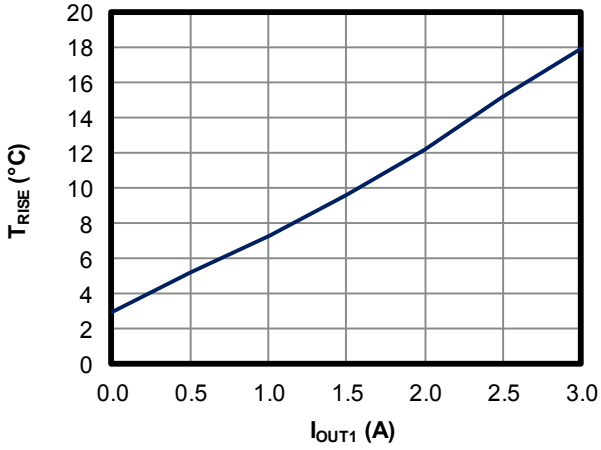
Case Thermal Rise

V_{IN} = 5V, I_{OUT1} = I_{OUT2} = 0A to 2A, AAM, both channels on



Case Thermal Rise

V_{IN} = 5V, I_{OUT1} = 0A to 3A, I_{OUT2} = 1A, AAM, L1 = 0.68µH, both channels on

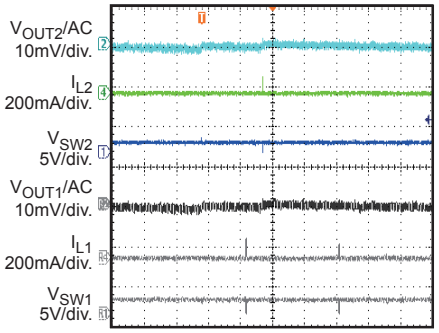


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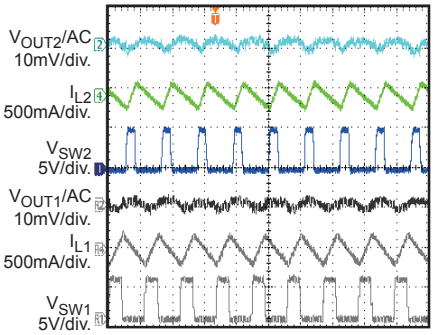
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT1} = 1.8V, V_{OUT2} = 1.2V, L1 = L2 = 1.5µH, f_{SW} = 2.25MHz, T_A = 25°C, unless otherwise noted.

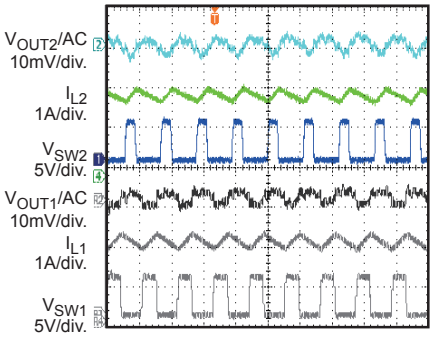
Steady State
I_{OUT1}=I_{OUT2}=0, AAM Mode



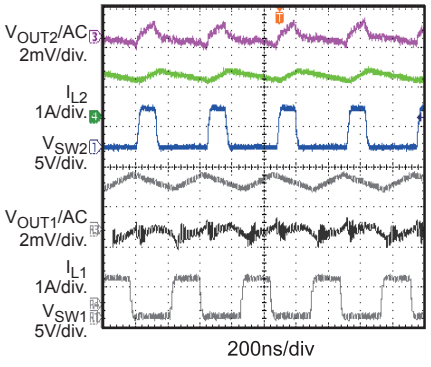
Steady State
I_{OUT1}=I_{OUT2}=0, Forced CCM Mode



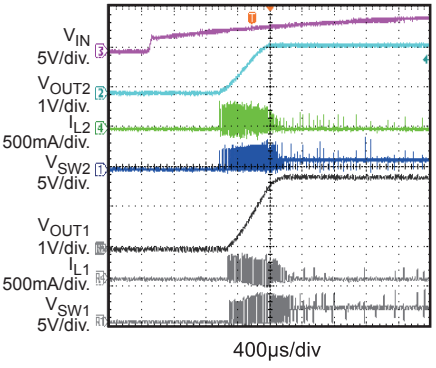
Steady State
I_{OUT1}=I_{OUT2}=2A



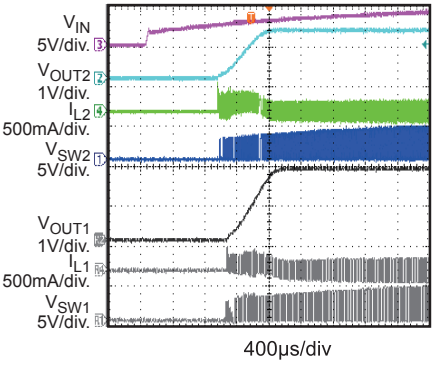
Steady State
I_{OUT1}=3A, I_{OUT2}=1A



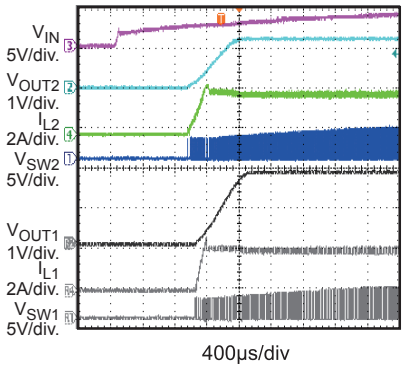
Start-Up through V_{IN}
I_{OUT1}=I_{OUT2}=0, AAM Mode



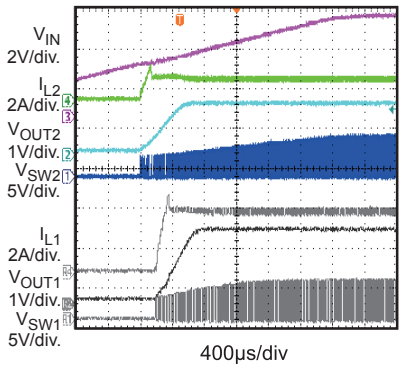
Start-Up through V_{IN}
I_{OUT1}=I_{OUT2}=0, Forced CCM Mode



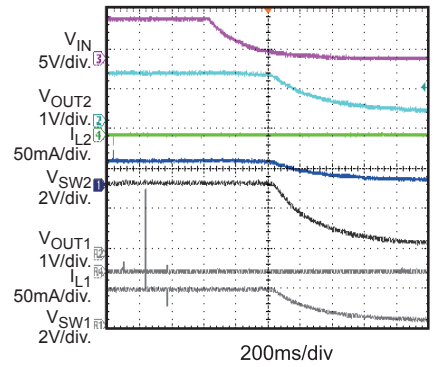
Start-Up through V_{IN}
I_{OUT1}=I_{OUT2}=2A



Start-Up through V_{IN}
I_{OUT1}=3A, II$_{OUT2}$=1A



Shutdown through V_{IN}
I_{OUT1}=I_{OUT2}=0, AAM Mode

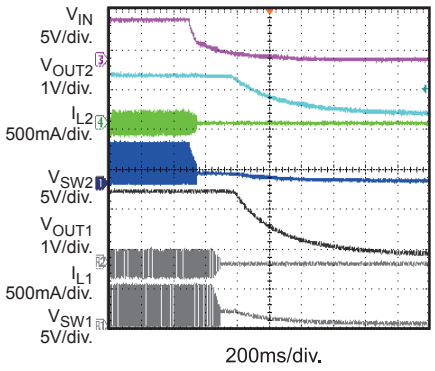


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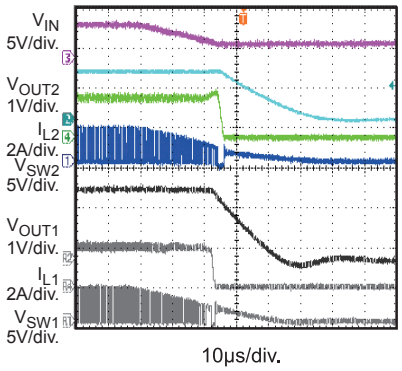
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT1} = 1.8V, V_{OUT2} = 1.2V, L1 = L2 = 1.5µH, f_{SW} = 2.25MHz, T_A = 25°C, unless otherwise noted.

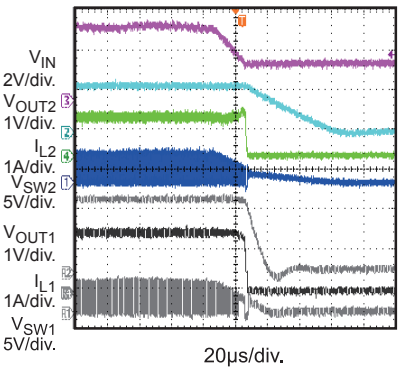
Shutdown through V_{IN}
I_{OUT1}=I_{OUT2}=0, Forced CCM Mode



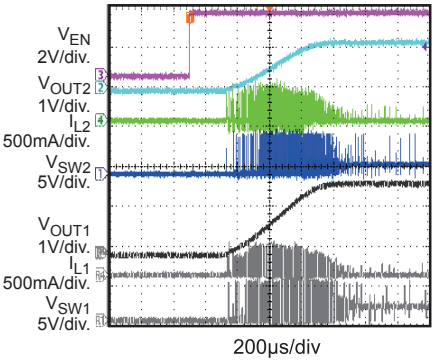
Shutdown through V_{IN}
I_{OUT1}=I_{OUT2}=2A



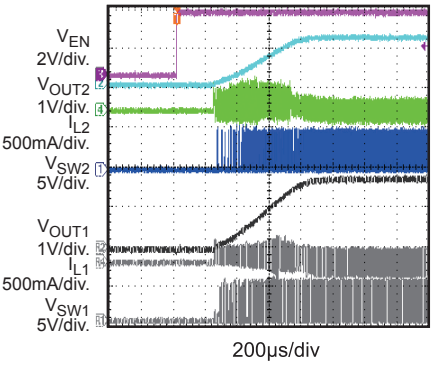
Shutdown through V_{IN}
I_{OUT1}=3A, I_{OUT2}=1A



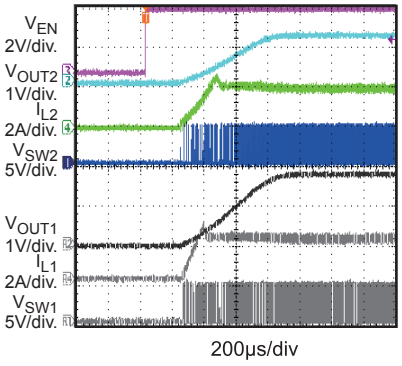
Start-Up through EN
I_{OUT1}=I_{OUT2}=0, AAM Mode



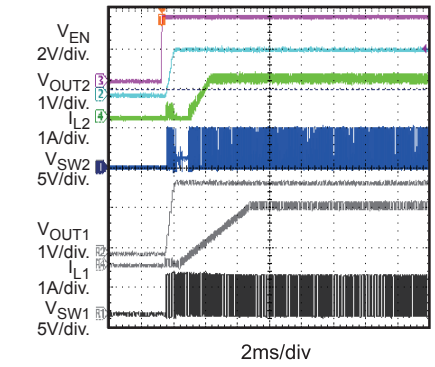
Start-Up through EN
I_{OUT1}=I_{OUT2}=0, Forced CCM Mode



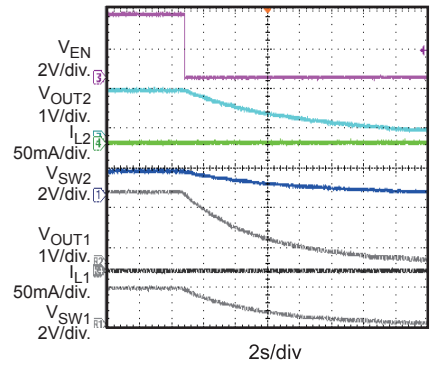
Start-Up through EN
I_{OUT1}=I_{OUT2}=2A



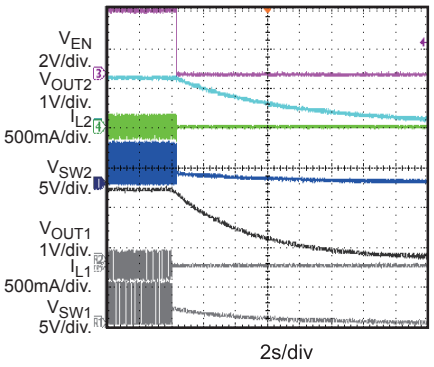
Start-Up through EN
I_{OUT1}=3A, I_{OUT2}=1A



Shutdown through EN
I_{OUT1}=I_{OUT2}=0, AAM Mode



Shutdown through EN
I_{OUT1}=I_{OUT2}=0, Forced CCM Mode



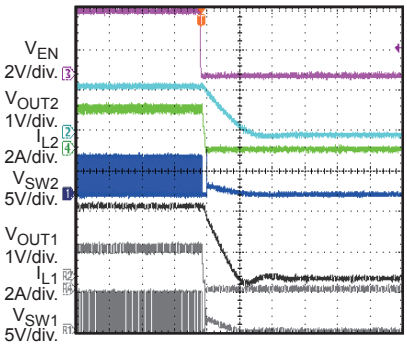
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TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT1} = 1.8V, V_{OUT2} = 1.2V, L1 = L2 = 1.5µH, f_{SW} = 2.25MHz, T_A = 25°C, unless otherwise noted.

Shutdown through EN

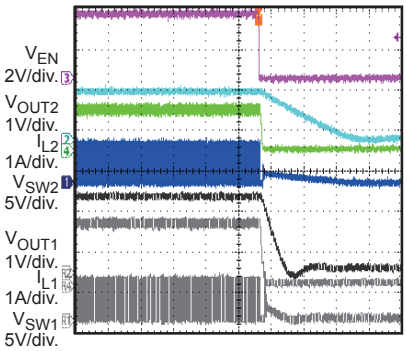
I_{OUT1}=I_{OUT2}=2A



20µs/div.

Shutdown through EN

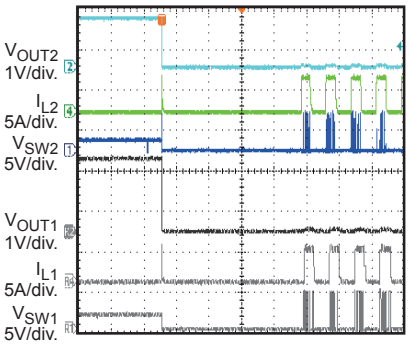
I_{OUT1}=3A, I_{OUT2}=1A



20µs/div.

SCP Entry

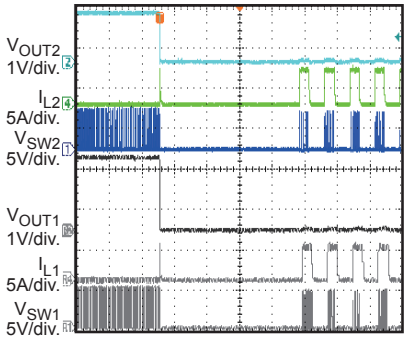
I_{OUT1}=I_{OUT2}=0, AAM Mode



2ms/div.

SCP Entry

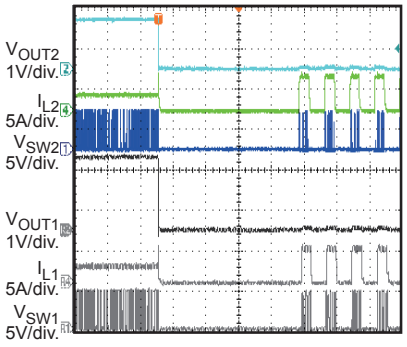
I_{OUT1}=I_{OUT2}=0, Forced CCM Mode



2ms/div

SCP Entry

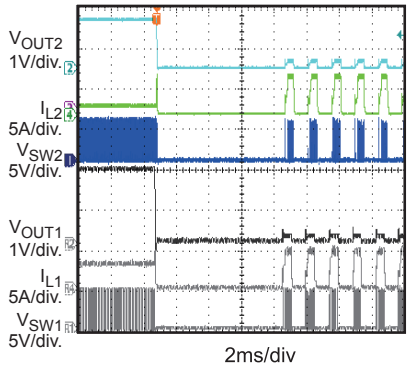
I_{OUT1}=I_{OUT2}=2A



2ms/div

SCP Entry

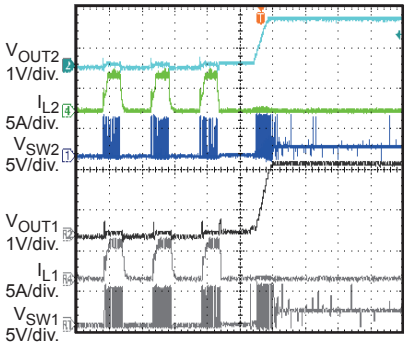
I_{OUT1}=3A, I_{OUT2}=1A



2ms/div

SCP Recovery

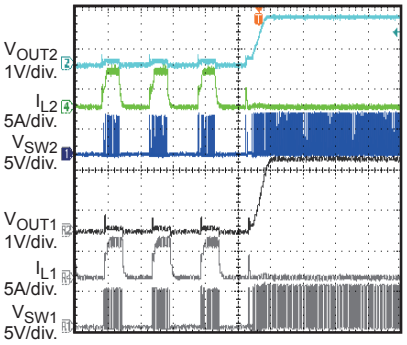
I_{OUT1}=I_{OUT2}=0, AAM Mode



1ms/div

SCP Recovery

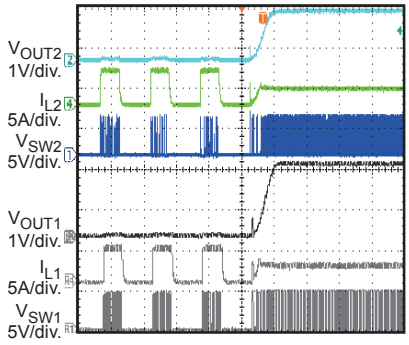
I_{OUT1}=I_{OUT2}=0, Forced CCM Mode



1ms/div

SCP Recovery

I_{OUT1}=I_{OUT2}=2A



1ms/div

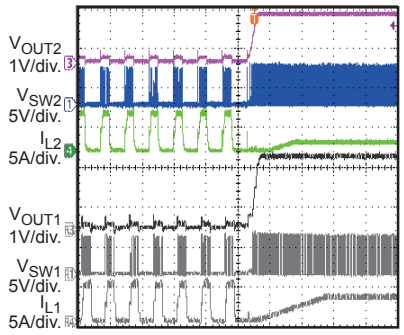
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TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

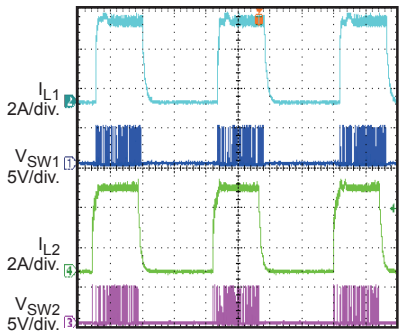
V_{IN} = 5V, V_{OUT1} = 1.8V, V_{OUT2} = 1.2V, L1 = L2 = 1.5µH, f_{SW} = 2.25MHz, T_A = 25°C, unless otherwise noted.

SCP Recovery

I_{OUT1}=3A, I_{OUT2}=1A

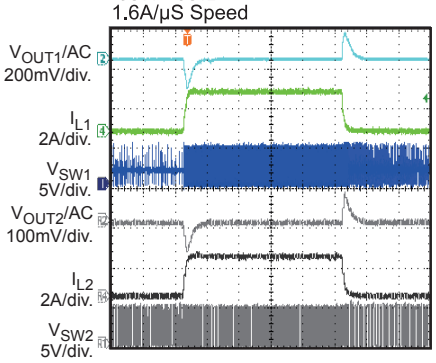


SCP Steady State



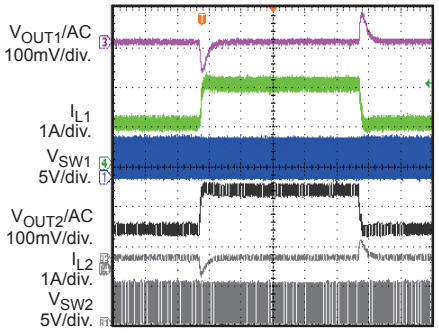
Load Transient

I_{OUT1}=I_{OUT2}=0 to 2A, AAM Mode, 1.6A/µS Speed



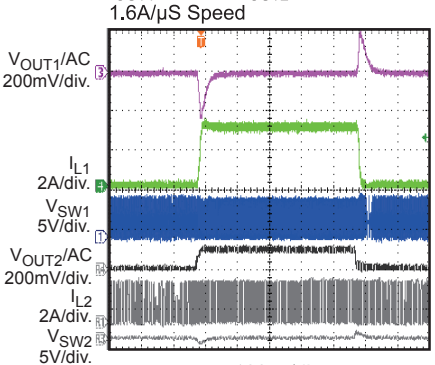
Load Transient

I_{OUT1}=I_{OUT2}=1 to 2A, AAM Mode, 1.6A/µS Speed



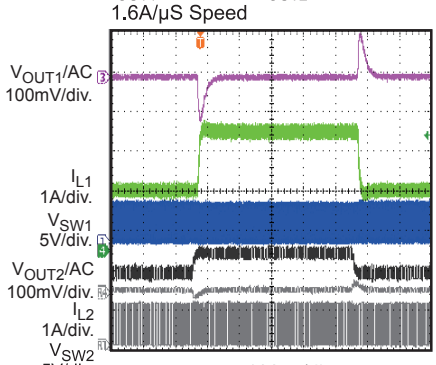
Load Transient

I_{OUT1}=0 to 3A, I_{OUT2}=0 to 1A, 1.6A/µS Speed



Load Transient

I_{OUT1}=1.5 to 3A, I_{OUT2}=0.5 to 1A, 1.6A/µS Speed



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PIN FUNCTIONS

QFN-18 (2mmx3mm) Pin #	QFN-18 (2.5mmx3.5mm) Pin #	Name	Description
1	2	PGND2	**Power ground of channel 2.** Connect PGND2 with larger copper areas to the negative terminals of the input and output capacitors. PGND2 must connect to PGND1 externally on board.
2	3	SW2	**Switch node connection to the inductor for channel 2.** SW2 connects to the internal high- and low-side power MOSFET switches of the channel 2 buck.
3	4	VIN2	**Input supply for channel 2.** Place a decoupling capacitor to ground close to VIN2 to reduce switching spikes.
4	5	SS2	**Soft start for channel 2.** Place a capacitor from SS2 to GND to set the soft-start time externally. Floating this pin will activate the internal default 0.5ms soft-start setting.
5	6	FB2	**Feedback for channel 2.** FB2 is the input to the error amplifier of channel 2. An external resistive divider connects FB2 between the output and ground. The voltage on FB2 compares to the internal 0.6V reference to set the regulation voltage of channel 2.
6	7	AGND	**Analog ground.** Connect AGND to PGND externally.
7	8	VCC	**Power supply to the internal regulator for both channels.** Decouple with a 0.1μF to 1μF capacitor between VCC and AGND. Connect VIN1, VIN2, VCC together externally, it is not recommended to power them from separated power supply.
8	9	CCM	**AAM or forced CCM control.** Pull CCM high to enter forced CCM mode; pull CCM low to enter AAM mode at light load. Do not float CCM.
9	10	FB1	**Feedback for channel 1.** FB1 is the input to the error amplifier of channel 1. An external resistive divider connects FB1 between the output and GND. The voltage on FB1 compares to the internal 0.6V reference to set the regulation voltage of channel 1.
10	11	SS1	**Soft start for channel 1.** Place a capacitor from SS1 to GND to set the soft-start time externally. Floating this pin will activate the internal default 0.5ms soft-start setting.
11	12	VIN1	**Input supply for channel 1.** Place a decoupling capacitor to ground close to VIN1 to reduce switching spikes.
12	13	SW1	**Switch node connection to the inductor for channel 1.** SW1 connects to the internal high- and low-side power MOSFET switches of the channel 1 buck.
13	14	PGND1	**Power ground of channel 1.** Connect PGND1 with larger copper areas to the negative terminals of the input and output capacitors. PGND1 must connect to PGND2 externally on board.
14	15	PG1	**Power good for channel 1.** The output of PG1 is an open drain, a pull-up resistor to power source is needed if used. PG1 is pulled high when V_{FB1} reaches 90% of V_{REF}, it is pulled low to GND if V_{FB1} drops to 82% of V_{REF}.

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PIN FUNCTIONS *(continued)*

QFN-18 (2mmx3mm) Pin #	QFN-18 (2.5mmx3.5mm) Pin #	Name	Description
15	16	EN1	**Enable control for channel 1.** Pull EN1 below the specified threshold 0.4V to shut the chip down. Pull EN above the specified threshold to 1.6V enable the chip. Do not float EN1.
16	17	FREQ	**Frequency set.** Connect a resistor to GND to set the switching frequency. The switching frequency can be synchronized by an external clock via FREQ.
17	18	EN2	**Enable control for channel 2.** Pull EN2 below the specified threshold 0.4V to shut the chip down. Pull EN above the specified threshold to 1.6V enable the chip. Do not float EN2.
18	1	PG2	**Power good for channel 2.** The output of PG2 is an open drain, a pull-up resistor to power source is needed if used. PG2 is pulled high when V_{FB2} reaches 90% of V_{REF}, it is pulled low to GND if V_{FB2} drops to 82% of V_{REF}.

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BLOCK DIAGRAM

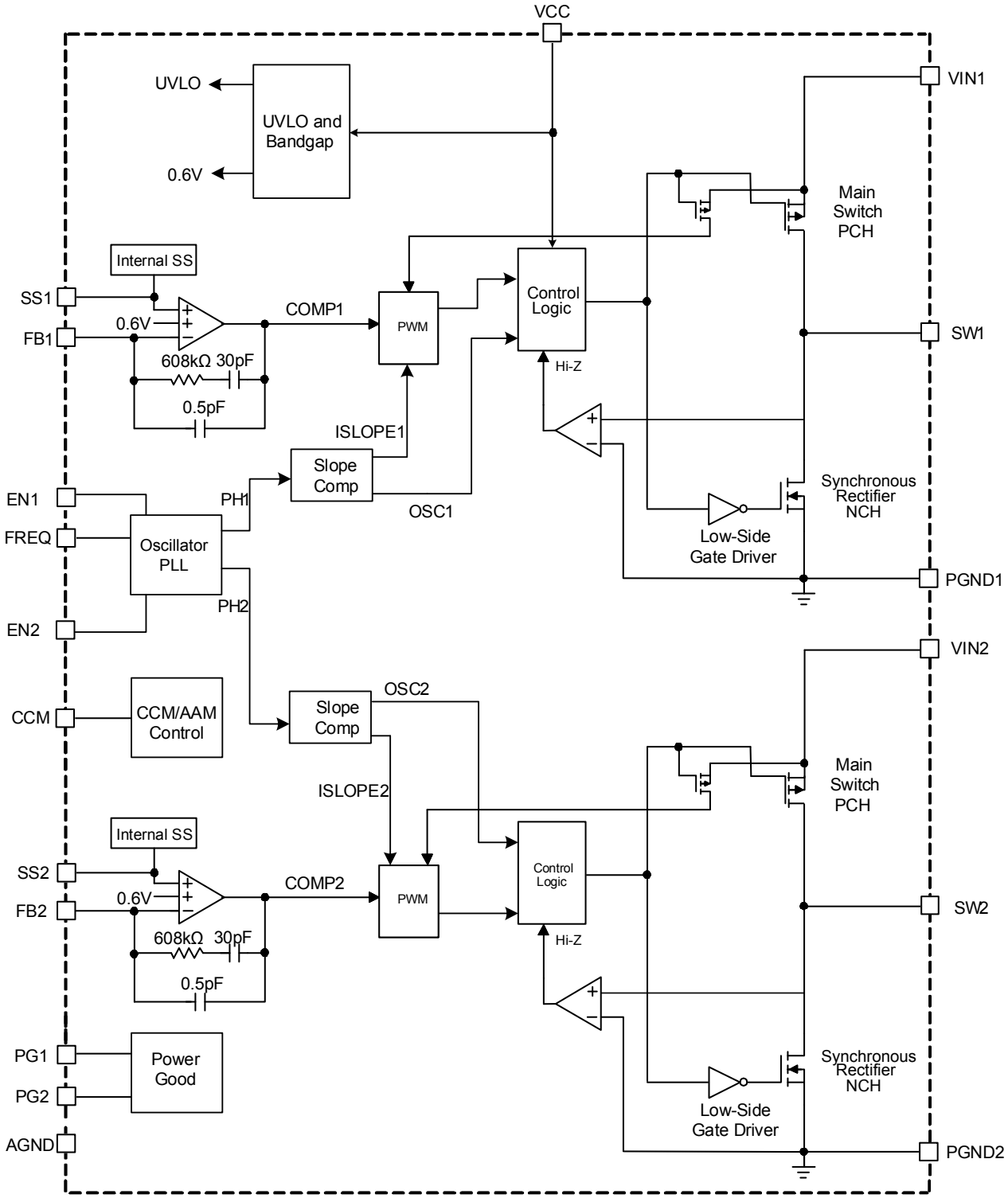


Figure 1: Functional Block Diagram

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OPERATION

The MPQ2166 is a fully integrated, dual-channel, synchronous, step-down converter. Both channels use peak-current-mode control with internal compensation for fast transient response and cycle-to-cycle current limit.

The MPQ2166 is optimized for low-voltage, portable applications where efficiency and small size are critical.

180° Out-of-Phase Operation

The MPQ2166 operates the two channels in 180° out-of-phase operation to reduce input current ripple, so a smaller input bypass capacitor can be used. When both channels operate in CCM, two internal clocks are used (see Figure 2). The high-side MOSFET is turned on at the clock rising edge of the corresponding channel.

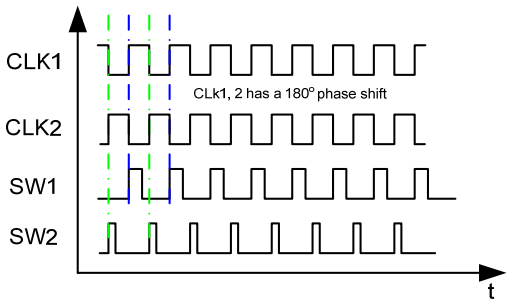


Figure 2: 180° Out-of-Phase Operation

At low dropout, when the switching frequency is stretched out for each channel, the MPQ2166 runs at a fixed-off time with its own independent switching frequency. After the input voltage rises high again, frequency stretch mode ends, and PWM mode resumes and synchronizes with the master oscillator for out-of-phase operation.

Light-Load Operation

In light-load condition, the MPQ2166 can work in two different operating modes by setting CCM to different statuses.

The MPQ2166 works in forced continuous conduction mode (CCM) when the CCM pin is pulled higher than 1.6V. The MPQ2166 works with fixed frequency from no load to full load in this mode. The advantage of CCM is the controllable frequency and lower output ripple at light load.

The shutdown current in forced CCM mode (50μA at 3.3V) is much higher than AAM mode due to some internal circuits are active. It is recommended to pull CCM pin LOW when part is shutdown if the high shutdown current is cared.

The MPQ2166 works in advanced asynchronous mode (AAM) when CCM is pulled lower than 0.4V. AAM is used to optimize efficiency during light-load and no-load conditions.

When AAM mode is enabled, the MPQ2166 first enters non-synchronous operation as the inductor current approaches zero at light load. If the load decreases further or is at no load, which makes the internal COMP voltage (V_{COMP}) decrease to the set value, then the MPQ2166 enters AAM. In AAM, the internal clock is reset whenever V_{COMP} crosses over the set value, and the crossover time is taken as the benchmark of the next clock. When the load increases and V_{COMP} is higher than the set value, the operation mode is in DCM or CCM, which has a constant switching frequency.

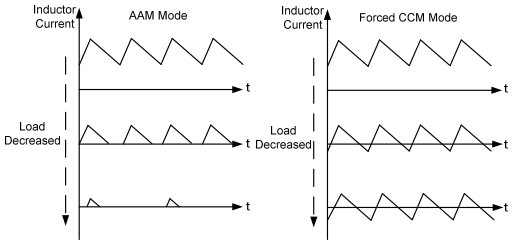


Figure 3: AAM Mode and Forced CCM Mode

Enable

EN is a digital control pin that turns the regulator on and off.

When EN is pulled below falling threshold voltage 0.4V, the chip is shutdown. Forcing this pin above EN rising threshold voltage 1.6V turns on the part. Do not float EN.

Soft Start (SS)

The MPQ2166 has a built-in soft start that ramps up the output voltage at a controlled slew rate, preventing an overshoot at start-up. The soft-start time is about 0.5ms, typically.

The soft-start time can also be programmed by an external capacitor connected to SS, shown in Equation (1):

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$$t_{SS}(ms) = \frac{C_{SS}(nF) \times V_{RFF}(V)}{I_{SS}(\mu A)} \quad (1)$$

Where C_{SS} is the external SS capacitor, V_{REF} is the internal reference voltage (0.6V), and I_{SS} is the 3.2μA SS charge current.

Oscillator and SYNC Function

The internal oscillator frequency is set by a single external resistor (R_{FREQ}) connected between FREQ and ground. The frequency setting resistor should be located close to the device. The relationship between the oscillator frequency and R_{FREQ} is shown in Figure 4.

F_{SW} vs. R_{FREQ}

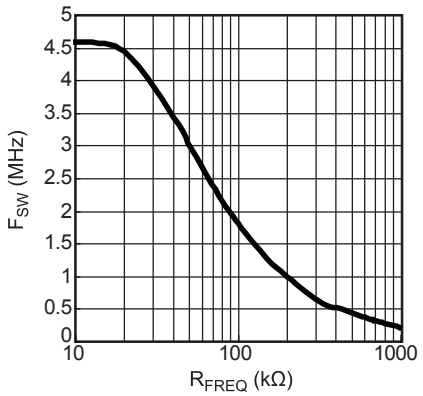


Figure 4: F_{SW} vs. R_{FREQ}

FREQ can also be used to synchronize the internal oscillator to an external clock. The rising edge of the channel 1 clock is synchronized to the external clock rising edge, while the channel 2 clock remains at 180° out-of-phase to channel 1. The recommended external SYNC frequency is in the range of 350kHz to 3MHz. While there is no pulse width requirement, note that there is always parasitic capacitance of the pad there, so if the pulse width is too short, a clear rising and falling edge may not be seen. The pulse is recommended to be longer than 100ns.

Ensure to add the external SYNC clock (350kHz to 3MHz) before the device starts up and keep the SYNC clock until the device is off. Constant high, constant low and high/low transition for the SYNC signal are all not allowed during the operation.

Power Good (PG)

The MPQ2166 has one power good (PG) output to indicate normal operation after the soft-start time. PG is the open drain of an internal MOSFET. It should be connected to VIN, VCC, or an external voltage source through a resistor (i.e.: 100kΩ). After the input voltage is applied, the MOSFET is turned on and PG is pulled to GND before SS is ready. After the FB voltage reaches 90% of the reference voltage (V_{REF}), the MOSFET turns off and PG is pulled high by an external voltage source. When the FB voltage drops to 82% of V_{REF}, the PG voltage is pulled to GND to indicate a failure output.

Current Limit and Short Circuit

Each channel of the MPQ2166 has a typical 4.5A current limit for the high-side switch. When FB drops to 60% of the reference value and SS is OK, the MPQ2166 treats this as a short and attempts to recover with hiccup mode.

In hiccup mode, the MPQ2166 disables the output power stage, slowly discharges the soft-start cap, and soft starts automatically. If the short-circuit condition still remains, the MPQ2166 repeats this operation cycle until the short circuit is removed and the output rises back to regulation levels.

Dropout Operation

The MPQ2166 allows the high-side switch to remain on for more than one switching cycle and increases the duty cycle while the input voltage drops down to the output voltage. When the duty cycle reaches 100%, the high-side switch is on to deliver current to the output up to its current limit. The output voltage is then the difference between the input voltage and the voltage drop across the main switch and the inductor.

Thermal Shutdown

The MPQ2166 has thermal protection by monitoring the IC temperature internally. This function prevents the chip from operating at an exceedingly high temperature. If the junction temperature exceeds the threshold value (typically 175°C), it shuts down the whole chip. This is a non-latch protection. There is a 40°C hysteresis. Once the junction temperature drops to about 135°C, the device resumes operation by initiating a soft start.

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APPLICATION INFORMATION

Setting the Output Voltage

The external resistor divider sets the output voltage. The feedback resistor (R1) also sets the feedback loop bandwidth with the internal compensation. The T-type network is recommended. (see Figure 5).

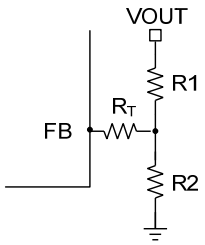


Figure 5: T-type Feedback Network

R_T+R1 is used to set the loop bandwidth. The lower R_T+R1 is, the higher the bandwidth. However, a high bandwidth may cause an insufficient phase margin, resulting in loop instability. Therefore, a proper R_T value is required to make a trade off between the bandwidth and phase margin. Table 1 lists the recommended feedback resistor and R_T values for output voltages.

R1 is estimated to be 100kΩ. R2 can then be calculated with Equation (2):

$$R2 = \frac{R1}{\frac{V_{OUT}}{0.6V} - 1} \quad (2)$$

Table 1: Resistor Selection vs. Output Voltage Setting

V_{OUT}	R_T	R1	R2
1.2V	100kΩ	100kΩ	100kΩ
1.5V	100kΩ	100kΩ	66.5kΩ
1.8V	100kΩ	100kΩ	49.9kΩ
2.5V	100kΩ	100kΩ	31.6kΩ
3.3V	100kΩ	100kΩ	22.1kΩ

In the case of ceramic capacitors used as output capacitors (C_O), the feedback loop bandwidth (f_C) is no higher than 1/10 of the switching frequency for optimal transient performance and good phase margin. If an electrolytic capacitor is used, the loop bandwidth is no higher than 1/4 of the ESR zero frequency (f_{ESR}). f_{ESR} can be calculated by Equation (3):

$$f_{ESR} = \frac{1}{2\pi \times R_{ESR} \times C_O} \quad (3)$$

For example, choose f_C = 80kHz with a ceramic capacitor and C_O = 22µF.

Inductor Selection

An inductor with a DC current rating at least 25% higher than the maximum load current is recommended for most applications. For best efficiency, the inductor DC resistance should be less than 20mΩ. For most designs, the inductance value can be derived from Equation (4):

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times f_{SW}} \quad (4)$$

Where ΔI_L is inductor ripple current. Choose the inductor ripple current to be approximately 30% of the maximum load current.

The maximum inductor peak current can be calculated with Equation (5):

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2} \quad (5)$$

Input Capacitor Selection

The input capacitor reduces the surge current drawn from the input and the switching noise from the device. The input capacitor impedance at the switching frequency should be less than the input source impedance to prevent high-frequency switching current from passing to the input source. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients. For most applications, a 22µF capacitor is sufficient.

Output Capacitor Selection

The output capacitor (C_O) keeps the output voltage ripple small and ensures a stable regulation loop. The output capacitor impedance should be low at the switching frequency. Use ceramic capacitors with X5R or X7R dielectrics. If an electrolytic capacitor is used, pay close attention to the output ripple voltage, extra heating, and the selection of the upper feedback resistor due to the large ESR of electrolytic capacitor (refer to the Setting the

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Output Voltage section). The output ripple (ΔV_{OUT}) can be approximated with Equation (6):

$$\Delta V_{OUT} = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times L \times f_{SW}} \times (ESR + \frac{1}{8 \times f_{SW} \times Co}) \quad (6)$$

Power Dissipation

IC power dissipation is important in circuit design, not only because of efficiency concerns, but also because of the chip's thermal requirements. Several parameters influence power dissipation, such as conduction loss (Cond), dead time (DT), switching loss (SW), MOSFET driver current (DR), and supply current (S).

Based on these parameters, we can estimate the power loss with Equation (7):

$$P_{LOSS} = P_{Cond} + P_{DT} + P_{SW} + P_{DR} + P_S \quad (7)$$

Thermal Regulation

Changes in IC temperatures change the electrical characteristics, especially when the temperature exceeds the IC's recommended operating range. Managing the IC's temperature requires additional considerations to ensure that the IC runs within the maximum allowable temperature junction. Specific layout designs can improve the thermal profile while limiting costs to either the efficiency or operating range.

For the MPQ2166, connect the ground pin on the package to a ground plane on top of the PCB to use this plane as a heat sink. Connect this ground plane to the ground planes beneath the IC using vias to improve heat dissipation. However, given that these ground planes can introduce unwanted EMI noise and occupy valuable PCB space, design their size and shape to match the thermal resistance requirement.

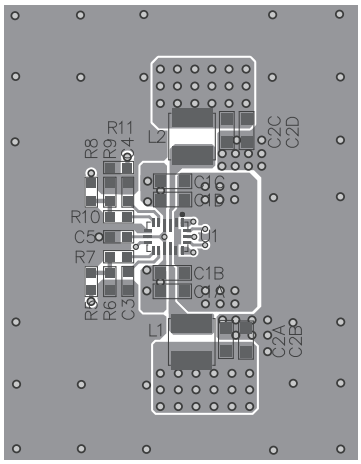
Connecting the ground pin to a heat sink cannot guarantee that the IC will not exceed its recommended temperature limits (i.e.: the ambient temperature exceeds the IC's temperature limits). If the ambient air temperature approaches the IC's temperature limit, the IC can be de-rated to operate using less power and help prevent thermal damage and unwanted electrical characteristics.

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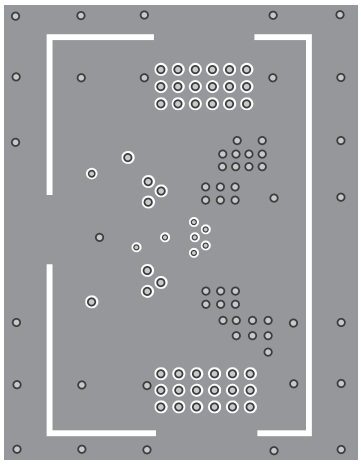
PCB Layout Guidelines[7]

Efficient PCB layout is critical for stable operation. A four-layer layout is strongly recommended to achieve better thermal performance. For best results, refer to Figure 6 and follow the guidelines below.

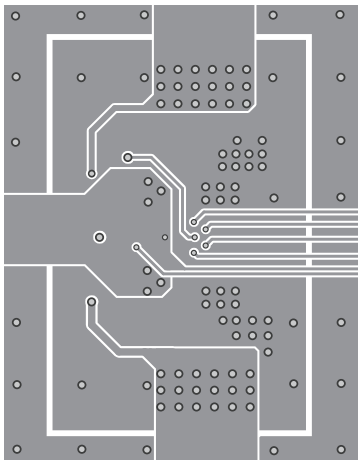
1. Place the high-current paths (PGND, VIN, and SW) very close to the device with short, direct, and wide traces.
2. Place input capacitors on both VIN sides and as close to VIN and PGND as possible.
3. Place the decoupling capacitor as close to VCC and AGND as possible.
4. Keep the switching node SW short and away from the feedback network.
5. Place the external feedback resistors next to FB. Do not place vias on the FB trace.
6. Connect PGND to a large copper area to achieve better thermal performance.



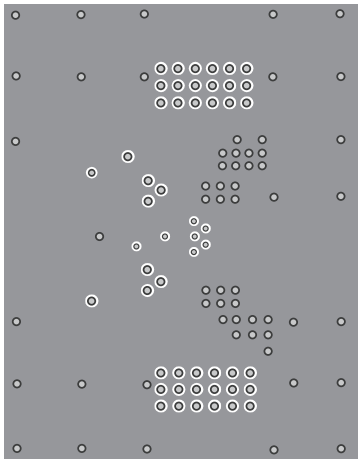
Top Layer



Inner Layer 1



Inner Layer 2



Bottom Layer

Figure 6: Recommended PCB Layout

NOTE:

7) The recommended PCB layout is based on Figure 7.

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TYPICAL APPLICATION CIRCUITS

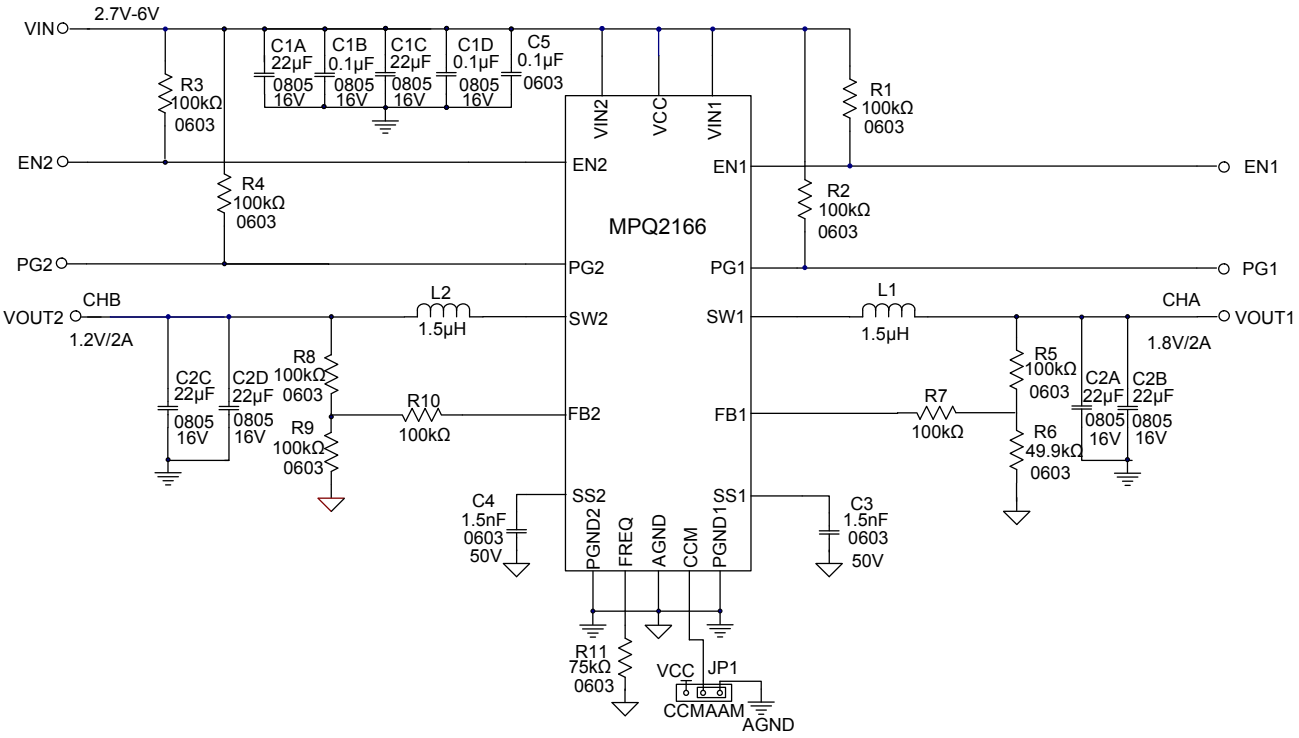


Figure 7: 2A/2A Application Circuit

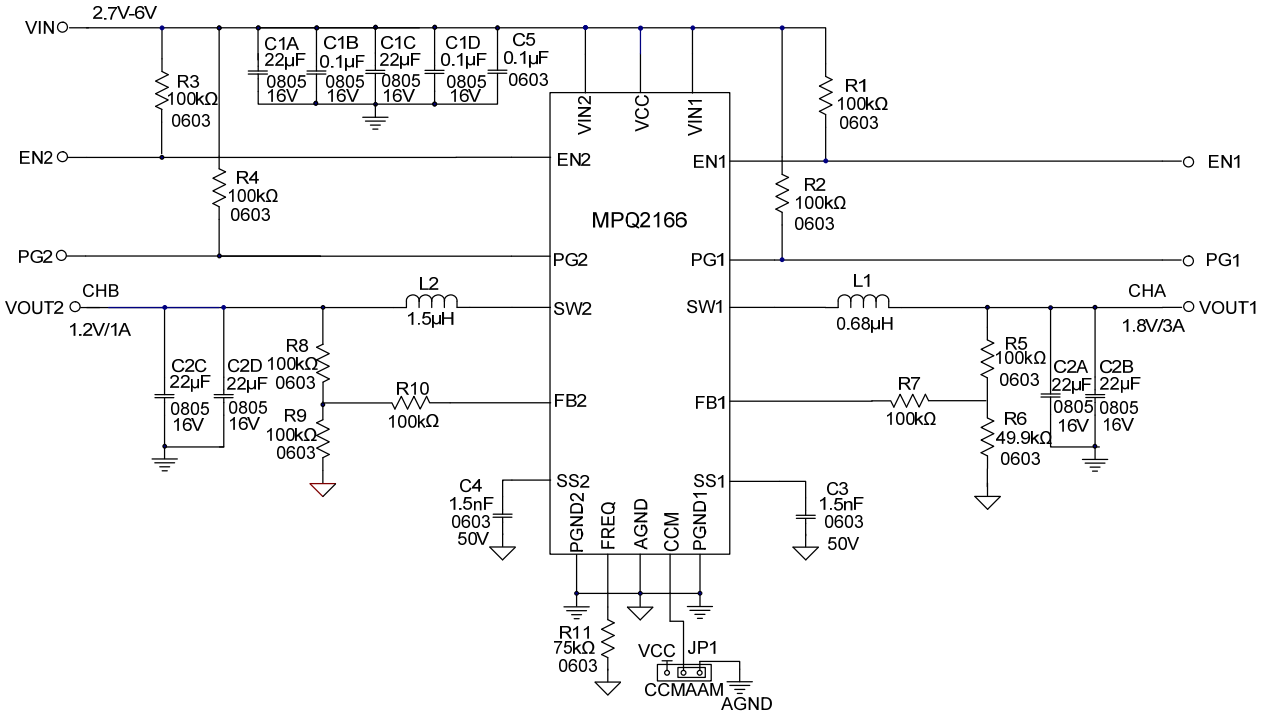
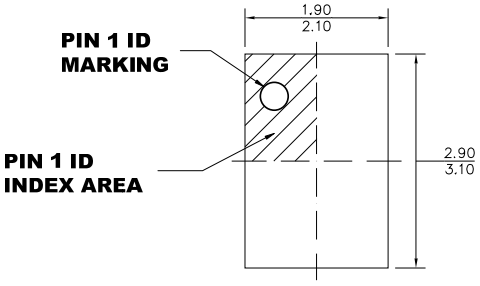


Figure 8: 3A/1A Application Circuit

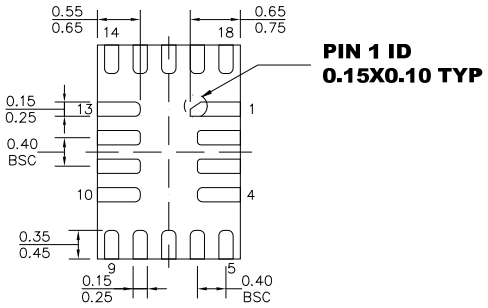
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PACKAGE INFORMATION

QFN-18 (2mmx3mm)
Non-Wettable Flank



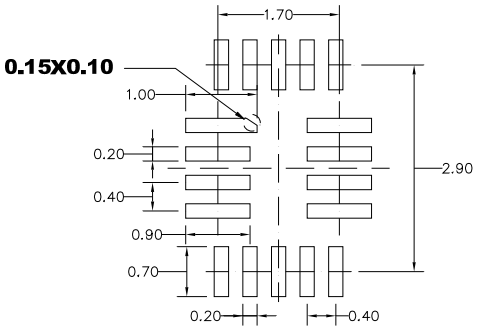
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

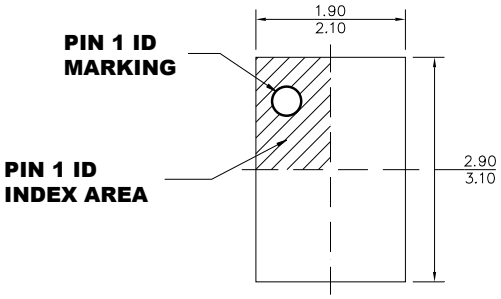
NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

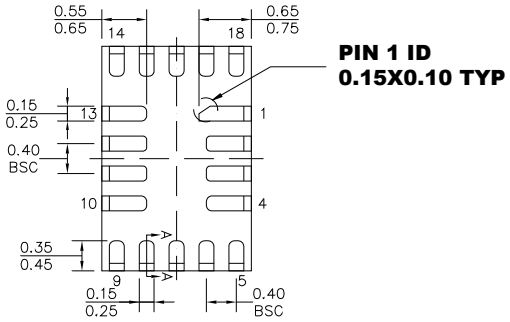
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PACKAGE INFORMATION *(continued)*

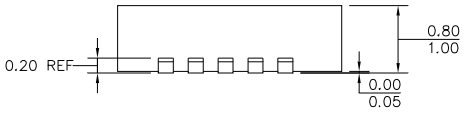
QFN-18 (2mmx3mm)
Wettable Flank



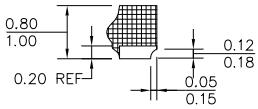
TOP VIEW



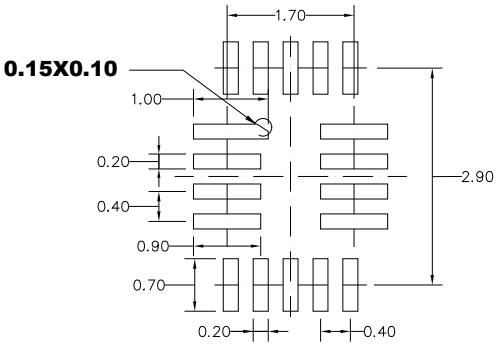
BOTTOM VIEW



SIDE VIEW



SECTION A-A



RECOMMENDED LAND PATTERN

NOTE:

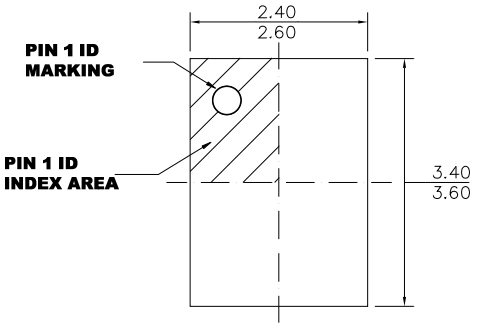
1) THE LEAD SIDE IS WETTABLE.
2) ALL DIMENSIONS ARE IN MILLIMETERS.
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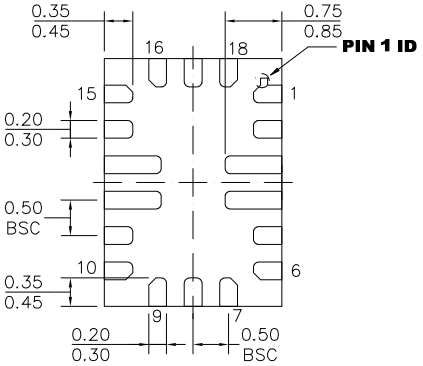
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QFN-18 (2.5mmx3.5mm)

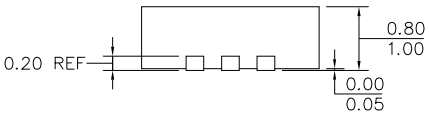
Non-Wettable Flank



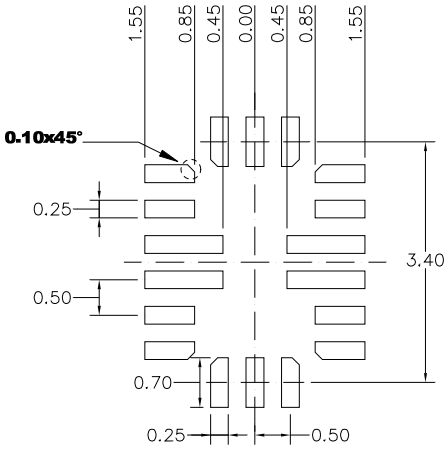
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

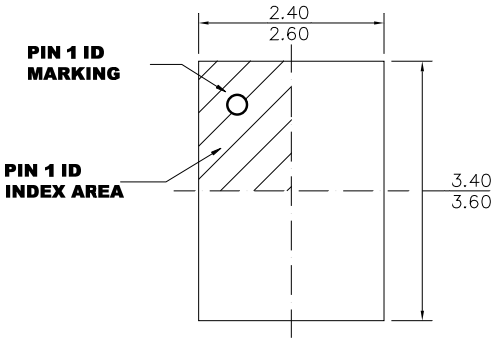
NOTE:

1) LAND PATTERNS OF PIN3, 4, 12 AND 13 HAVE THE SAME LENGTH AND WIDTH.
2) ALL DIMENSIONS ARE IN MILLIMETERS.
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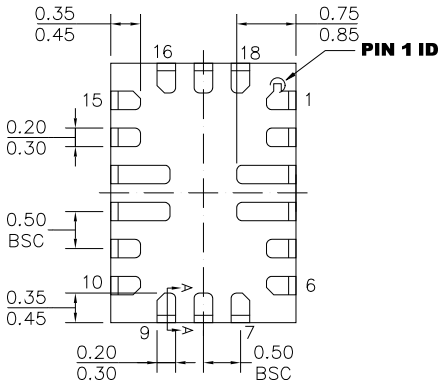
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PACKAGE INFORMATION *(continued)*

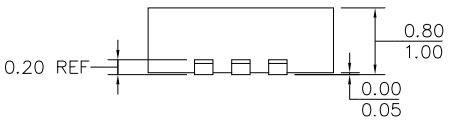
QFN-18 (2.5mmx3.5mm)
Wettable Flank



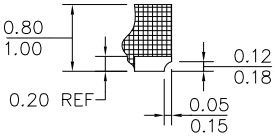
TOP VIEW



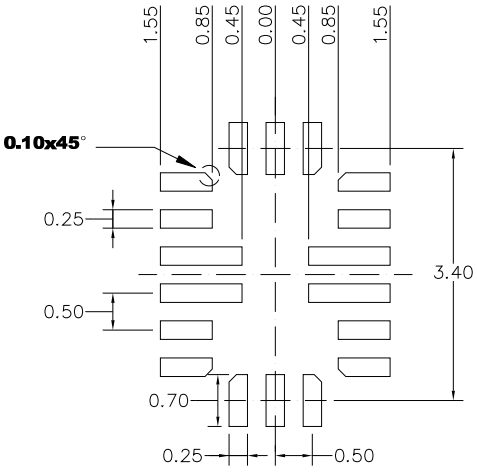
BOTTOM VIEW



SIDE VIEW



SECTION A-A



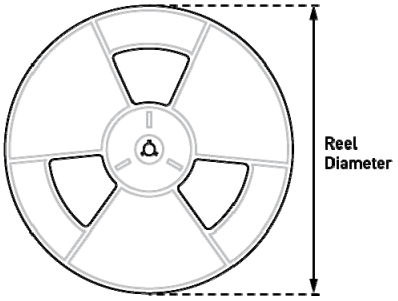
RECOMMENDED LAND PATTERN

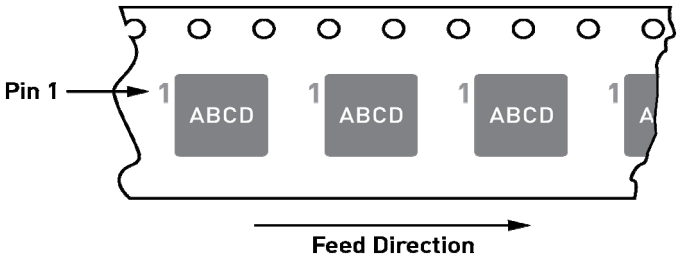
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CARRIER INFORMATION





Part Number	Package Description	Quantity /Reel	Quantity/ Tube*	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MPQ2166GD-Z	QFN-18 (2mmx3mm)	5000	N/A	13in.	12mm	8mm
MPQ2166GD-AEC1-Z						
MPQ2166GDE-AEC1-Z						
MPQ2166GRH-Z	QFN-18 (2.5mmx3.5mm)					
MPQ2166GRH-AEC1-Z						
MPQ2166GRHE-AEC1-Z						

* N/A indicates “not available” in tubes. For 500 piece tape & reel prototype quantities, see factory. (Order code for 500 piece partial reel is “-P”, tape & reel dimensions same as full reel.)

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Revision History

Revision #	Revision Date	Description	Pages Updated
1.2	4/30/2020	Add three auto relative application: Automotive Infotainment Automotive Clusters Automotive Telematics	P1
		Add MSL rating, ESD and Carrier information.	P3,P5,P29
		Add the thermal resister data on EVB result.	P5
		Update the efficiency, load and line regulation based on the new version of MPQ2166.	P9, P10
		Add the comments: Ensure to add the external SYNC clock (350kHz to 3MHz) before the device starts up and keep the SYNC clock until the device is off. Constant high, constant low and high/low transition for the SYNC signal are all not allowed during the operation.	P20
		Add the specific descriptions for the pin functions.	P16,P17
		Add the compensation parameters and modify V_{CC} connection in the functional block.	P18
		Add the “Enable” description in OPERATION part	P19
		Add the “Thermal shutdown” description in OPERATION part	P20

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