MPQ2483

Industrial/Automotive-Grade 55V, 2.5A Programmable Frequency LED Driver Avaiable in AEC-Q100

The Future of Analog IC Technology

DESCRIPTION

The MPQ2483 is a 55V, LED driver suitable for either step-down or inverting step-up/down applications. It achieves 2.5A peak current over a wide input supply range with excellent load and line regulation. Current mode operation provides fast transient response and eases loop stabilization. Fault condition protection includes thermal shutdown, cycle-by-cycle peak current limiting, output over voltage protection, open strings protection and output short circuit protection.

The MPQ2483 incorporates both DC and PWM dimming onto a single control pin. The separate input reference ground pin allows for direct enable and/or dimming control for a positive to negative power conversion.

The MPQ2483 requires a minimum number of readily available standard external components and is available in a 10-pin 3mm x 3mm QFN and SOIC 14-pin packages.

FEATURES

- 2.5A Maximum Peak Current
- Buck or Buck-Boost Modes
- Wide 4.5V to 55V Operating Input Range
- 0.28Ω Internal Power MOSFET Switch
- Analog and PWM Dimming
- 0.198V Reference Voltage
- 5μA Shutdown Mode
- Stable with Low ESR Capacitors
- Cycle-by-Cycle Over Current Protection
- Thermal Shutdown, Over Voltage, Short Circuit & Open String Protection
- AEC-Q100 Qualified

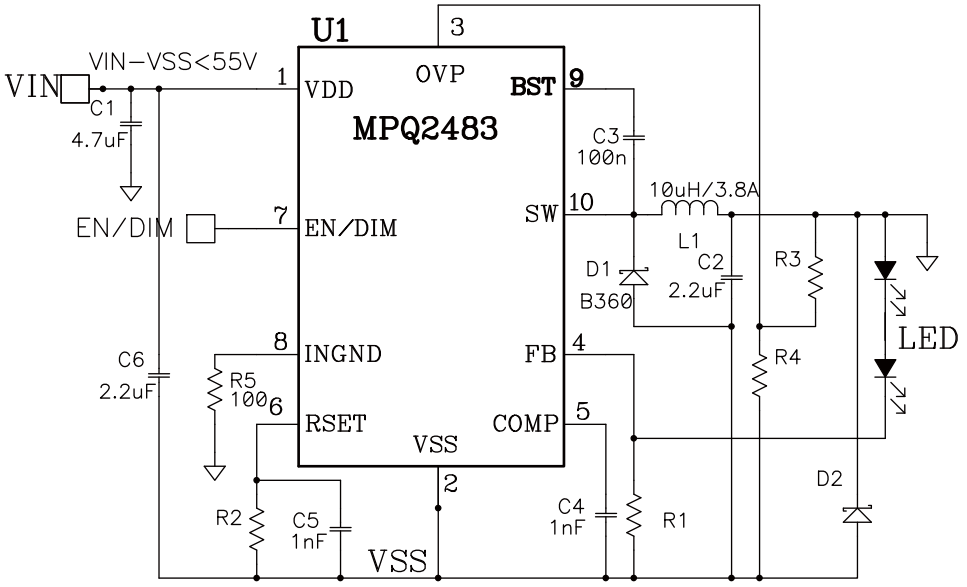
APPLICATIONS

- General LED Illumination
- LCD Backlight Panels
- Automotive Lighting

All MPS parts are lead-free, halogen free, and adhere to the RoHS directive. For MPS green status, please visit MPS website under Quality Assurance.

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TYPICAL APPLICATION



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ORDERING INFORMATION

Part Number	Package	Top Marking
MPQ2483DQ*	QFN-10(3mmx3mm)	*See Below*
MPQ2483DQ-AEC1	QFN-10(3mmx3mm)	
MPQ2483DS**	SOIC-14	*See Below*
MPQ2483DS-AEC1	SOIC-14	

* For Tape & Reel, add suffix –Z (e.g. MPQ2483DQ–Z).
For RoHS compliant packaging, add suffix –LF (e.g. MPQ2483DQ–LF–Z)

** For Tape & Reel, add suffix –Z (e.g. MPQ2483DS–Z).
For RoHS compliant packaging, add suffix –LF (e.g. MPQ2483DS–LF–Z)

TOP MARKING (MPQ2483DQ)

9MYW
LLL

9M: product code of MPQ2483DQ;
Y: year code;
W: week code:
LLL: lot number;

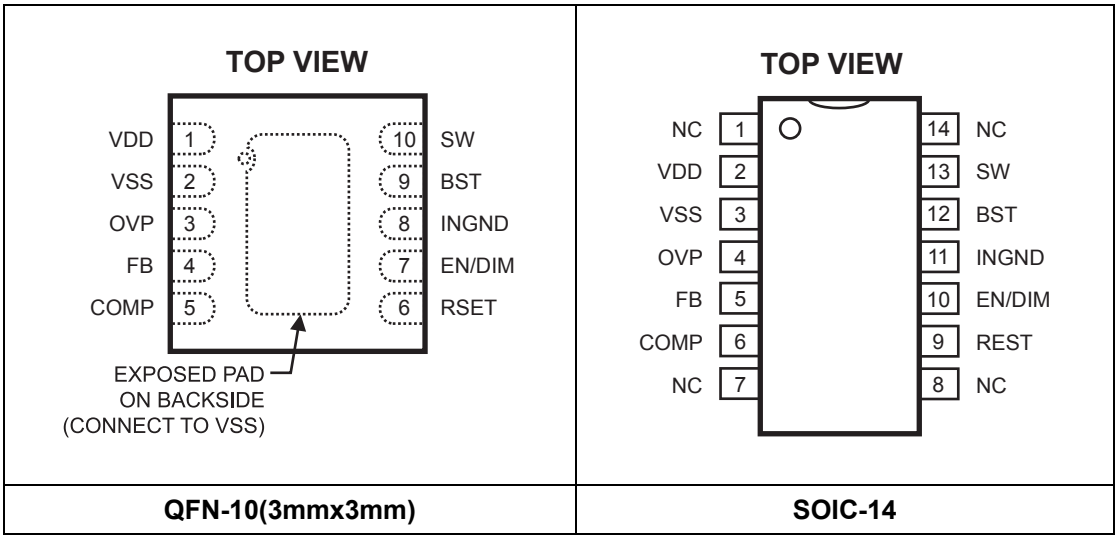
TOP MARKING (MPQ2483DS)

MPS YYWW
MP2483DS
LLLLLLLLL

MP2483DS: product code of MPQ2483DS;
MPS: MPS prefix;
YY: year code;
WW: week code:
LLL: lot number;

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PACKAGE REFERENCE



QFN-10(3mmx3mm)	SOIC-14

ABSOLUTE MAXIMUM RATINGS (1)

V_{DD} – V_{SS} (0°C≤T_J≤125°C) 60V
V_{DD} – V_{SS} (-40°C≤T_J<0°C) 58V
V_{SW} – V_{SS} .....–0.3V to V_{DD} + 0.3V
V_{BST} ..... V_{SW} + 6V
V_{OVP} – V_{SS} .....–0.3V to +6V
V_{EN} – V_{INGND}.....–0.3V to +6V
V_{DIM} – V_{INGND}.....–0.3V to +6V
V_{INGND} – V_{SS}.....–0.3V to 60V
Other pins – V_{SS}.....–0.3V to 6V
Continuous Power Dissipation (T_A = +25°C) (2)
QFN-10(3mmx3mm)……...2.5W
SOIC-14…….. ……..1.45W
Junction Temperature.....150°C
Lead Temperature .....260°C
Storage Temperature..... –65°C to +150°C

Recommended Operating Conditions (3)

Supply Voltage V_{DD} – V_{SS}:
0°C≤T_J≤125°C……...4.5V to 55V
-40°C≤T_J<0°C……..4.5V to 50V
Operating Junction Temp. (T_J). -40°C to +125°C

Thermal Resistance (4)

	θ_{JA}	θ_{JC}	
QFN-10(3mmx3mm)	50	12	°C/W
SOIC-14	86	38	°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device function is not guaranteed outside of the recommended operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

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ELECTRICAL CHARACTERISTICES

V_{IN} = 12V, T_J = -40°C to +125°C, all voltages with respect to V_{SS}. Typical values are at T_J = +25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Feedback Voltage	V_{FB}	4.5V ≤ V_{IN} ≤ 12V	0.180	0.198	0.215	V
		12V ≤ V_{IN} ≤ 55V	0.170	0.198	0.220	
Feedback Current	I_{FB}	V_{FB} = 0.22V			1.0	uA
Switch-On Resistance	$R_{DS(ON)}$			280		mΩ
Switch Leakage		V_{EN} = 0V, V_{SW} = 0V			2	μA
Current Limit (5)	I_{LIM}	-40°C ≤ T_J ≤ 125°C Duty cycle ≤ 61%	2.7	3.0		A
Oscillator Frequency	f_{SW}	V_{FB} = 0.19V, Rset=200kΩ		0.25		MHz
Default oscillator frequency	$f_{SW_default}$	V_{FB} = 0.19V, Rset open	1.0	1.35	1.7	MHz
Fold-back Frequency		V_{FB} = 0V, V_{OVP}=0V, Rset open		250		kHz
Maximum Duty Cycle		V_{FB} = 0.19V		90		%
Minimum On-Time	t_{ON}			100		ns
Under Voltage Lockout Threshold Rising			2.9	3.3	3.7	V
Under Voltage Lockout Threshold Hysteresis				200		mV
EN Input Current		V_{EN} = 2V		1.4		μA
EN OFF Threshold (w/Respect to INGND)		V_{EN} Falling	0.4			V
EN ON Threshold (w/Respect to INGND)		V_{EN} Rising			0.6	V
Minimum EN Dimming Threshold		V_{FB} = 0V	0.55	0.7	0.85	V
Maximum EN Dimming Threshold		V_{FB} = 0.2V	1.2	1.4	1.55	V
Supply Current (Quiescent)	I_Q	V_{EN} = 2V, V_{FB} = 1V		0.8	1.5	mA
Shutdown Current	I_{off}	V_{EN}=0V		3.4	20	μA
Thermal Shutdown				150		°C
Open LED OV Threshold	V_{OVP_th}		1.1	1.2	1.3	V
Open LED OV Hysteresis	V_{OVP_hys}			60		mV

Notes:

5) Derived from part characterization. Not tested in production.

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PIN FUNCTIONS

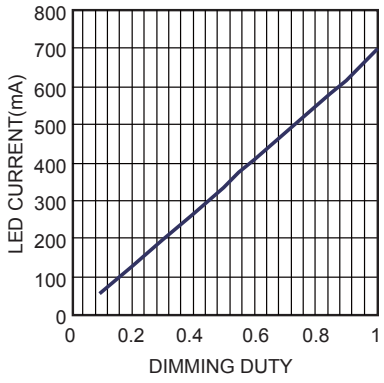
SOIC-14 Pin #	QFN-10 (3mmx3mm) Pin #	Name	Description
2	1	VDD	Supply Voltage. The MPQ2483 operates from a +4.5V to +55V unregulated input (with respect to VSS). C1 & C2 is needed to prevent large voltage spikes from appearing at the input.
3	2	VSS	Power Return Pin. Connect to the lowest potential in the circuit, which is typically the anode of the Schottky rectifier. This pin is the voltage reference for the regulated output voltage. For this reason care must be taken in its layout. This node should be placed outside of the D1 to C1 & C2 ground path to prevent switching current spikes from inducing voltage noise into the part. The exposed pad is also connected to this pin.
4	3	OVP	Over Voltage Protection Pin. Use a voltage divider to program OVP threshold. When the OVP pin voltage reaches the shutdown threshold 1.2V, the switch will be turned off and will recover when OVP voltage decreases sufficiently. When the OVP pin voltage (with respect to VSS) is lower than 0.4V and FB pin voltage is lower than 0.1V, the chip recognizes this as short circuit condition and the operating frequency will be folded back. Program the OVP pin voltage from 0.4V to 1.2V for normal operation.
5	4	FB	LED Current Feedback Input. MPQ2483 regulates the voltage across the current sensing resistor between FB and VSS. Connect the current sensing resistor from the bottom of the LED strings to VSS. The FB pin is connected to the bottom of the LED strings. The regulation voltage is 0.198V.
6	5	COMP	Output of error amplifier. Connect a 1nF or larger capacitor on COMP to improve the stability and to provide a soft on at start up and PWM dimming.
9	6	RSET	Frequency Set Pin. Connect a resistor to VSS to set the switching frequency and a 1nF capacitor to VSS to bypass the noise. Leaving this pin open gets a default operating frequency 1.35MHz.
10	7	EN/DIM	On/Off Control Input and Dimming Command Input. A voltage greater than 0.6V will turn on the chip. Both DC and PWM dimming are implemented on this pin. When the EN/DIM pin voltage (with respect to INGND) rises from 0.7V to 1.4V, the LED current will change from 0% to 100% of the maximum LED current. To use PWM dimming, apply a 100Hz to 2kHz square wave signal with amplitude greater than 1.4V to this pin.
11	8	INGND	Input Ground Reference. This pin is the reference for the EN/DIM signal.
12	9	BST	Bootstrap. A capacitor is connected between SW and BST pin to form a floating supply across the power switch driver. A 100nF or larger ceramic capacitor is recommended to provide sufficient energy to drive the power switch's gate above the supply voltage.
13	10	SW	Switch Output. SW is the source of the internal MOSFET switch. Connect this pin to the power inductor and the cathode of the Schottky rectifier.
1,7,8,14		NC	No Connection.
			Exposed pad should be connected to VSS in step up/down mode.

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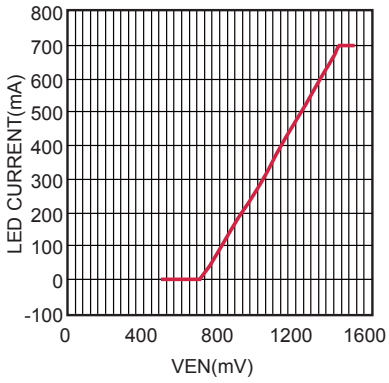
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN}=20V, I_{LED}=0.7A, two 3W LED in series, step down application, unless otherwise noted.

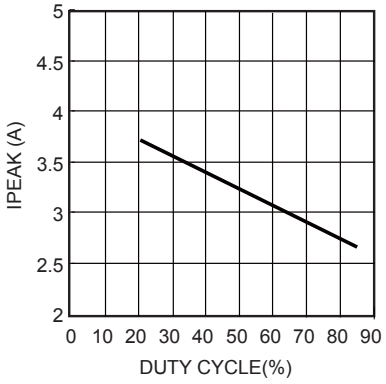
LED current vs. Dimming Duty



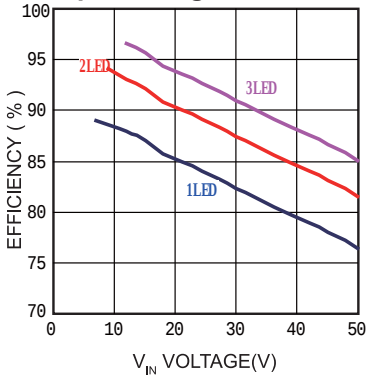
LED Current vs. VEN



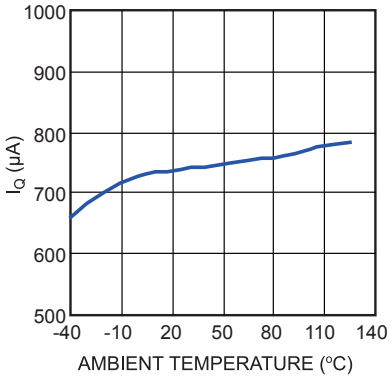
Ipeak vs. Duty



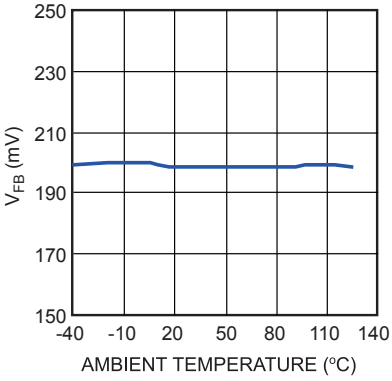
Efficiency vs. Input Voltage



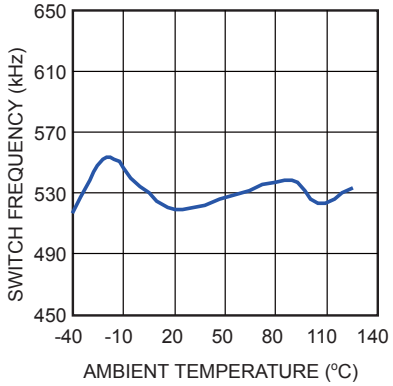
I_Q vs. Temperature



V_{FB} vs. Temperature



F_{SW} vs. Temperature

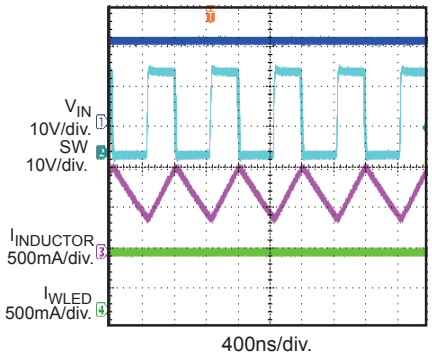


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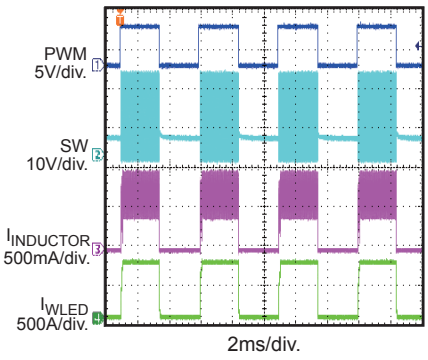
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN}=20V, I_{LED}=0.7A, two 3W LED in series, step down application, unless otherwise noted.

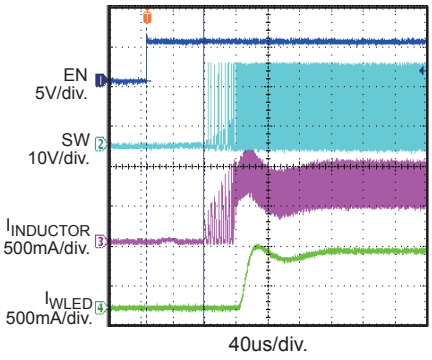
Steady State



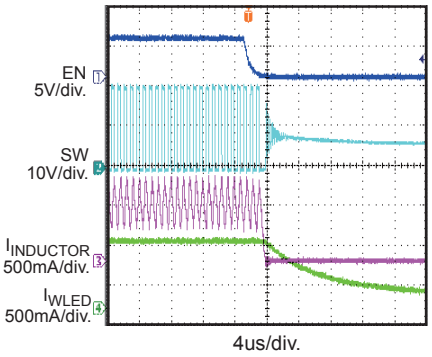
PWM Dimming



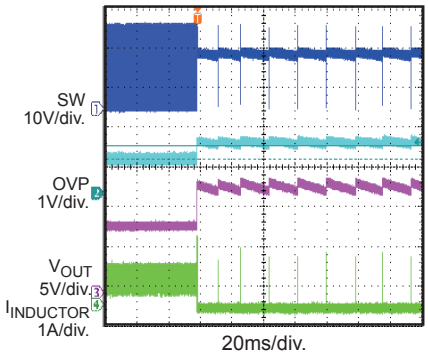
EN on



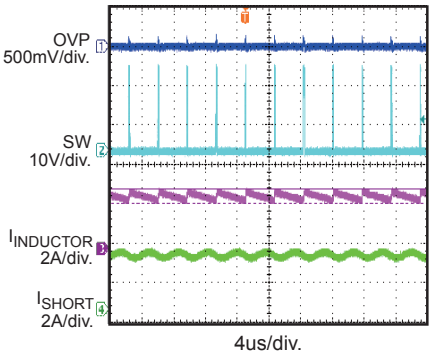
EN off



Open LED Protection



Short Circuit Protection (short LED+ to INGND)

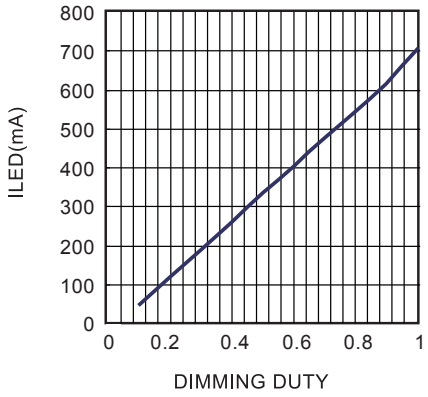


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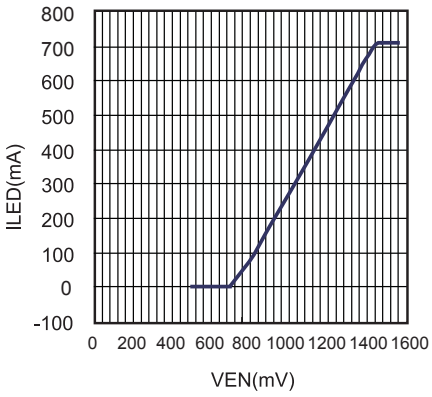
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN}=20V, I_{LED}=0.7A, seven 3W LED in series, Buck-boost application, referred to V_{SS}, unless otherwise noted

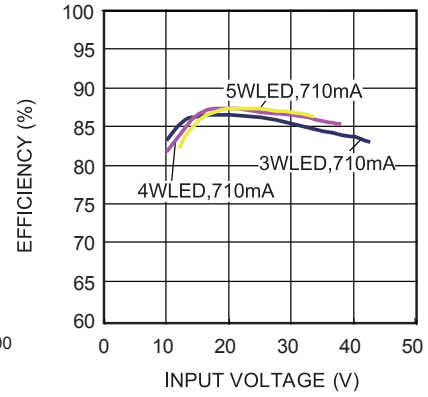
ILED vs. Dimming Duty



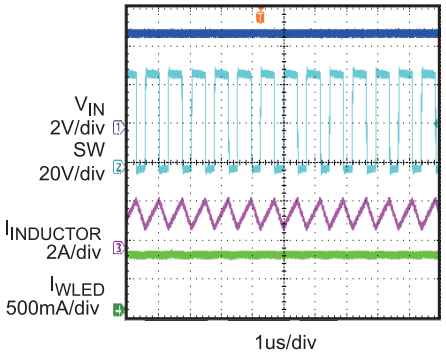
ILED vs. VEN



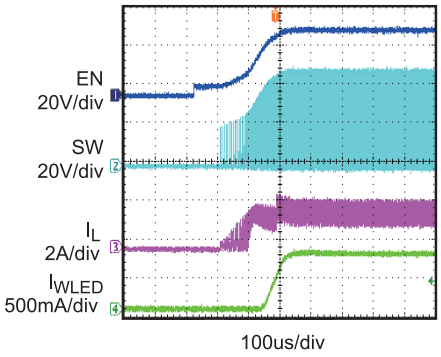
Efficiency vs. Input Voltage



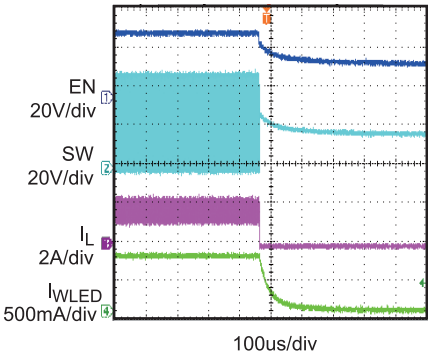
Steady state



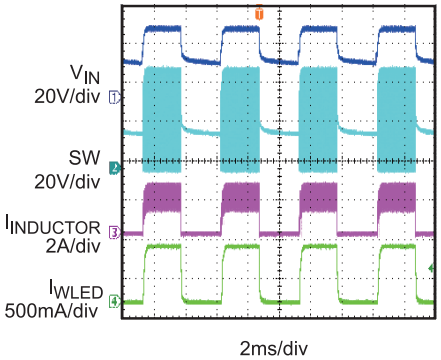
EN on



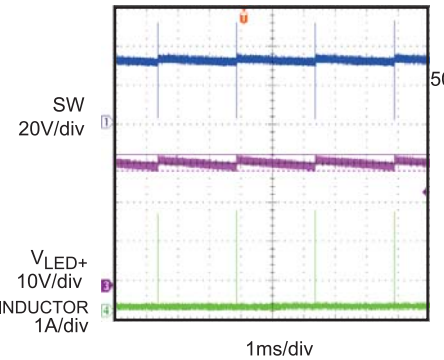
EN off



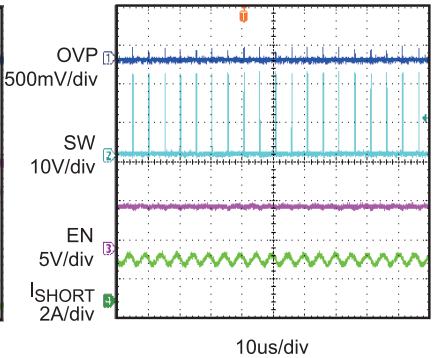
PWM dimming



Open LED Protection



Short Circuit Protection (short LED + to VSS)



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FUNCTIONAL BLOCK DIAGRAM

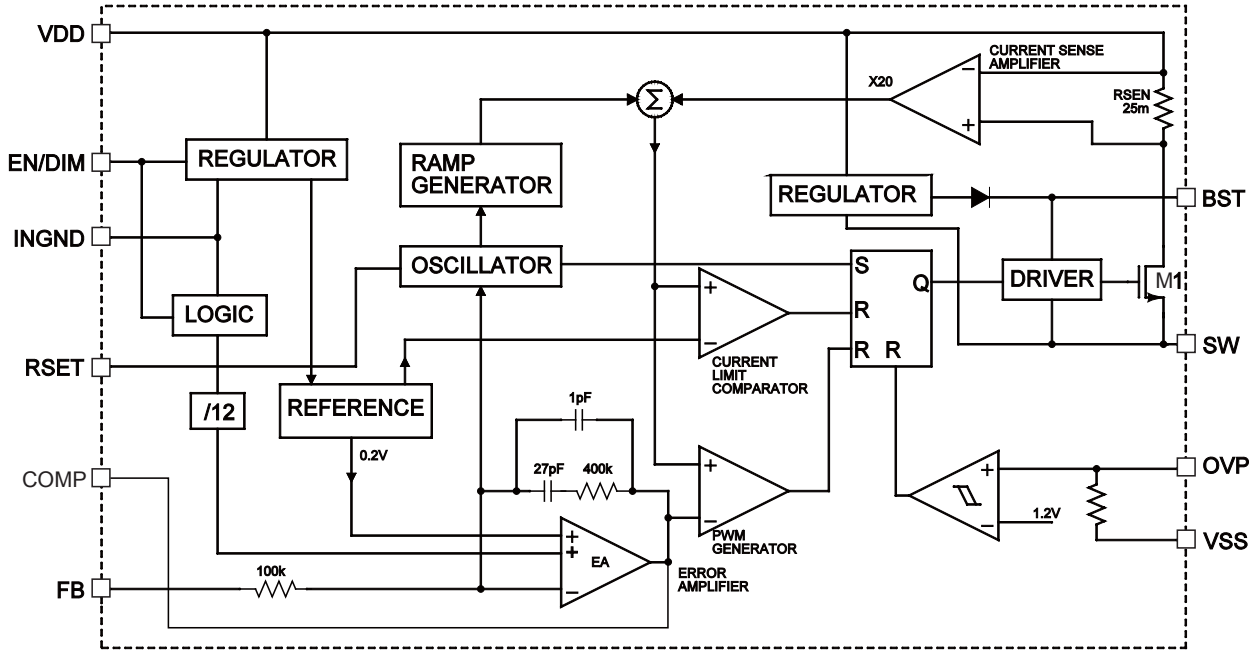


Figure 1: Functional Block Diagram

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OPERATION

The MPQ2483 is a current mode regulator. The EA output voltage is proportional to the peak inductor current.

At the beginning of a cycle, M1(Fig1) is off. The EA output voltage is higher than the current sense amplifier output, and the current comparator's output is low. The rising edge of the 1.35MHz CLK signal sets the RS Flip-Flop. Its output turns on M1(Fig1) thus connecting the SW pin and inductor to the input supply.

The increasing inductor current is sensed and amplified by the Current Sense Amplifier. Ramp compensation is summed to the Current Sense Amplifier output and compared to the Error Amplifier output by the PWM Comparator. When the sum of the Current Sense Amplifier output and the Slope Compensation signal exceeds the EA output voltage, the RS Flip-Flop is reset and M1 is turned off. The external Schottky rectifier diode (D1) conducts the inductor current.

If the sum of the Current Sense Amplifier output and the Slope Compensation signal does not exceed the EA output for a whole cycle, then the falling edge of the CLK resets the Flip-Flop.

The output of the Error Amplifier integrates the voltage difference between the feedback and the 0.198V reference. The polarity is a FB pin voltage lower than 0.198V increases the EA output voltage. Since the EA output voltage is proportional to the peak inductor current, an increase in its voltage also increases the current delivered to the output.

Open LED Protection

If the LED is open, there is no voltage on the FB pin. The duty cycle will increase until OVP-VSS reaches the shutdown threshold set by the external resistor divider. The top switch will turn off till the voltage OVP-VSS decreases sufficiently.

Dimming Control

The MPQ2483 allows both DC and PWM dimming. When the voltage on EN is less than 0.6V, the chip is turned off. For analog dimming, when the voltage on EN is from 0.7V to 1.4V, the LED current will change from 0% to 100% of the maximum LED current. If the voltage on EN pin is higher than 1.4V, maximum LED current will be generated. For PWM dimming, its amplitude (VDIM – VINGND) must exceed 1.4V. The PWM frequency is recommended in range of 100Hz to 2kHz to get a good dimming linearity.

Output Short Circuit Protection

The MPQ2483 integrates output short circuit protection. When the output is shorted to VSS, the voltage on OVP pin which detects the output voltage gets smaller than 0.4V, and FB pin senses no voltage (<0.1V) as no current goes through the LED. At this condition, the operating frequency is folded back to decrease the power consumption.

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APPLICATION INFORMATION

Setting the LED Current

The external resistor is used to set the maximum LED current (see the schematic on front page) through the use of the equation:

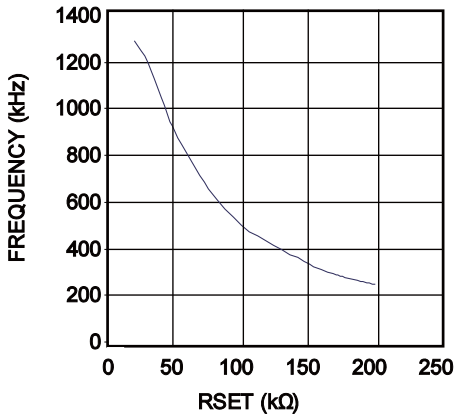
$$R_{SENSE} = \frac{0.198V}{I_{LED}}$$

Setting the Operating Frequency

The resistor on Rset pin is used to set the operating frequency. A 1nF capacitor is recommended to bypass this pin to GND.

The relationship between the operating frequency and the Rest resistor is as the following curve. A 20kΩ to 200kΩ Rset resistor is recommended, which sets the operating frequency from around 1.35MHz to 250 kHz. Leaving the RSET pin open will set the operating frequency to the default operating frequency 1.35MHz.

Frequency vs. RSET



Selecting the Inductor

(Step-Down Applications, see Figure 3)

A 1μH to 47μH inductor with a DC current rating of at least 25% percent higher than the maximum load current is recommended for most applications. For high efficiency, the inductor's DC resistance should be less than 200mΩ. Refer to Table 2 for suggested surface mount inductors. For most designs, the required inductance value can be derived from the following equation.

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times f_{SW}}$$

Where ΔI_L is the inductor ripple current.

Choose the inductor ripple current to be 30% of the maximum load current. The maximum inductor peak current is calculated from:

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2}$$

Under light load conditions below 100mA, a larger inductance is recommended for improved efficiency.

Also note that the maximum recommended load current is 2A if the duty cycle exceeds 35%.

Selecting the Input Capacitor

The input capacitor reduces the surge current drawn from the input supply and the switching noise from the device. The input capacitor impedance at the switching frequency should be less than the input source impedance to prevent high frequency switching current from passing through the input. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients. For most applications, a 4.7μF capacitor is sufficient.

Selecting the Output Capacitor

The output capacitor keeps the output voltage ripple small and ensures feedback loop stable. The output capacitor impedance should be low at the switching frequency. Ceramic capacitors with X5R or X7R dielectrics are recommended for their low ESR characteristics. For most applications, a 2.2μF ceramic capacitor will be sufficient.

Selecting VSS-INGND Positive Spike Protection Circuit

In some applications, such as input power on, LED+ short circuit from LED+ to VSS in both Buck-Boost and Boost applications, when INGND and VSS are not connected together, there is potential risk that VSS-INGND has >0.3V (allowed maximum positive voltage) positive spike, which might cause false actions, even damage.

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To clamp VSS-INGND positive spike, it is recommended to add a 100Ω resistor from INGND pin to input GND to clamp the current from VSS to INGND, and to add a low forward voltage schottky diode (B160) from VSS to INGND to clamp the negative oscillation voltage. The voltage rating of the schottky diode should be higher than the OVP voltage set by R3 and R4 (Figure 5).

To extremely high VSS-INGND spike conditions, bigger R2 is needed to clamp the current, and higher current rating D2 is needed too.

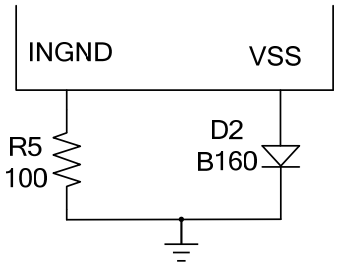


Figure 2: VSS-INGND Positive Spike Protection Circuit

Selecting FB Positive Spike Protection Circuit

In applications when there is possibility that FB has abnormal high positive spike, such as Load transients from high to low or LED+ short circuit from LED+ to LED- in Buck, Boost and Buck-Boost applications. In applications above, once FB has abnormal high positive spike, false actions, even damage might happen.

To protect FB from too high positive spike, it is recommended to add a 10kohm resistor between LED- to FB to clamp the current from LED- to FB, and to add a <2V voltage range zener diode (BZT52C2V0) from FB to VSS to clamp the voltage from FB to VSS.

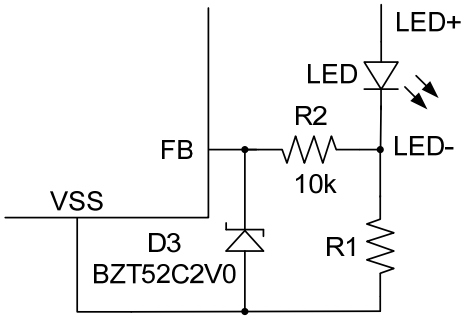


Figure 3: FB Positive Spike Protection Circuit

PC Board Layout

The high current paths (VSS, VDD and SW) should be placed very close to the device with short, direct and wide traces. The input capacitor needs to be as close as possible to the VDD and VSS pins. The external feedback resistors should be placed next to the FB pin. Keep the switch node traces short and away from the feedback network.

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Table 2—Suggested Surface Mount Inductors

Manufacturer	Part Number	Inductance(μH)	Max DCR(Ω)	Current Rating (A)	Dimensions L x W x H (mm^3)
Toko	DS84LC-B1015AS-4R7N	4.7	0.038	3.8	8.2*8.1*3.7
Cooper	DR73-4R7-R	4.7	0.0297	3.78	7.35*7.35*3.3
TDK	SLF7055T-4R7N3R1-3PF	4.7	0.028	3.6	7.1*7.3*5.5

TYPICAL APPLICATION CIRCUITS

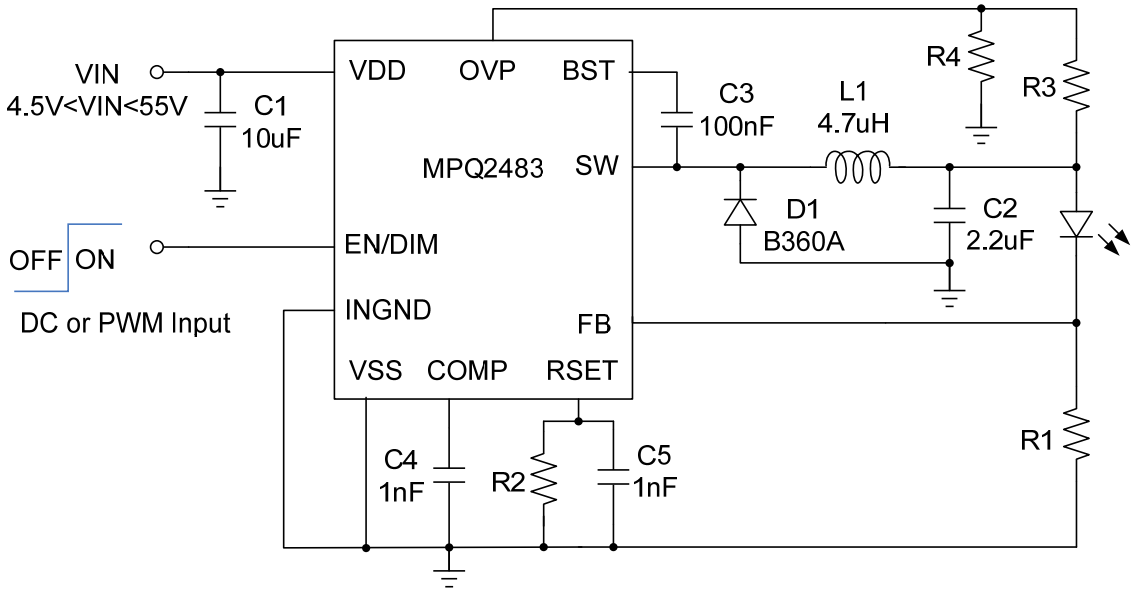


Figure 4: Step-Down LED Driver Application

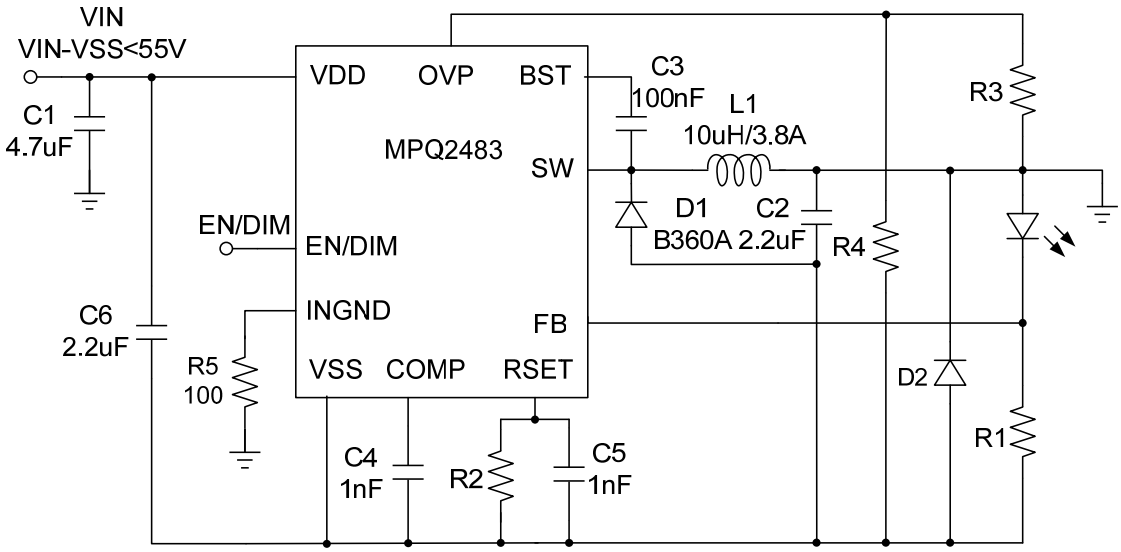


Figure 5: Step Up/Down LED Driver Application

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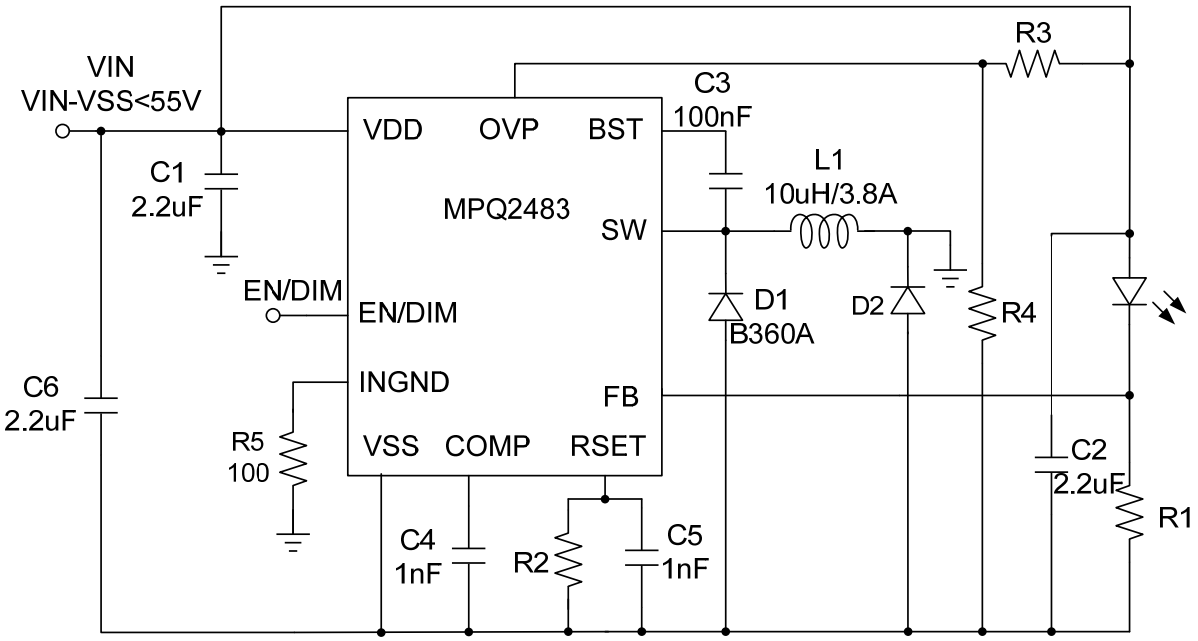
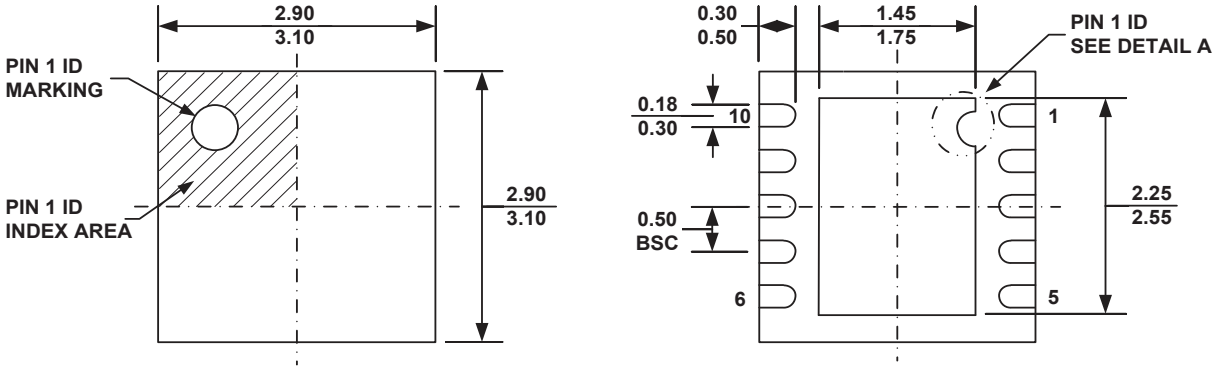


Figure 6: Step-up LED Driver Application

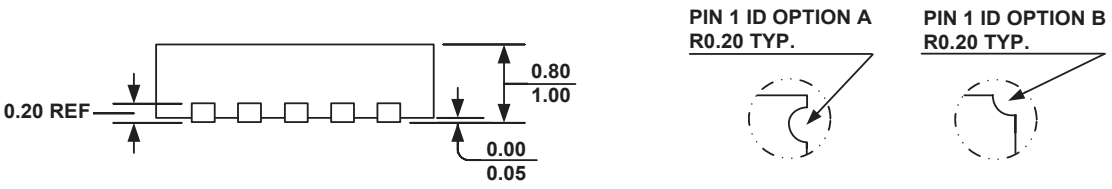
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PACKAGE INFORMATION

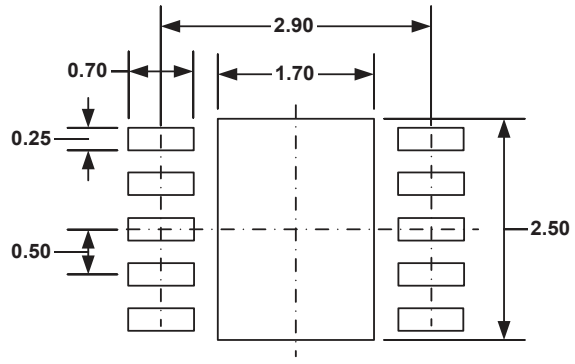
QFN-10(3mmx3mm)



TOP VIEW **BOTTOM VIEW**



SIDE VIEW **DETAIL A**



RECOMMENDED LAND PATTERN

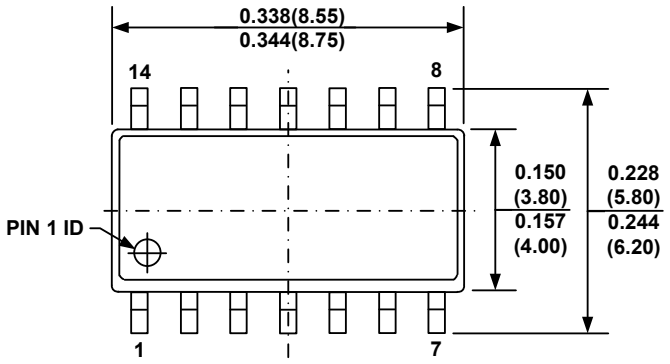
NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETER MAX.
4) DRAWING CONFORMS TO JEDEC MO-229, VARIATION VEED-5.
5) DRAWING IS NOT TO SCALE.

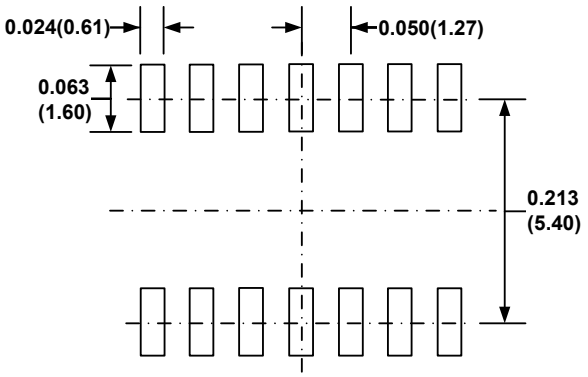
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PACKAGE INFORMATION

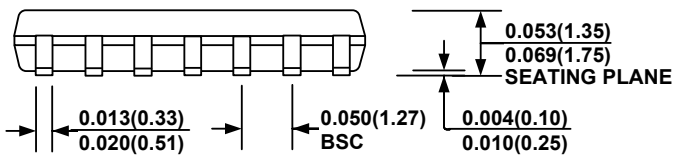
SOIC-14



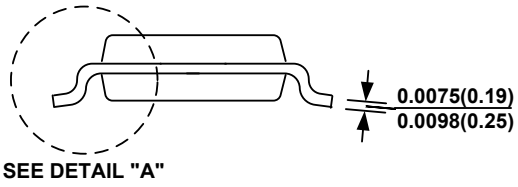
TOP VIEW



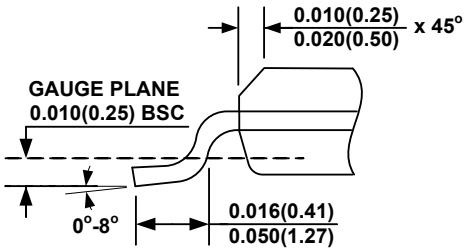
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW



DETAIL "A"

NOTE:

1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
5) DRAWING CONFORMS TO JEDEC MS-012, VARIATION AB.
6) DRAWING IS NOT TO SCALE.

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