# MPQ5066

## 28V, 6A, 7mΩ $R_{DS(ON)}$ Hot-Swap Protection Device with Current Monitoring, AEC-Q100 Qualified

## DESCRIPTION

The MPQ5066 is a hot-swap protection device designed to protect circuitry on its output from transients on its input. It also protects its input from undesired shorts and transients coming from its output.

During start-up, the slew rate at the output limits the inrush current. An external capacitor connected to the SS pin controls the slew rate. The maximum output load is current-limited using a sense FET topology, and a low-power resistor from the ISET pin to ground controls the magnitude of the current limit. An internal charge pump drives the gate of the power device, allowing for a power FET with a very low on resistance of 7mΩ. The MPQ5066 includes an IMON option to produce a voltage proportional to the current through the power device, which is set by a resistor from the IMON pin to ground.

The MPQ5066's fault protections include current limit protection, thermal shutdown, and damaged-MOSFET detection. Both the current limit and thermal shutdown offer configurable auto-retry or latch-off mode. The device also features under-voltage protection.

The MPQ5066 is available in a QFN-22 (3mmx5mm) package, and is AEC-Q100 qualified.

## FEATURES

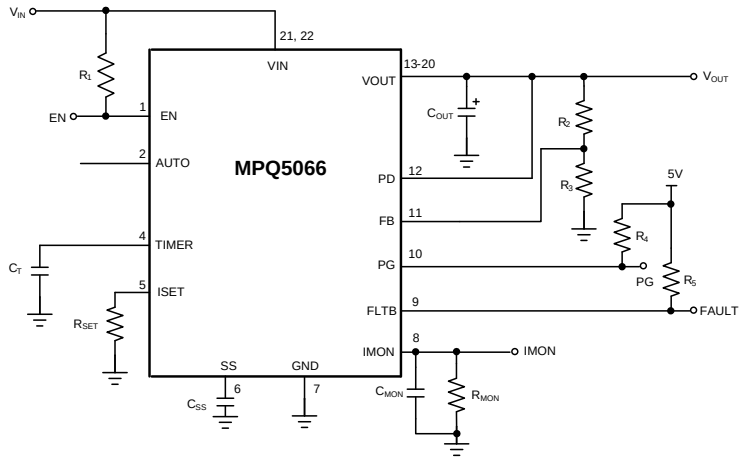
- Integrated 7mΩ Power MOSFET
- Adjustable Current Limit (5A to 15A)
- Output Current Measurement
- ±10% Current Monitor Accuracy
- Fast Response (200ns) for Short Protection
- PG Detector and FLTB Indication
- PG Asserts Low when $V_{IN}$ = 0V
- Damaged MOSFET Detection
- External Soft Start
- Under-Voltage Lockout
- Thermal Protection
- Available in a QFN-22 (3mmx5mm) Package
- Available in AEC-Q100 Grade 1

## APPLICATIONS

- Automotive Infotainment
- Automotive Clusters
- Advanced Driver Assistance Systems
- Automotive Systems

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## TYPICAL APPLICATION





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## ORDERING INFORMATION

| Part Number* | Package | Top Marking | MSL Rating** |
|---|---|---|---|
| MPQ5066GQV-AEC1–Z | QFN-22 (3mmx5mm) | *See Below* | 1 |

* For Tape & Reel, add suffix –Z (e.g. MPQ5066GQV-AEC1–Z).

** Moisture Sensitivity Level Rating.

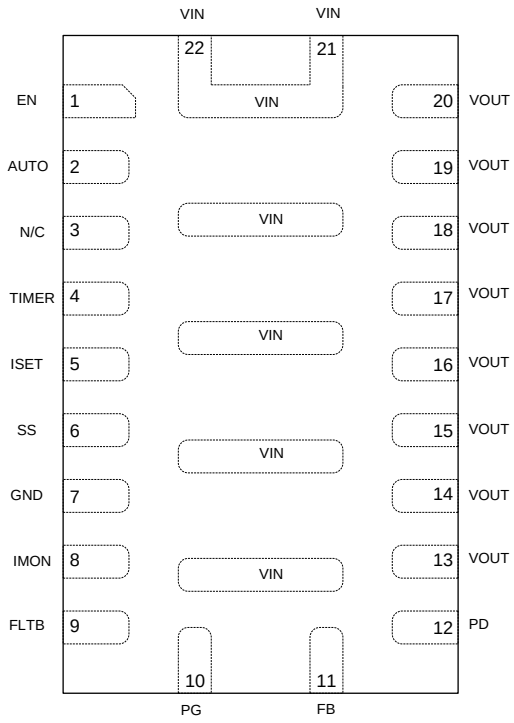
## TOP MARKING

MPYW
5066
LLL

MP: MPS prefix
Y: Year code
W: Week code
5066: First four digits of the part number
LLL: Lot number

## PACKAGE REFERENCE

**TOP VIEW**




**QFN-22 (3mmx5mm)**


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## PIN FUNCTIONS

| Pin # | Name | Description |
|---|---|---|
| 1 | EN | **Enable input.** Pull the EN pin above its threshold (1.8V) to enable the chip. Pull EN below its threshold (1.6V) to shut down the chip. |
| 2 | AUTO | **Auto-reset enable.** Float or pull the AUTO pin above 2.5V to enable auto-reset mode after a fault is removed. If AUTO is grounded, the MPQ5066 latches off if a fault occurs. |
| 3 | NC | **Not connected.** Float this pin. |
| 4 | TIMER | **Timer set.** An external capacitor sets the hot-plug insertion time delay, fault timeout period, and restart time. |
| 5 | ISET | **Current limit set.** Place a resistor from this pin to ground to set the value of the current limit. |
| 6 | SS | **Soft start.** An external capacitor connected to the SS pin sets the soft-start time. The internal circuit controls the output voltage slew rate during start-up. Float this pin to set the soft-start time at a minimum of 1ms. |
| 7 | GND | **Ground.** |
| 8 | IMON | **Output current monitor.** Provide a voltage proportional to the current flowing through the power device. Place a resistor to ground to set the gain. Floating this pin is not recommended. |
| 9 | FLTB | **Fault bar.** This is an open-drain output that drives to ground if an over-current fault or thermal shutdown occurs. Pull FLTB up to an external power supply through a 100kΩ resistor. |
| 10 | PG | **Power good.** This is an open-drain output. Pull PG up to an external power supply through a resistor. When PG is high, it indicates power good. When PG is low, it indicates that the output is outside the under-voltage lockout (UVLO) window. PG starts to work when the pull-up supply is enabled, even if VIN and EN are still disabled. |
| 11 | FB | **Feedback.** An external resistor divider from the output sets the output voltage where the PG pin switches. The rising threshold is 0.6V, with a 60mV hysteresis. |
| 12 | PD | **Output discharge.** Connect to the output to provide a 500Ω load to discharge the output when $V_{IN}$ is below its under-voltage lockout (UVLO) threshold, or the EN pin is within 0.6V of the rising threshold. Floating PD disables this function. |
| 13–20 | VOUT | **Output.** The output voltage is controlled by the IC. |
| 21, 22 (exposed pads) | VIN | **Input power supply.** |


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## ABSOLUTE MAXIMUM RATINGS (1)

$V_{IN}$ .....-0.3V to +36V
VOUT, PD.....-0.3V to +30V
All other pins .....-0.3V to +6.5V
Continuous power dissipation ($T_A$ = 25°C) (2)
…… ..... 2.7W
Power dissipation ($T_A$ = 25°C, 10ms single pulse)
….. ..... 215W
Maximum current ($T_A$ = 25°C)…… 25A
Junction temperature .....150°C
Lead temperature .....260°C
Storage temperature ..... -65°C to +150°C

### *Electrostatic Discharge (ESD) Rating*

Human body model (HBM) .....±2kV
Charged device model (CDM) ..... ±750V

### *Recommended Operating Conditions*

Input voltage operating range .....6V to 28V
Operating junction temp ($T_J$).... -40°C to +125°C

### *Thermal Resistance* $\theta_{JA}$ $\theta_{JC}$

| | | |
|---|---|---|
| QFN-22 (3mmx5mm) | | |
| JESD51-7 (3)…..... | 46..... | 10.....°C/W |
| EV5066-QV-00A (4)..... | 30..... | 2.....°C/W |

**Notes:**

1) Absolute maximum ratings are rated under room temperature, unless otherwise noted. Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature, $T_J$ (MAX), the junction-to-ambient thermal resistance, $\theta_{JA}$, and the ambient temperature, $T_A$. The maximum allowable continuous power dissipation at any ambient temperature is calculated by $P_D$ (MAX) = ($T_J$ (MAX) - $T_A$) / $\theta_{JA}$. Exceeding the maximum allowable power dissipation can lead to excessive die temperature, and the regulator may go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) Measured on JESD51-7, 4-layer PCB.
4) Measured on an MPS standard EVB, 8.5cmx8.5cm, 2-layer PCB.


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## ELECTRICAL CHARACTERISTICS

**$V_{IN}$ = 12V, $R_{SET}$ = 10kΩ, $C_{OUT}$ = 220µF, $T_J$ = -40°C to +125°C, typical values are at $T_J$ = 25°C, unless otherwise noted.**

| Parameters | Symbol | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Supply Current** | | | | | | |
| Quiescent current | $I_Q$ | EN = high, no load | | 1 | 2 | mA |
| | | Fault latch-off | | 0.7 | 1.2 | mA |
| | | EN = 0V, $V_{IN}$ = 12V | | 1 | 10 | µA |
| **Power FET** | | | | | | |
| On resistance | $R_{DS(ON)}$ | | | 7 | 12 | mΩ |
| Off-state leakage current | $I_{OFF}$ | $V_{IN}$ = 28V, EN = 0V, OUT = 0V, $T_J$ = 25°C | | | 1 | µA |
| **Thermal Shutdown** | | | | | | |
| Shutdown temperature (5) | | | | 167 | | °C |
| Hysteresis (5) | | Auto-retry mode only | | 28 | | °C |
| **Under-Voltage Protection** | | | | | | |
| Under-voltage lockout (UVLO) threshold | $V_{UVLO}$ | Rising | | 4.15 | 5.5 | V |
| | | Falling | 2.7 | 3.8 | 5 | V |
| UVLO hysteresis | $V_{UVLOHYS}$ | | | 250 | | mV |
| **AUTO Pin** | | | | | | |
| Low-level input voltage | $V_{AUTOL}$ | Latch-off mode | | | 1 | V |
| High-level input voltage | $V_{AUTOH}$ | Auto-retry mode | 2.5 | | | V |
| **Soft Start** | | | | | | |
| SS pull-up current | $I_{SS}$ | $I_{SS}$ changes with input | 3 | 6 | 9 | µA |
| **Current Limit** | | | | | | |
| Current limit in normal operation | $I_{LIMIT_NO}$ | $R_{SET}$ = 10kΩ | 10.5 | 12.5 | 14.5 | A |
| Current monitor accuracy | | $I_{OUT}$ = 6A | -10 | | +10 | % |
| Current limit response time (5) | | $I_{LIMIT}$ = 3A, add a 3Ω load | | 20 | | µs |
| Secondary current limit (5) | $I_{LIMIT_H}$ | Any value of $R_{SET}$ | | 25 | | A |
| Short-circuit protection response time (5) | | | | 200 | | ns |
| **Timer** | | | | | | |
| Upper threshold voltage | $V_{TMRH}$ | | 1 | 1.23 | 1.4 | V |
| Lower threshold voltage | $V_{TMRL}$ | Over-current restart cycles | 0.09 | 0.20 | 0.35 | V |
| Fault restart duty cycle | | | 0.1 | 0.25 | 0.5 | % |
| Insertion delay charge current | $I_{INSERT}$ | | 15 | 40 | 60 | µA |
| Fault detection charge current | $I_{FLTD}$ | | 80 | 200 | 300 | µA |
| Fault restart sink current | $I_{FLTS}$ | | 0.15 | 0.5 | 0.8 | µA |
| Discharge $R_{ON}$ | | $I_{OUT}$ < $I_{LIMIT}$ | 15 | 35 | 80 | Ω |


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## ELECTRICAL CHARACTERISTICS *(continued)*

**$V_{IN}$ = 12V, $R_{SET}$ = 10kΩ, $C_{OUT}$ = 220µF, $T_J$ = -40°C to +125°C, typical values are at $T_J$ = 25°C, unless otherwise noted.**

| Parameters | Symbol | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Enable** | | | | | | |
| Rising threshold | $V_{ENRS}$ | | 1.4 | 1.8 | 2.2 | V |
| Falling threshold | $V_{ENFS}$ | | 1.2 | 1.6 | 2 | V |
| Hysteresis | $V_{ENHYS}$ | | | 200 | | mV |
| **FB (Power Good Feedback)** | | | | | | |
| Feedback rising threshold | $V_{FBRS}$ | | 0.51 | 0.6 | 0.69 | V |
| Feedback falling threshold | $V_{FBFS}$ | | 0.45 | 0.54 | 0.63 | V |
| Hysteresis | $V_{FBHYS}$ | | | 60 | | mV |
| **Fault Bar/Power Good** | | | | | | |
| Low-level output voltage | $V_{OL}$ | 1mA sink current | | 0.1 | 0.3 | V |
| Off-state leakage current | $I_{FLT_LKG}$ | $V_{FLTB}$ = 5V | | | 1 | µA |
| Fault bar propagation delay | | Pull up $I_{SET}$ from 0V to 1V | 5 | 20 | 40 | µs |
| PG low-level output voltage | $V_{OL_100}$ | $V_{IN}$ = 0V, pull PG up to 3.3V through a 100kΩ resistor | | 500 | 800 | mV |
| | $V_{OL_10}$ | $V_{IN}$ = 0V, pull PG up to 3.3V through a 10kΩ resistor | | 600 | 800 | mV |

**Note:**

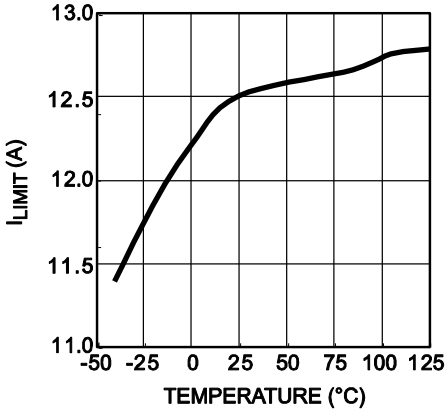
5) Derived from bench characterization. Not tested in production.


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## TYPICAL CHARACTERISTICS

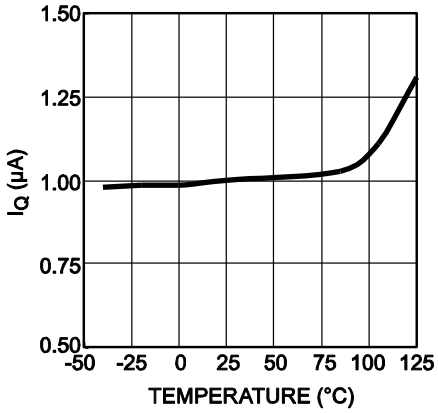
**$V_{IN}$ = 12V, $C_{OUT}$ = 220µF, $C_T$ = 220nF, $R_{SET}$ = 10kΩ, unless otherwise noted.**

**Current Limit vs. Temperature**



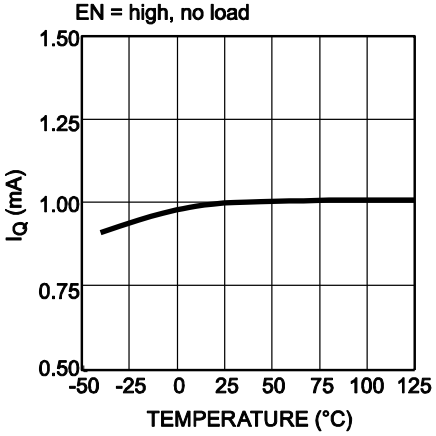

**Quiescent Current vs. Temperature**

EN = 0

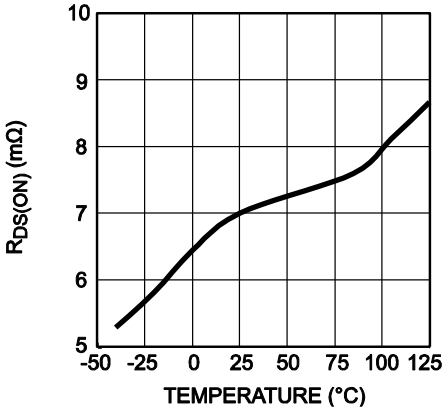



**Quiescent Current vs. Temperature**

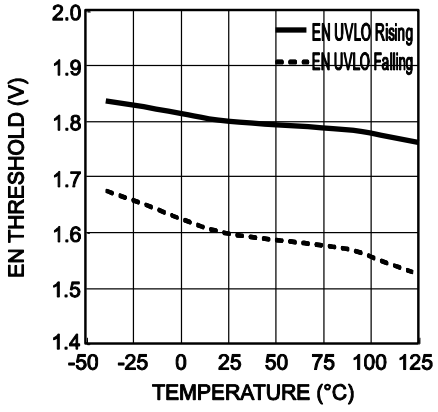
EN = high, no load



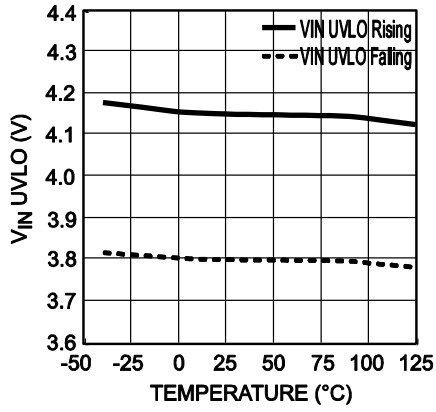

**$R_{DS(ON)}$ vs.Temperature**




**EN Threshold vs. Temperature**




**$V_{IN}$ UVLO vs. Temperature**



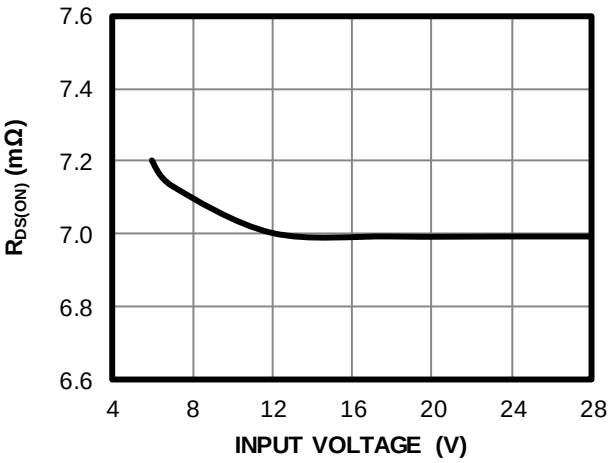


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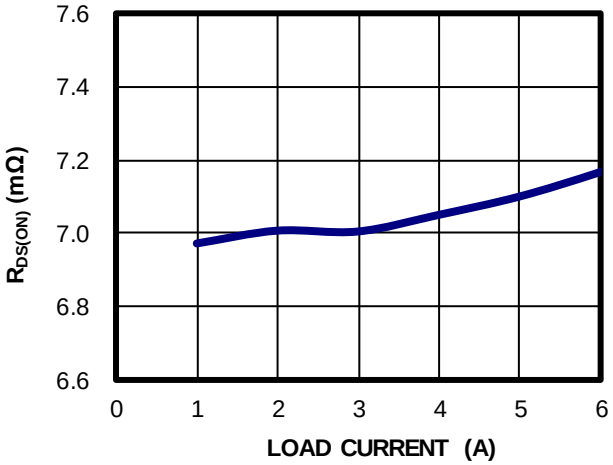
## TYPICAL PERFORMANCE CHARACTERISTICS

**$V_{IN}$ = 12V, $C_{OUT}$ = 220µF, $C_T$ = 220nF, $C_{SS}$ = 10nF, $R_{SET}$ = 10kΩ, $T_A$ = 25°C, unless otherwise noted.**

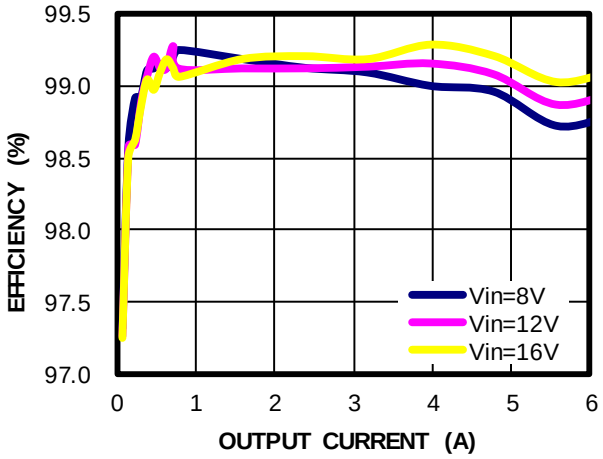
**$R_{DS(ON)}$ vs. Input Voltage**



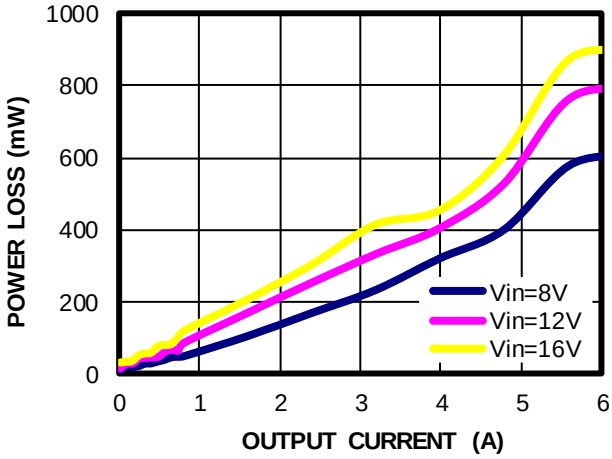

**$R_{DS(ON)}$ vs. Load Current**




**Efficiency vs. Load Current**




**Power Loss vs. Load Current**



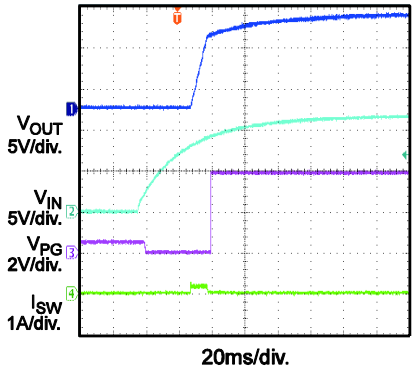


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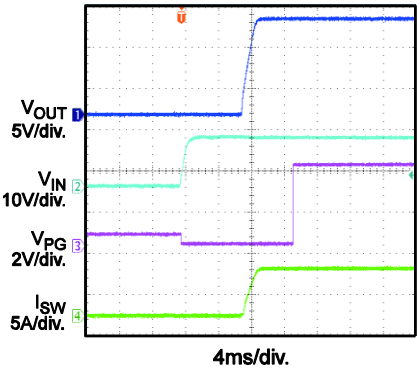
## TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

**$V_{IN}$ = 12V, $C_{OUT}$ = 220µF, $C_T$ = 220nF, $C_{SS}$ = 10nF, $R_{SET}$ = 10kΩ, $T_A$ = 25°C, unless otherwise noted.**

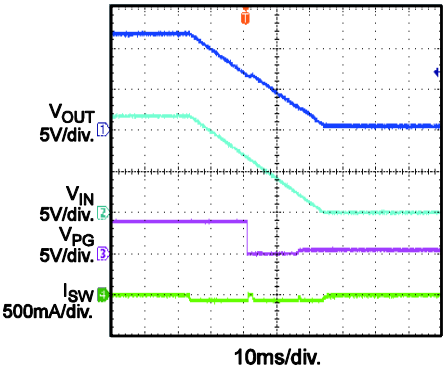
**Start-Up through VIN**
$I_{OUT}$ = 0A



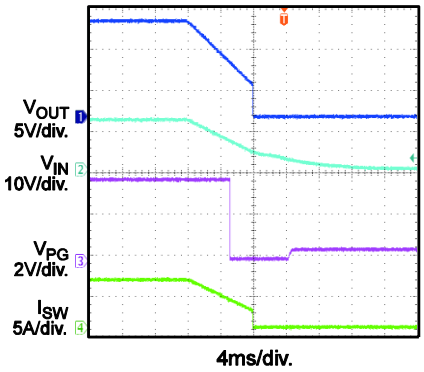

**Start-Up through VIN**
$I_{OUT}$ = 6A



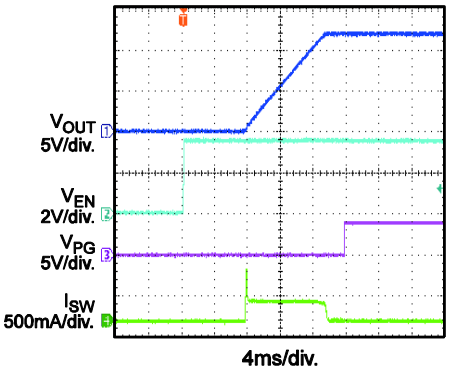

**Shutdown through VIN**
$I_{OUT}$ = 0A



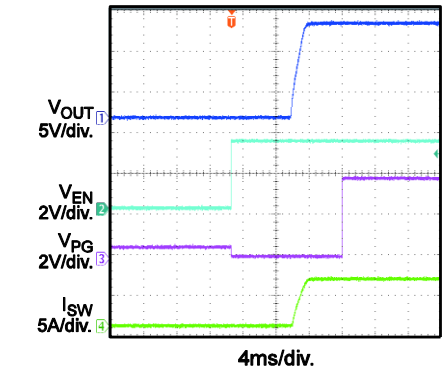

**Shutdown through VIN**
$I_{OUT}$ = 6A



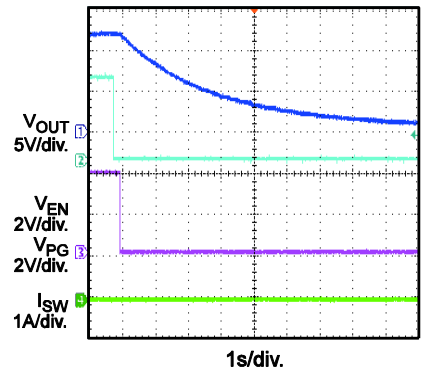

**Start-Up through EN**
$I_{OUT}$ = 0A



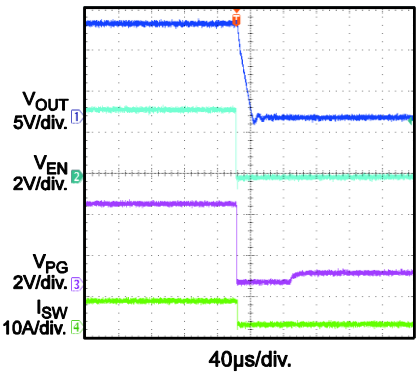

**Start-Up through EN**
$I_{OUT}$ = 6A



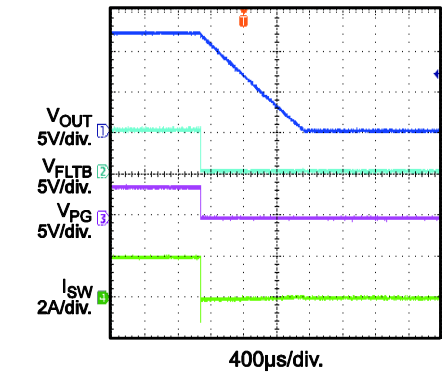

**Shutdown through EN**
$I_{OUT}$ = 0A




**Shutdown through EN**
$I_{OUT}$ = 6A




**Thermal Shutdown**
$I_{OUT}$ = 2A, latch-off mode



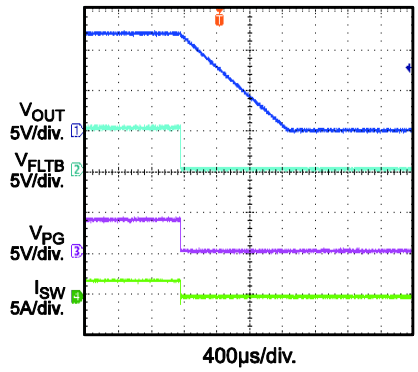


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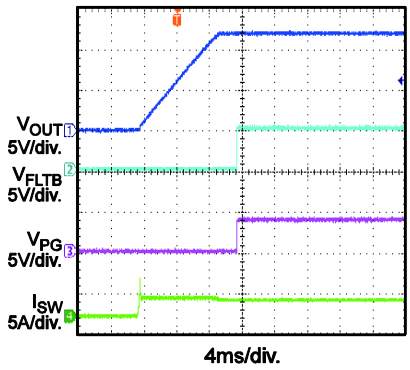
## TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

**$V_{IN}$ = 12V, $C_{OUT}$ = 220µF, $C_T$ = 220nF, $C_{SS}$ = 10nF, $R_{SET}$ = 10kΩ, $T_A$ = 25°C, unless otherwise noted.**

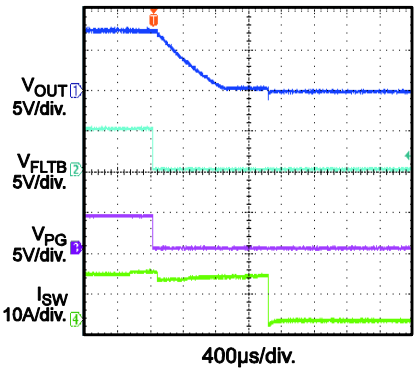
**Thermal Shutdown**
$I_{OUT}$ = 2A, auto-retry mode



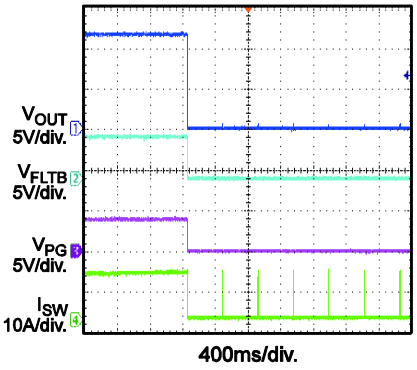

**Thermal Recovery**
$I_{OUT}$ = 2A, auto-retry mode



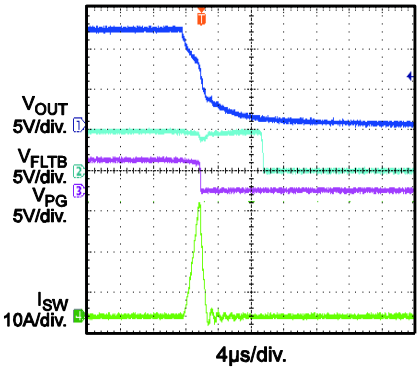

**OCP**
$V_{IN}$ = 12V, latch-off mode



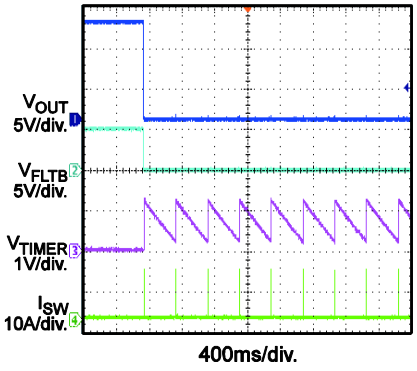

**OCP**
$V_{IN}$ = 12V, auto-retry mode



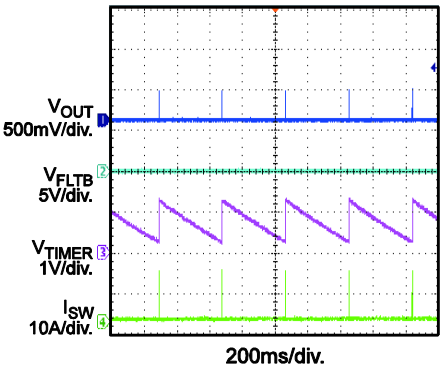

**SCP Entry**
$V_{IN}$ = 12V, latch-off mode



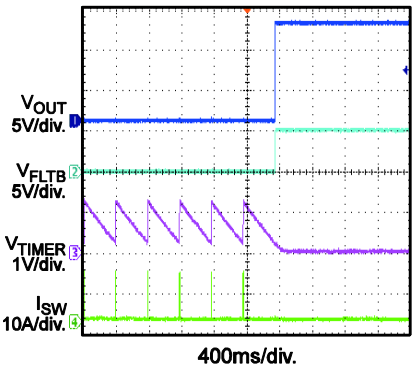

**SCP Entry**
$V_{IN}$ = 12V, auto-retry mode




**SCP Steady State**
$V_{IN}$ = 12V, auto-retry mode




**SCP Recovery**
$V_{IN}$ = 12V, auto-retry mode





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# FUNCTIONAL BLOCK DIAGRAM

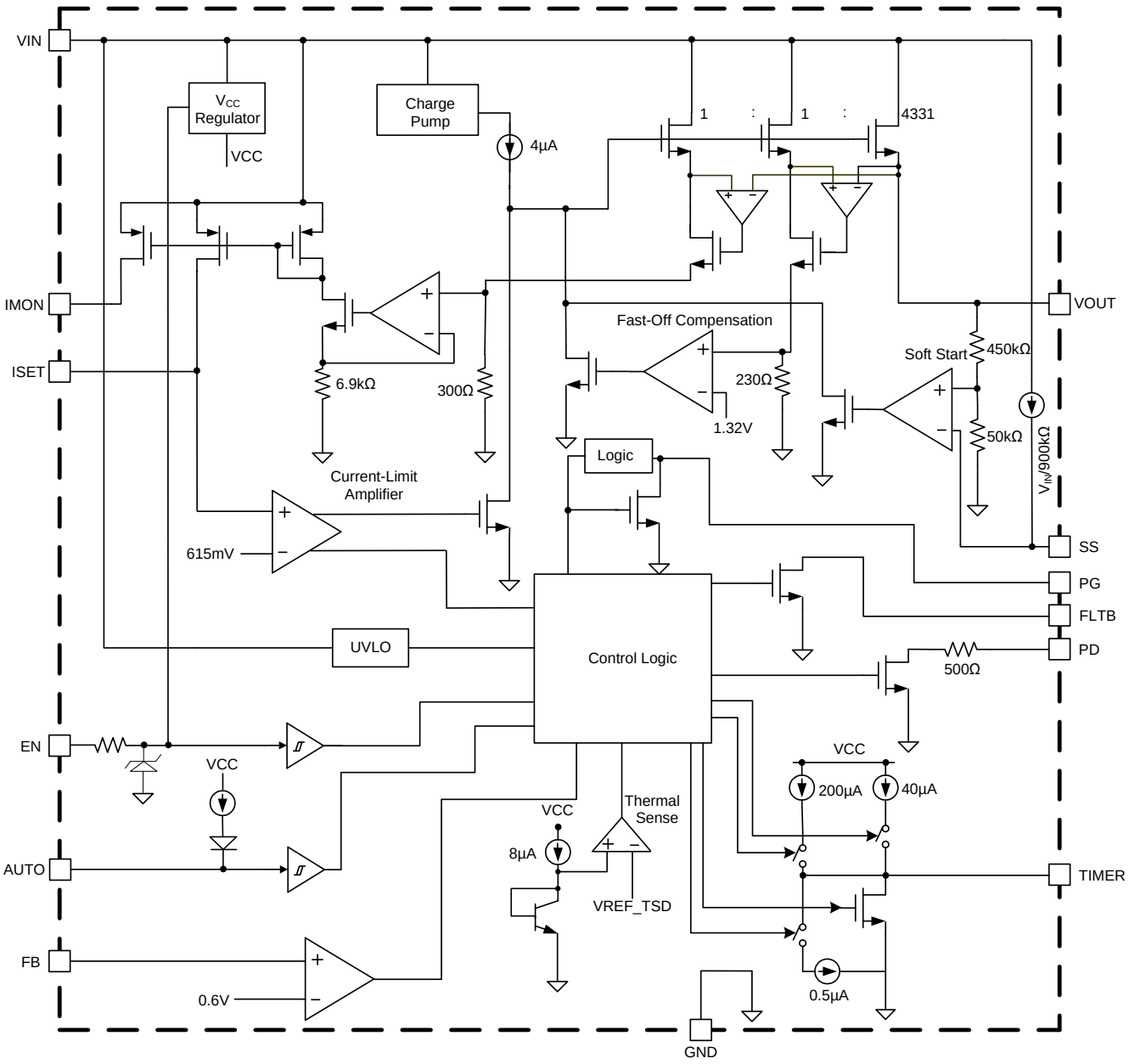



**Figure 1: Functional Block Diagram**


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## OPERATION

The MPQ5066 protects circuitry on its output from transients on its input. It also protects its input from undesired shorts and transients coming from its output. The device provides an integrated solution to monitor the input voltage, output voltage, output current, and die temperature. This means an external current-sense resistor, power MOSFET, and thermal sense device are not required for this solution.

### Current Limit

The MPQ5066 provides a constant current limit that can be configured by an external resistor. If the device reaches its current limit threshold, the internal circuit regulates the gate voltage to hold the current in the MOSFET constant. To limit the current, the gate-to-source voltage must drop from 5V to about 1V. The typical response time is about 20µs, and the output current may have a small overshoot during this time period.

If the current limit is triggered, the fault timer starts. If the output current falls below the current limit threshold before the end of the fault timeout period, the MPQ5066 resumes normal operation. If the current limit duration remains after the fault timeout period, the MOSFET turns off. The subsequent behavior relates to the AUTO pin configuration. If the temperature reaches the thermal protection threshold during the fault timeout period, the MOSFET turns off.

When the AUTO pin is floating, the part functions in auto-retry mode for over-current protection (OCP). The part enters latch-off mode if the device detects an OC condition and pulls the AUTO pin to ground.

If the device reaches either its current limit or its over-temperature threshold, the FLTB pin is driven low with a 20µs propagation delay to indicate a fault. The desired current limit during normal operation is set by the external current limit resistor.

### Thermal Shutdown

Thermal shutdown is implemented to prevent the chip from thermal runaway. If the silicon die temperature exceeds its upper threshold (167°C), the power MOSFETs shut down. Once the temperature drops below its lower threshold (139°C), the chip is enabled again.

### Short-Circuit Protection

If the load current increases rapidly due to a short circuit, the current may significantly exceed the current limit threshold before the control loop can respond. If the current reaches the 25A secondary current limit level, a fast turn-off circuit activates to turn off the MOSFET using a 100mA pull-down gate discharge current (see Figure 2). This limits the peak current through the switch to limit the input voltage drop. The total short circuit response time is about 200ns. The FLTB pin switches low once it reaches a 25A current limit, and asserts low until the circuit resumes normal operation.

### Fault Timer and Restart

When the current reaches its over-current limit threshold, a 200µA fault timer current source charges the external capacitor ($C_T$) at the TIMER pin. If the current limit state is removed before the TIMER pin reaches 1.23V, the MPQ5066 returns to normal operation, and a low-value resistor discharges $C_T$ after the TIMER voltage reaches 1.23V. If the current limit state continues after the TIMER pin voltage reaches 1.23V, the MOSFET switches off. The subsequent restart procedure then depends on the selected retry configuration.

If the AUTO pin is connected to ground or pulled low, the MPQ5066 latches off. Restart the input power or cycle the EN signal to resume normal function.

Floating the AUTO pin or pulling it above 2.5V causes the device to operate in hiccup mode (see Figure 3). At the end of the fault timeout period, the MOSFET turns off, and a low-current (0.5µA) sink discharges the external capacitor ($C_T$).

If the TIMER voltage reaches the low threshold (0.2V), the part restarts. If the fault condition remains, the fault timeout period and restart timer repeat.


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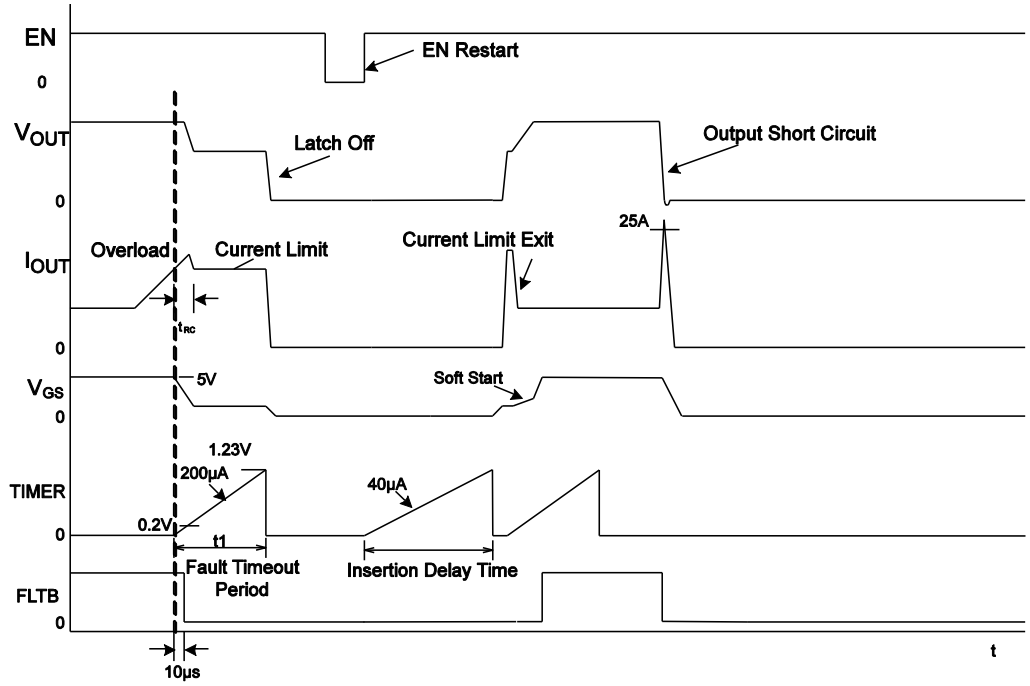



**Figure 2: Over-Current Protection (Latch-Off Mode, AUTO = Low)**

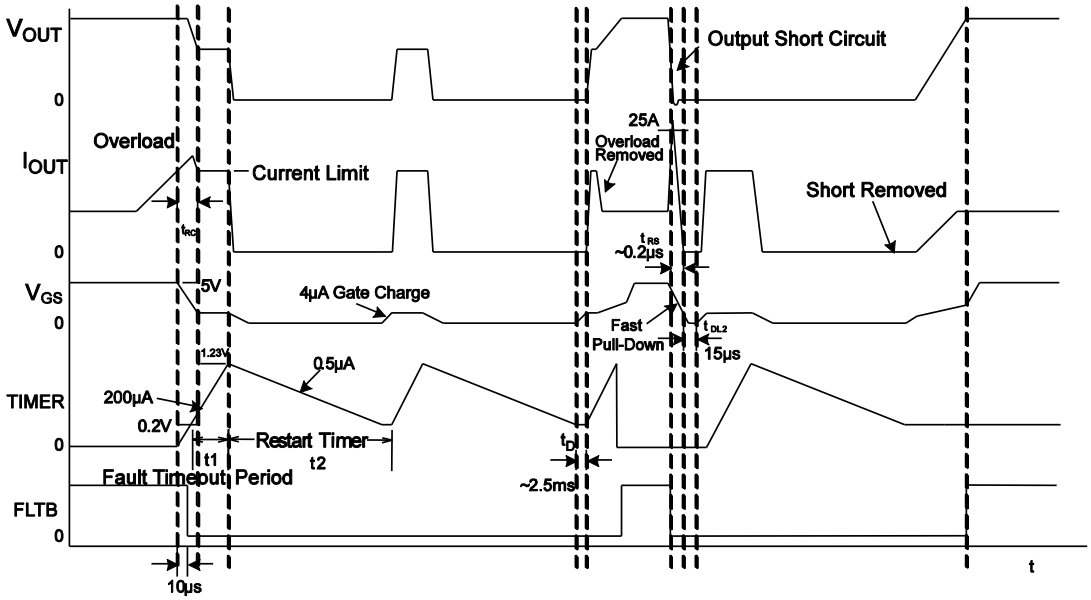



**Figure 3: Over-Current Protection (Auto-Retry Mode, AUTO = High)**


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### Power Good (PG)

Power good (PG) indicates whether the output voltage is in the normal range relative to the input voltage. It is the open drain of a MOSFET. Pull the PG pin up to the external power supply through a 100kΩ resistor. During start-up, PG's output is driven low. This directs the system to remain off, and minimizes the output load to reduce inrush current and power dissipation during start-up.

The PG signal is pulled high when the device reaches all of the following conditions:

- $V_{FB}$ > 0.6V
- $V_{GS}$ > 3V
- $V_{OUT}$ > $V_{IN}$ - 1V

Then the system can draw full power.

If the FB voltage drops below 0.54V, the MOSFET's $V_{GS}$ voltage falls below 3V, or the output voltage drops below $V_{IN}$ - 1V, PG is pulled low.

The PG output is also pulled low when either the EN pin is below its threshold or input under-voltage lockout (UVLO) is triggered.

With no input, PG remains at logic low in the presence of a pull-up supply.

### The FLTB Pin

The fault bar (FLTB) pin is an open-drain output used to indicate whether a fault has occurred. Pull the FLTB pin up to the external power supply through a 100kΩ resistor.

When the device reaches its current limit, the die temperature exceeds the thermal shutdown threshold, or the MOSFET is shorted before start-up, the fault output is driven low with a 20μs propagation delay. If a short occurs and the current reaches its 25A secondary current limit, FLTB goes low with an 8μs delay.

FLTB goes high when the MPQ5066 resumes normal operation, which means the output voltage has exceeded the set voltage of the PG rising threshold and the MOSFET is fully on ($V_{GS}$ > 3V).

### External Pull-Up Voltage for PG and FLTB

PG and FLTB require an external power supply. The open-drain output of PG can work well with an external pull-up voltage, even when $V_{IN}$ = 0V and EN is disabled. Use a 100kΩ pull-up resistor for PG and FLTB.

### Start-Up Sequence

For hot-swap applications, the MPQ5066's input can experience a voltage spike or transient during the hot swap. This spike is caused by the parasitic inductance of the input trace and the input capacitor. An insertion delay determined by the external capacitor at the TIMER pin stabilizes the input voltage.

The input voltage rises immediately, and a 30Ω resistor pulls the internal $V_{GS}$ voltage low (see Figure 4).

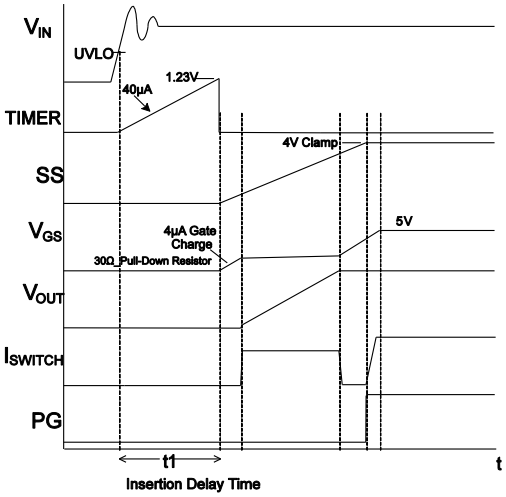



**Figure 4: Start-Up Sequence**

The TIMER pin charges through a 40μA constant-current source when the input voltage reaches its UVLO threshold. When the TIMER pin voltage reaches 1.23V, a 4μA current source pulls up the MOSFET's gate-source voltage. Meanwhile, the TIMER pin's voltage drops. Once the gate voltage reaches its threshold ($V_{GSTH}$), the output voltage rises. The soft-start capacitor determines the rising time.

### Soft Start

A capacitor connected to the SS pin determines the soft-start time: When the insertion delay time ends, a constant-current source that is proportional to the input voltage ramps up the voltage on the SS pin. The output voltage rises at a similar slew rate to the SS voltage.


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The SS capacitor value can be calculated with Equation (1):

$$C_{SS} = \frac{10 \times t_{SS}}{R_{SS}} \quad (1)$$

Where $t_{SS}$ is the soft-start time, and $R_{SS}$ = 2MΩ.

For example, a 100nF capacitor gives a soft-start time of 20ms.

If the load capacitance is extremely large, the current required to maintain the preset soft start exceeds the current limit. At this point, the load capacitor and the current limit control the rising time.

Float the SS pin to generate a fast ramp-up voltage. A 4μA current source pulls up the gate of the MOSFET. The gate charge current controls the output voltage rising time. The approximate soft-start time is about 1ms, which is the minimum soft-start time.

### The EN Pin

When the EN pin is above its rising threshold, the part is enabled; when EN is below that threshold, the part is disabled.

If EN drops below 0.6V, the chip goes into the lowest shutdown current mode. If EN is above 0.6V but below its rising threshold, the chip remains in shutdown mode with a slightly larger current.

When EN enables the part, the insertion delay timer starts. When the insertion delay time ends, the internal 4μA current source charges the MOSFET's gate. Charging takes about 1.5ms for $V_{GS}$ to reach its threshold. Then the output voltage rises following the soft-start slew rate.

### Damaged MOSFET Detection

The MPQ5066 can detect a shorted pass MOSFET during start-up by treating an output voltage that exceeds $V_{IN}$ - 1V during start-up as a short on the MOSFET. The FLTB pin goes low to indicate a fault condition, and the MOSFET remains off. Once $V_{OUT} \leq V_{IN}$ - 1V, the device starts up and resumes normal operation.

### Internal VCC Sub-Regulator

The MPQ5066 has an internal 5V linear sub-regulator that powers low-voltage circuitry. This regulator takes the input voltage ($V_{IN}$) and operates in the full $V_{IN}$ range. When $V_{IN}$ is above 5.0V, the output of the regulator is in full regulation. Lower $V_{IN}$ values result in lower output voltages. The regulator is enabled when $V_{IN}$ exceeds its UVLO threshold and EN is high. In EN shutdown mode, the internal VCC regulator is disabled to reduce power dissipation.

### The PD Pin

When the PD pin connects to the output, the part is in pull-down mode. If $V_{IN}$ is below its UVLO threshold, or the EN pin is between 0.6V and its rising threshold in this mode, an integrated 500Ω pull-down resistor attached to the output discharges the output. Add a resistor between the PD pin and the output for a slower output drop. If the PD pin is floating, pull-down mode is disabled.

### The AUTO Pin

When the AUTO pin is floating, the part works in auto-retry mode. In auto-retry mode, the part turns off if it exceeds its thermal limit or current limit timeout. The part turns back on when the part cools by 28°C or the restart timer completes.

If the AUTO pin is tied to ground, the part works in latched fault mode. In latched fault mode, a thermal fault or current limit fault latches the output off until EN is toggled from low to high or the input voltage restarts.

### Under-Voltage Lockout (UVLO)

If the input supply falls below the under-voltage lockout (UVLO) threshold, the output is disabled and the PG pin goes low. If the supply exceeds the UVLO threshold, the output is enabled and PG is released.

### Monitoring the Output Current

The IMON pin provides a voltage proportional to the output current (the current through the power device). Tie a resistor to ground to set the output gain. Place a 100nF capacitor from IMON to GND to smooth the indicator voltage.


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# APPLICATION INFORMATION

### Setting the Current Limit ($R_{SET}$)

The MPQ5066's current limit value should exceed the normal maximum load current. This allows for tolerance in the current-sense value. Estimate the current limit with Equation (2):

$$I_{LIMIT} = \frac{0.6(V)}{R_{SET}} \times 20 \times 10^4 (A) \quad (2)$$

Table 1 shows the bench results from the evaluation board.

**Table 1: Current Limit vs. Current Limit Resistor**

| Current Limit Resistor (kΩ) | 7.5 | 10 | 20 |
|---|---|---|---|
| **Current Limit (A)** | 15.9 | 12 | 6.08 |

Figure 5 shows the relationship between the set resistance ($R_{SET}$) and the current limit.

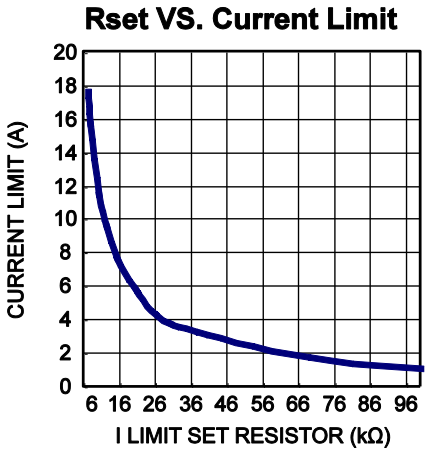



**Figure 5: $R_{SET}$ vs. Current Limit**

### Current Monitoring

The MPQ5066 provides MOSFET current monitoring. Place a resistor ($R_{IMON}$) to ground to set the output gain. $I_{IMON}$ can be calculated with Equation (3):

$$I_{IMON} = \frac{I_{POWERFET}}{10^5} \quad (3)$$

Where $I_{POWERFET}$ is the power MOSFET current.

The IMON pin provides a voltage proportional to the output current. Place a 10kΩ resistor from the IMON pin to GND to obtain a value of 100mV/A, which is the voltage proportional to the output current. Place a 100nF capacitor from IMON to GND to smooth the indicator voltage.

### Design Example

Figure 7 on page 18 shows the detailed application schematic. For the typical performance and circuit waveforms, see the Typical Performance Characteristics section on page 8. For more detailed device applications, refer to the related evaluation board datasheet.


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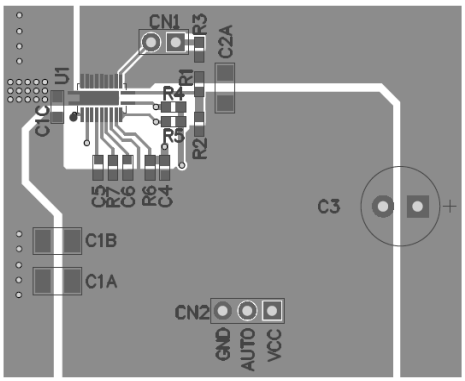
## PCB Layout Guidelines [6]

Efficient PCB layout is crucial for proper device performance. For the best results, refer to Figure 6 and follow the guidelines below:

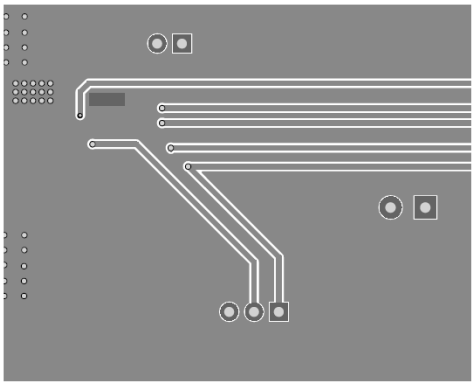
1. Place the high-current paths (GND, IN, and OUT) very close to the device using short, direct, and wide traces.
2. Place a small bypass capacitor next to VIN to minimize transients that may occur on the input supply line.
3. Place the external feedback resistors next to the FB pin.
4. Avoid placing any vias on the FB trace.
5. Connect the IN and GND pads to a large copper plane to improve thermal performance.
6. Place the input and output capacitors as close to the device as possible to minimize the effects of parasitic inductance.
7. Put vias on the thermal pad, and provide a large copper area near the IN pin to improve thermal performance. Ensure that all pins are connected to obtain equal current distribution in all legs.
8. Put vias on the thermal pad, and provide a large copper area near the OUT pin to improve thermal performance. Ensure that all pins are connected to obtain equal current distribution in all legs.

**Note:**

6) The recommended PCB layout is based on the Typical Application Circuit on page 18.




**Top Layer and Top Silk**



**Bottom Layer and Bottom Silk**

**Figure 6: Recommended PCB Layout**


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# TYPICAL APPLICATION CIRCUIT

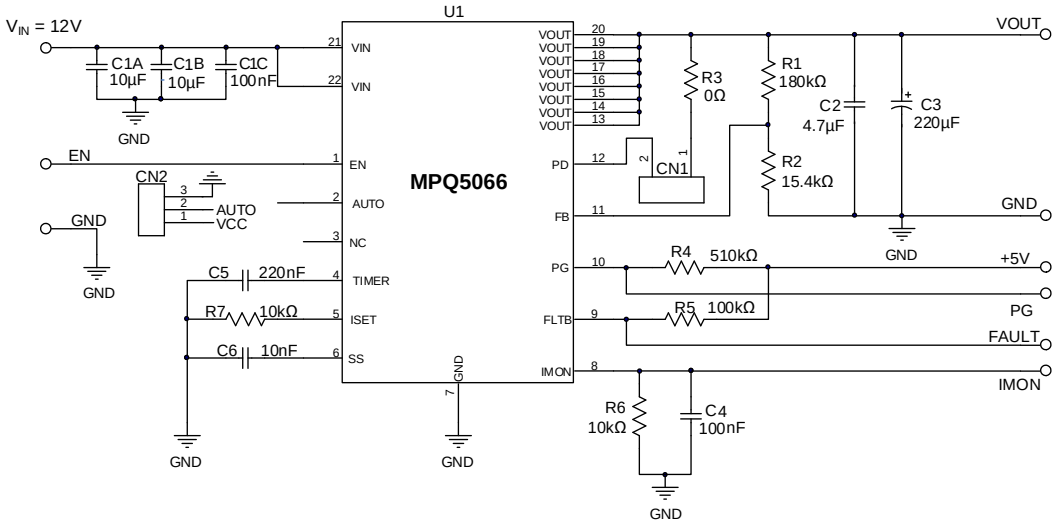
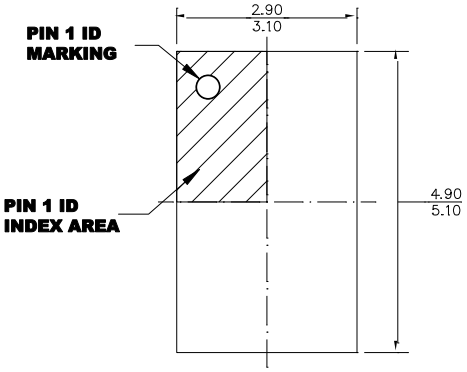



**Figure 7: Typical Application Circuit**

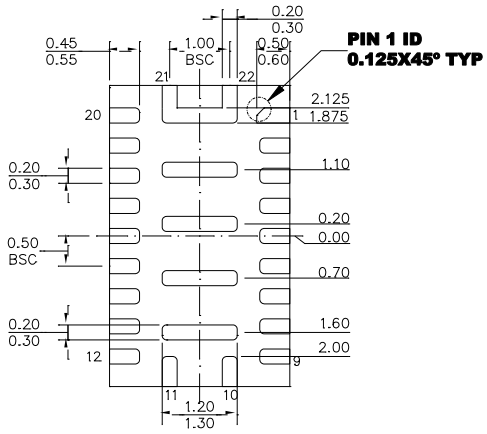

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# PACKAGE INFORMATION

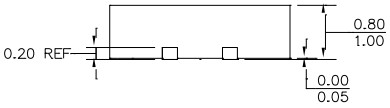
## QFN-22 (3mmx5mm)



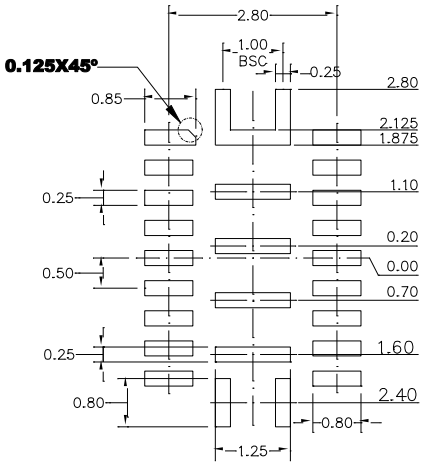

**TOP VIEW**




**BOTTOM VIEW**




**SIDE VIEW**



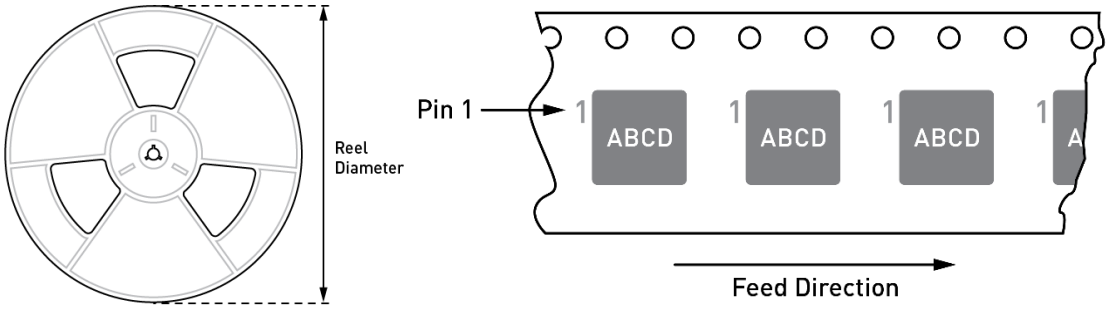

**RECOMMENDED LAND PATTERN**

**NOTE:**

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.


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## CARRIER INFORMATION




| Part Number | Package Description | Quantity/ Reel | Reel Diameter | Carrier Tape Width | Carrier Tape Pitch |
|---|---|---|---|---|---|
| MPQ5066GQV-AEC1–Z | QFN-22 (3mmx5mm) | 5000 | 13in | 12mm | 8mm |


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## Revision History

| Revision # | Revision Date | Description | Pages Updated |
|---|---|---|---|
| 1.0 | 8/6/2020 | Initial Release | - |

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