MPQ6527

40V, 0.8A, 10-Channel Half-Bridge Motor Driver with Serial Input Control, AEC-Q100 Qualified

DESCRIPTION

The MPQ6527 is a ten-channel half-bridge DMOS output driver with integrated power MOSFETs. The device has a 5.5V to 40V input voltage range, with a maximum 0.8A of output current capability.

The device's ten half-bridges can be controlled separately from a standard serial data interface, and each channel has various diagnostic functions. The MPQ6527 has very low quiescent current in standby mode.

Full protection includes short-circuit protection (SCP), under-voltage protection (UVP), and thermal shutdown.

The MPQ6527 requires a minimal number of readily available, standard external components, and is available in a TSSOP-28 EP package.

FEATURES

- Wide 5.5V to 40V Operating Input Range
- High-Side and Low-Side Drivers Connected in Half-Bridge Configurations
- Up to 0.8A Output Current
- $R_{DS(ON)}$ (HS-FET and LS-FET), Typically 1.3Ω
- Very Low Quiescent Current in Standby Mode vs. Total Temperature Range
- Output Short-Circuit Protection (SCP)
- Over-Temperature Protection (OTP) and Pre-Warning
- Under-Voltage (UV) and Over-Voltage Lockout (OVLO)
- Serial Data Interface
- Various Diagnostic Functions: Shorted Output, Open Load, and Over-Temperature, Over-Voltage, and Under-Voltage Conditions
- Serial Interface Clock Frequency Up to 5MHz
- Compliance with 3.3V and 5V Systems
- Available in a TSSOP-28 EP Package
- Available in AEC-Q100 Grade 1

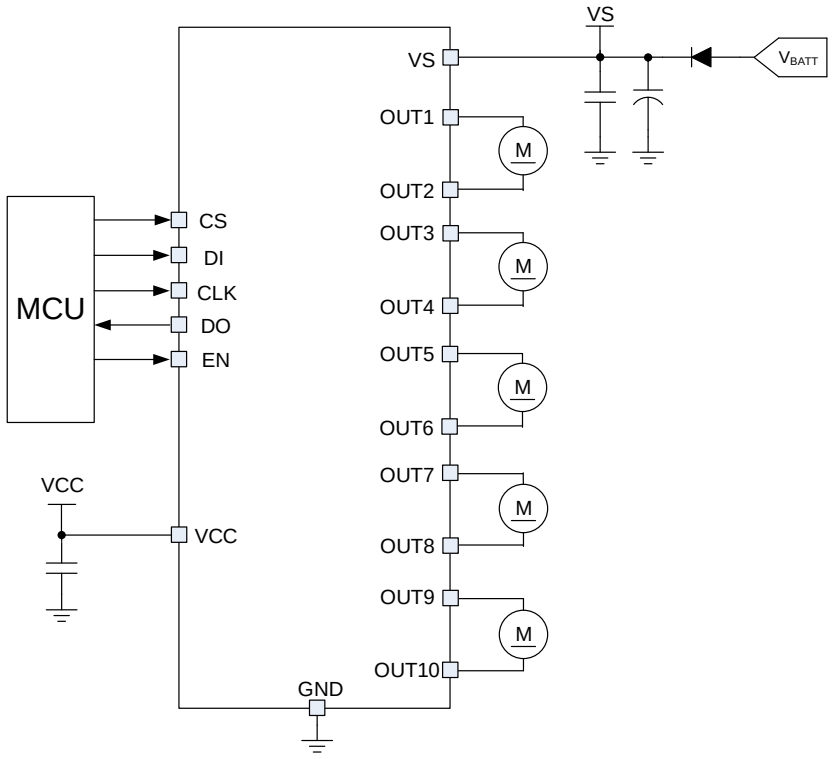
APPLICATIONS

- Drive Various Loads in Automotive and Industrial Applications
- DC Motors

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TYPICAL APPLICATION



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ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MPQ6527GF-AEC1	TSSOP-28 EP	*See Below*	2A

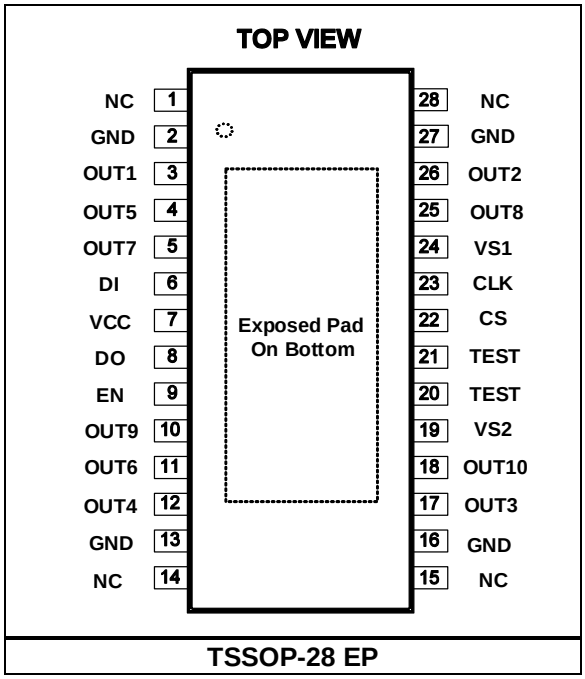
* For Tape & Reel, add suffix -Z (e.g. MPQ6527GF-AEC1-Z).

TOP MARKING

MPSYYWW
MP6527
LLLLLLLLL

MPS: MPS prefix
YY: Year code
WW: Week code
MP6527: Part number
LLLLLLLLL: Lot number

PACKAGE REFERENCE



TSSOP-28 EP

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PIN FUNCTIONS

Pin #	Name	Description
1, 14, 15, 28	**NC**	**No connection.**
2, 13, 16, 27	**GND**	**Ground.**
3	**OUT1**	**Channel 1 half-bridge output.**
4	**OUT5**	**Channel 5 half -bridge output.**
5	**OUT7**	**Channel 7 half -bridge output.**
6	**DI**	**Serial data input.**
7	**VCC**	**Logic supply voltage.**
8	**DO**	**Serial data output.**
9	**EN**	**Enable pin.** When EN is low, the drive is in standby mode; when EN is high, the device operates normally.
10	**OUT9**	**Channel 9 half-bridge output.**
11	**OUT6**	**Channel 6 half-bridge output.**
12	**OUT4**	**Channel 4 half-bridge output.**
17	**OUT3**	**Channel 1 half-bridge output.**
18	**OUT10**	**Channel 10 half-bridge output.**
19	**VS2**	**Power supply for drivers 3, 4, 6, 9, and 10.** This pin must be connected to VS1 externally.
20, 21	**TEST**	**Testing pin.** The TEST pin must be connected to ground.
22	**CS**	**Chip selection input.** The CS pin is active low.
23	**CLK**	**Serial clock input.**
24	**VS1**	**Power supply for drivers 1, 2, 5, 7, and 8, internal LDO, and charge pump.** This pin must be connected to VS2 externally.
25	**OUT8**	**Channel 8 half-bridge output.**
26	**OUT2**	**Channel 2 half-bridge output.**

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ABSOLUTE MAXIMUM RATINGS (1)

Supply voltage (V_{VS}) 45V
V_{OUTx} .....-0.3V to V_{IN} + 0.3V
Logic supply voltage (V_{VCC})..... -0.3V to +6V
Logic input voltage..... -0.3 to V_{VCC} + 0.3V
Logic output voltage..... -0.3 to V_{VCC} + 0.3V
All other pins..... -0.3V to +6.5V
Continuous power dissipation (T_A = 25°C) (2).....
TSSOP-28EP 3.9W
Junction temperature .....150°C
Lead temperature .....260°C
Storage temperature.....-65°C to +150°C

ESD Ratings (3)

Human body model (OUTx and VSx pins) 4kV
Human body model (all other pins) 2kV
Machine mode (MM).....200V
Charged device model (CDM).....750V

Recommended Operating Conditions (4)

Supply voltage (V_{VS}) ..... 5.5V to 40V
Logic supply voltage (V_{VCC})..... 3.15V to 5.25V
Operating junction temp (T_J) .... -40°C to +150°C

Thermal Resistance (5) θ_{JA} θ_{JC}

TSSOP-28 EP……32…....6….°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can cause excessive die temperature, and the regulator may go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) Devices are ESD-sensitive. It is recommended to handle them with caution.
4) The device is not guaranteed to function outside of its operating conditions.
5) Measured on JESD51-7, 4-layer PCB.

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ELECTRICAL CHARACTERISTICS

5.5V ≤ V_{VS} ≤ 40V, 3.15V ≤ V_{VCC} ≤ 5.25V, EN = V_{VCC}, T_J = -40°C to +125°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Operating supply current (VS)	I_{VSO}	V_{VS} < 28V, EN = V_{CC}, no load		5.5	6.5	mA
Operating supply current (VCC)	I_{VCCO}	3.15V < V_{VCC} < 5.25V, EN = high, DI = CLK = low, CS = high, no load		100	150	µA
Quiescent current (VS)	I_{VSQ}	V_{VS} = 13.2V, V_{VCC} = 0V or 5V, EN = low		1	5	µA
Quiescent current (VCC)	I_{VCCQ}	3.15V < V_{VCC} < 5.25V, EN = low, DI = CLK = low, CS = high		1	5	µA
Discharge current (VS)	I_{VS}	V_{VS} = 40V, EN = low			3	mA
Power-on reset threshold	V_{VCC}	VCC increasing	2.3	2.7	3.0	V
Power-on reset delay		After switching on V_{VCC}	30	100	160	µs
VS under-voltage lockout threshold	V_{VS}	VS decreasing	3.5		4.5	V
VS under-voltage lockout threshold hysteresis	V_{UVOFF}		0.1	0.3	0.5	V
VS under-voltage lockout delay time			7		21	ms
VS over-voltage lockout threshold	V_{OVOFF}	OVLO = 1, VS increasing	33	36	39	V
VS over-voltage lockout threshold hysteresis			1	2.5	4	V
Output Specification						
HS and LS switch on resistance	$R_{DS(ON)}$	T_J = -40°C to +125°C		1.3	2.2	Ω
		T_J = 150°C			2.8	Ω
Over-current limit	I_{OCP}	V_{VS} = 13.2V	1	1.3	2.5	A
Over-current shutdown delay time	t_{dOC}		10	25	50	µs
Open-load detection current	I_{OLD}	V_{VS} = 13.2V, LS switch on	1	16	45	mA
Open-load delay time	t_{dOLD}		200	350	600	µs
Output enable time		V_{VS} = 13.2V, R_{LOAD} = 50Ω		50	65	µs
Output disable time				50	65	
Delay time		HBCNFx high to OUTx high, V_{VS} = 13.2V, R_{LOAD} = 50Ω		75	105	
		HBCNFx low to OUTx low, V_{VS} = 13.2V, R_{LOAD} = 50Ω		65	95	
Output rise time		V_{VS} = 13.2V, 10% to 90% V_{OUT}, R_{LOAD} = 50Ω	13	27	42	µs
Output fall time			11	20	27	

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ELECTRICAL CHARACTERISTICS *(continued)*

5.5V ≤ V_{VS} ≤ 40V, 3.15V ≤ V_{VCC} ≤ 5.25V, T_J = -40°C to +125°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Dead time		V_{VS} = 13V, R_{LOAD} = 50Ω	1.5			µs
EN Input						
EN low-level threshold					0.6	V
EN high-level threshold			2.0			V
EN threshold hysteresis				0.4		V
Pull-down resistor		V_{EN} = V_{VCC}		125		kΩ
Serial Interface: Logic Inputs DI, CLK, CS						
Input low-level threshold					0.6	V
Input high-level threshold			2.0			V
Input threshold hysteresis				150		mV
Pull-down resistor for DI, CLK pin		V_{DI}, V_{CLK} = V_{VCC}		125		kΩ
Pull-up current for CS pin		V_{CS} = 0V		125		kΩ
Input capacitance (6)	C_{IN}				15	pF
Serial Interface: Logic Output DO						
Output low level					0.4	V
Output high level			V_{VCC} - 0.6			V
Leakage current (tri-state)		0V < V_{DO} < V_{VCC}, V_{CS} = V_{VCC}	-5		+5	µA
Thermal Shutdown and Pre-Warning (6)						
Thermal pre-warning threshold	T_{JW}		120	140	170	°C
Thermal pre-warning hysteresis				20		°C
Thermal shutdown threshold	T_{JSD}		150	175	200	°C
Thermal shutdown hysteresis				20		°C
Ratio for thermal shutdown and thermal pre-warning			1.05	1.2		

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SERIAL INTERFACE TIMING CHARACTERISTICS (6)

5.5V < V_{VS} < 40V, 3.15V ≤ V_{VCC} ≤ 5.25V, T_J = -40°C to +125°C, unless otherwise noted.

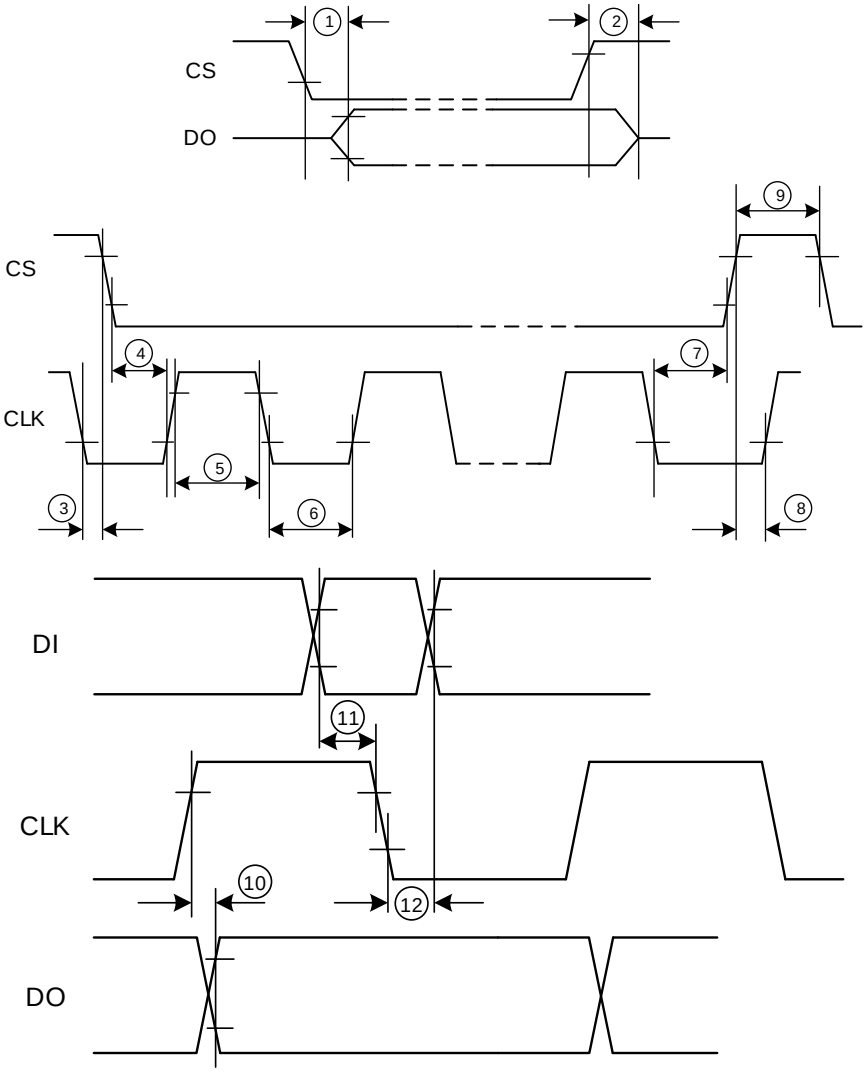
Parameters	Symbol	Condition	Min	Typ	Max	Units
CLK frequency	f_{CLK}				5	MHz
CLK period time	t_{PCLK}	V_{CC} = 5V	200			ns
		V_{CC} = 3.3V	500			
CLK high time	t_5		85			ns
CLK low time	t_6		85			ns
CLK set-up time (high to low)	t_7		85			ns
CLK set-up time (low to high)	t_3		85			ns
DI set-up time	t_{11}		50			ns
DI hold time	t_{12}		50			ns
CS set-up time (low to high)	t_8		100			ns
CS set-up time (high to low)	t_4		100			ns
CS high time	t_9		5			µs
DO enabled after CS falling edge	t_1	C_{DO} = 40pF			200	ns
DO disabled after CS rising edge	t_2	C_{DO} = 40pF			200	ns
DO fall/rise time		C_{DO} = 40pF		10	25	ns
DO valid time	t_{10}	C_{DO} = 40pF		20	50	ns
EN low valid time		V_{CC} = 5V, EN high to low, 50% to OUTx turning off 50%		50		µs
EN high to SPI valid					100	µs
Time between two consecutive SRR commands			100			µs

Note:

6) Not subject to production testing. Specified by design.

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SERIAL INTERFACE TIMING DIAGRAM



Inputs DI, CLK, CS: High Level = 0.7 x V_{CC}, Low Level = 0.3 x V_{CC}
Output DO: High Level = 0.8 x V_{CC}, Low Level = 0.2 x V_{CC}

Figure 1: Serial Interface Timing Diagram

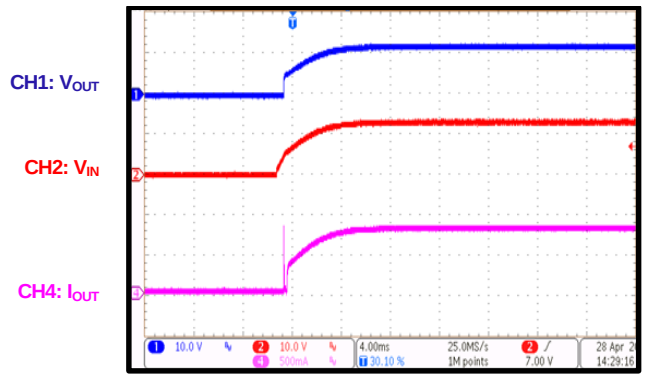
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TYPICAL PERFORMANCE CHARACTERISTICS

V_{VS} = 13V, V_{VCC} = 3.3V, T_A = 25°C, unless otherwise noted.

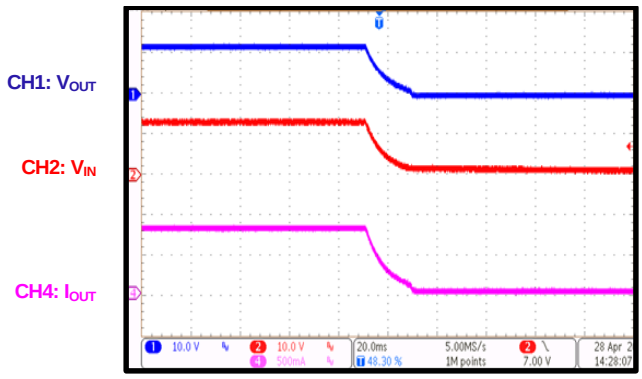
VIN Start-Up

HS on, I_{OUT} = 800mA



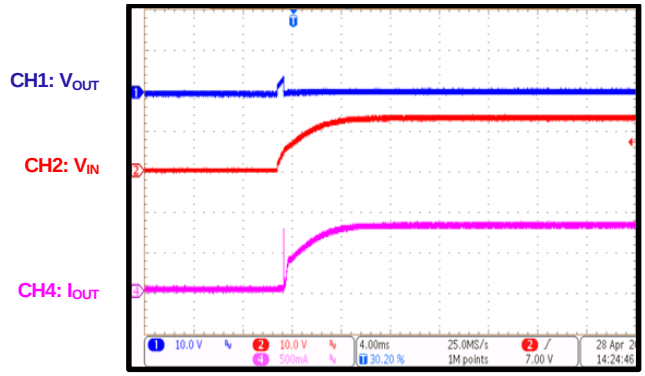
VIN Shutdown

HS on, I_{OUT} = 800mA



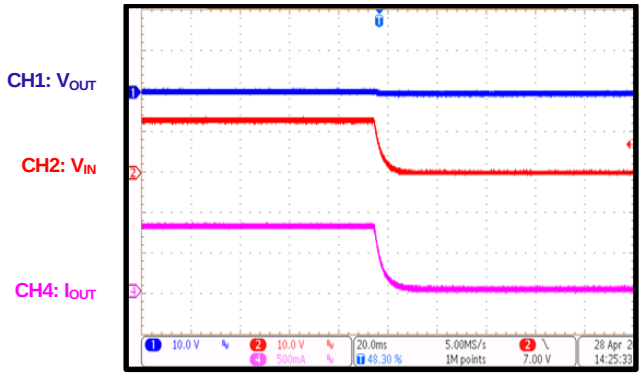
VIN Start-Up

LS on, I_{OUT} = 800mA



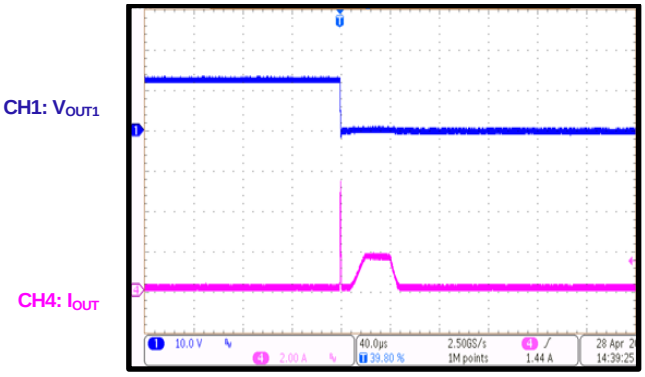
VIN Shutdown

LS on, I_{OUT} = 800mA



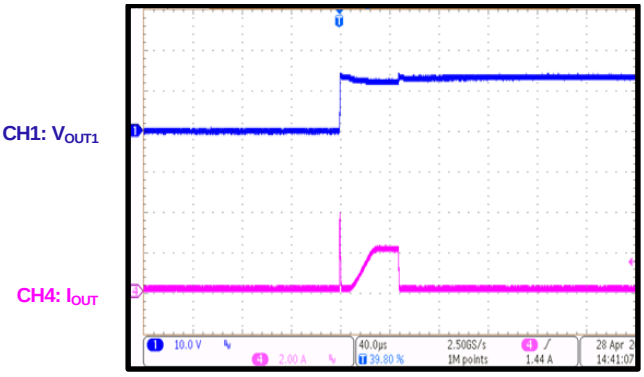
OCP

OUT shorted to GND



OCP

OUT shorted to VIN



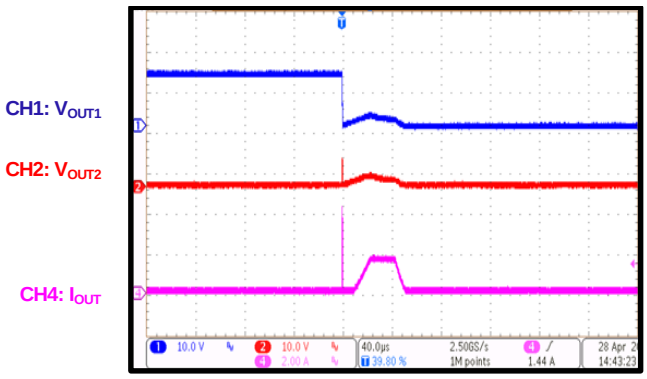
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TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{VS} = 13V, V_{VCC} = 3.3V, T_A = 25°C, unless otherwise noted.

OCP

OUT shorted to OUT



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FUNCTIONAL BLOCK DIAGRAM

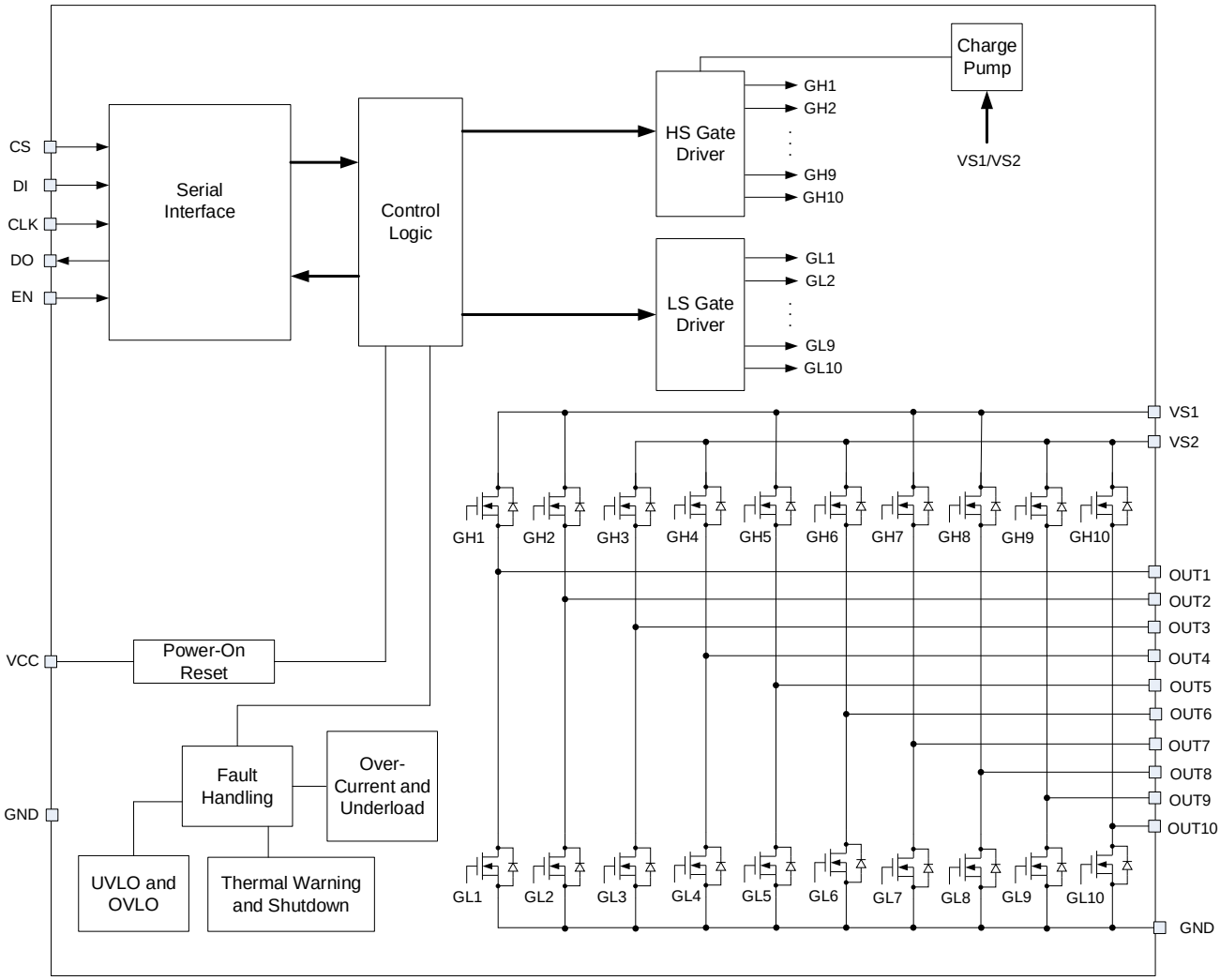


Figure 2: Functional Block Diagram

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OPERATION

The MPQ6527 is a ten-channel half-bridge DMOS output driver with integrated power MOSFETs. The device's ten half-bridges can be controlled separately from a standard serial data interface, and each has various diagnostic functions.

Serial Interface

Data transfer starts with the falling edge of the CS signal. Execution of new input data is enabled on the rising edge of the CS signal. Data must appear at DI and be synchronized to CLK; it is then accepted on the falling edge of the CLK signal. For DI, the MSB (SRR, bit[15]) has to be transferred first. The last 16 bits clocked into DI are transferred to the device's data register if there is no frame error. Otherwise, all DI data is ignored and the previous input data is preserved.

The output data at DO is enabled on the falling edge of the CS signal. In addition to the 16-bit status data, a pseudo-bit (PRE_15) can also be retrieved from the DO output. The latched thermal shutdown (TSD) status bit (also PRE_15) is available on DO until the first rising CLK edge after CS goes low. Output data changes its state with the rising edge of CLK, and remains stable until the next CLK rising edge appears. When CS is high, the DO pin is in a tri-state condition.

The following conditions must be met for a valid TSD read to be captured:

1. CLK and DI are low before the CS cycle.
2. CS transitions from high to low.
3. CS set-up time is complete.

Figure 3 shows the SPI communication. Table 1, Table 2, Table 3, and Table 4 define the input control registers and the output diagnosis registers.

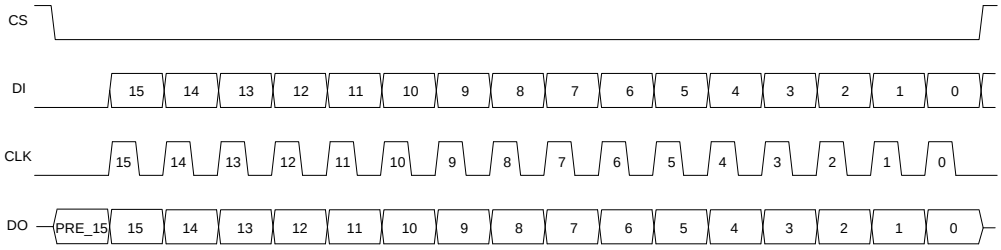


Figure 3: Data Transfer

Table 1: Input Control Registers for Channels 1–6

Channels 1–6 (Input Bit[14] = 0)		
Bit	**Input Register**	**Function**
15	SRR	This bit resets the status register. If SRR is set to 1, the error bits in the corresponding status register in the output data register are set to low.
14	CH_SEL	This bit selects the channel group. 1: Half-bridge, bits[10:7] 0: Half-bridge, bits[6:1]
13	OLSD_EN	This bit enables open-load detection shutdown (OLD_SD) for HB1 to HB6. This feature allows the affected output stage to be switched off if an open-load or underload condition has been detected. 1: Enabled 0: Disabled
12	HBEN6	This bit enables half-bridge 6. 1: Half-bridge 6 is active 0: Half-bridge is in Hi-Z

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11	HBEN5	This bit enables half-bridge 5. 1: Half-bridge 5 is active 0: Half-bridge 5 is in Hi-Z
10	HBEN4	This bit enables half-bridge 4. 1: Half-bridge 4 is active 0: Half-ridge 4 is in Hi-Z
9	HBEN3	This bit enables half-bridge 3. 1: Half-bridge 3 is active 0: Half-bridge 3 is in Hi-Z
8	HBEN2	This bit enables half-bridge 2. 1: Half-bridge 2 is active 0: Half-bridge 2 is in Hi-Z
7	HBEN1	This bit enables half-bridge 1. 1: Half-bridge is active 0: Half-bridge is in Hi-Z
6	HBCNF6	This bit configures half-bridge 6. 1: High-side MOSFET (HS-FET) on and low-side MOSFET (LS-FET) off 0: HS-FET off and LS on
5	HBCNF5	This bit configures half-bridge 5. 1: HS-FET on and LS-FET off 0: HS-FET off and LS-FET on
4	HBCNF4	This bit configures half-bridge 4. 1: HS-FET on and LS-FET off 0: HS-FET off and LS-FET on
3	HBCNF3	This bit configures half-bridge 3. 1: HS-FET on and LS-FET off 0: HS-FET off and LS-FET on
2	HBCNF2	This bit configures half-bridge 2. 1: HS-FET on and LS-FET off 0: HS-FET off and LS-FET on
1	HBCNF1	This bit configures half-bridge 1. 1: HS-FET on and LS-FET off 0: HS-FET off and LS-FET on
0	OVLO	This bit enables VSx over-voltage lockout (OVLO). 1: Enabled 0: Disabled

Table 2: Input Control Registers for Channels 7–10

Channels 7–10 (Input Bit[14] = 1)		
Bit	**Input Register**	**Function**
15	SRR	This bit resets the status register. If SRR is set to 1, the error bits in the corresponding status register in the output data register are set to low.

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14	CH_SEL	This bit selects the channel group. 1: Half-bridge, bits[10:7] 0: Half-bridge, bits[6:1]
13	OLSD_EN	This bit enables open-load detection shutdown (OLD_SD) for HB7 to HB10. This feature allows the affected output stage to be switched off if an open-load or underload condition has been detected. 1: Enabled 0: Disabled
12	RESERVED	Reserved.
11	RESERVED	Reserved.
10	HBEN10	This bit enables half-bridge 10. 1: Half-bridge 10 is active 0: Half-bridge 10 is in Hi-Z
9	HBEN9	This bit enables half-bridge 9. 1: Half-bridge 9 is active 0: Half-bridge 9 is in Hi-Z
8	HBEN8	This bit enables half-bridge 8. 1: Half-bridge 8 is active 0: Half-bridge 8 is in Hi-Z
7	HBEN7	This bit enables half-bridge 7. 1: Half-bridge 7 is active 0: Half-bridge 7 is in Hi-Z
6	RESERVED	Reserved.
5	RESERVED	Reserved.
4	HBCNF10	This bit configures half-bridge 10. 1: High-side MOSFET (HS-FET) on and low-side MOSFET (LS-FET) off 0: HS-FET off and LS-FET on
3	HBCNF9	This bit configures half-bridge 9. 1: HS-FET on and LS-FET off 0: HS-FET off and LS-FET on
2	HBCNF8	This bit configures half-bridge 8. 1: HS-FET on and LS-FET off 0: HS-FET off and LS-FET on
1	HBCNF7	This bit configures half-bridge 7. 1: HS-FET on and LS-FET off 0: HS-FET off and LS-FET on
0	OVLO	This bit enables VSx over-voltage lockout (OVLO). 1: Enabled 0: Disabled

Note:

7) All input bits are set to 0 after V_{CC} power-on reset (POR).

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Table 3: Output Diagnosis Registers for Channels 1–6

Channels 1–6 (Input Bit[14] = 0)		
Bit	**Input Register**	**Function**
PRE_15	TSD	If thermal shutdown occurs, this bit is latched and the corresponding output is switched off. This bit can only be reset via SRR or a power-on reset. 1: Thermal shutdown has occurred 0: Thermal shutdown has not occurred
15	OC (HB [6:1])	If over-current shutdown occurs, this bit is latched. An over-current error is set if any of the HB1 to HB6 bits experiences an overload or short-circuit condition. Then the relevant bit is latched and the corresponding output is switched off. This bit can only be reset via SRR or a power-on reset. 1: An over-current (OC) fault has occurred 0: No OC fault has occurred
14	PSF	If there is a power supply failure (VS1 and/or VS2 experiences an over-voltage or under-voltage condition), this bit is set and all outputs are switched off. Bit[14] is automatically reset if VSx returns to its normal operating range. 1: A power supply fault has occurred 0: No power supply fault has occurred
13	OLD (HB [6:1])	If an open-load error occurs, this bit is set. If any of the HB1 to HB6 bits experiences an open-load or underload condition, this bit is latched and the corresponding output is switched off if this bit is high. Bit[13] can only be reset via SRR or a power-on reset. 1: A load error has occurred 0: No load error has occurred
12	SHBEN6	Half-bridge 6 output status. 1: Half-bridge 6 is active 0: Half-bridge 6 is in Hi-Z
11	SHBEN5	Half-bridge 5 output status. 1: Half-bridge 5 is active 0: Half-bridge 5 is in Hi-Z
10	SHBEN4	Half-bridge 4 output status. 1: Half-bridge 4 is active 0: Half-bridge 4 is in Hi-Z
9	SHBEN3	Half-bridge 3 output status. 1: Half-bridge 3 is active 0: Half-bridge 3 is in Hi-Z
8	SHBEN2	Half-bridge 2 output status. 1: Half-bridge 2 is active 0: Half-bridge 2 is in Hi-Z
7	SHBEN1	Half-bridge 1 output status. 1: Half-bridge 1 is active 0: Half-bridge 1 is in Hi-Z

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6	HBCNF6	Half-bridge 6 configuration status. 1: High-side MOSFET (HS-FET) on and low-side MOSFET (LS-FET) off 0: HS-FET off and LS-FET on
5	HBCNF5	Half-bridge 5 configuration status. 1: HS-FET on and LS-FET off 0: HS-FET off and LS-FET on
4	HBCNF4	Half-bridge 4 configuration status. 1: HS-FET on and LS-FET off 0: HS-FET off and LS-FET on
3	HBCNF3	Half-bridge 3 configuration status. 1: HS-FET on and LS-FET off 0: HS-FET off and LS-FET on
2	HBCNF2	Half-bridge 2 configuration status. 1: HS-FET on and LS-FET off 0: HS-FET off and LS-FET on
1	HBCNF1	Half-bridge 1 configuration status. 1: HS-FET on and LS-FET off 0: HS-FET off and LS-FET on
0	TW	This bit indicates if there is a thermal warning, and is set high if the junction temperature reaches T_{JW}. The output remains on until one or more sensors reach T_{SD}. This bit automatically resets if the junction temperature drops below the thermal warning recovery point. 1: A thermal warning fault has occurred 0: A thermal warning fault has not occurred

Table 4: Output Diagnosis Registers for Channels 7–10

Channels 7–10 (Input Bit[14] = 1)		
Bit	**Input Register**	**Function**
PRE_15	TSD	If thermal shutdown is detected, the bit is latched and the corresponding output is switched off. This bit can only be reset via SRR or a power-on reset. 1: Thermal shutdown has occurred 0: Thermal shutdown has not occurred
15	OC (HB [10:7])	This bit latches if over-current shutdown occurs. An over-current error is set if any one of HB7 to HB10 has an overload or short-circuit condition. Then the bit is latched and the corresponding output is switched off. This bit can only be reset via SRR or a power-on reset. 1: An over-current (OC) fault has occurred 0: No OC fault has occurred
14	PSF	This bit is set if there is a power supply failure (VS1 and/or VS2 experiences an over-voltage or under-voltage condition). All outputs are switched off. Bit[14] is automatically reset if VSx returns to its normal operating range. 1: A power supply fault has occurred 0: No power supply fault has occurred

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13	OLD (HB [10:7])	If an open-load error occurs, this bit is set. If and of the HB1 to HB6 bits experiences an open-load or underload condition, this bit is latched and the corresponding output is switched off if this bit is high. Bit[13] can only be reset via SRR or a power-on reset. 1: A load error has occurred 0: No load error has occurred
12	RESERVED	Reserved.
11	RESERVED	Reserved.
10	SHBEN10	Half-bridge 10 output status. 1 = Half-bridge 10 is active 0 = Half-bridge 10 is in Hi-Z
9	SHBEN9	Half-bridge 9 output status. 1 = Half-bridge 9 is active 0 = Half-bridge 9 is in Hi-Z
8	SHBEN8	Half-bridge 8 output status. 1 = Half-bridge is active 0 = Half-bridge is in Hi-Z
7	SHBEN7	Half-bridge 7 output status. 1 = Half-bridge 7 is active 0 = Half-bridge 7 is in Hi-Z
6	RESERVED	Reserved.
5	RESERVED	Reserved.
4	HBCNF10	Half-bridge 10 configuration status. 1: High-side MOSFET (HS-FET) on and low-side MOSGET (LS-FET) off 0: HS-FET off and LS-FET on
3	HBCNF9	Half-bridge 9 configuration status. 1: HS-FET on and LS-FET off 0: HS-FET off and LS-FET on
2	HBCNF8	Half-bridge 8 configuration status. 1: HS-FET on and LS-FET off 0: HS-FET off and LS-FET on
1	HBCNF7	Half-bridge 7 configuration status. 1: HS-FET on and LS-FET off 0: HS-FET off and LS-FET on
0	TW	This bit indicates if there is a thermal warning, and is set high if the junction temperature reaches T_{JW}. The output remains on until one or more sensors reach T_{SD}. This bit automatically resets if the junction temperature drops below the thermal warning recovery point. 1: A thermal warning fault has occurred 0: A thermal warning fault has not occurred

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Enable Control

The MPQ6527 enters low-power mode (also called sleep mode) when the EN pin is pulled low. The EN input has an internal pull-down resistor. In sleep mode, all output stages turn off and the SPI register banks are reset. The output stages can be activated again by switching the EN pin high.

Status Register Reset (SRR)

The Status Register Reset (SRR) command bit is executed after the next SPI transmission. Sending SRR = 1 clears the status memory and reactivates faulted outputs for the channels selected by CH_SEL.

If a fault is still present when SRR is sent, the protection is re-enabled and the device can shut down. The device can also be reset by toggling the EN pin or by VCC power-on reset.

Open-Load Detection

Open-load detection is turned on by the low-side MOSFETs (LS-FETs) on the bridge outputs. If the current through the low-side transistor is below the reference current (I_{OLD}) for longer than the open-load detection delay time (t_{DOLD}), the corresponding open-load diagnosis bit is set. If an underload condition occurs in another channel after the global timer has started, the delay for any subsequent underload conditions is the remainder of the timer. The timer runs continuously if there is a persistent underload condition.

If the OLSD_EN bit is set and an open load is detected on the LS-FET, the respective output is disabled and the open-load error bit is latched. Otherwise, the output remains on and the open-load error bit is set. If the OLSD_EN bit is set, the error remains latched and the output remains off until an SRR or power-on reset is performed. The channel group select (CH_SEL) input bit determines which channels are affected by SRR. SRR also determines which half-bridges are latched off via the OLSD_EN command bit. This provides the ability to independently diagnose and isolate error flags to their corresponding failed output.

For example, a motor can be connected between outputs OUT1 and OUT2 with a broken wire (see Figure 4).

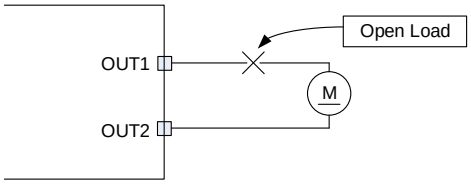


Figure 4: H-Bridge Open Load Example

Table 5 lists the resulting diagnostic information.

Table 5: Open-Load Diagnosis Examples

Control				Diagnostic Information	
				Motor Connected	Motor Disconnected
LS1	HS1	LS2	HS2	OLD (Output Bit[13])	
0	0	0	0	0	0
1	0	0	1	0	1
0	1	1	0	0	1
0	1	0	1	0	0
1	0	1	0	1	1

In motor applications, it is useful to actively brake the motor by turning on both the high-side (HS) and low-side (LS) drivers in two half-bridge channels. If the configuration is two LS drivers (LS brake), an underload may be triggered as the motor current decays normally, so use the HS brake to avoid an underload condition.

Discharge Circuit

Figure 5 shows a typical application that uses an inverse-polarity protection diode (D1).

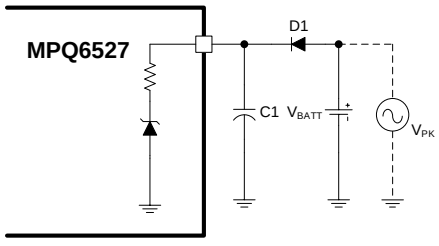


Figure 5: Discharger Circuit Functional Principle

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However, this method can be dangerous. The IC consumes an extremely low current (I_{VS}) while in inhibit mode (maximum 20μA). Any peaks on the supply voltage gradually charge the blocking capacitor. D1 prevents the capacitor from discharging via the power supply. due to the extremely small quiescent current, discharging via the IC is negligible. This means that during long periods in inhibit mode, the IC's voltage supply could increase until it exceeds the 40V voltage limit and damages the IC. The MPQ6527 provides a discharger circuit to prevent this. If V_{VS} exceeds a threshold value of about 37V, the blocking capacitor is discharged via an integrated resistor until V_{VS} drops below the threshold.

Diagnostics and Protections Overview

Table 6 lists the diagnostic classes and functions associated with the MPQ6527.

Table 6: Diagnostic Classes and Functions

Fault	Qualifier	State and Recovery	
		OUTx	Output Register
Thermal Shutdown	N/A	Hi-Z, need SRR to reset	TSD = 1, requires SRR to reset
Over-Current Shutdown	N/A		OC = 1, requires SRR to reset
Open-Load Detection	OLSD_EN = 1		OLD = 1, requires SRR to reset
	OLSD_EN = 0	Unaffected	
Ove-Voltage Lockout	OVLO = 1	Hi-Z, unlatched (8)	PSF = 1, unlatched (9)
	OVLO = 0	Unaffected	
Under-Voltage Lockout	N/A	Hi-Z, unlatched (8)	
Thermal Warning	N/A	Unaffected	TW = 1, unlatched (9)

Notes:

8) OUTx returns to its previous state or a new state once the fault is removed.
9) The corresponding output register returns to its no-fault state once the fault is removed.

Over-Current Protection (OCP)

The MPQ6527 has internal overload and short-circuit protection. The currents in both the high-side MOSFETs (HS-FETs) and LS-FETs are measured. If any current exceeds the current limit, an internal timer starts. If the over-current shutdown delay time (t_{OC}) is reached, the short-circuit detection bit (OC) is set, and the shorted output is disabled. The OC bit is reset by writing the SSR bit in the register to 1, and then the disabled outputs are enabled. The channel group selection input bit (CH_SEL) determines which channels are affected by SRR.

Thermal Shutdown and Pre-Warning

Thermal monitoring is integrated into the MPQ6527. Each half-bridge monitors the driver pair's thermal sensor. If the junction temperature exceeds the thermal pre-warning threshold, the temperature pre-warning bit (TW) in the output register is set. If the temperature returns below the thermal pre-warning threshold, the TW bit is reset.

If the junction temperature exceeds the thermal shutdown threshold, the channel's HS and LS drivers latch off, the TW bit remains set, and the TSD (PRE_15) bit is set. If the junction temperature falls below the thermal shutdown threshold, the TSD bit is cleared and all affected channels in the group resume immediately. This can also be accomplished by setting the SRR bit in the input register to 1. The channel group selection input bit (CH_SEL) determines which channels are affected by SRR.

The thermal pre-warning and shutdown thresholds have a hysteresis.

VS Under-Voltage Lockout (UVLO)

If the voltage on the VS pin falls below the under-voltage lockout (UVLO) threshold, an internal timer starts.

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If the UVLO delay time is reached, the power supply fail bit (PSF) in the output register is set, and all outputs are disabled. Once VS exceeds the UVLO threshold and the PSF bit is cleared, then normal operation resumes immediately.

VCC Under-Voltage Conditions

The SPI interface cannot operate if VCC is below its under-voltage threshold. In this case, all outputs turn off, and the command input and status output registers are cleared.

Once the VCC voltage exceeds the under-voltage threshold, SRR is released and the under-voltage status is reset.

VS Over-Voltage Lockout (OVLO)

If the supply voltage (V_{VS}) exceeds the switch-off voltage (V_{OVOFF}), all outputs are switched off if the over-voltage lockout input bit is set (OVLO = 1), and the PSF error bit is set. The error is not latched. This means that if V_{VS} falls below the switch on threshold voltage, the power stages restart and the error flags are reset.

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APPLICATION INFORMATION

PCB Layout Guidelines

PCB layout is critical for stable operation. For the best results, follow the guidelines below:

1. Place a bulk capacitor on the VIN pin to absorb the energy flowing from the motor or power supply. The capacitor should be sized according to the application requirements.
2. Place the supply bypass capacitor as close as possible to the IC. It is recommended to use a supply-rated X5R or X7R capacitor.
3. Place as much copper as possible on the long pads.
4. Place thermal vias inside the pad area to move heat to the copper layers.
5. Place vias just outside the pad area if vias cannot be placed in the pad area.

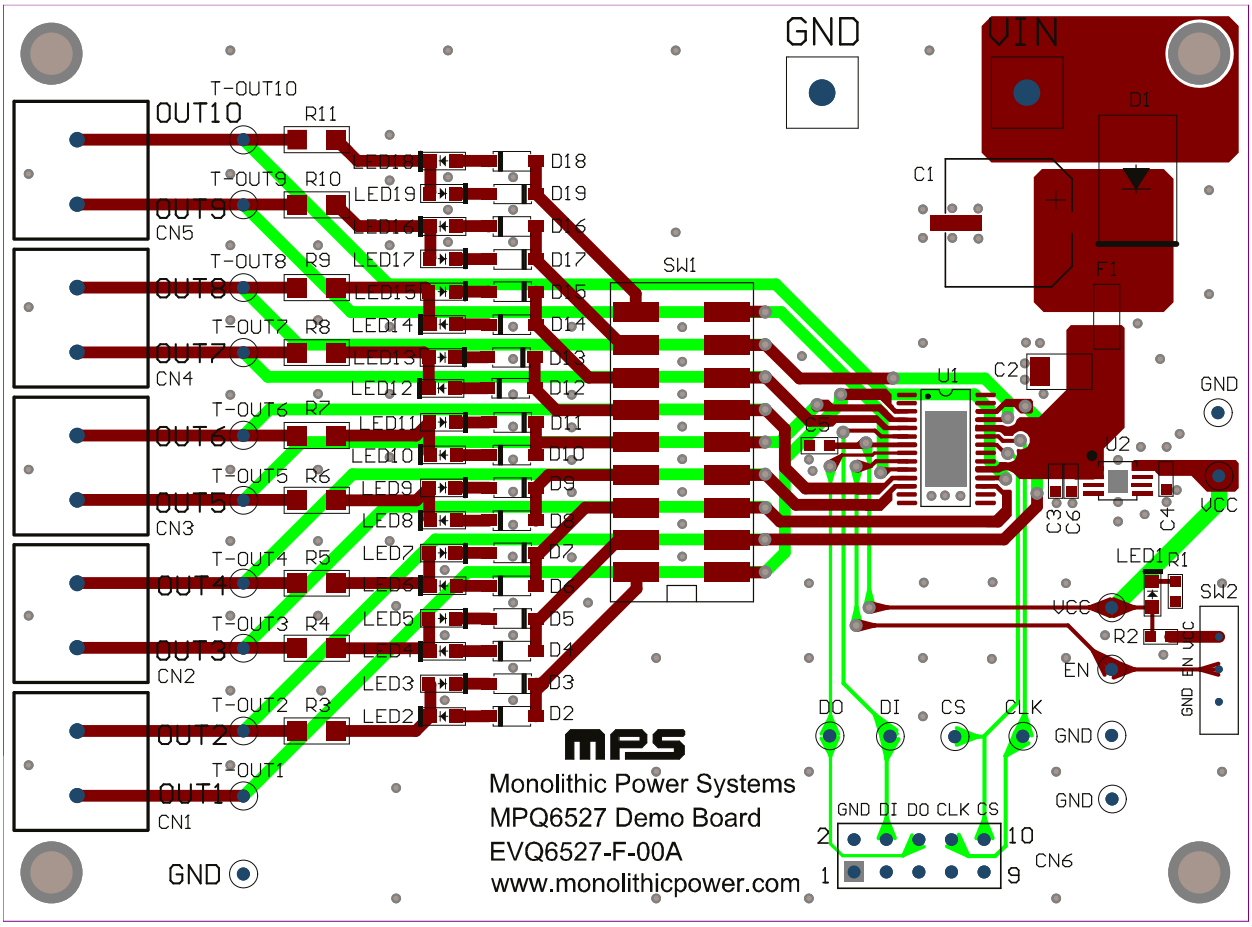
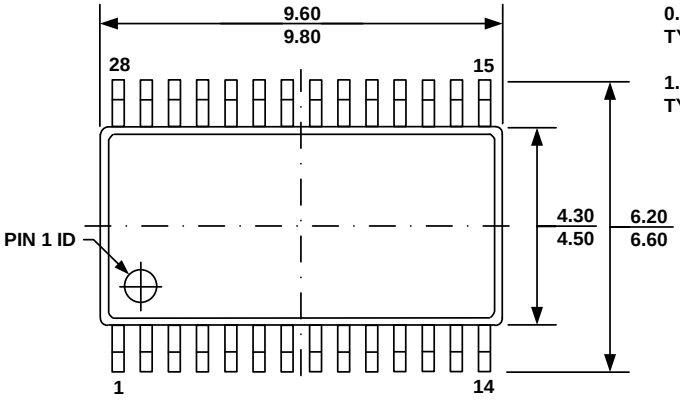


Figure 6: Recommended PCB Layout

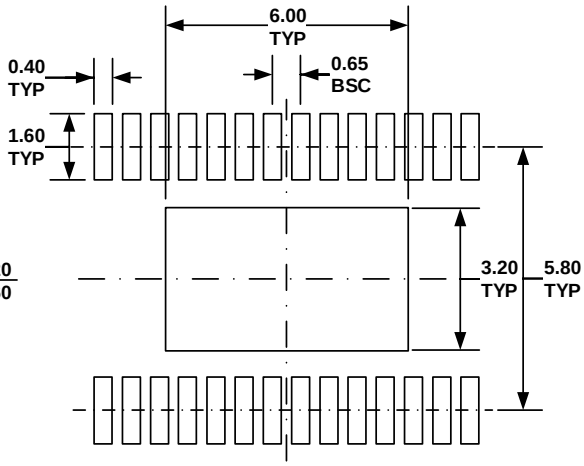
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PACKAGE INFORMATION

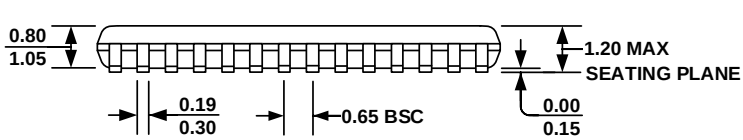
TSSOP-28EP



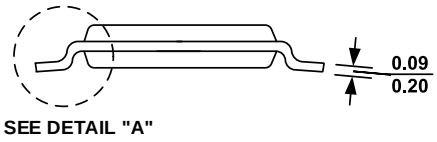
TOP VIEW



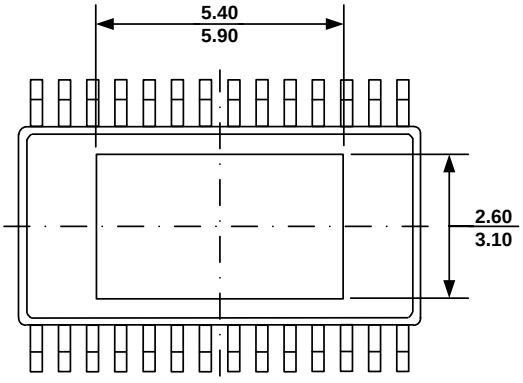
RECOMMENDED LAND PATTERN



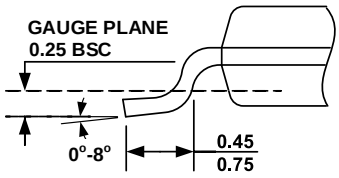
FRONT VIEW



SIDE VIEW



BOTTOM VIEW



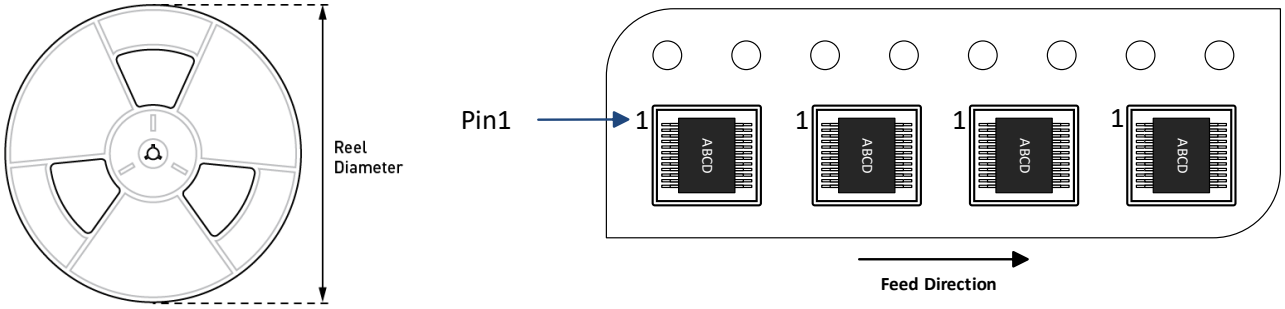
DETAIL “A”

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION, OR GATE BURR.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
5) DRAWING CONFORMS TO JEDEC MO-153, VARIATION AET.
6) DRAWING IS NOT TO SCALE.

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CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MPQ6527GF-AEC1-Z	TSSOP-28EP	2500	50	13in	16mm	8mm

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REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	9/23/2021	Initial Release	-

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