# MPQ7790

## 18V, 15W, Low-EMI, Mono BTL Class-D Audio Amplifier AEC-Q100 Qualified

## DESCRIPTION

The MPQ7790 is an automotive grade, low-EMI, analog input class-D audio amplifier, which can drive mono speakers in a bridge-tied load configuration. It is a fully integrated audio amplifier that dramatically reduces solution size, featuring 300mΩ power MOSFETs, start-up/shutdown pop elimination, short-circuit protection circuits, and EMI reduction technique.

The MPQ7790 utilizes a BTL structure capable of delivering 15W into 8Ω speakers with a 16V power supply. MPS class-D audio amplifiers exhibit the high fidelity of class-AB amplifiers at high efficiency.

The MPQ7790 includes an internal circuit that allows the system to shut down automatically after the absence of an audio signal is detected. This feature is ideal for battery-operated systems.

The MPQ7790 also has an adjustable power-limit function. The PLIMIT circuit sets a limit on the output peak-to-peak voltage by limiting the duty cycle to a fixed maximum value. This limit can be thought of as a “virtual” voltage rail, which is lower than the supply connected to PVCC.

The MPQ7790 is available in a TSSOP-20 EP package.

## FEATURES

- 5.5 to 18V PVCC
- ±4.5A Peak Current Output
- Output Power:
  9W at 12V, 8Ω Load, 10% THD
  15W at 16V, 8Ω Load, 10% THD
- 90% Efficiency with 8Ω Load, 10% THD
- 300mΩ Power MOSFETs
- Start-Up/Shutdown Pop Elimination
- Short-Circuit Protection Circuits
- EMI Reduction Technique
- All Switches Current Limited
- Internal Under-Voltage Protection
- Internal Thermal Protection
- Adjustable Power Limiter
- Automatic Shutdown with Zero Input Signal Detection
- Fault Output Flag
- Available in AEC-Q100 Grade-1
- Available in a TSSOP-20 EP Package

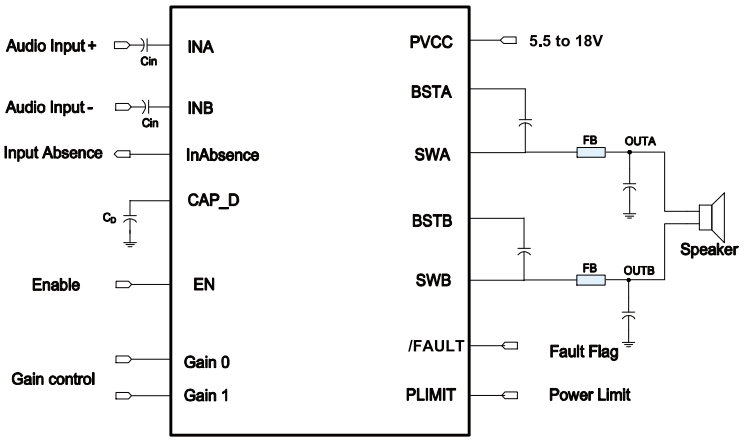
## APPLICATIONS

- Automotive E-Call
- Telematic System

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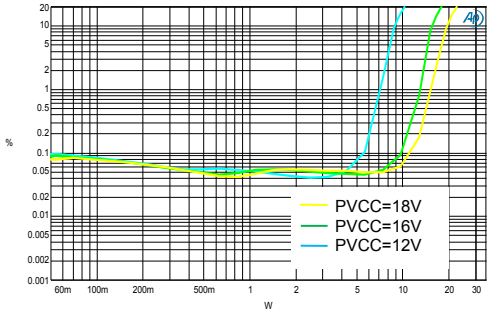

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## TYPICAL APPLICATION




**THD + N vs. $P_{OUT}$**

1kHz, 8Ω + 66μH





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## ORDERING INFORMATION

| Part Number* | Package | Top Marking |
|---|---|---|
| MPQ7790GF-AEC1 | TSSOP20-EP | *See Below* |

* For Tape & Reel, add suffix –Z (e.g. MPQ7790GF-AEC1–Z).

## TOP MARKING

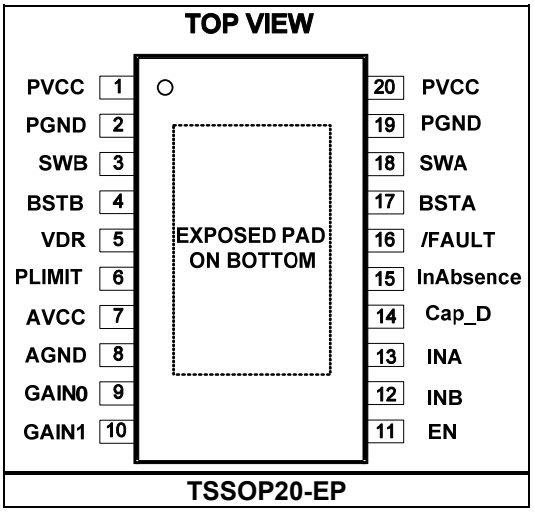
MPSYYWW

MP7790

LLLLLLLLL

MPS: MPS prefix
YY: Year code
WW: Week code
MP7790: Part number
LLLLLLLLL: Lot number

## PACKAGE REFERENCE





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## PIN FUNCTIONS

| Pin # | Name | Description |
|---|---|---|
| 1, 20 | PVCC | **Power supply input.** Bypass PVCC to PGND with a 1µF X7R capacitor (in addition to the main bulk capacitor) placed close to the PVCC and PGND pins. |
| 2, 19 | PGND | **Power ground for amplifier.** |
| 3 | SWB | **Switched power output for amplifier B** (the negative output). |
| 4 | BSTB | **High-side MOSFET bootstrap input for amplifier B.** A capacitor from BSTB to SWB supplies the gate drive current to the internal high-side MOSFET. |
| 5 | VDR | **Gate drive supply bypass.** VDR powers the internal circuitry, internal MOSFET gate drive, and the PLIMIT function. Bypass VDR to AGND with a 0.1µF to 10µF capacitor. |
| 6 | PLIMIT | **Power limit and anti-clipping feature control.** Connect a resistor divider from AVCC to GND to set the power limit. Connect directly to AVCC for no power limit. |
| 7 | AVCC | **Internal analog reference.** Requires a bypass capacitor connected from AVCC to AGND. |
| 8 | AGND | **Analog ground.** |
| 9 | GAIN0 | **Gain selection bit.** |
| 10 | GAIN1 | **Gain selection bit.** |
| 11 | EN | **Enable input.** Drive EN high to turn on the amplifiers. Drive EN low to turn them off. |
| 12 | INB | **Negative audio input.** Biased at 2.5V. |
| 13 | INA | **Positive audio input.** Biased at 2.5V. |
| 14 | Cap_D | **Delay time control for input signal absence report function.** This hold time can be adjusted with an external capacitor. Connect this pin to AGND to disable automatic shutdown with the zero signal input function. |
| 15 | In Absence | **Open-drain output used to report the input signal absence.** |
| 16 | /FAULT | **Fault output.** A low output at /FAULT indicates that the IC has detected an over-temperature or over-current condition. This output is open drain. |
| 17 | BSTA | **High-side MOSFET bootstrap input for amplifier A.** A capacitor from BSTA to SWA supplies the gate drive current to the internal high-side MOSFET. |
| 18 | SWA | **Switched power output for amplifier A** (the positive output). |

## ABSOLUTE MAXIMUM RATINGS (1)

Supply voltage PVCC ..... -0.3V to +24V
$V_{SW}$ ..... -1V to $V_{PVCC}$ + 1V
$V_{EN}$, $V_{/FAULT}$, $V_{GAIN}$ ..... -0.3V to $V_{PVCC}$ + 0.3V
BS voltage $V_{BST}$..... $V_{SW}$ - 0.3V to $V_{SW}$ + 6.5V
$V_{PLIMIT}$ ..... -0.3V to $V_{AVCC}$ + 0.3V
$V_{INA}$, $V_{INB}$ ..... -0.3V to 6.5V
VGND to PGND..... -0.3V to +0.3V
Continuous power dissipation ($T_A$ = +25°C) (2)
..... 3.9W
Junction temperature.....150°C
Lead temperature.....260°C
Storage temperature..... -65°C to +150°C

## *Recommended Operating Conditions*

Supply voltage PVCC ..... 5.5V to 18V
Operating junction temp ($T_J$)
.....-40°C to +125°C (3)

## *Thermal Resistance* $\theta_{JA}$ $\theta_{JC}$

TSSOP20-EP .....40.....8...°C/W (4)
TSSOP20-EP .....25 ....6.5..°C/W (5)

**NOTES:**

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature $T_J$ (MAX), the junction-to-ambient thermal resistance $\theta_{JA}$, and the ambient temperature $T_A$. The maximum allowable continuous power dissipation at any ambient temperature is calculated by $P_D$ (MAX) = ($T_J$ (MAX) - $T_A$) / $\theta_{JA}$. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) Operating devices at junction temperatures greater than 125°C is possible; please contact MPS for details.
4) Measured on JESD51-7, 4-layer PCB.
5) Measured on standard EVB, 8.5cmx8.5cm, 2-layer PCB.


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## ELECTRICAL CHARACTERISTICS

**PVCC = 12V, $V_{EN}$ = 5V, $T_J$ = -40°C to +125°C, typical values are at $T_J$ = +25°C, unless otherwise noted.**

| Parameters | Symbol | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| Standby current | $I_{QSTBY}$ | $V_{EN}$ = 0V, $N_{IN}$ = $P_{IN}$ = float | | 50 | 100 | μA |
| Quiescent current | $I_Q$ | $V_{EN}$ = 5V, no load, no LC filter | | 5 | 7 | mA |
| Output offset voltage | $V_{OS}$ | $V_I$ = 0V, gain = 36dB, $T_J$ = 25°C | -60 | 1 | 60 | mV |
| | | $V_I$ = 0V, gain = 36dB, $T_J$ = -40°C to 125°C | -80 | | 80 | mV |
| SW on resistance | $R_{DSON}$ | $I_O$ = 500mA, $T_J$ = 25°C | | 0.3 | 0.4 | Ω |
| | | $I_O$ = 500mA, $T_J$ = -40°C to 125°C | | | 0.5 | |
| Short-circuit current | | Sourcing and sinking | 3 | 4.5 | 6 | A |
| Closed loop gain | G | GAIN0 = L, GAIN1 = L | 19 | 20 | 21 | dB |
| | | GAIN0 = L, GAIN1 = H | 25 | 26 | 27 | |
| | | GAIN0 = H, GAIN1 = L | 31 | 32 | 33 | |
| | | GAIN0 = H, GAIN1 = H | 35 | 36 | 37 | |
| EN enable threshold voltage | | $V_{EN}$ rising | | 1.4 | 2.0 | V |
| | | $V_{EN}$ falling | 0.4 | 1.0 | | V |
| EN enable input current | | $V_{EN}$ = 5V | | 12 | 25 | μA |
| PVCC rising | PVCC-rising | $T_J$ = 25°C | 4 | 4.6 | 5.1 | V |
| | | $T_J$ = -40°C to 125°C | 4 | 4.6 | 5.2 | |
| PVCC falling | PVCC-falling | $T_J$ = 25°C | 3.9 | 4.3 | 4.9 | V |
| | | $T_J$ = -40°C to 125°C | 3.7 | 4.3 | 4.9 | |
| Dead time (6) | | $I_O$ = 0.5A, $T_J$ = 25°C | | 40 | | ns |
| Turn-on time | $t_{ON}$ | | 8 | 15 | 22 | ms |
| Turn-off time | $t_{OFF}$ | | 100 | 250 | 500 | ns |
| Switching frequency | | $T_J$ = 25°C | 270 | 300 | 360 | kHz |
| | | $T_J$ = -40°C to 125°C | 240 | 300 | 360 | kHz |
| Thermal shutdown (6) | | $T_J$ rising | | 150 | | °C |
| Thermal shutdown hysteresis (6) | | | | 20 | | °C |

**NOTE:**

6) Not tested in production. Guaranteed by design and characterization.


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## OPERATING SPECIFICATIONS (7)

**PVCC = 12V, $V_{EN}$ = 5V, $T_J$ = -40°C to +125°C, typical values are at $T_J$ = +25°C, unless otherwise noted.**

| Parameters | Symbol | Condition | | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|
| Power output | | f = 1kHz, THD + N = 10%, PVCC = 12V, $R_{LOAD}$ = 8Ω | | | 9 | | W |
| | | f = 1kHz, THD + N = 10%, PVCC = 16V, $R_{LOAD}$ = 8Ω | | | 15 | | |
| THD + noise | | $P_{OUT}$ = 5W, f = 1kHz, $PV_{CC}$ = 12V, $R_{LOAD}$ = 8Ω | | | 0.1 | | % |
| | | $P_{OUT}$ = 5W, f = 1kHz, $PV_{CC}$ = 18V, $R_{LOAD}$ = 8Ω | | | 0.05 | | % |
| | | $P_{OUT}$ = 7.5W, f = 1kHz, $PV_{CC}$ = 12V, $R_{LOAD}$ = 4Ω | | | 0.15 | | % |
| | | $P_{OUT}$ = 7.5W, f = 1kHz, $PV_{CC}$ = 18V, $R_{LOAD}$ = 4Ω | | | 0.1 | | % |
| Efficiency | | $P_{OUT}$ = 9W, THD + N = 10%, $V_{CC}$ = 12V, 1kHz, $R_{LOAD}$ = 8Ω | | | 90 | | % |
| Noise floor | | A-weighted, 20Hz to 22kHz | | | 115 | | μV |
| Signal-to-noise ratio | | f = 1kHz, THD + N = 1%, A-weighted | | | -102 | | dB |
| Power supply rejection | | $V_{RIPPLE}$ = 300m$V_{PP}$, inputs AC-coupled to AGND | f = 1kHz | | -50 | | dB |
| | | | f = 217Hz | | -50 | | dB |

**NOTE:**

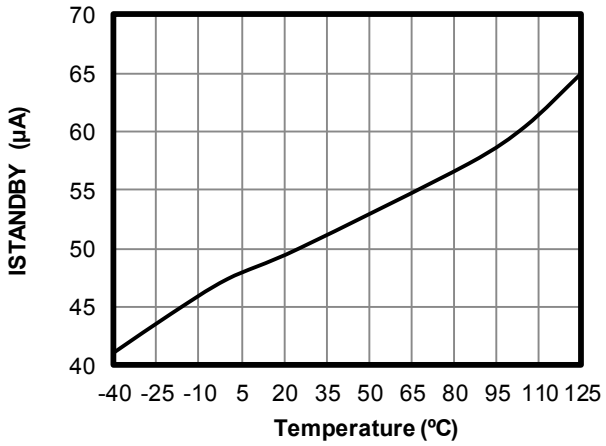
7) Operating specifications are for the IC in a typical application circuit. Not production tested.


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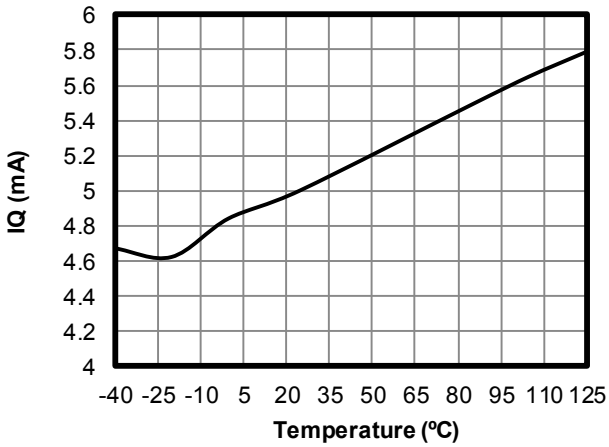
## TYPICAL CHARACTERISTICS

**PVCC = 12V, $T_J$ = -40°C to +125°C, unless otherwise noted.**

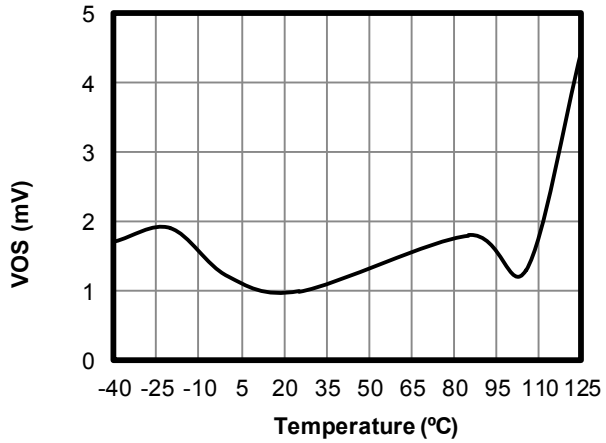
### $I_{STANDBY}$ vs. Temperature



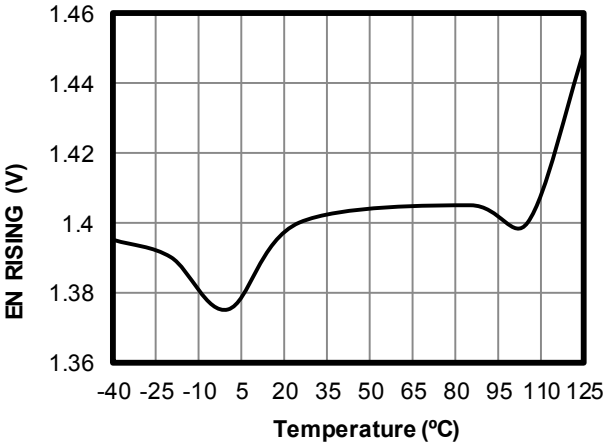

### $I_Q$ vs. Temperature



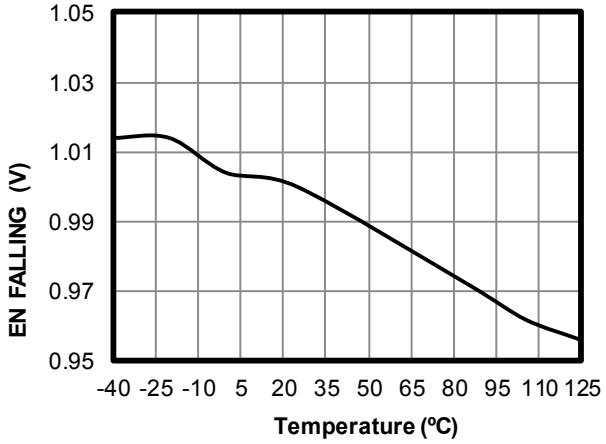

### $V_{OS}$ vs. Temperature



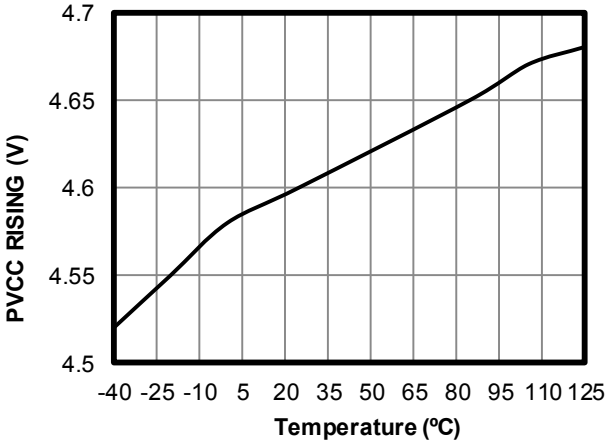

### EN Rising vs. Temperature




### EN Falling vs. Temperature




### PVCC Rising vs. Temperature



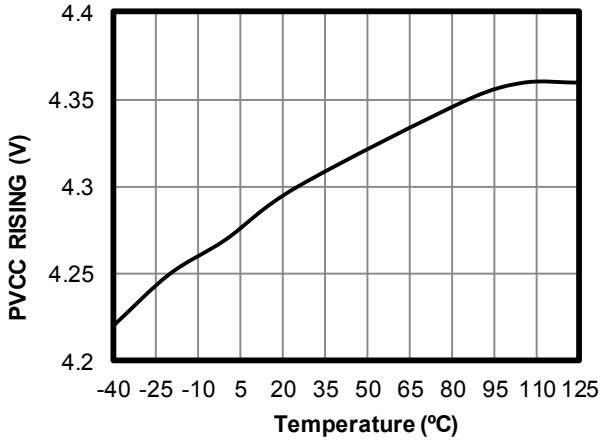


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## TYPICAL CHARACTERISTICS *(continued)*

**PVCC = 12V, $T_J$ = -40°C to +125°C, unless otherwise noted.**

**PVCC Falling vs. Temperature**



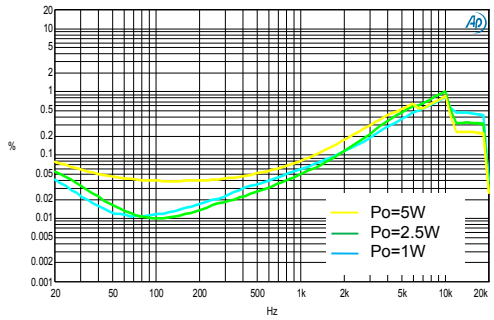


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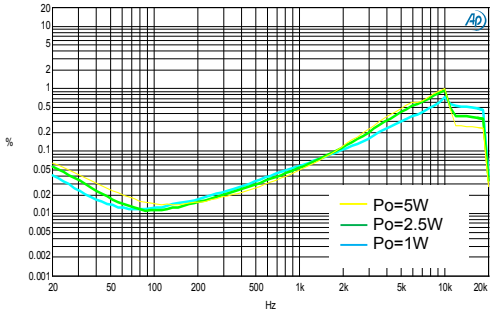
## TYPICAL PERFORMANCE CHARACTERISTICS

**PVCC = 12V, gain = 20dB, f = 1kHz, $T_J$ = 25°C, unless otherwise noted.**

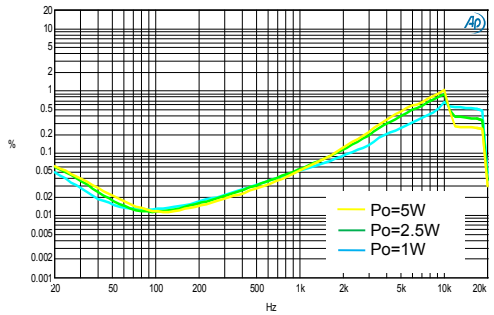
### THD + N vs. Frequency
12V, 8Ω + 66μH



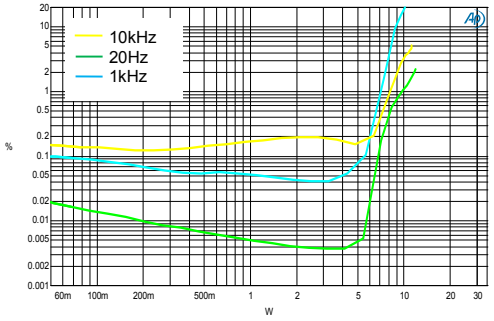

### THD + N vs. Frequency
16V, 8Ω + 66μH



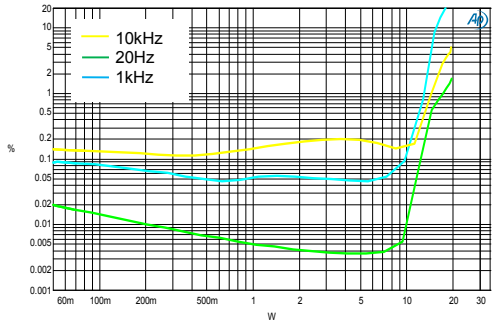

### THD + N vs. Frequency
18V, 8Ω + 66μH



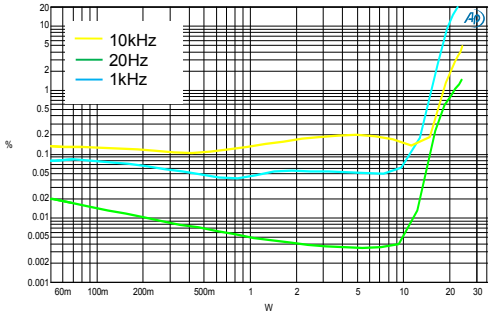

### THD + N vs. $P_{OUT}$
12V, 8Ω + 66μH




### THD + N vs. $P_{OUT}$
16V, 8Ω + 66μH




### THD + N vs. $P_{OUT}$
18V, 8Ω + 66μH





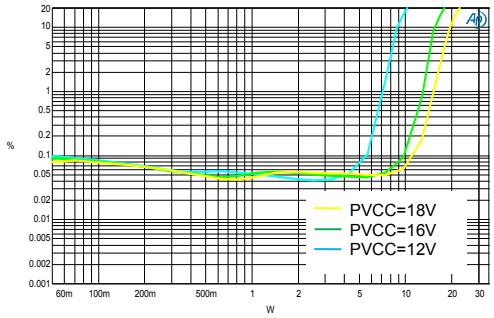
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## TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

**PVCC = 12V, gain = 20dB, f = 1kHz, $T_J$ = 25°C, unless otherwise noted.**

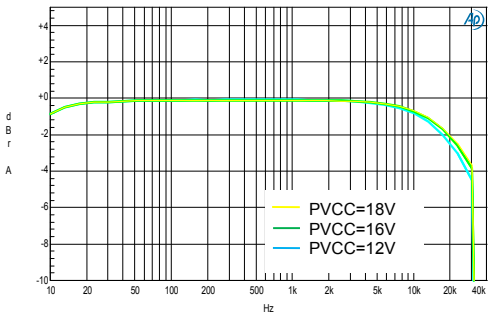
### THD + N vs. $P_{OUT}$

1kHz, 8Ω + 66μH



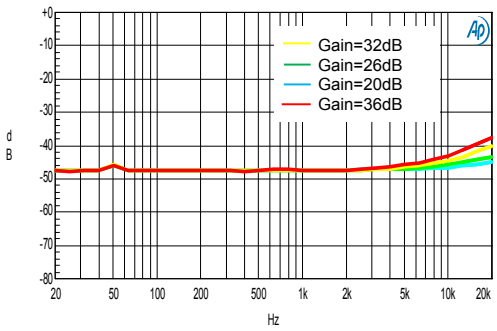

### Frequency Response

1W, 8Ω + 66μH



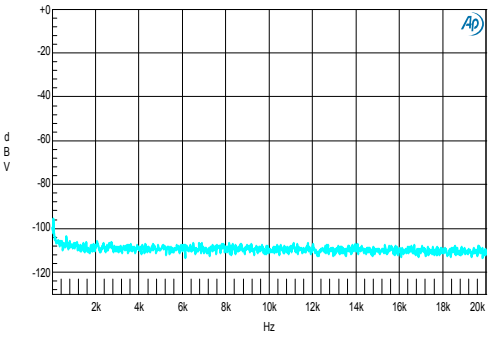

### PSRR

Vac-ripple = 300mVpp



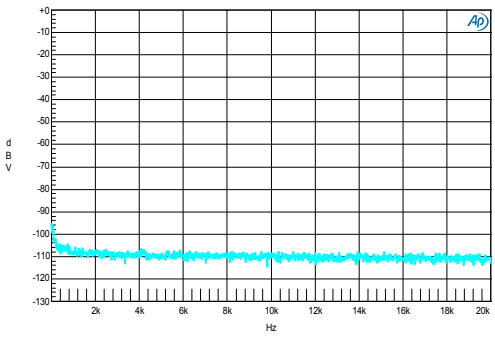

### FFT Noise Floor Test

12V, 8Ω + 66μH



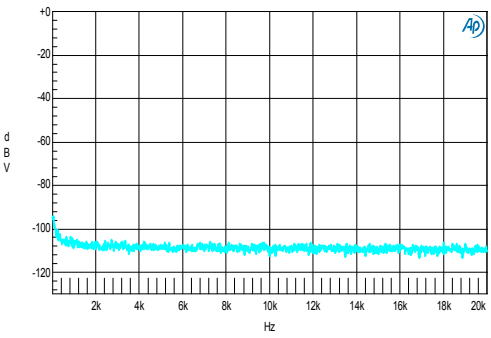

### FFT Noise Floor Test

16V, 8Ω + 66μH




### FFT Noise Floor Test

18V, 8Ω + 66μH



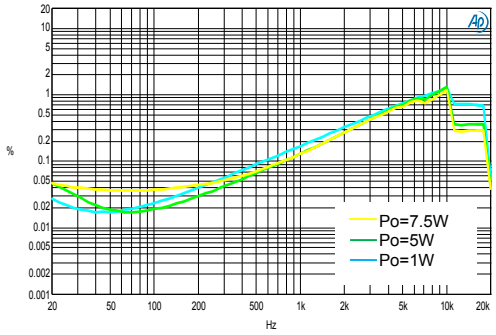


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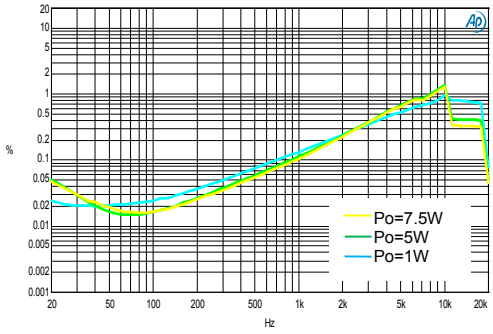
## TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

**PVCC = 12V, gain = 20dB, f = 1kHz, $T_J$ = 25°C, unless otherwise noted.**

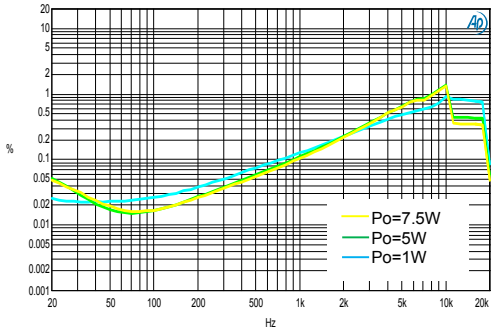
### THD + N vs. Frequency
12V, 4Ω + 33μH



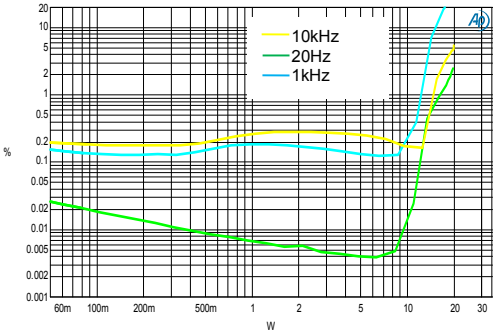

### THD + N vs. Frequency
16V, 4Ω + 33μH



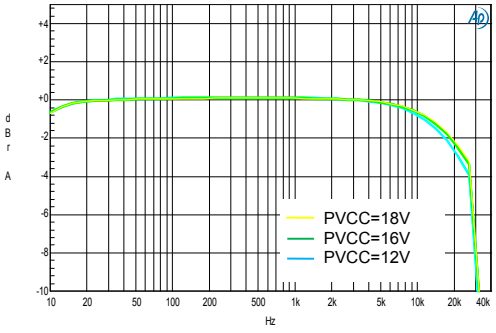

### THD + N vs. Frequency
18V, 4Ω + 33μH



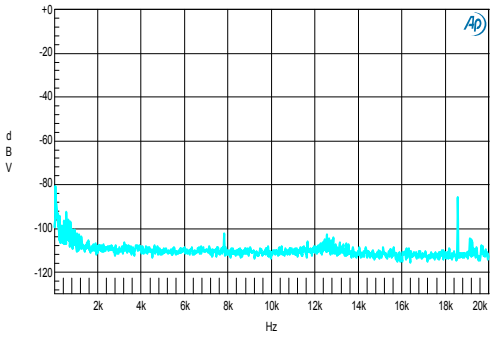

### THD + N vs. $P_{OUT}$
12V, 4Ω + 33μH




### Frequency Response
1W, 4Ω + 33μH




### FFT Noise Floor Test
12V, 4Ω + 33μH



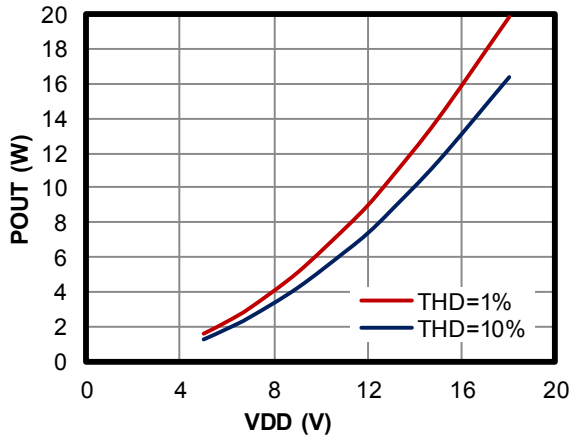


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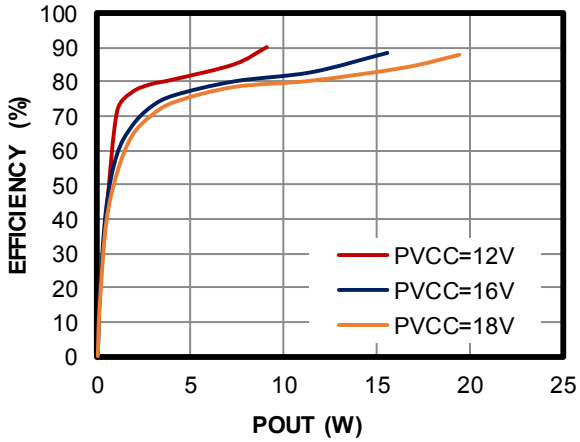
## TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

**PVCC = 12V, gain = 20dB, f = 1kHz, $T_J$ = 25°C, unless otherwise noted.**

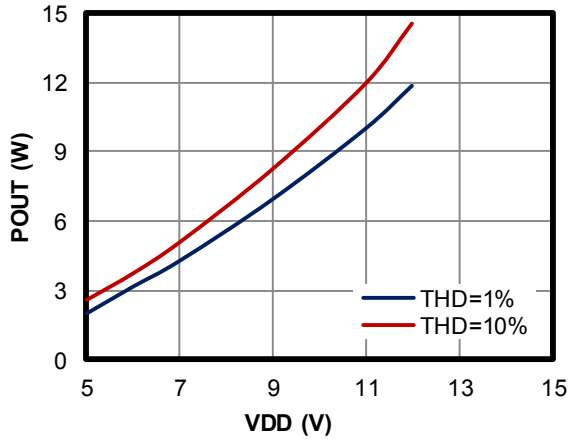
**$V_{DD}$ vs. $P_{OUT}$**
8Ω + 66μH



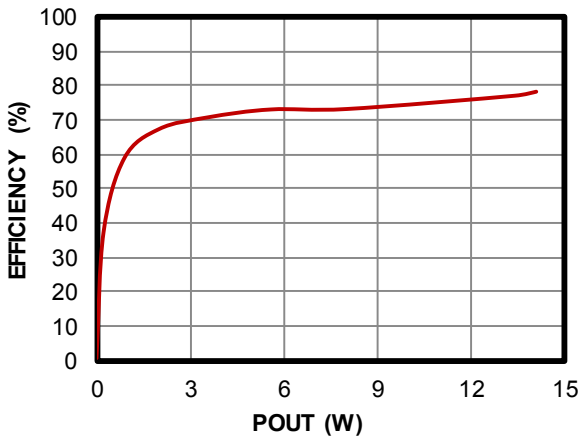

**Efficiency vs. $P_{OUT}$**
8Ω + 66μH




**$V_{DD}$ vs. $P_{OUT}$**
4Ω + 33μH




**Efficiency vs. $P_{OUT}$**
4Ω + 33μH





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# BLOCK DIAGRAM

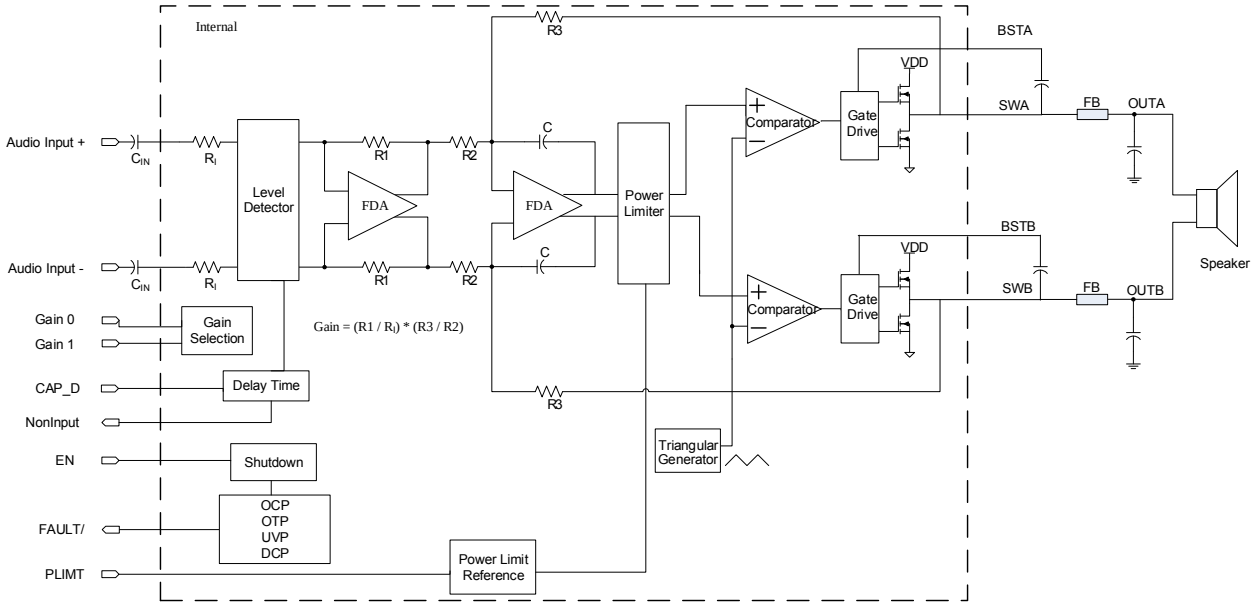



**Figure 1: Functional Block Diagram**


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## OPERATION

The MPQ7790 is a fully integrated, class-D mono BTL audio amplifier. Because of the switching class D output stage, power dissipation in the amplifier is reduced drastically when compared to class A, B, or A/B amplifiers, while maintaining high fidelity and low distortion.

The MPQ7790 includes four high-power MOSFETs. For each half-bridge channel, the output driver stage uses two N-channel MOSFETs to deliver the pulses to the LC output filter, which in turn drives the load. To fully enhance the high-side MOSFET, the gate is driven to a voltage higher than the source by the bootstrap capacitor between OUTx and BSTx. When the output is driven low, the bootstrap capacitor is charged from the power supply through an internal circuit. The gate of the high-side MOSFET is driven high from the voltage at the bootstrap supply, forcing the MOSFET gate to a voltage higher than the power supply voltage and allowing the MOSFET to fully turn on, reducing power loss in the amplifier.

The gain of the MPQ7790 is set by the input terminals, GAIN0 and GAIN1. The actual gain settings are controlled by ratios of the input and feedback resistors.

### Enable Function

The MPQ7790 EN input is an active high enable control. To enable the MPQ7790, drive EN with a voltage of 2.0V or higher. To disable the amplifier, drive it below 0.4V. While the MPQ7790 is disabled, the PVCC operating current is about 50μA and the output driver MOSFETs are turned off.

### Input Signal Absence Detect

The MPQ7790 includes an internal circuit that allows the system to automatically shut down after the absence of the audio signal. This feature is ideal for battery-operated applications.

The part also includes a delay circuit, which allows the IC to hold the flag after the absence of the audio signal. This hold time can be adjusted with an external capacitor.

The input absence flag is initially high when the device powers on. After the device is enabled, the internal circuit starts to detect the input signal. Then the MPQ7790 holds the output report and normal operation for a delay time, which can be adjusted by the capacitor value at pin CAP_D. The MPQ7790 turns off all the MOSFETs and pulls the input absence output low until the input signal is detected again (see Figure 2).

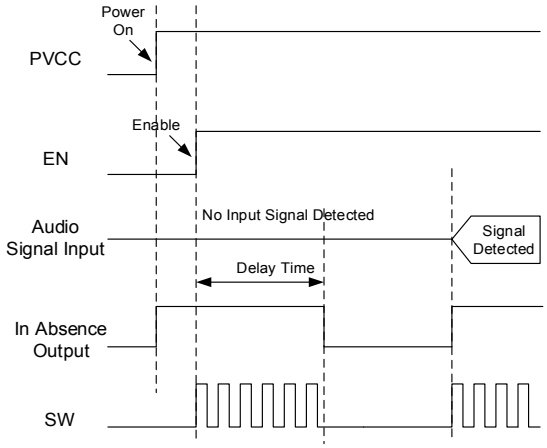



**Figure 2: Enable On with No Signal Detected**

The input absence flag output is high when an input signal is detected. The delay circuit is only activated if there is an input signal absence. The MPQ7790 then holds the output report for a delay time, which can be adjusted by the capacitor value at pin 14. Then the MPQ7790 turns off the all MOSFETs and pulls the input absence output low until the input signal is detected again.

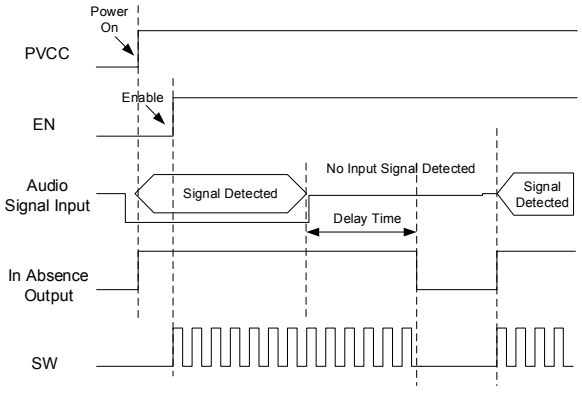



**Figure 3: Enable On with Audio Signal Present**


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### Adjustable Power Limit

The voltage at PLIMIT can be used to limit the power that is possible based on the supply rail. Connect a resistor divider from AVCC to GND to set the power limit. Connect directly to AVCC for no power limit.

An external reference may also be used if tighter tolerance is required. It is recommended to add a 1µF capacitor from PLIMIT to GND.

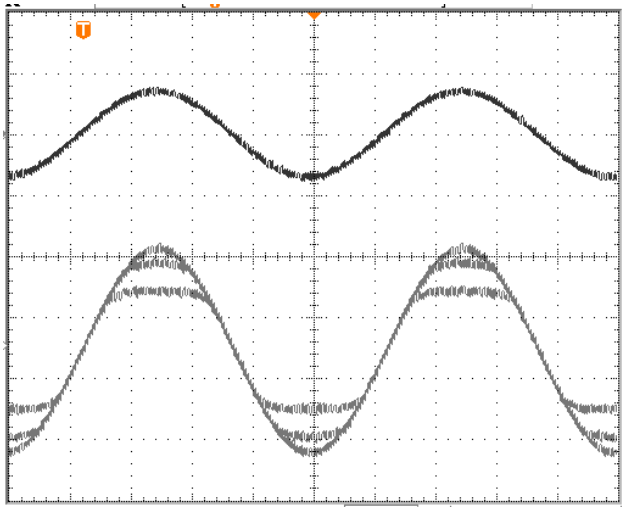


**Figure 4: PLIMIT Circuit Operation**

The PLIMIT circuit sets a limit on the output peak-to-peak voltage by limiting the duty cycle to a fixed maximum value (see Figure 4). This limit can be thought of as a “virtual” voltage rail, which is lower than the supply connected to PVCC. This “virtual” rail is 9 times the voltage at PLIMIT. This output voltage can be used to calculate the maximum output power for a given maximum input voltage and speaker impedance with Equation (1):

$$P_{OUT} = \frac{\left(\left(\frac{R_L}{R_L + 2 \times R_S}\right) \times V_P\right)^2}{2 \times R_L} \quad (1)$$

For unclipped power where $R_S$ is the total output series resistance (including $R_{DS(ON)}$ and the resistance of the output filter). $R_L$ is the load resistance. $V_P$ is the peak amplifier of the output voltage. $V_P \approx 9$ x PLIMIT voltage if 8 x PLIMIT < PVCC. $P_{OUT}@10\%THD \approx 1.25 \times unclipped\ P_{OUT}$.

Table 1 shows typical power limit operations.

**Table 1: Power Limit Typical Operation**

| Test Conditions | PLIMIT Voltage | Output Voltage (Vp-p) | Output Power (10% THD) |
|---|---|---|---|
| PVCC = 12V, $V_{IN}$ = 0.75Vrms, load = 8Ω, gain = 20dB | 0.93V | 18.5 | 5.0W |
| PVCC = 16V, $V_{IN}$ = 0.75Vrms, load = 8Ω, gain = 20dB | 0.93V | 18.5 | 5.0W |
| PVCC = 16V, $V_{IN}$ = 1Vrms, load = 8Ω, gain = 20dB | 1.40V | 26.0 | 10.0W |
| PVCC = 18V, $V_{IN}$ = 1Vrms, load = 8Ω, gain = 20dB | 1.40V | 26.0 | 10.0W |

### Gain Setting

The gain of the MPQ7790 is set by the input terminals, GAIN0 and GAIN1. The actual gain settings are controlled by ratios of the internal input and feedback resistors (see Table 2).

**Table 2: Gain Setting**

| GAIN0 | GAIN1 | Typ. Gain (dB) | Typ. Input Impedance (kΩ) |
|---|---|---|---|
| 0 | 0 | 20 | 75 |
| 1 | 0 | 26 | 50 |
| 0 | 1 | 32 | 30 |
| 1 | 1 | 36 | 20 |

### Over-Temperature Shutdown

Thermal monitoring is integrated into the MPQ7790. If the die temperature rises above 150°C, all switches turn off. The temperature must fall below 130°C before normal operation resumes, with the same power-up sequence used to prevent popping noise.

### Short-Circuit Performance

The MPQ7790 has internal overload and short-circuit protection. The currents in both the high-side and low-side MOSFETs are measured. Upon detection of a short circuit, all MOSFETs on the over-current full-bridge channel go into high impedance for a fixed duration before resuming normal operation. After the fixed


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duration and the short-circuit condition is removed, the MPQ7790 restarts with the normal start-up sequence to prevent a pop from occurring.

### Fault Output

The MPQ7790 includes an open-drain, active low fault indicator output on the /FAULT pin. A fault triggers if either the current limit or thermal shutdown is tripped.

A fault on any channel causes /FAULT to pull low, and causes all the outputs to go into high impedance. When the fault trigger is no longer present, the MPQ7790 resumes normal operation (see Figure 5).

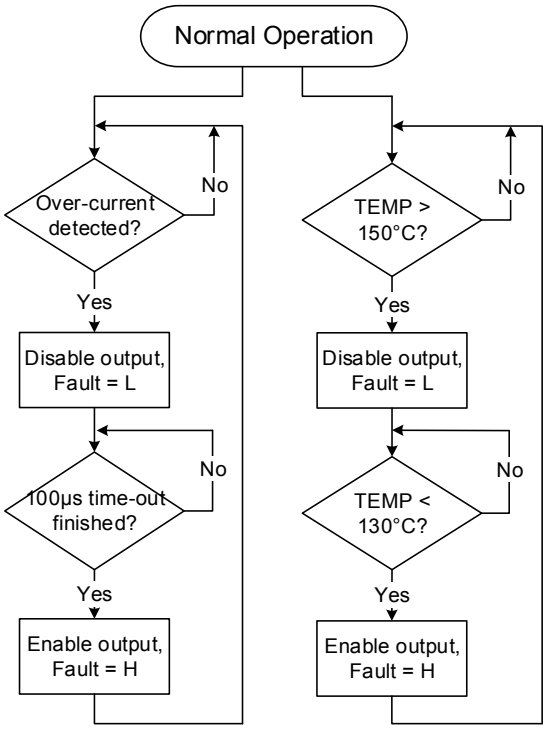



**Figure 5: Fault Timing Chart**


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# APPLICATION INFORMATION

## COMPONENT SELECTION

### Delay Time for Input Signal Absence Report

The recovery time is determined with Equation (2):

$$T_{delay} = 1.6 \times 10^8 \times C_R [sec] \quad (2)$$

### Choosing the Output EMI Filter

The magnetic bead-capacitor filter converts the pulses at SW to the output voltage that drives the speaker. Both the PVCC line and output current flow need magnetic beads to prevent large radiation from the high slew-rate pulse. The larger the impedance of the magnetic bead, the better the EMI performance achieved.

### Input Coupling Capacitor

The input coupling capacitor transmits the AC signal from the source to the MPQ7790 while blocking the DC voltage. Choose an input coupling capacitor with a corner frequency ($f_{IN}$) that is less than the passband frequency. The corner frequency is calculated with Equation (3):

$$f_{IN} = \frac{1}{2 \times \pi \times R_{IN} \times C_{IN}} \quad (3)$$

The impedance of the input resistor is different depending on the gain setting. At the same gain setting, the input impedance from part to part may shift by ±20% due to shifts in the actual resistance of the input resistors. However, the gain variation from part to part is small.

For design purposes, the input network should assume an input impedance of 16kΩ, which is the absolute minimum input impedance of the MPQ7790. At the lower gain settings, the input impedance could increase as high as 90kΩ.

### Power Source

For maximum output power, the amplifier circuit requires a regulated external power source. A high power-supply voltage can deliver more power to a given load resistance, but a power-source voltage exceeding the maximum voltage (18V) can damage the device. The MPQ7790's power supply rejection is excellent, though power-supply noise can pass to the output. Care must be taken to minimize power supply noise within the passband frequencies. Bypass the power supply with a large capacitor (typically aluminum electrolytic), along with two smaller 1μF and 1nF ceramic capacitors at the $V_{CC}$ supply pins.

### Output Short to Battery Protection

If the output shorts to a voltage bus that is higher than the PVCC, the body diode of the MOSFET turns on. Depending on the current, the power loss may generate a lot of heat. A reverse blocking diode or MOSFET is recommended in series with PVCC.

### Electromagnetic Interference (EMI) Considerations

Due to the switching nature of class D amplifiers, care must be taken to minimize EMI effects from the amplifier. Proper component selection and careful attention to circuit layout can minimize the effects of EMI due to amplifier switching.

Magnetic beads are used for blocking radiated emissions from SW nodes. For the best EMI performance, use high-current and high-impedance magnetic beads. The muRata NFZ2M series CLASS D EMI filter works well in series with PVCC and four SW outputs.

The size of high-current loops that carry rapidly changing currents must be minimized. Ensure that the $V_{CC}$ bypass capacitors are as close to the MPQ7790 as possible.

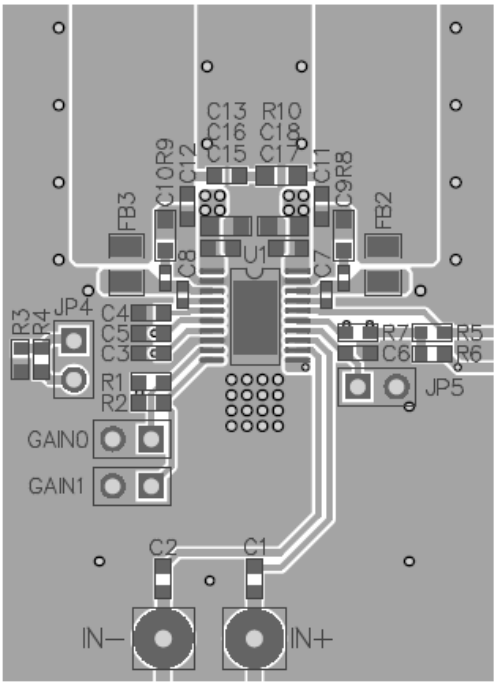
Nodes that carry rapidly changing voltage, such as SW, need to be made as small as possible. If sensitive traces run near a trace connected to SW, place a ground shield between the traces.


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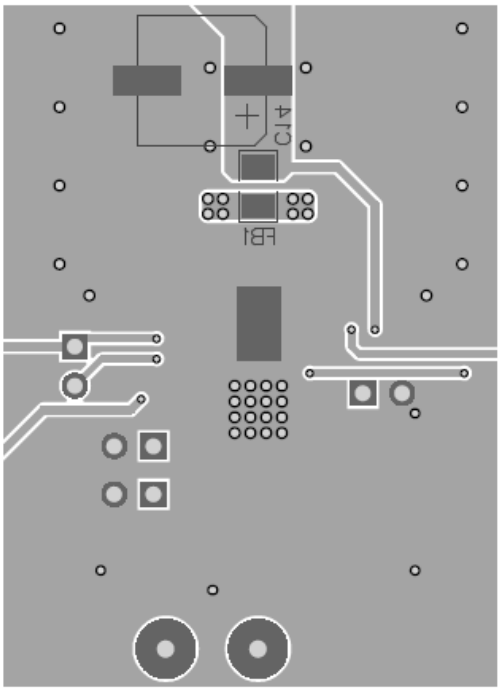
## PCB Layout [8]

Efficient PCB layout is critical for optimal performance, including low output distortion and noise. For best results, refer to Figure 6 and follow the guidelines below:

1. Place the following components as close to the MPQ7790 as possible:
   a. Bootstrap Capacitors: $C_{BS}$ supplies the gate drive current to the internal HS-FET. Place $C_{BS}$ as close to BST and SW as possible.
   b. Power Supply Bypass Capacitors: $C_{BYP}$ carries the transient current for the switching power stage. To avoid overstressing the MPQ7790 and creating excessive output noise, place $C_{BYP}$ as close to the PVCC pins as possible.
2. Keep the filter capacitor close to the magnetic bead. The magnetic bead-capacitor filter converts the pulse train at SW to the output voltage that drives the speaker.
3. Ensure that any traces carrying the SW voltages are routed far from any input signal traces. If the trace must run near the SW trace near the input, shield the input with a ground plane between the traces.
4. Physically separate each channel to prevent crosstalk.
5. Route each power supply from the source to each channel individually, not serially. This prevents channel-to-channel coupling through the power supply input.




**Top Layer**




**Bottom Layer**

**Figure 6: Recommended PCB Layout**

**NOTE:**

8) The recommended PCB layout is based on Figure 7.


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# TYPICAL SYSTEM CIRCUITS FOR AUTOMOTIVE APPLICATION

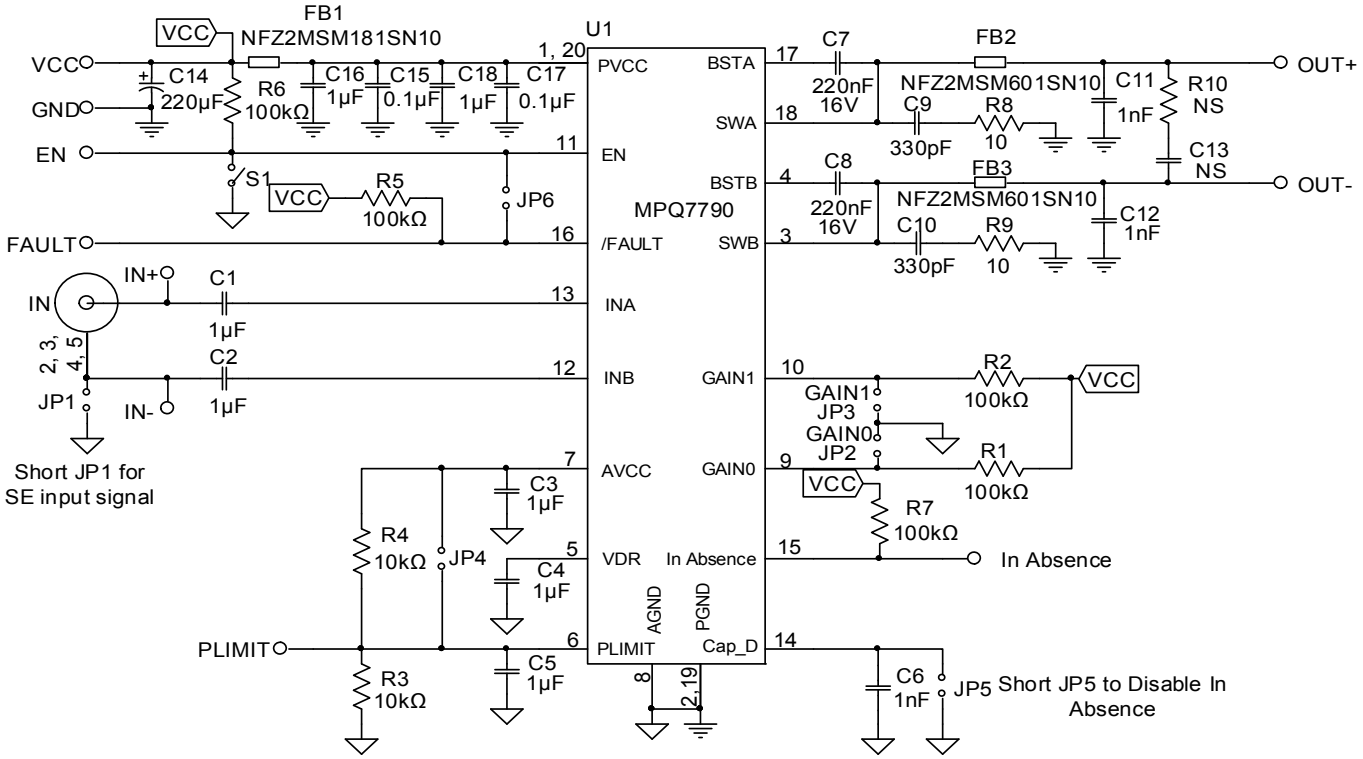
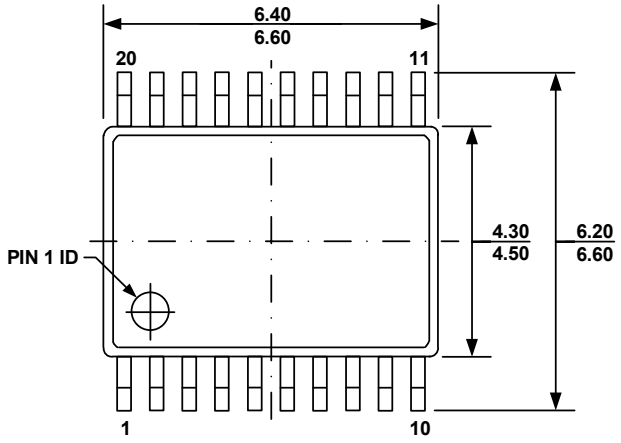



**Figure 7: Typical Application Circuit**

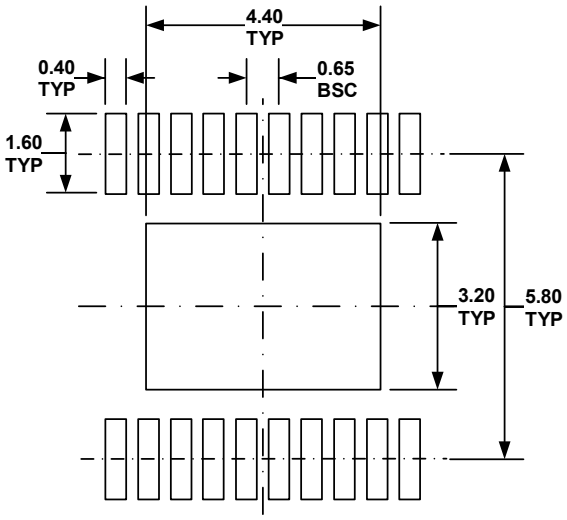

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# PACKAGE INFORMATION

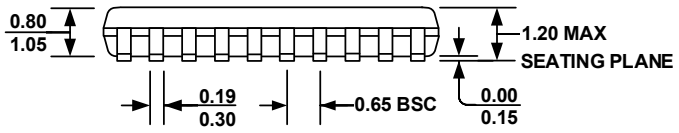
## TSSOP20-EP



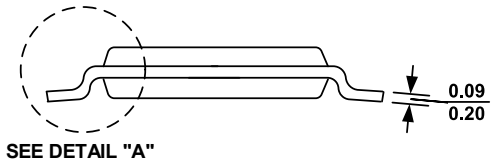

TOP VIEW



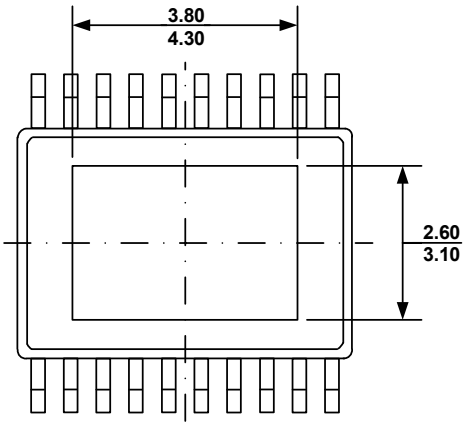

RECOMMENDED LAND PATTERN



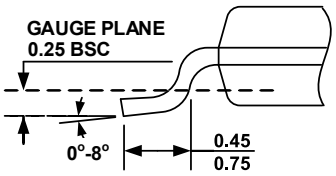

FRONT VIEW




SIDE VIEW




BOTTOM VIEW




DETAIL "A"

**NOTE:**

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2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION, OR GATE BURR.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
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