MPQ8039

High Current Power Half Bridge

AEC-Q100 Qualified

The Future of Analog IC Technology

DESCRIPTION

The MPQ8039 is a general purpose, high frequency half bridge power driver capable of driving a 9A load. The device integrates both top and bottom N-Channel MOSFET power switches and is fully protected from both sourcing and sinking current by a preset cycle-by-cycle current limit. It has a wide input voltage range from 7.5V to 25V.

The MPQ8039 features a low-current shutdown mode, input under-voltage protection, thermal shutdown. It interfaces with standard logic signals and is available in a small SOIC8E package.

FEATURES

- Guaranteed Industrial/Automotive Temp. Range Limits
- ±9A Peak Current Output
- ±4.25A Continuous Current Output
- Up to 1.2MHz Switching Frequency
- Protected Integrated Power 100mΩ Switches
- All Switches Current Limited
- Integrated Under-Voltage Protection
- Integrated Thermal Protection
- 2.5μA Standby Mode
- True 2-Quadrant Operation
- Sources and Sinks Current
- Available in AEC-Q100 Qualified Grade

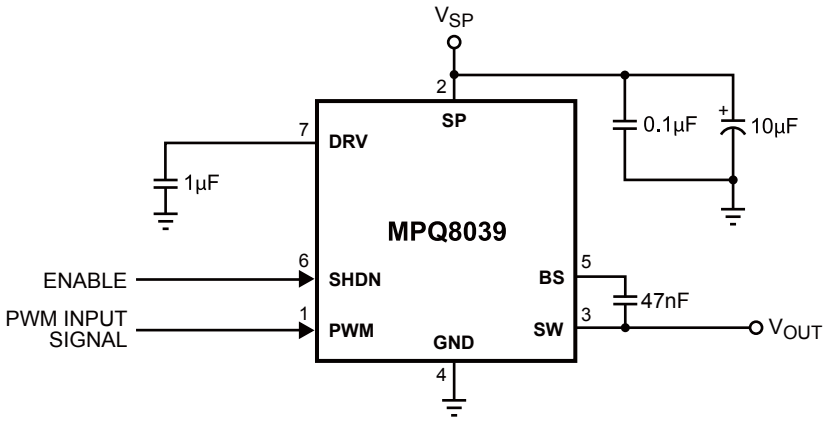
APPLICATIONS

- Class D Audio Driver
  - o 25W/4Ω/10% Output Power Single Ended
  - o 70W/4Ω/10% Output Power Full Bridge
- Full or Half Bridge DC-DC Switching Regulator
- Motor Driver

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TYPICAL APPLICATION



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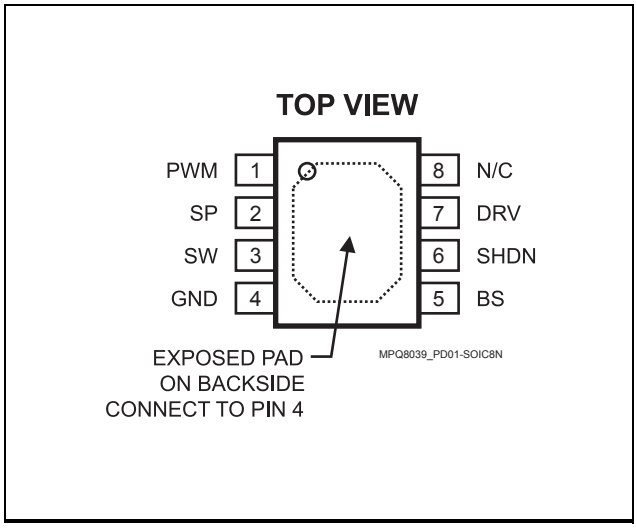
ORDERING INFORMATION

Part Number	Package	Top Marking
MPQ8039GN*	SOIC8E	MP8039
MPQ8039GN-AEC1**	SOIC8E	MP8039

* For Tape & Reel, add suffix –Z (eg. MPQ8039GN–Z)

** For Tape & Reel, add suffix –Z (eg. MPQ8039GN-AEC1–Z)

PACKAGE REFERENCE



ABSOLUTE MAXIMUM RATINGS (1)

SP Supply Voltage (V_{SP}) ..... -0.3V to +28V(5)
SW Pin Voltage ..... –0.3V to V_{SP}
SW to BS ..... –0.3V to +6V
Voltage at All Other Pins ..... –0.3V to +6V
Continuous Power Dissipation (T_A = +25°C) (2) 2.5W
Storage Temperature ..... –55°C to +150°C

Recommended Operating Conditions (3)

SP Supply Voltage (V_{SP}) ..... 7.5V to 24V
Peak Output Current ..... 9A Maximum
Operating Junction Temp. (T_J). -40°C to +125°C

Thermal Resistance (4)

	θ_{JA}	θ_{JC}
SOIC8E	48	10 ... °C/W

Notes:
1) Absolute maximum ratings are rated under room temperature unless otherwise noted. Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature TJ (MAX), the junction-to-ambient thermal resistance θJA, and the ambient temperature TA. The maximum allowable continuous power dissipation at any ambient temperature is calculated by PD (MAX) = (TJ (MAX)-TA)/θJA. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the device will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on approximately 1" square of 1 oz copper.
5) For room temperature only.

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ELECTRICAL CHARACTERISTICS

V_{SP} = 12V, V_{SHDN} = 0V, T_J = -40°C to +125°C, Typical value are T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
SP Operating Current				1.5	2.5	mA
SP Shutdown Current		V_{SHDN} = 2V		2.5	10	µA
SHDN, SP Threshold Low					1	V
SHDN, SP Threshold High			2			V
SHDN, SP Input Bias Current				1		µA
SW On Resistance		V_{SP} = 7.5V, High-Side and Low-Side		0.1	0.25	Ω
SW Current Limit (5)		V_{PWM} = 5, (Sinking)		9		A
		V_{PWM} = 0, (Sourcing)		9		A
SW Switching Frequency		V_{PWM} = 0 to 2V, 50% Duty Cycle			1.2	MHz
SW Maximum Duty Cycle (6)		V_{SP} = 7.5V, V_{PWM} = 2V, C_{SW} 100nF, f_{SW} = 3.3kHz		99.5		%
SW Rise/Fall Time		V_{PWM} = 0 to 5V		20		ns
PWM Pulse Width		V_{PWM} = 0 to 2V, High or Low Pulse	200			ns
PWM to SW Delay Time Rising		V_{PWM} = 0 to 5V		70		ns
PWM to SW Delay Time Falling		V_{PWM} = 5 to 0V		70		ns
Thermal Shutdown Temperature (5)		T_J Rising, Hysteresis = 20°C		160		°C
IN UVLO		Rising Edge	5.5		7.5	V
DRV Voltage	V_{DRV}	V_{SP}=10V	5.1	5.6	6.0	V
PWM Threshold Voltage		V_{PWM} Rising			2.4	V
		V_{PWM} Falling	1.3			V

Notes:

6) Not production tested.

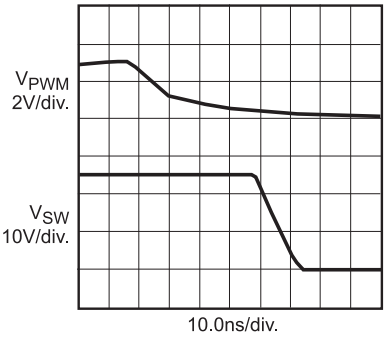
7) SW drives low for 1.5µs every 300µs to charge the BS to SW capacitor.

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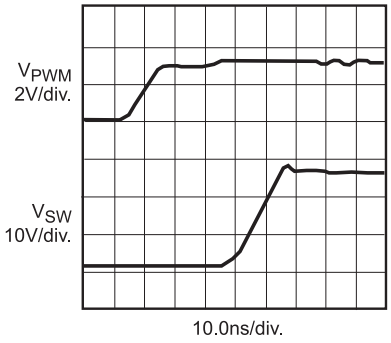
TYPICAL PERFORMANCE CHARACTERISTICS

Circuit of Figure 4, T_A = +25°C, unless otherwise noted.

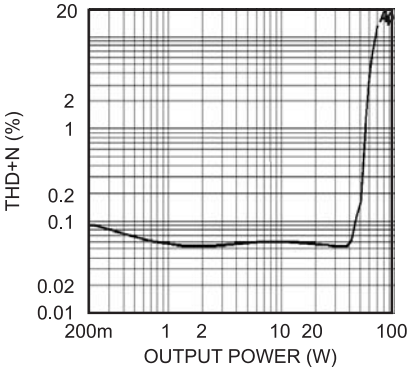
Delay Time
SW Falling (V_{SP}=25V)



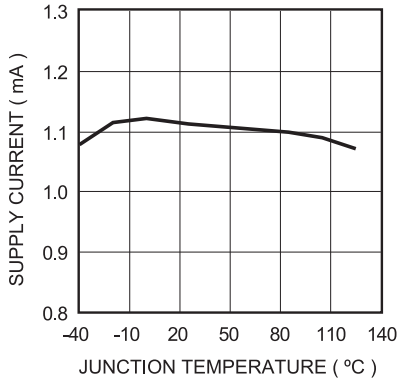
Delay Time
SW Rising (V_{SP}=25V)



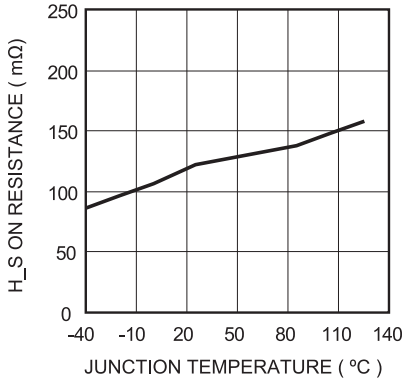
THD+N vs Output Power
(V_{SP}=24V) Bridged Output into 4Ω
(Class D Application using closed loop circuit)



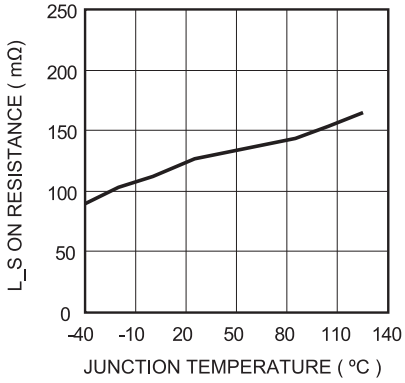
Supply Current vs. T_J



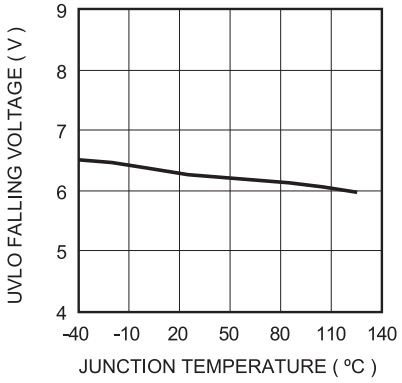
H_S R_{DS_ON} vs. T_J



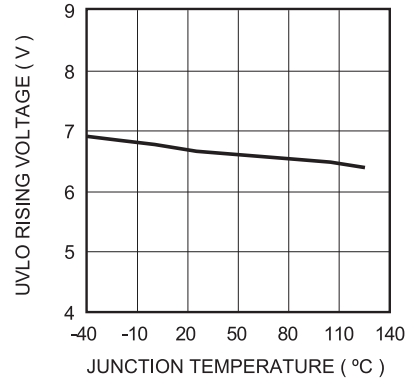
L_S R_{DS_ON} vs. T_J



UVLO Falling Voltage vs. T_J



UVLO Rising Voltage vs. T_J

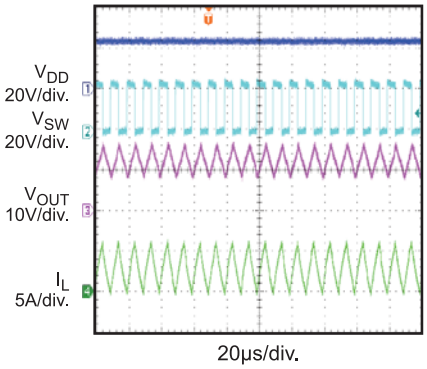


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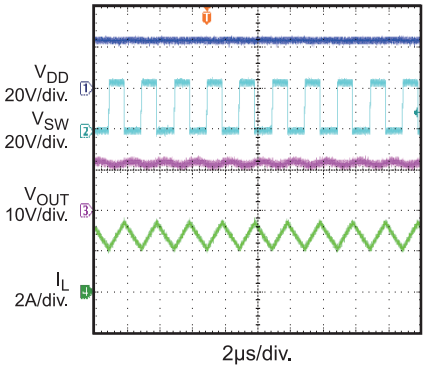
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN}=24V, R_{LOAD}=4Ω, L=10uH, F_{IN}=0.5MHz, T_A=25ºC, Unless otherwise noted.

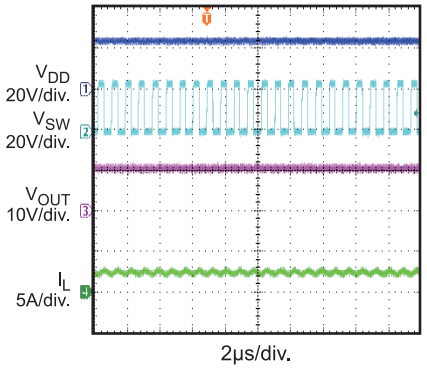
Steady State
F_{IN}= 0.1MHz



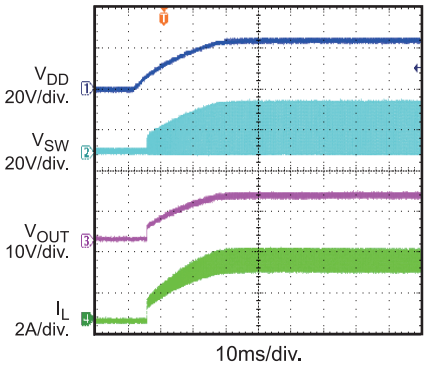
Steady State



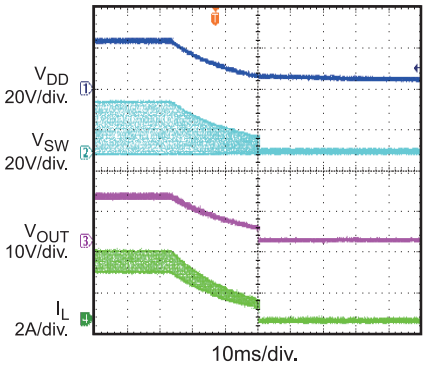
Steady State
F_{IN}= 1.2MHz



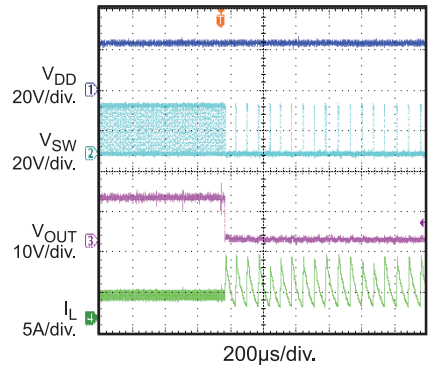
Power Ramp Up



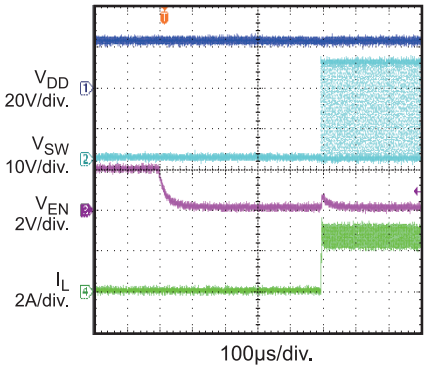
Power Ramp Down



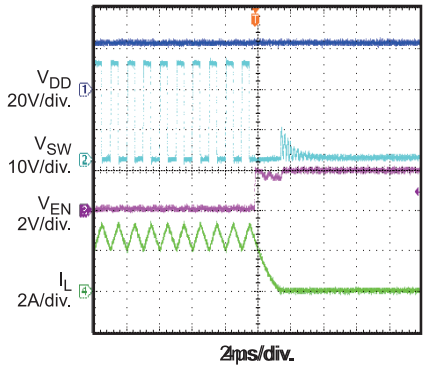
Short Output Protection



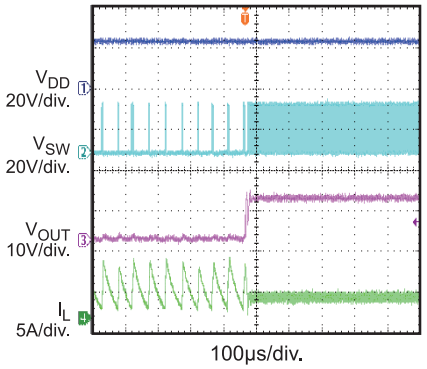
Enable On



Enable Off



Short Output Recovery



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PIN FUNCTIONS

Pin #	Name	Description
1	PWM	Driver Logic Input. Drive PWM with the signal that controls the MPQ8039 output. Drive PWM high to turn on the high-side switch; drive PWM low to turn on the low-side switch.
2	SP	Power Supply Input. Connect SP to the positive side of the input power supply. Bypass SP to GND as close to the IC as possible.
3	SW	Switched Output. SW is the power output of the MPQ8039. Connect the output LC filter to SW. SW is valid approximately 100μs after SP goes high.
4	GND	Ground. (Note: Connect the exposed pad on the bottom side to Pin 4).
5	BS	Bootstrap Supply. BS powers the high-side gate of the MPQ8039. Connect a 0.1μF or greater capacitor between BS and SW.
6	SHDN	Shutdown Input. SHDN enables/disables the MPQ8039. Drive SHDN low to turn on the MPQ8039, drive it high to turn it off. If not used, connect SHDN to GND.
7	DRV	Gate Drive Supply Bypass. The voltage at DRV is supplied from an internal regulator from SP. DRV powers the internal circuitry and internal MOSFET gate drives. Bypass DRV to GND with a 0.1μF to 10μF capacitor.
8	N/C	

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OPERATION

The MPQ8039 is a general purpose, power driver. It takes a logic input and drives a half bridge comprised of 0.1Ω high-side and low-side N-Channel MOSFET switches.

It operates at frequencies up to 1.2MHz, can accept a DC supply voltage as high as 25V, and produce peak output current as high as 9A.

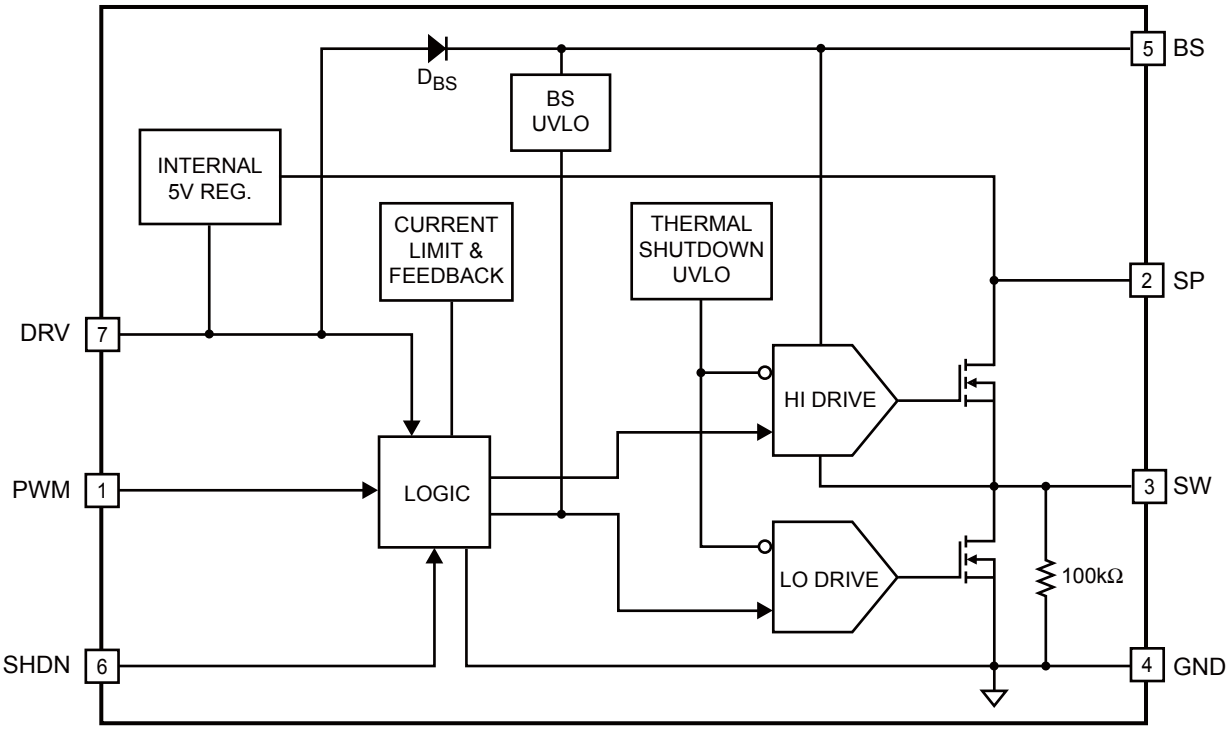


Figure 1: Function Block Diagram

SW Output

The SW output drives the load. It is controlled by the logic input signal at PWM. When the signal at PWM is high (above 2V), the high-side switch is turned on. When the signal at PWM is low (less than 0.4V), the low-side switch is turned on.

The MPQ8039 uses internal N-Channel MOSFETs for both the high-side and low-side switches. The high-side MOSFET gate drive is powered from the voltage between SW and BS, allowing BS to rise above the SP input voltage to power the high-side MOSFET. To do this a bootstrap capacitor is connected between SW and BS. When the low-side switch is on, the capacitor is internally charged from the voltage at DRV, which is also internally generated. There is a dead time region (typically 40ns) where both the upper and lower switches are off (see Figure 2).

Both the high-side and low-side switches have internal current limits to prevent failure due to excessive load current. Once the current limit is reached, both output switches are turned off and the fault output is asserted (driven low).

Shutdown

The MPQ8039 includes a 2.5μA shutdown mode. When SHDN is high, both output switches are turned off and the input current drops to 2.5μA. When the MPQ8039 is shutdown, the internally generated voltage at DRV drops to 0V. If the shutdown mode is not used, connect SHDN directly to GND.

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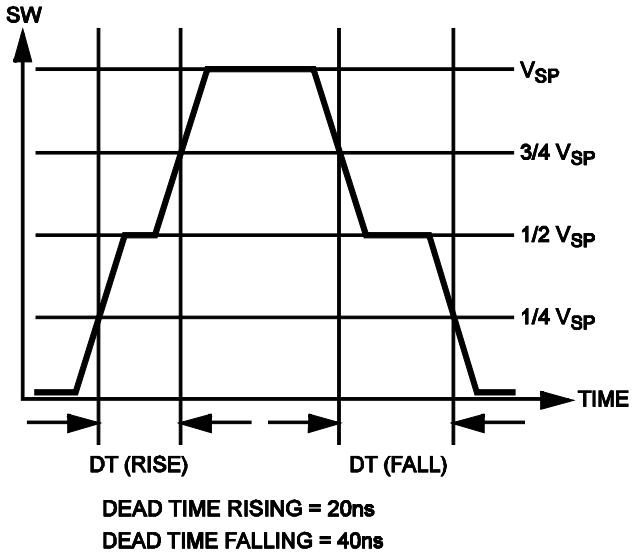


Figure 2: Dead Time

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TYPICAL APPLICATION CIRCUITS

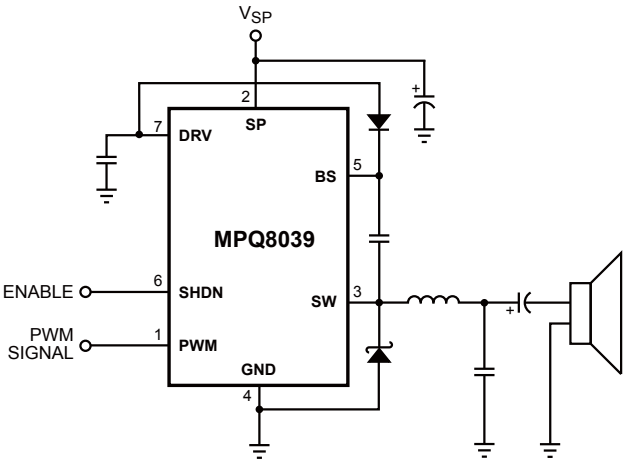


Figure 3: Single Ended Audio Amplifier

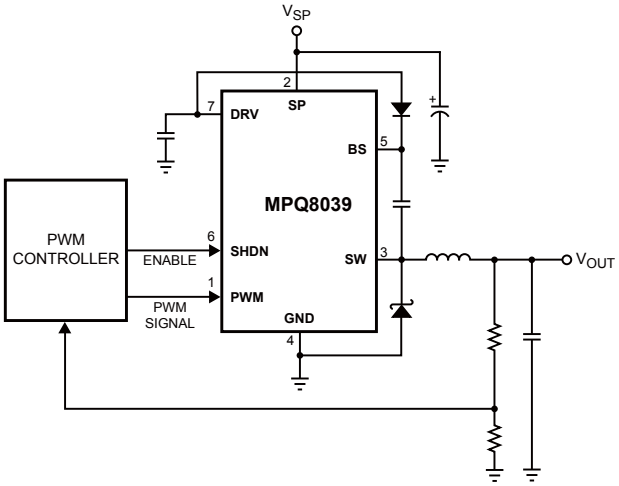


Figure 4: General Purpose DC to DC Converter

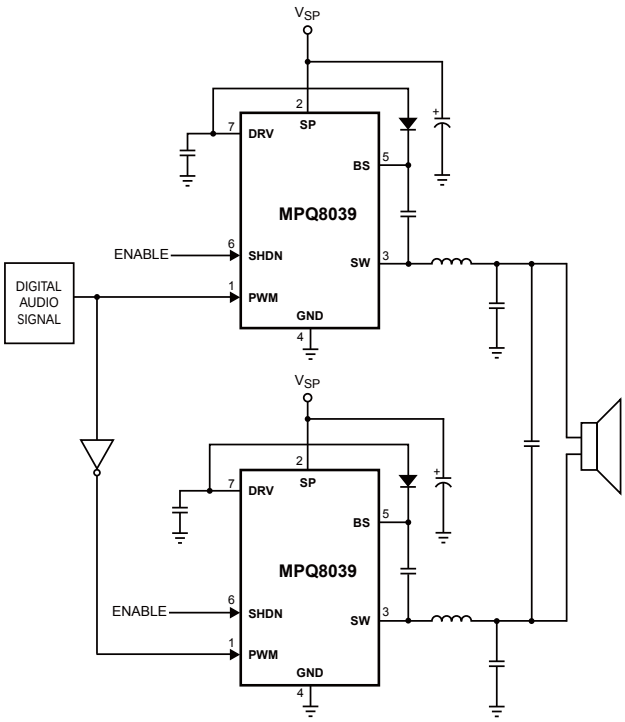


Figure 5: 80W Full Bridge Audio Amplifier

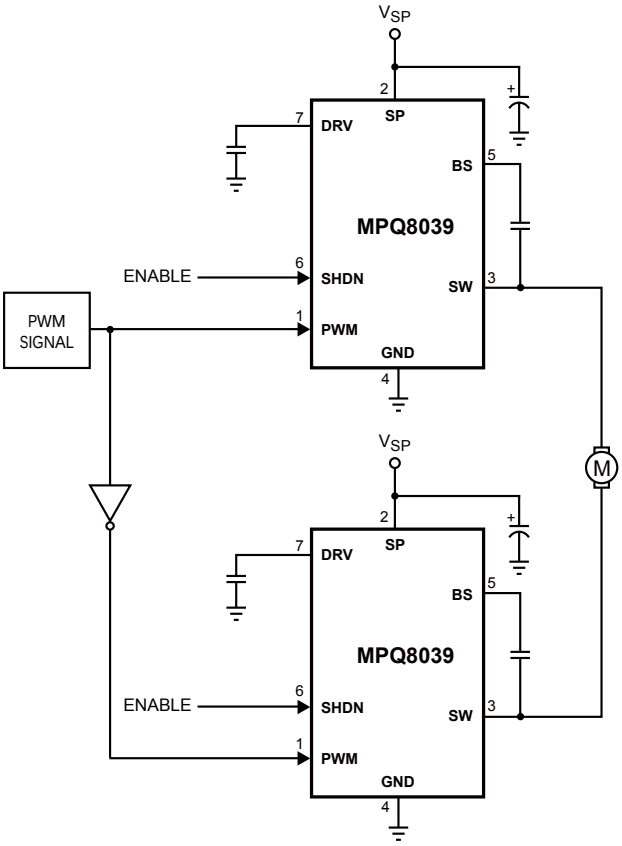


Figure 6: Full Bridge Motor Driver

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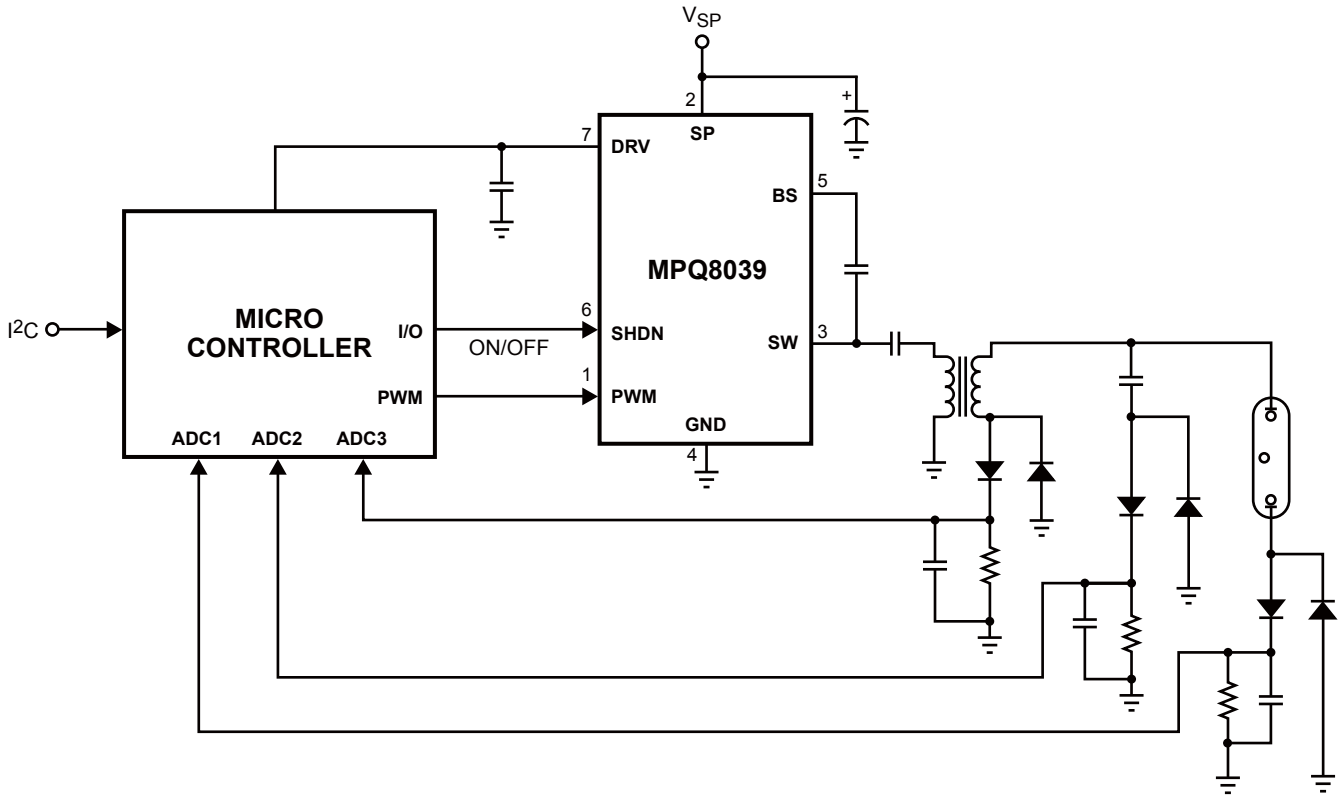
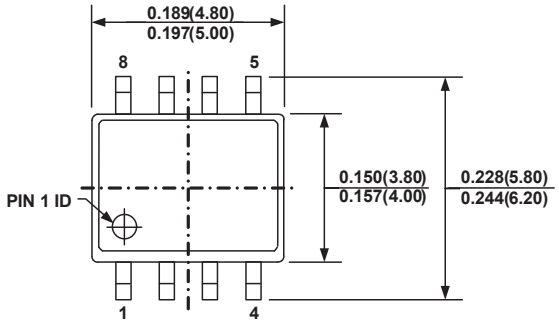


Figure 7: CCFL Driver Circuit

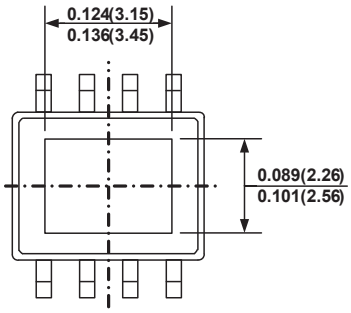
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PACKAGE INFORMATION

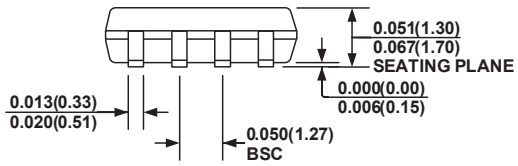
SOIC8N (EXPOSED PAD)



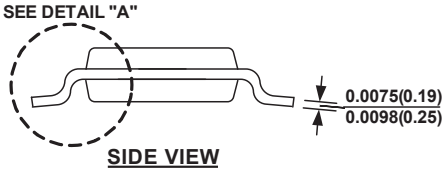
TOP VIEW



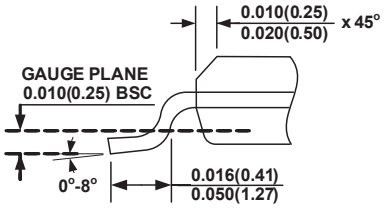
BOTTOM VIEW



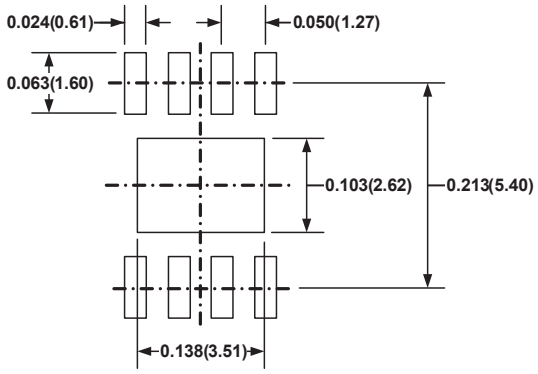
FRONT VIEW



SIDE VIEW



DETAIL "A"



RECOMMENDED LAND PATTERN

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