Features

- Integrated Single Chip Receiver (Rx) Solution
  - Integrated Full-Bridge Synchronous Rectifier
  - Integrated 5.3V, 1A LDO Regulator Output
- WPC-1.1.2 compliant
- Advanced WPC v1.1.2 Foreign Object Detection (FOD)
- Programmable FOD setting via external resistor
- Closed-loop power transfer control between Tx and Rx
- Support I^2C interface with access to:
  - Rectifier voltage
  - Output current
  - Resonance frequency
- Open-Drain LED Indicator Output
- Over-Temperature/Voltage/Current Protection
- 0° to +85°C temperature range
- 5 x 5 mm 32-VFQFPN package

Applications

- PC peripherals
- Rugged electronic gear
- Small appliances
- Battery-powered electronics

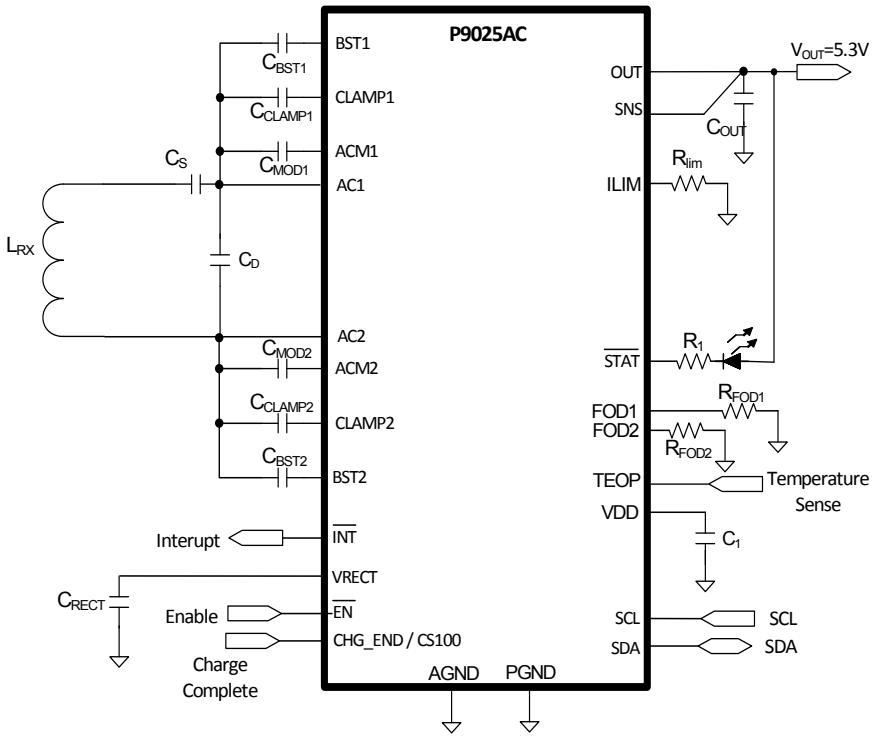
Introduction

The P9025AC is an integrated single-chip, WPC-1.1.2 compliant wireless power receiver with an advanced Foreign Object Detection (FOD) feature. This device operates with an AC power signal from a resonant tank and converts it into a regulated 5.3V output voltage. The receiver includes a high efficiency Synchronous Full Bridge Rectifier and 5.3V tracking LDO output stage. The P9025AC automatically detects the transmitter's presence and initiates WPC AC modulation communication protocols with optimal efficiency.

The device includes the control circuit required to modulate the load to transmit WPC-compliant message packets to the base station. It uses minimal external components to reduce overall solution area and costs.

The P9025AC employs advanced programmable WPC FOD techniques to detect foreign metallic objects placed on the transmitter base station derived from a transmitted and received power transfer algorithm.

Typical Application Circuit



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Absolute Maximum Ratings

Stresses above the ratings listed below (Table 1 and Table 2) can cause permanent damage to the P9025AC. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Table 1: Absolute Maximum Ratings Summary

Pins	Rating	Units
AC1, AC2, VRECT, ACM1, ACM2, CLAMP1, CLAMP2 to PGND_	-0.3 to 20	V
BST1, BST2 to PGND1	-0.3 to (AC1, AC2 + 6)	V
$\overline{INT}$, $\overline{EN}$, $\overline{STAT}$, SCL, SDA, OUT, SNS, TEOP, RLIM, CHG_END/CS100, FOD1, FOD2, VDD to AGND	-0.3 to 6	V
PGND, PGND1, PGND2, to AGND	-0.3 to 0.3	V
Out Current	1.5	A
AC1, AC2 Current	2	A_{RMS}

Table 2: Package Thermal Information[1,2,3,4]

Symbol	Description	Rating (VFQFPN)	Units
Θ_{JA}	Thermal Resistance Junction to Ambient	35	°C/W
Θ_{JC}	Thermal Resistance Junction to Case	29.6	°C/W
Θ_{JB}	Thermal Resistance Junction to Board	2.4	°C/W
T_J	Operating Junction Temperature	0 to +125	°C
T_A	Ambient Operating Temperature	0 to +85	°C
T_{STG}	Storage Temperature	-55 to +150	°C
T_{LEAD}	Lead Temperature (soldering, 10s)	300	°C

NOTES:

1. The maximum power dissipation is $P_{D(MAX)} = (T_{J(MAX)} - T_A) / \Theta_{JA}$ where $T_{J(MAX)}$ is 125°C. Exceeding the maximum allowable power dissipation will result in excessive die temperature, and the device will enter thermal shutdown.
2. This thermal rating was calculated on JEDEC 51 standard 4-layer board with dimensions 3" x 4.5" in still air conditions.
3. Actual thermal resistance is affected by PCB size, solder joint quality, layer count, copper thickness, air flow, altitude, and other unlisted variables.
4. For the NBG32 package, connecting the 5 mm X 5 mm EP to internal/external ground planes with a 5x5 matrix of PCB plated-through-hole (PTH) vias, from top to bottom sides of the PCB, is recommended for improving the overall thermal performance.

Table 3: ESD Information

Test Model	Pins	Ratings	Units
HBM	All pins	±1500	V
CDM	All pins	±500	V

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Electrical Specifications Table

Table 4: Device Characteristics

V_{RECT} = 6V, C_{OUT} = 1µF, C_{VRECT} = 20µF, $V_{\overline{EN}}$ = GND, T_A = 0 to +85°C, unless otherwise noted. Typical values are at 25°C.

Symbol	Description	Conditions	Min	Typ	Max	Units
V_{RECT} Under-Voltage Lock-out						
V_{UVLO}	Under-voltage Lockout	Rising voltage on V_{RECT}	2.3	2.5	2.7	V
$V_{UVLO-HYS}$	UVLO Hysteresis			50		mV
V_{RECT} Over-Voltage Protection						
V_{OVP}	Over-Voltage V_{RECT}	Rising voltage on V_{RECT}		13.3		V
$V_{OVP-HYS}$	Over-Voltage Hysteresis			1.5		V
Power Supply Current						
I_{RECT}	Quiescent Current	I_{OUT} = 0mA, with internal load	14	16	18	mA
		I_{OUT} = 0mA, no internal load	2	3	4	mA
Low-drop-out Regulator						
I_{LIM}	Output Current Limit	R_{LIM} = 30kΩ	1.15	1.6	1.95	A
		R_{LIM} < 25KΩ[1]			2.0	
V_{OUT}	Regulated Output Voltage	I_{OUT} = 0mA to 1000mA	5.04	5.3	5.56	V
V_{DD} Voltage (For Internal Supply Use Only)						
V_{DD_INT}	Internal Supply Voltage	I_{VDD} = 100µA, maximum allowable load for test purposes	4.44	4.54	4.64	V
Thermal Shutdown						
T_{SHD}	Thermal Shutdown Threshold	Temperature rising		150		°C
		Temperature falling		130		°C
Digital Input and Output Characteristics						
V_{IL}	Logic Level Input Low	$\overline{EN}$, TEOP			0.4	V
V_{IH}	Logic level Input High	$\overline{EN}$, TEOP	1.3			V
V_{OL}	Open Drain; $\overline{STAT}$, $\overline{INT}$	I_{STAT} = 4mA			400	mV
R_{PD}	Pull-down Resistance	EN		200		kΩ
		TEOP		1000		
Switch On-resistance						
R_{DSON}	ACM1, ACM2 Switches	150mA		2500		mΩ
	CLAMP1, CLAMP2 Switches			600		mΩ
	Rectifier Bridge Switches			250		mΩ
SCL, SDA (I^2C Interface)						
f_{SCL}	Clock Frequency		0		400	kHz
t_{LOW}	Clock Low Period		1.3			µs
t_{HIGH}	Clock High Period		0.6			µs
$t_{HD,STA}$	Hold Time (Repeated) for START Condition		0.6			µs

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Symbol	Description	Conditions	Min	Typ	Max	Units
$t_{SU:STA}$	Set-up Time for Repeated START Condition		0.6			µs
$t_{SU:DAT}$	Data Setup Time		100			ns
$t_{HD:DAT}$	Data Hold Time				0.9	µs
$t_{SU:STO}$	Setup Time for STOP		0.6			µs
t_{BUF}	Bus Free Time between STOP & START		1.3			µs
t_R	Rise Time of both SDA and SCL Signals (Note 1,2)		20 + 0.1 C_B		300	ns
t_F	Fall Time of both SDA and SCL Signals[1,2]		20 + 0.1 C_B		300	ns
T_{SP}	Spike Pulse Widths Suppressed by Input Filter[1,2]		0		50	ns
C_B	Capacitive Load for each Bus Line[1,2]				400	pF
C_{BIN}	SCL, SDA Input Capacitance[1,2]				60	pF
V_{IL}	Input Threshold Low				0.4	V
V_{IH}	Input Threshold High		1.4			V
I_I	Input Leakage Current		-1.0		1.0	µA

NOTES:

1. Guaranteed by design and not subject to 100% production testing.
2. Guaranteed by design and simulation.

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Typical Performance Characteristics

Figure 1. System Efficiency vs. Load Current

V_{IN} = 5V, V_{OUT} = 5.3V, Spacer = 3.7mm, Cs = 247nF, T_A = 25°C
Measured using the P9025AC-R-EVK V1.0 (receiver) and P9038-R-EVK V1.0 (transmitter) reference boards.

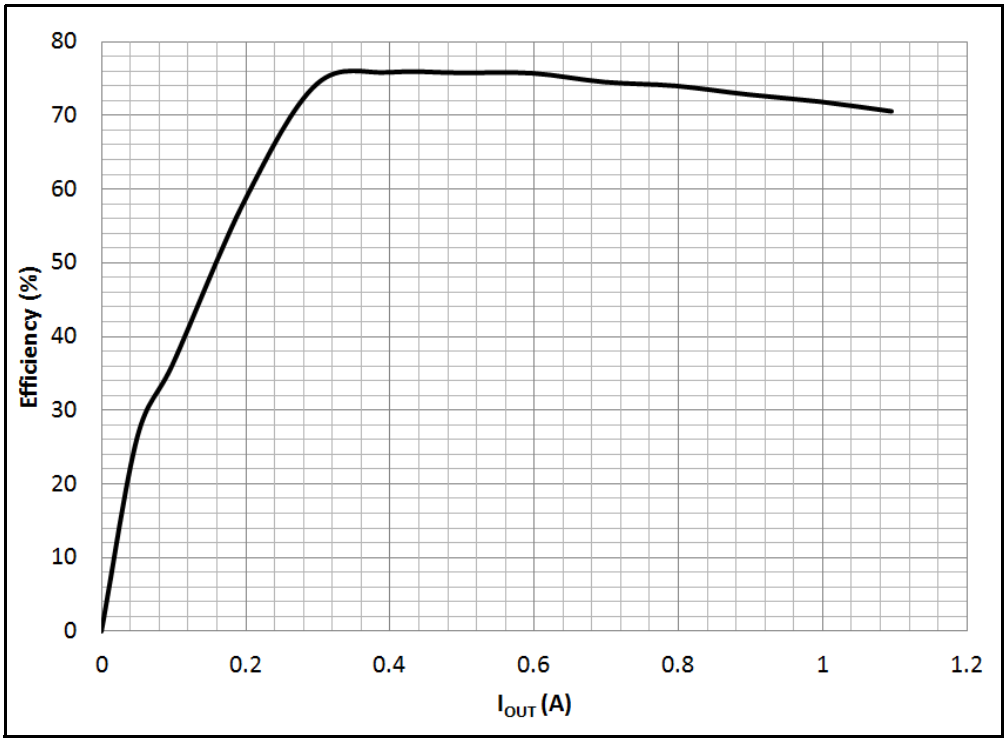
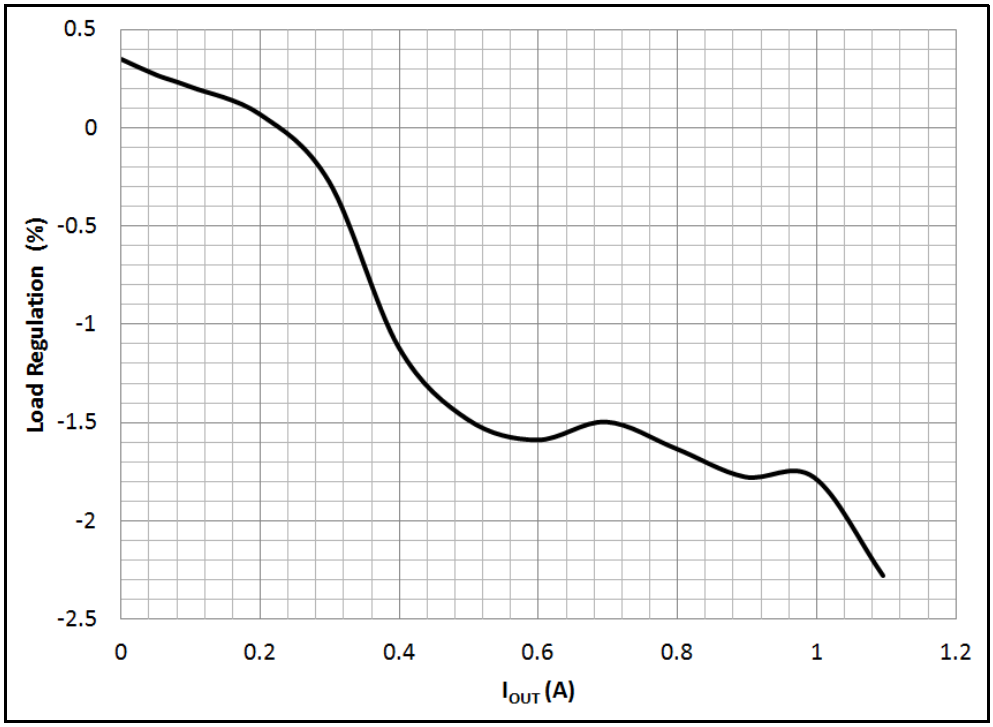


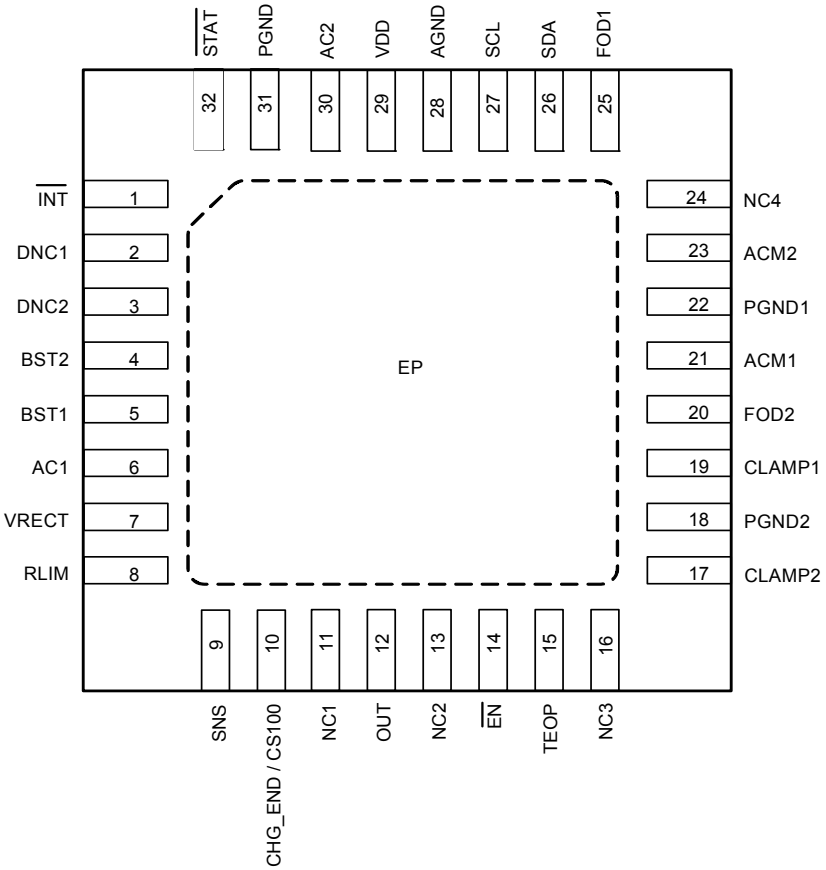
Figure 2. Load Regulation vs. Load Current

V_{IN} = 5V, V_{OUT} = 5.3V, Spacer = 3.7mm, Cs = 247nF, T_A = 25°C
Measured using the P9025AC-R-EVK V1.0 (receiver) and P9038-R-EVK V1.0 (transmitter) reference boards.



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Pin Configuration



Pin Descriptions

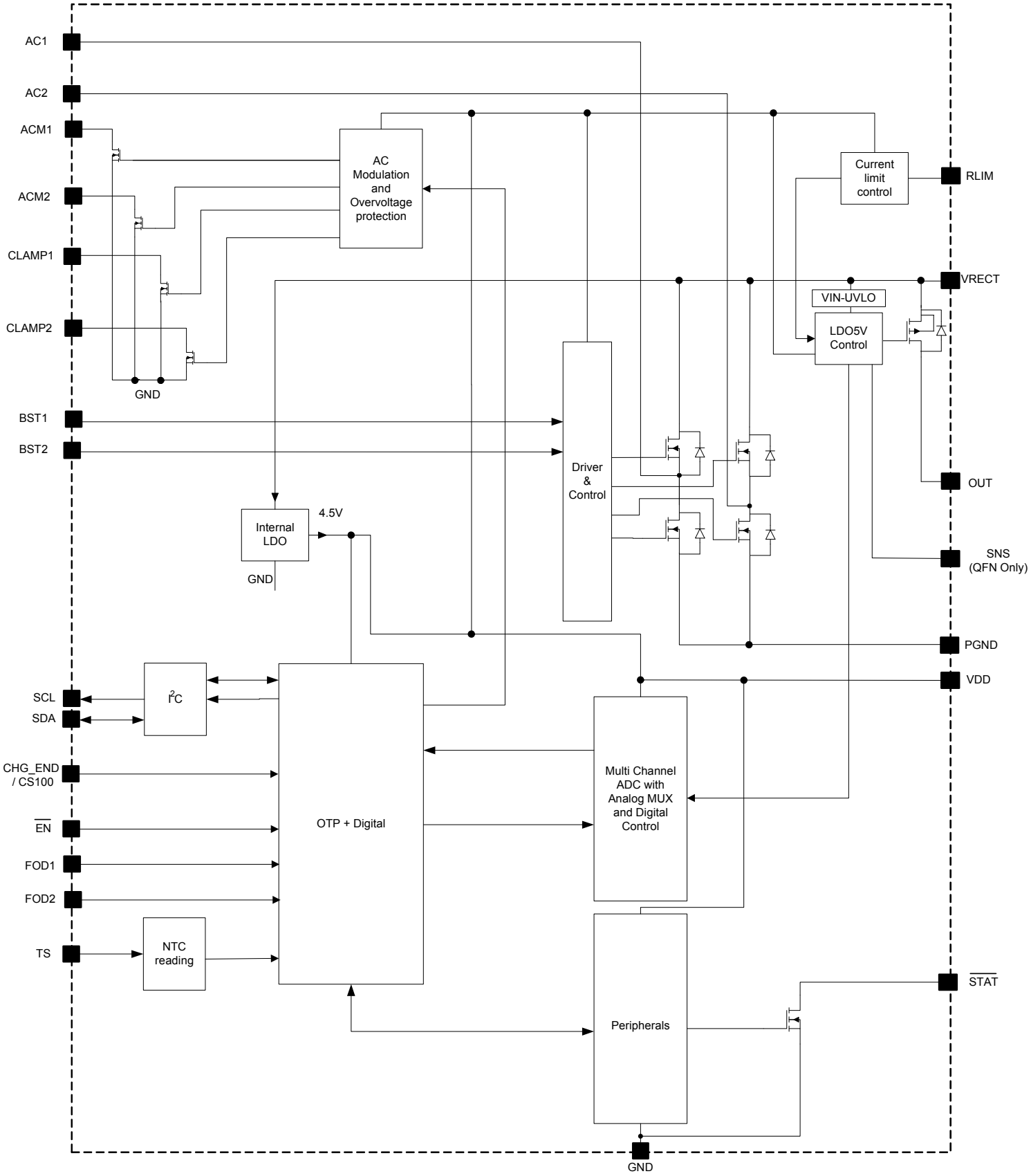
Pin #	Name	Type	Function
1	$\overline{INT}$	O	Interrupt output. Open drain output pin. A low state indicates that an over-current, over-voltage, or over-temperature condition has occurred. If used, connect a 100KΩ pullup resistor to the OUT pin or compatible system I/O voltage rail.
2	DNC1	DNC	DO NOT connect. It is internally connected. This pin must be left floating.
3	DNC2	DNC	DO NOT connect. It is internally connected. This pin must be left floating.
4	BST2	O	Bootstrap output for high-side rectifier FET 2. Connect a 0.01µF capacitor from AC2 pin to BST2.
5	BST1	O	Bootstrap output for high-side rectifier FET 1. Connect a 0.01µF capacitor from AC1 pin to BST1.
6	AC1	I	AC1 input to the Internal full-wave rectifier.
7	VRECT	O	Output of the full-wave rectifier. Bypass this pin with ceramic capacitors to power ground.
8	RLIM	I	Current-limit resistor. A resistor connected between this pin and ground sets the current limit of the 5V LDO output.
9	SNS	I	LDO output sense pin. Connect to the OUT pin.
10	CHG_END / CS100	I	Active-high input pin. Default setting is a Charge-End active-high input from an external battery charger to terminate power transfer. Alternatively, a Charge-Status active high input which will send a WPC Charge Status packet with value 100 (100% charge). This pin has an internal pull down resistor.

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Pin #	Name	Type	Function
11	NC1	NC	Not internally connected. This pin may be connected to others to facilitate routing or to improve thermal performance.
12	OUT	O	Regulated 5.3V output voltage. Connect a 1µF in parallel with 4.7 µF capacitor between the pin and ground.
13	NC2	NC	Not internally connected. This pin may be connected to others to facilitate routing or to improve thermal performance.
14	$\overline{EN}$	I	Active-low enable pin. The chip is suspended and placed in low-current (sleep) mode when this pin is pulled high. This pin has internal pulldown resistor to Analog Ground (AGND).
15	TEOP	I	Active-high over-temperature input pin. When pulled high, the chip will disable the LDO output and send a WPC End-of-Power packet with code 0x03 (over-temperature code). This pin has an internal pull down resistor to ground.
16	NC3	NC	Not internally connected. This pin may be connected to others to facilitate routing or to improve thermal performance.
17	CLAMP2	I	AC clamp input 2. Connect a 0.47uF capacitor from this pin to AC2 pin.
18	PGND2	-	Power ground for the AC clamp FETs.
19	CLAMP1	I	AC clamp input 1. Connect a 0.47uF capacitor from this pin to AC1 pin.
20	FOD2	I	FOD2 adjustment. A resistor between this pin and AGND sets the FOD offset value used in the internal FOD calculation.
21	ACM1	I	AC Modulation input 1. Connect a 22nF capacitor from this pin to AC1 pin.
22	PGND1	-	Power ground for the full-wave rectifier.
23	ACM2	I	AC Modulation input 2. Connect a 22nF capacitor from this pin to AC2 pin.
24	NC4	NC	Not internally connected. This pin may be connected to others to facilitate routing or to improve thermal performance.
25	FOD1	I	A resistor between this pin and Analog Ground selects the FOD compensation curve that is used for the internal FOD calculation.
26	SDA	I/O	I^2C data port. Connect a 2.2k pullup resistor from this pin to OUT (PIN) voltage or the system IO voltage rail. If not used, connect to ground.
27	SCL	I	I^2C clock port. Connect a 2.2k pullup resistor from this pin to OUT voltage or the system IO voltage rail. If not used, connect to ground.
28	AGND	-	Analog Ground connection.
29	VDD	O	Internal voltage supply. Connect a 1uF capacitor between this pin and Analog Ground. Do not connect any external load to this pin.
30	AC2	I	AC2 input to the Internal full-wave rectifier.
31	PGND	-	Power ground for the full-wave rectifier.
32	$\overline{STAT}$	O	Status output. A logic low state indicates that power is being transferred.

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Block Diagram



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Description of the Wireless Power Charging System

A wireless power charging system has a base station with one or more transmitters that make power available via DC-to-AC inverter(s) and transmit the power over a strongly-coupled inductor pair to a receiver in a mobile device. The transmitter may be a *free-positioning* or *magnetically-guided* type. A *free-positioning* type of transmitter has one coil or an array of coils that offers limited spatial freedom to the end-user, whereas a *magnetically-guided* type of transmitter helps the end-user align the receiver to the transmitter with a magnetic attraction.

The amount of power transferred to the mobile device is controlled by the receiver. The receiver sends communication packets to the transmitter to increase power, decrease power, maintain the power level, or terminate power transfer. The bit rate for Rx-to-Tx communication link is 2kbps. The communication is digital and communication of 1's and 0's is achieved by the Rx modulating the amount of load on the receiver coil.

To conserve power, the transmitter places itself in a very-low-power sleep mode unless it detects the presence of a receiver. Once a receiver is detected, the transmitter exits sleep mode and begins the power transfer per the WPC specification.

Theory of Operation

The P9025AC is a highly-integrated WPC (Wireless Power Consortium)-compliant wireless power receiver IC for mobile devices. It can transfer 5W of power from a wireless transmitter to a load (ex. a battery charger) in WPC "Qi" mode using near-field magnetic induction. For complete details of the WPC wireless power systems, refer to the WPC specifications and other materials at http://www.wirelesspowerconsortium.com.

Overview

The simplified internal block diagram of the P9025AC is shown on page 8. An external inductor and capacitor transfers energy from the transmitter's coil through the P9025AC's AC1 and AC2 pins to be full-wave-rectified and stored on a capacitor connected to $V_{RECT.}$ Until the voltage across the capacitor exceeds the threshold of the VIN_UVLO block, the rectification is performed by the body diodes of the Synchronous Full Bridge Rectifier FETs. After the internal biasing circuit is enabled, the Driver and Control block operates the MOSFET switches in the rectifier synchronously with the applied AC signal for increased efficiency. An internal ADC monitors the voltage at V_{RECT} and the load current.

Using this information, the P9025AC sends instructions to the wireless power transmitter to increase, maintain, or decrease the amount of power transferred. The P9025AC may also instruct the transmitter to terminate power transmission based on various conditions and other inputs.

Power Control

The voltage at V_{RECT} and the current through the rectifier are sampled periodically and digitized by the ADC. The digital equivalents of the voltage and current are supplied to the internal control logic, which decides whether the loading conditions on V_{RECT} indicate that a change in the operating point is required. If the load is heavy enough to bring the voltage at V_{RECT} below its target, the transmitter is instructed to move its frequency lower, closer to resonance. If the voltage at V_{RECT} is higher than its target, the transmitter is instructed to increase its frequency. To maximize efficiency, the voltage at V_{RECT} is programmed to decrease and become closer to the LDO output voltage as the LDO's load current increases. When the load current is small, a higher V_{RECT} is desirable so that the system can better handle a sudden load increase.

WPC Characteristics

Startup and Power Transfer

When a mobile device containing the P9025AC is placed on a WPC "Qi" charging pad, it responds to the transmitter's "ping" signal by rectifying the AC power from the transmitter and storing it on a capacitor connected to $V_{RECT.}$ During the "ping" phase, the rectifier provides about 5V at the V_{RECT} pin. An internal linear voltage regulator provides the supply voltage for the digital section to enable WPC communication. To increase the reliability of the communication, an internal load of about 15mA is connected to V_{RECT} until the external load is large enough to support communication.

The P9025AC then communicates its Identification and Configuration information to the transmitter. After this, the system is in the Power Transfer state. The control loop of the P9025AC then adjusts the rectifier voltage to 7V by sending Control Error Packets instruction to the transmitter. The LDO output is enabled and power is delivered to the load after V_{RECT} initially reaches 7V.

During power delivery to the load, the P9025AC control circuit continues to send Control Error Packets to the transmitter to adjust the rectifier voltage to the level required to maximize the efficiency of the linear regulator.

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Advanced Foreign Object Detection (FOD)

When metallic objects are exposed to an alternating magnetic field, eddy currents cause such objects to heat up. Examples of parasitic metal objects as such are coins, keys, paper clips, etc. The amount of heating depends on the strength of coupled magnetic field, as well as on the characteristics of the object, such as its resistivity, size, and shape. In a wireless power transfer system, the heating manifests itself as a power loss, and therefore a reduced power transfer efficiency. Moreover, if no appropriate measures are taken, the heating could be sufficient that the foreign objects may become heated to an undesirable temperature.

During Power Transfer state, the receiver periodically will communicate to the transmitter the amount of power received by means of a Received Power packet. The transmitter will compare this power with the amount of power transmitted during the same time period. If there is a significant unexplained loss of power, then the transmitter will shut off power delivery, because a possible foreign object may be absorbing too much energy.

For a WPC system to perform this function with sufficient accuracy, both the transmitter and receiver need each to account for and compensate for all of their known losses. Such losses could be to resistive losses, nearby metals that are part of the transmitter or receiver, etc. Because the system accurately measures its power and accounts for all known losses, it can thereby detect foreign objects owing to their creation of an unknown loss.

The P9025AC employs advanced FOD techniques to both accurately measure its received power, and to accurately compensate all of its known losses. This compensation is implemented by means of a curve fitting table. This table supports up to 10 different curves stored in OTP (One Time Programmable) memory. The 10 programmed OTP settings are externally selected by means of the FOD1 selection resistor value (see page 14) which selects the settings that best match a particular system characteristic. Additionally, the I^2C interface supports 1 volatile FOD compensation setting that can be selected that will override the OTP memory settings. A further enhancement is selected by the FOD2 offset resistor which adds a -300 to +300mW power offset to the values selected by the FOD1 resistor. This is useful to tune the selected compensation curve up or down to optimally match the actual known receiver system losses.

For more information about how to determine and program the FOD settings, refer to application note AN-886 P9025AC FOD Tuning Guide.

Over-Voltage Protection

In the event that the input voltage increases above 15V, the control loop disables the LDO, and sends error packets to the transmitter in an attempt to bring the rectifier voltage below 7V. If the voltage at V_{RECT} exceeds VOVP, two internal FETs turn on to clamp the AC inputs to quickly reduce the V_{RECT} voltage. This is accomplished through loading the receiver resonant tank with extra capacitance shorted to ground through the above mentioned internal FETs. This changes the parallel resonance of the tank circuit which causes the Tx to Rx gain to decrease dramatically. The clamp is released when the V_{RECT} voltage falls below the VOVP hysteresis level. V_{RECT} must not be directly loaded.

Over-Current Protection and Thermal Shutdown

The P9025AC employs over-current and thermal protection by sending an End of Power packet to the transmitter when the output current reaches the current limit level or the die temperature exceeds the thermal shutdown level. The LDO output is also disabled during these conditions.

The current limit level is programmable with an external resistor:

$$I_{LIM} = \frac{45000}{R_{LIM}}$$

For any value of RLIM below 25kΩ, the output current is limited to 2-Amps. However, RLIM is not recommended to be set higher than 60 kΩ.

Rectifier and V_{RECT} Level

Once V_{RECT} powers up to greater than 7V, the full-bridge rectifier switches to half synchronous or full synchronous mode (depending on the loading conditions) to efficiently transfer energy from the transmitter to V_{RECT}. The control loop of the P9025AC maintains the rectifier voltage between 5.45V and 7V, depending upon the output current (I_{OUT}). The RLIM resistor sets both the current limit (I_{LIM}) and the V_{RECT} steps based on I_{SET} which is a reference current used to partition the I_{OUT} load range into 4 regions, each with a V_{RECT} target for efficiency and transient optimization. I_{SET} is equal to:

$$I_{SET} = \frac{38000}{R_{LIM}}$$

The recommended value of R_{LIM} for a 1A output is 30 kΩ.

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Table 5: V_{RECT} Target Range

VRECT	I_{OUT}
7V	I_{OUT} < 10% of I_{SET}
6.3V	10% of I_{SET} < I_{OUT} < 20% of I_{SET}
5.5V	20% of I_{SET} < I_{OUT} < 40% of I_{SET}
5.45V	40% of I_{SET} < I_{OUT}

Status Output

The $\overline{STAT}$ output goes low when the LDO output is enabled.

Interrupt Output

The $\overline{INT}$ output goes low to indicate that an Over-Current, Over-Voltage or Over-Temperature event has occurred. See the Electrical Specifications for threshold levels.

Enable Input

If the particular application requires the P9025AC to be disabled, this can be accomplished with the $\overline{EN}$ pin. When the $\overline{EN}$ pin is pulled high, the device is suspended and placed in low current (sleep) mode. If the $\overline{EN}$ pin is pulled low or floating, the device is active.

TEOP Input

The P9025AC can optionally be shut down with the TEOP pin. This pin is typically used to shut down the P9025AC if the battery charger or host system determines an over-limit high temperature condition. When the TEOP pin is pulled high, the P9025AC will disable its LDO output, and also send an End-of-Power packet to the transmitter with code 0x03 (Over-Temperature code). In response to the End-of-Power packet, the transmitter will immediately stop power transfer and go into a sleeping (no power offered) condition for some period of time. The amount of sleep time is not prescribed by WPC and varies among different transmitters. A common value used for this over-temperature sleep time is approximately 5-minutes.

CHG_END / CS100

This pin has two functions. The Charge-End default function can be used to terminate power transfer with the transmitter. When CHG_END is pulled high, the P9025AC will send a WPC End-of-Charge packet with a code value of 0x01 (Charge Complete code). In response to this, the transmitter should immediately stop power transfer and go into a sleeping (no power offered) condition for some period of time. The amount of sleep time is not prescribed by WPC and varies from 5-seconds to much longer, depending on the transmitter design.

If the pin is set in Charge-Status mode, the device will send a WPC Charge Status packet with value 100 (100% charge) indicating a fully charged battery.

LDO

The primary output of the P9025AC device is a linear regulator that receives its input from V_{RECT}. The LDO supplies power to the system and/or charging circuitry. The output provides a nominal 5.3V with 1 A output current capability. The voltage is intentionally set 0.3V higher than the standard 5V rail to provide extra headroom for voltage drops that may be encountered in the system under heavy loads.

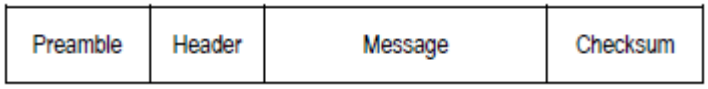
Modulation/Communication

Receiver-to-transmitter communication is accomplished by modulating the load seen by the receiver's inductor. To the transmitter, this appears as an impedance change, which results in measurable variations of the transmitter's output waveform. Modulation is done with AC Modulation, using internal switches to connect external capacitors from AC1 and AC2 to ground. The communication protocol is covered in the next section.

WPC Communication

The P9025AC communicates with the base via communication packets. Each communication packet has the following structure:

Figure 3. Communication Packet Structure



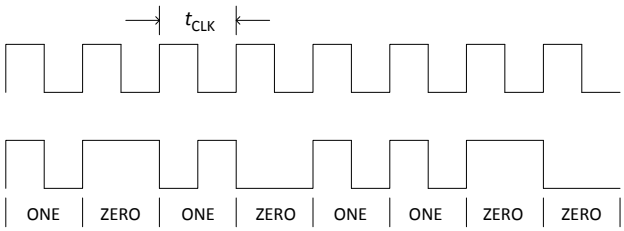
In accordance with the WPC specification, the power receiver communicates with the power transmitter using load modulation. The load seen by the power transmitter's inductor is modulated on the receiver side in a periodic fashion to send packets. The power transmitter detects this as a modulation of coil current/voltage to receive the packet information.

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Bit Encoding Scheme

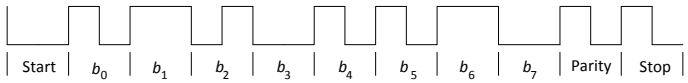
As required by the WPC, the P9025AC uses a differential bi-phase encoding scheme to modulate data bits onto the Power Signal. A clock frequency of 2kHz is used for this purpose. A logic ONE bit is encoded by generating two transitions per clock period, whereas a logic ZERO bit is encoded using only one transition per clock period as shown below:

Figure 4. Bit Encoding Scheme



Each byte in the communication packet comprises 11bits in an asynchronous serial format, as shown below:

Figure 5. Byte Encoding Scheme



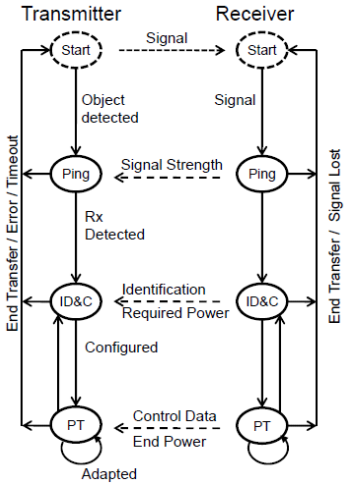
Each byte has a start bit, 8 data bits, a parity bit, and a single stop bit.

System Feedback Control

The P9025AC is fully compatible with WPC specification Rev. 1.1.2 and has all necessary circuitry to communicate with the base station via WPC-compliant communication packets.

The overall WPC-compliant system behavior between the transmitter and receiver follows the state machine below:

Figure 6. WPC System Feedback Control



The P9025AC goes through four phases: Start/Selection, Ping, Identification & Configuration, and Power Transfer.

Start/Selection

In this phase, the P9025AC senses the incoming power from the base station transmitter and proceeds to the PING state. It monitors the rectified voltage, and when the voltage is above the $V_{RECT,}$ UVLO threshold, the P9025AC wakes up its digital electronics and prepares to communicate with the base station. If the P9025AC does not proceed to PING, then it does not transmit any communication packets.

Ping

In this phase, the P9025AC transmits a Signal Strength Packet as the first communication packet to instruct the base to keep the power signal ON. After sending the Signal Strength Packet, the P9025AC proceeds to the Identification and Configuration phase. If, instead, the P9025AC sends End of Power Packets, then it remains in the PING phase.

In this phase, the P9025AC sends the following packets:

- Signal Strength Packet
- End of Power Packet

Identification and Configuration (ID & Config)

In this phase, the P9025AC may send the following packets:

- Identification Packet
- Configuration Packet

After sending the Configuration Packet, the P9025AC proceeds to the power transfer phase.

Power Transfer

In this phase, the P9025AC controls the power transfer from the Power Transmitter by means of the following Control Data Packets:

- Control Error Packets
- Rectified Power Packet
- End Power Transfer Packet

Modulation

The P9025AC is compatible with WPC V1.1.2 transmitter coils. Each receiver coil type has a unique inductance value and various physical properties as are best for a given application. As such, the resonant capacitor (CS) that is used with a given receiver coil should be optimized for the overall application. The WPC guidance for Cs is that the resonant frequency of the receiver coil and Cs capacitor should be 100kHz while placed on the surface of a transmitter with the normal spacing.

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Application Information

External Components

The P9025AC requires a minimum number of external components for proper operation, as indicated in the Reference schematic.

LDO

Input Capacitor (V_{RECT} Capacitors)

The LDO input capacitors (V_{RECT} capacitors) should be located as close as possible to the V_{RECT} pins, and ground (PGND). Ceramic capacitors are recommended for their lower ESR and small profile.

V_{DD} Capacitor

The P9025AC has an internal LDO regulator that must be bypassed with a 1µF capacitor connected from the V_{DD} pin to GND. This capacitor should be as close as possible to the V_{DD} pin with a close GND connection.

Output Capacitor

A 0.1µF and a 4.7µF capacitors in parallel must be connected from this pin to ground (PGND). The trace should be made as short as practical for maximum device performance. Since the LDO has been designed to function with very low ESR capacitors, a ceramic capacitor is recommended for best performance. For better transient response increase the total amount of output capacitance. For 1-Amp load steps, an output capacitance of at least 10µF is recommended.

NC and DNC Pins

NC pins that are indicated as “Not Internally Connected” should be soldered to the PCB ground plane to improve thermal performance with multiple vias exiting the bottom side of the PCB. This improves heat flow away from the package and minimizes package thermal gradients.

DNC pins that are indicated as “Internally connected” must be left floating.

PCB Layout Considerations

For optimum device performance and lowest output phase noise, IDT recommends that customers copy the reference layout used in the P9025AC-R-EVK reference kit. More information and layout files can be found at http://www.idt.com/P9025AC-R-EVK.

Additional layout guidelines can be found in application note AN-889 P9025AC Layout Guidelines. Users are encouraged to read this document prior to starting a board design.

Power Dissipation and Thermal Requirements

The P9025AC is offered in a VFQFPN-32 package which has a maximum power dissipation capability of about 1.9W. The maximum power dissipation is determined by the number of thermal vias between the package and the printed circuit board, combined with the ability of the board to ultimately transfer the thermal energy into the ambient environment. The maximum power dissipation is defined by the dies specified maximum operating junction temperature, T_J, of 125°C. The junction temperature rises when the heat generated by the device's power dissipation goes through the package thermal resistance. The VFQFPN package offers a typical thermal resistance, junction to ambient (Θ_{JA}), of 35°C/W when the PCB layout and surrounding devices are optimized as described in application note AN-889 P9025AC Layout Guidelines.

Thermal Overload Protection

The P9025AC integrates thermal overload shutdown circuitry to prevent damage resulting from excessive thermal stress that may be encountered under fault conditions. This circuitry will shut down and reset the device if the die temperature exceeds 150°C. To allow the maximum load current on each regulator and the synchronous rectifier, and to prevent thermal overload, it is important to ensure that the heat generated by the P9025AC is dissipated efficiently into the PCB and environment

End of Charge (EOC)

In the event of thermal shutdown (150°C), EN, CHG_END or TEOP pins assertion the device turns off the LDO and continually sends End Of Power (EOP) packets until the transmitter removes the power and the rectifier voltage on the receiver side drops below the UVLO threshold.

Special Notes

32-VFQFPN Package Assembly

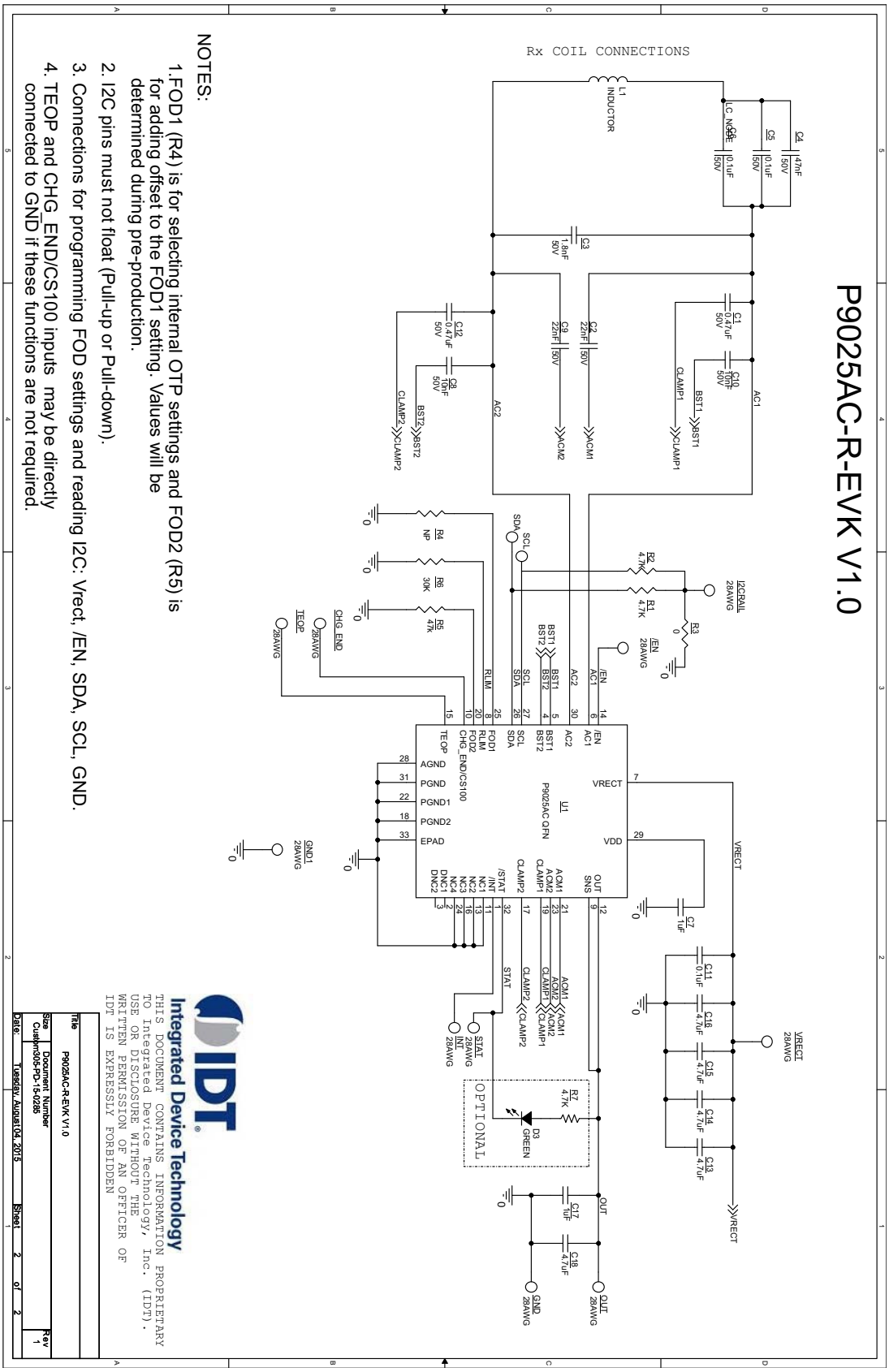
Note 1: Unopened Dry Packaged Parts have a one year shelf life.

Note 2: The HIC indicator card for newly-opened Dry Packaged Parts should be checked. If there is any moisture content, the parts must be baked for a minimum of 8 hours at 125°C within 24 hours of the assembly reflow process.

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Reference Schematic (P9025AC-R-EVK V1.0)

The reference schematic bill-of-materials can be found in the P9025AC-R-EVK reference board manual.



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I²C Register Map

The P9025AC has a one-time programmable I²C address that is set to default 0X25h.

Table 6: READ Registers – V_{RECT} Voltage: V_{RECT} = 5 X ADC1<12:1> = [ADC1<12:1>] X 5 X [1.8V/2^{12}]

Byte Address	Byte Name	Bit Field	Field Name	Type	Default Value	Description
0x40	REG0	7	ADC1<12>	R		V_{RECT} ADC code (average of 8 consecutive measurements)
0x40	REG0	6	ADC1<11>	R		V_{RECT} ADC code (average of 8 consecutive measurements)
0x40	REG0	5	ADC1<10>	R		V_{RECT} ADC code (average of 8 consecutive measurements)
0x40	REG0	4	ADC1<9>	R		V_{RECT} ADC code (average of 8 consecutive measurements)
0x40	REG0	3	ADC1<8>	R		V_{RECT} ADC code (average of 8 consecutive measurements)
0x40	REG0	2	ADC1<7>	R		V_{RECT} ADC code (average of 8 consecutive measurements)
0x40	REG0	1	ADC1<6>	R		V_{RECT} ADC code (average of 8 consecutive measurements)
0x40	REG0	0	ADC1<5>	R		V_{RECT} ADC code (average of 8 consecutive measurements)
0x41	REG1	7	ADC1<4>	R		V_{RECT} ADC code (average of 8 consecutive measurements)
0x41	REG1	6	ADC1<3>	R		V_{RECT} ADC code (average of 8 consecutive measurements)
0x41	REG1	5	ADC1<2>	R		V_{RECT} ADC code (average of 8 consecutive measurements)
0x41	REG1	4	ADC1<1>	R		V_{RECT} ADC code (average of 8 consecutive measurements)
0x41	REG1	3	Reserved	R		Reserved
0x41	REG1	2	Reserved	R		Reserved
0x41	REG1	1	Reserved	R		Reserved
0x41	REG1	0	Reserved	R		Reserved

Table 7: Read Registers – I_{OUT} Current:

I_{OUT} is read directly from I_{OUT} = ADC2<12:1> = [ADC1<12:1>] X [1.8A/2^{12}]

Byte Address	Byte Name	Bit Field	Field Name	Type	Default Value	Description
0x42	REG2	7	ADC2<12>	R		I_{OUT} ADC code (average of 8 consecutive measurements)
0x42	REG2	6	ADC2<11>	R		I_{OUT} ADC code (average of 8 consecutive measurements)
0x42	REG2	5	ADC2<10>	R		I_{OUT} ADC code (average of 8 consecutive measurements)
0x42	REG2	4	ADC2<9>	R		I_{OUT} ADC code (average of 8 consecutive measurements)
0x42	REG2	3	ADC2<8>	R		I_{OUT} ADC code (average of 8 consecutive measurements)
0x42	REG2	2	ADC2<7>	R		I_{OUT} ADC code (average of 8 consecutive measurements)
0x42	REG2	1	ADC2<6>	R		I_{OUT} ADC code (average of 8 consecutive measurements)
0x42	REG2	0	ADC2<5>	R		I_{OUT} ADC code (average of 8 consecutive measurements)
0X43	REG3	7	ADC2<4>	R		I_{OUT} ADC code (average of 8 consecutive measurements)
0X43	REG3	6	ADC2<3>	R		I_{OUT} ADC code (average of 8 consecutive measurements)
0X43	REG3	5	ADC2<2>	R		I_{OUT} ADC code (average of 8 consecutive measurements)
0X43	REG3	4	ADC2<1>	R		I_{OUT} ADC code (average of 8 consecutive measurements)
0X43	REG3	3	Reserved	R		Reserved
0X43	REG3	2	Reserved.	R		Reserved
0X43	REG3	1	Reserved.	R		Reserved
0x43	REG3	0	Reserved.	R		Reserved

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Table 8: READ Registers - Frequency:

$f_{CLK} = \frac{65536}{COUNT}$ where COUNT is the decimal number represented by FREQ<10:1>.

Byte Address	Byte Name	Bit Field	Field Name	Type	Default Value	Description
0X44	REG4	7	FREQ<10>	R		Frequency value (10 bits)
0X44	REG4	6	FREQ<9>	R		Frequency value (10 bits)
0X44	REG4	5	FREQ<8>	R		Frequency value (10 bits)
0X44	REG4	4	FREQ<7>	R		Frequency value (10 bits)
0X44	REG4	3	FREQ<6>	R		Frequency value (10 bits)
0X44	REG4	2	FREQ<5>	R		Frequency value (10 bits)
0X44	REG4	1	FREQ<4>	R		Frequency value (10 bits)
0X44	REG4	0	FREQ<3>	R		Frequency value (10 bits)
0X45	REG5	7	FREQ<2>	R		Frequency value (10 bits)
0X45	REG5	6	FREQ<1>	R		Frequency value (10 bits)
0X45	REG5	5	Reserved	R		Reserved
0X45	REG5	4	Reserved	R		Reserved
0X45	REG5	3	Reserved	R		Reserved
0X45	REG5	2	Reserved	R		Reserved
0X45	REG5	1	Reserved	R		Reserved
0X45	REG5	0	Reserved	R		Reserved

Table 9: READ Registers – Miscellaneous Functions

Byte Address	Byte Name	Bit Field	Field Name	Type	Default Value	Description
0X47	REG7	3	UVLO	R		1: V_{RECT} is higher than UVLO threshold 0: No meaning.
0X47	REG7	2	CLAMP_ON	R		0: VRECT is lower than AC clamp threshold 1: VRECT is higher than AC clamp threshold
0X47	REG7	1	LDO_CL	R		0: Normal Operation 1: LDO current limit exceeded.
0X47	REG7	0	Reserved	R		Reserved
0X48	REG8	7	CHARGE_COMPLETE	R		0: No meaning 1: Charge Complete
0X48	REG8	6	Reserved	R		Reserved
0X48	REG8	5	Reserved	R		Reserved
0X48	REG8	4	Reserved	R		Reserved
0X48	REG8	3	Reserved	R		Reserved
0X48	REG8	2	Reserved	R		Reserved
0X48	REG8	1	DIE_TEMP	R		0: Die Temperature < 150C 1: Die Temperature >150C
0x48	REG8	0	TX_TYPE	R		0: TX is WPC
0x54	REG20	[7:0]	WPC_ID_B0	R		Unique IC identifier per WPC specification
0x55	REG21	[7:0]	WPC_ID_B1	R		Unique IC identifier per WPC specification

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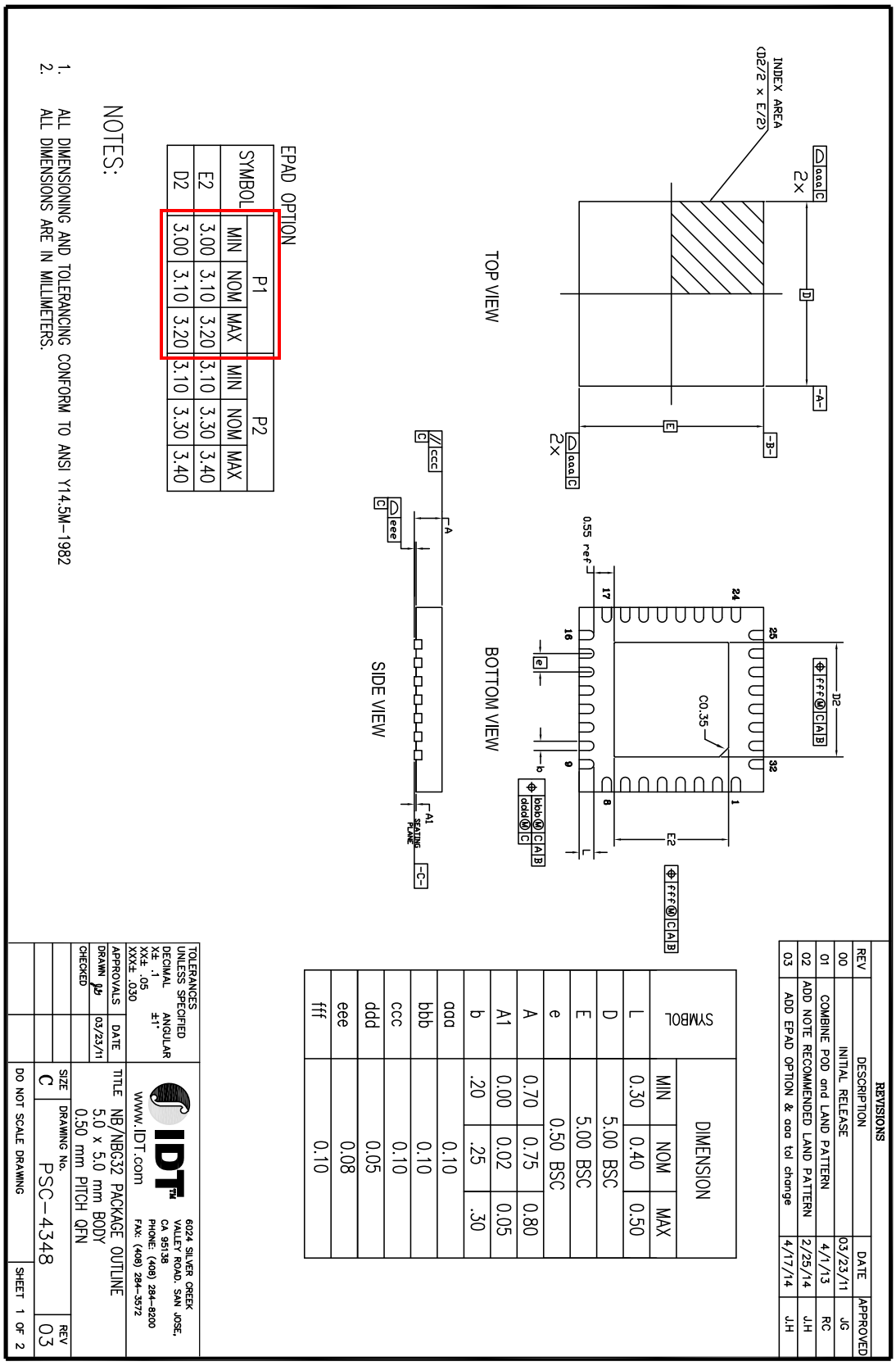
Byte Address	Byte Name	Bit Field	Field Name	Type	Default Value	Description
0x56	REG22	[7:0]	WPC_ID_B2	R		Unique IC identifier per WPC specification
0x57	REG23	[7:0]	WPC_ID_B3	R		Unique IC identifier per WPC specification
0x58	REG24	[7:0]	WPC_ID_B4	R		Unique IC identifier per WPC specification
0x59	REG25	[7:0]	WPC_ID_B5	R		Unique IC identifier per WPC specification
0x5A	REG26	[7:0]	WPC_ID_B6	R		Unique IC identifier per WPC specification
0x5B	REG27	[7:0]	Reserved	R		Reserved
0x5C	REG28	[7:0]	Reserved	R		Reserved
0x5D	REG29	[7:0]	Reserved	R		Reserved
0x5E	REG30	[7:0]	Reserved	R		Reserved
0x5F	REG31	[7:0]	Reserved	R		Reserved
0x60	REG32	[7:0]	Reserved	R		Reserved
0x61	REG33	[7:0]	Reserved	R		Reserved
0x62	REG34	[7:0]	Reserved	R		Reserved
0x63	REG35	[7:0]	Reserved	R		Reserved
0x64	REG36	[7:0]	Reserved	R		Reserved
0x65	REG37	[7:0]	Reserved	R		Reserved

Table 10: Read-Write physical FOD registers:

Byte Address	Byte Name	Bit Field	Field Name	Type	Default Value	Description
0x49	REG9	0-7	FOD9<0-7>	R/W	0	mcf correction for Region 1 IO1, IO2, IO3 = 000
0x4A	REG10	0-7	FOD10<0-7>	R/W	0	bcf correction for Region 1 IO1, IO2, IO3 = 000
0x4B	REG11	0-7	FOD11<0-7>	R/W	0	mcf correction for Region 2 IO1, IO2, IO3 = 010
0x4C	REG12	0-7	FOD12<0-7>	R/W	0	bcf correction for Region 2 IO1, IO2, IO3 = 010
0x4D	REG13	0-7	FOD13<0-7>	R/W	0	mcf correction for Region 3 IO1, IO2, IO3 =100
0x4E	REG14	0-7	FOD14<0-7>	R/W	0	bcf correction for Region 3 IO1, IO2, IO3 = 100
0x4F	REG15	0-7	FOD15<0-7>	R/W	0	mcf correction for Region 4 IO1,IO2,IO3 = 110
0x50	REG16	0-7	FOD16<0-7>	R/W	0	bcf correction for Region 4 IO1, IO2, IO3 = 110
0x51	REG17	0-7	FOD17<0-7>	R/W	0	mcf correction for Region 5 IO1, IO2, IO3 = 111
0X52	REG18	0-7	FOD18<0-7>	R/W	0	bcf correction for Region 5 IO1, IO2, IO3 = 111
0X53	REG19	0-7	FOD19<0-7>	R/W	0	bcf correction for start-up phase

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Package Outline and Package Dimensions (NBG32) – use EPAD option P1



REVISIONS

REV	DESCRIPTION	DATE	APPROVED
00	INITIAL RELEASE	03/23/11	JG
01	COMBINE POD and LAND PATTERN	4/1/13	RC
02	ADD NOTE RECOMMENDED LAND PATTERN	2/25/14	JH
03	ADD EPAD OPTION & aaa tol change	4/17/14	JH

SYMBOL	DIMENSION		
	MIN	NOM	MAX
L	0.30	0.40	0.50
D		5.00 BSC	
E		5.00 BSC	
e		0.50 BSC	
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
b	.20	.25	.30
aaa		0.10	
bbb		0.10	
ccc		0.10	
ddd		0.05	
eee		0.08	
fff		0.10	

EPAD OPTION

SYMBOL	P1			P2		
	MIN	NOM	MAX	MIN	NOM	MAX
E2	3.00	3.10	3.20	3.10	3.30	3.40
D2	3.00	3.10	3.20	3.10	3.30	3.40

NOTES:

1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M-1982
2. ALL DIMENSIONS ARE IN MILLIMETERS.

TOLERANCES UNLESS SPECIFIED
DECIMAL ANGULAR
X± .1 ±1°
XX± .05
XXX± .030

APPROVALS DATE
DRAWN 03/23/11
CHECKED

IDT™ 6024 SILVER CREEK VALLEY ROAD, SAN JOSE, CA 95138
PHONE: (408) 284-8200 FAX: (408) 284-3572
WWW.IDT.com

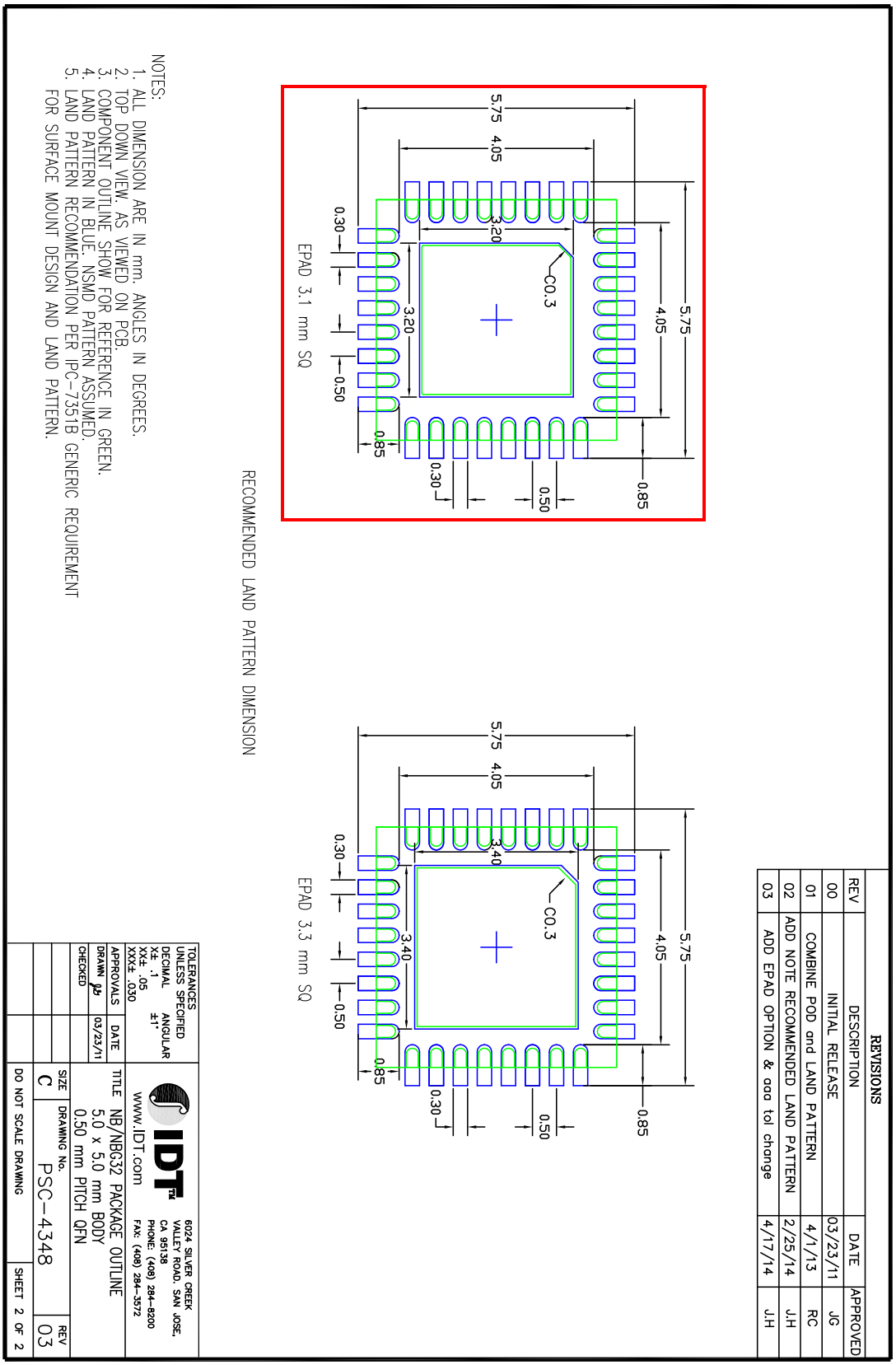
TITLE NB/NBG32 PACKAGE OUTLINE
5.0 x 5.0 mm BODY
0.50 mm PITCH QFN

SIZE C | DRAWING No. PSC-4348 | REV 03

DO NOT SCALE DRAWING | SHEET 1 OF 2

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Package Outline and Package Dimensions (NBG32), cont. Use Epad 3.1mm Sq.



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Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Ambient Temperature
P9025AC-RNBGI	P9025AC-RNBGI	5 x 5 x 0.75 mm 32-VFQFPN	Tray	0 to +85°C
P9025AC-RNBGI8	P9025AC-RNBGI	5 x 5 x 0.75 mm 32-VFQFPN	Tape and Reel	0 to +85°C

Note 1: Custom configurations and a compact CSP package is available for qualified customers. Contact your IDT Sales Representative for more information

Note 2: Factory-customized versions are available for qualified customers. Contact your IDT Sales Representative for more information.

Revision History

Date	Originator	Description of Change
08/19/15	A.L.	Initial release.
09/01/15	A.L.	1. Updated Block Diagram. 2. Updated T_J from “0 to 150°C” to “0 to 125°C”. 3. Corrected minor textual typos.

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(Rev.1.0 Mar 2020)

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