Description

The P9027LP-R is a highly integrated, low Bill-of-Materials (BOM) count, single-chip receiver targeted for 0.5 to 3 W applications. Using the magnetic inductive charging technology, it converts an AC power signal from a resonant tank into a regulated programmable DC output voltage ranging from 4.5 to 6.0 Volts.

The receiver has a patented internal scheme for communication and modulation using zero external components. As a result, it provides an extremely small application area. Together with the P9235A-R transmitter, the P9027LP-R is a complete wireless power system solution.

The P9027LP-R is available in a WLCSP-40 package (2.24 mm × 3.62 mm, 0.4 mm pitch), and it is rated for 0 to 85°C ambient operating temperature range.

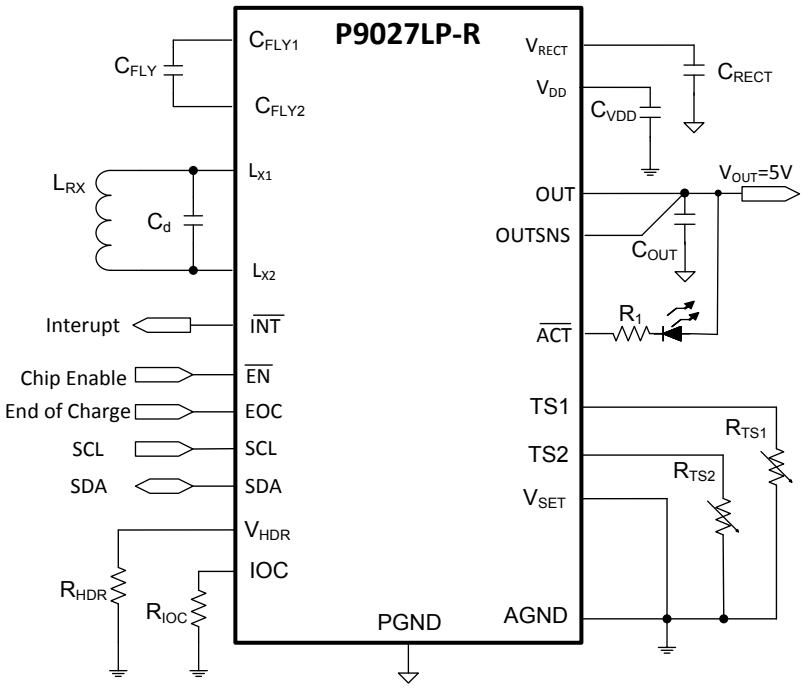
Typical Applications

- Smart Watches
- Headsets
- Digital Cameras
- Portable Medical Applications

Features

- Small solution area: ~32mm^2
- Patented over-voltage protection clamp eliminating external capacitors
- Optimized for 0.5 to 3 W applications
- Integrated low dropout tracking LDO
- Low synchronous rectifier $R_{DS(ON)}$ for high efficiency
- Programmable rectifier voltage for optimal transient response versus efficiency
- Integrated charge pump for startup under weak coupling or poor alignment
- Programmable output voltage: 4.5 to 6.0 V
- Programmable current limit
- Open-drain interrupt flag
- Power transfer LED indicator
- Dedicated remote temperature sensing
- Active low enable pin for electrical on/off
- I^{2}C interface
- 0 to +85°C ambient operating temperature range
- WLCSP 2.24 mm X 3.62 mm, 40 pin package

Figure 1. Typical Applications Circuit



Absolute Maximum Ratings

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Table 1. Thermal Information [1,2]

Pins	Rating	Units
RECT, OUT, OUTSNS	-0.3 to 9.0	V
LX1, LX2	-0.8 to 9.0	V
PGND, AGND	-0.3 to 0.3	V
VDD, CFLY1, CFLY2, SDA, SCL, $\overline{EN}$, $\overline{ACT}$, IOC, VSET, VHDR, $\overline{INT}$, EOC, TS1, TS2,	-0.3 to 6.0	V
Maximum input current into SFBR	3.0	A

All voltages here are measured with respect to analog ground pin (AGND).

Table 2. Thermal Symbol Information [1,2]

Symbol	Description	Rating	Units
Θ_{JA}	Thermal Resistance (WLCSP-40)	71	°C/W
Θ_{JC}	Thermal Resistance Junction to Case	18	°C/W
T_A	Ambient Operating Temperature Range	0 to 85	°C
T_J	Junction Operating Temperature Range	0 to 125	°C
T_{Js}	Junction Storage Temperature Range	-55 to 150	°C
T_{LEAD}	Maximum Soldering Temperature (at Leads)	300	°C

Notes:

1. The maximum power dissipation is $P_{D(MAX)} = (T_{J(MAX)}-T_A)/\theta_{JA}$ where $T_{J(MAX)}$ is 125°C. Exceeding the maximum allowable power dissipation will result in excessive die temperature, and the device will enter thermal shutdown.
2. The thermal rating was calculated based on a JEDEC 51 standard 4-layer board, 6 vias with dimensions 4 in × 4.5 in still air conditions. Actual thermal resistance will be affected by PCB size, solder joint quality, PCB layer count, copper thickness, air flow, altitude, and other unlisted variables.

Table 3. ESD Information

Test Model	Pins	Rating	Units
HBM	All	2,000	V
CDM	All	500	V

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Electrical Specification Table

V_{RECT}= 6.5 V, C_{OUT}=C_{VRECT}=20 µF, C_{FLY}=47 nF, C_{VDD}=1 µF, $\overline{EN}$=GND, V_{OUT}=5 V, T_A= 0 to +85°C, unless otherwise noted. Typical values are 25°C.

Table 4. Electrical Specification Table

Symbol	Description	Conditions	Min	Typical	Max	Units
Synchronous Full Bridge Rectifier (SFBR)						
V_{LX}	Voltage across SFBR		0.0		7.0	V
R_{ON-HS}	High-side R_{DS_ON}	Forward current = 0.7 - 1.0 A, T_A=25°C		45		mΩ
R_{ON-LS}	Low-side R_{DS_ON}	Forward current = 0.2 - 0.5 A, T_A=25°C		30		mΩ
V_{CLAMP}	Internal clamping voltage	Rectifier clamp (hardwired)		7.4		V
Charge Pump[2]						
VDD	Charge pump output Voltage	I_{VDD} = 0 – 5 mA; V_{RECT} = 3 - 8 V	4.0	5.0	5.5	V
V_{RECT_MIN}	Minimum V_{RECT}	I_{VDD} = 5 mA	1.9			V
I_{RECT}	Bias current	V_{RECT} = 5 V		5.0	8.0	mA
		V_{RECT} = 3 V		8.0		
$UVLO_{RISE}$	Rising voltage of UVLO		2.7	3.0	3.4	V
$UVLO_{HYST}$	Hysteresis of UVLO			0.4		V
Output Current						
I_{OUT}	Output current range	V_{OUT} = 5.0V	0		600	mA
I_{OUT_LEAK}	Leakage current	No transmitter present; V_{OUT}=5V		30	60	µA
I_{OUT_RES}	Output current resolution	ADC resolution		0.5		mA
	FSR Error[1]	V_{OUT} = 5.0 V, I_{OUT} = 0.2 – 0.5A		0.2	8.2	% FSR
		V_{OUT} = 5.0 V, I_{OUT} = 0.2 – 0.5 A, T_A = 25 °C		0.2	4.4	
Programmable LDO						
V_{OUT}	Output voltage range		4.5	5.0	6.0	V
V_{ACCU}	Output voltage accuracy	V_{OUT} = 3.0 – 5.0V, I_{OUT}= 0			2.3	%
		V_{OUT} = 3.0 – 5.0V, T_A = 25 °C			0.6	
V_{DROP}	Dropout voltage	I_{OUT} = 500mA			25	mV

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Electrical Specification Table (Continued)

V_{RECT}=6.5 V, C_{OUT}=C_{VRECT}=20 µF, C_{FLY}=47 nF, C_{VDD}=1 µF, $\overline{EN}$=GND, V_{OUT}=5 V, T_A= 0 to +85°C, unless otherwise noted. Typical values are 25°C.

Table 4. Electrical Specification Table (Continued)

Symbol	Description	Conditions	Min	Typical	Max	Units
12-bit Analog to Digital Converter						
V_{REF}	Reference voltage			1.8		V
	FSR Error[1]	VDD = 5.0 V		0.1	2.3	% FSR
		V_{DD} = 5.0 V, T_A = 25 °C		0.1	0.6	
f_{SAMPLE}	Sampling rate			60		kS/s
VHDR, VSET, TS1, TS2, IOC						
I_{SRC}	Source current	VDD = 3.0 - 5.5V	98	100	102	µA
V_{RSNS}	Sense voltage		0		1.8	V
R_{SET}	Resistor range	1% tolerance	0		18	kΩ

Digital Inputs and Outputs (SCL, SDA, $\overline{EN}$, $\overline{INT}$, $\overline{ACT}$, EOC)						
V_{OL}	Open drain: $\overline{INT}$, $\overline{ACT}$	I_{SINK} = 4 mA			0.4	V
V_{IH}	Input logic high voltage		1.0			V
V_{IL}	Input logic low Voltage				0.4	V
I²C Interface						
V_{IH}	Input high voltage	SCL, SDA	1.1			V
V_{IL}	Input low Voltage	SCL, SDA			0.4	V
f_{SCL}	Clock frequency				400	kHz
C_B	Capacitive load			150		pF
C_{BIN}	SCL, SDA input capacitance			5		pF
$t_{HD,STA}$	Hold Time (Repeated) for START Condition		0.6			µs
$t_{HD:DAT}$	Data Hold Time		0			ns
t_{LOW}	Clock Low Period		1.3			µs
t_{HIGH}	Clock High Period		0.6			µs

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Electrical Specification Table (Continued)

V_{RECT}=6.5 V, C_{OUT}=C_{VRECT}=20 µF, C_{FLY}=47 nF, C_{VDD}=1 µF, $\overline{EN}$=GND, V_{OUT}=5 V, T_A= 0 to +85°C, unless otherwise noted. Typical values are 25°C.

Table 4. Electrical Specification Table (Continued)

Symbol	Description	Conditions	Min	Typical	Max	Units
12-bit Analog to Digital Converter						
$t_{SU:STA}$	Set-up Time for Repeated START Condition		0.6			µs
t_{BUF}	Bus Free Time Between STOP and START Condition		1.3			µs
Thermal Shutdown[1]						
T_{SHD}	Thermal shutdown			130		°C
$T_{SHD-HYS}$	Thermal shutdown hysteresis			20		°C

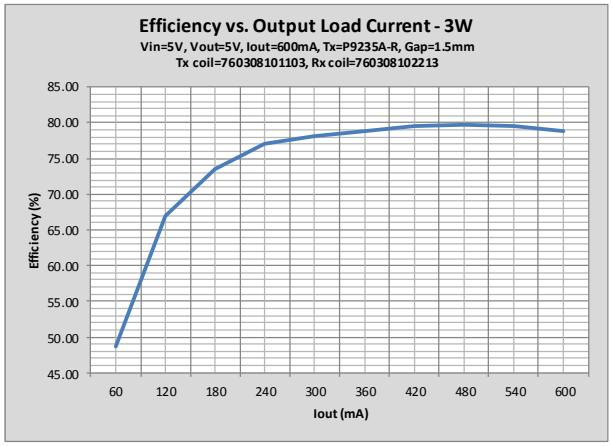
Notes:

1. Guaranteed by design and not subject to 100% production testing.
2. Do not externally load. For internally biasing only.

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Typical Performance Characteristics

Figure 2. Typical Performance Characteristics – 3W



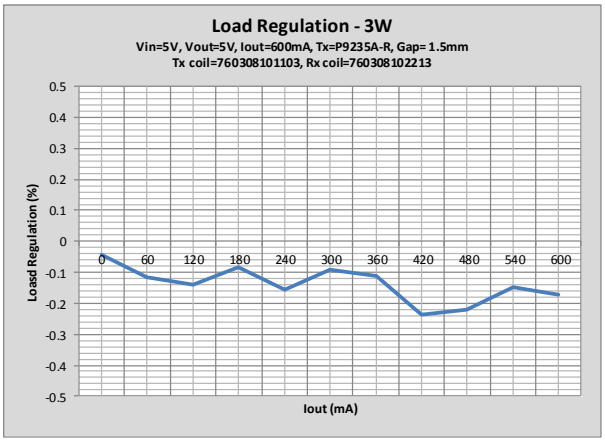
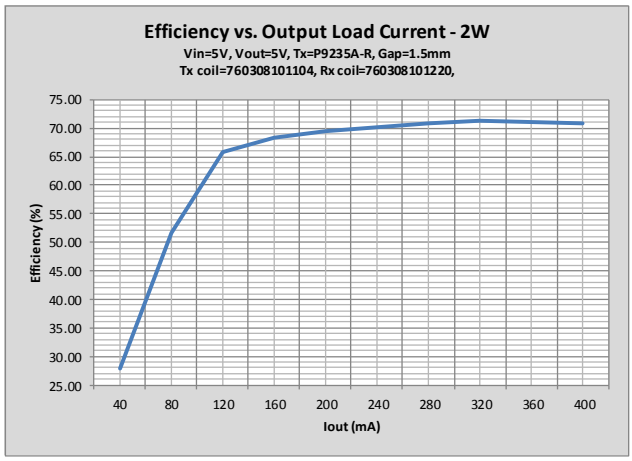


Figure 3. Typical Performance Characteristics – 2W



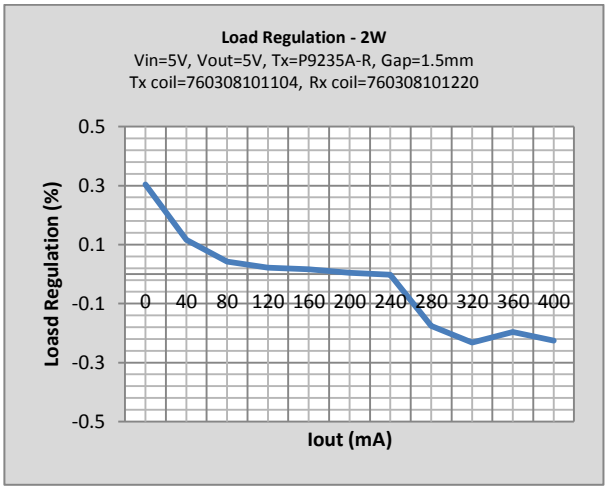
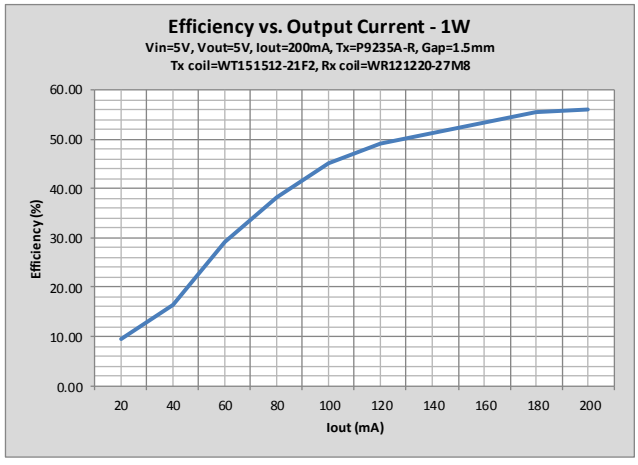
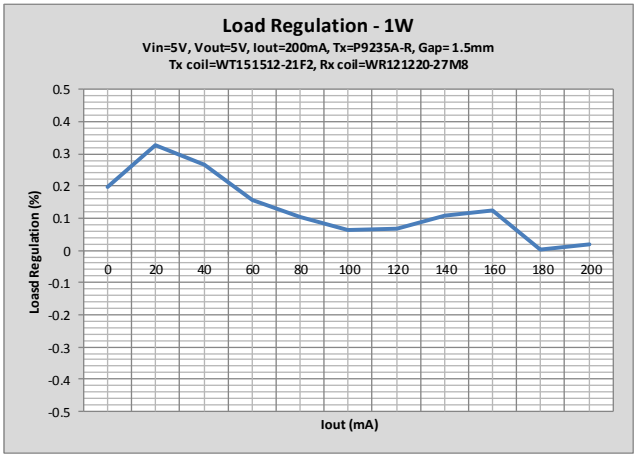


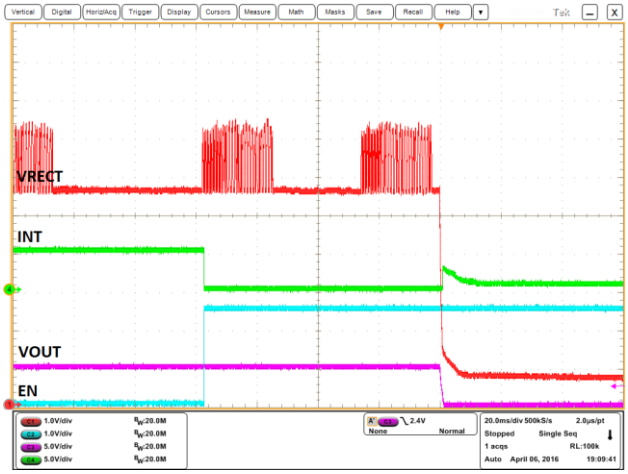
Figure 4. Typical Performance Characteristics – 1W





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Figure 5. EBN and ENB EPT



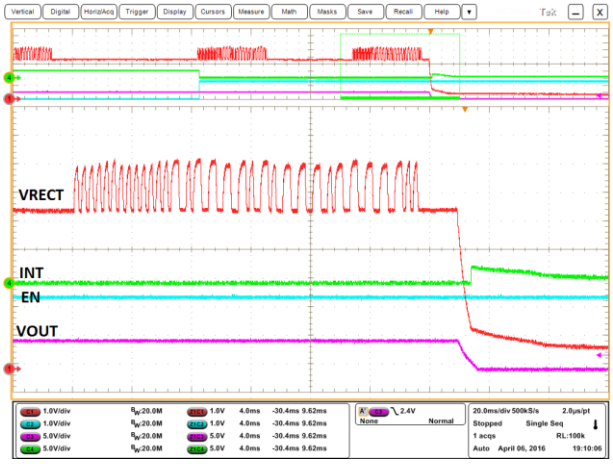
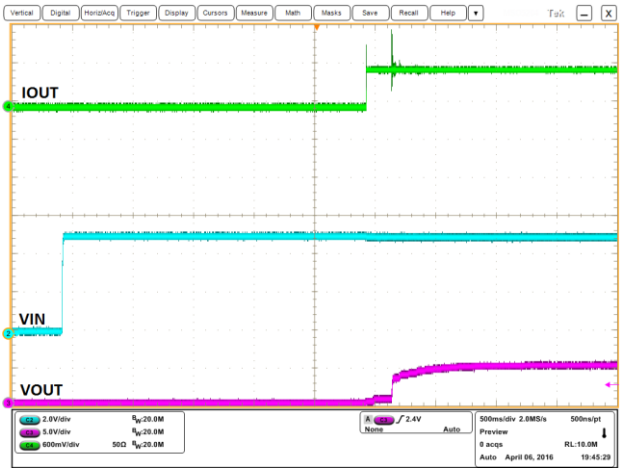


Figure 6. Vin_start_up_600mA_1 and ENB_startup_600mA_1ENB_startup_600mA_1



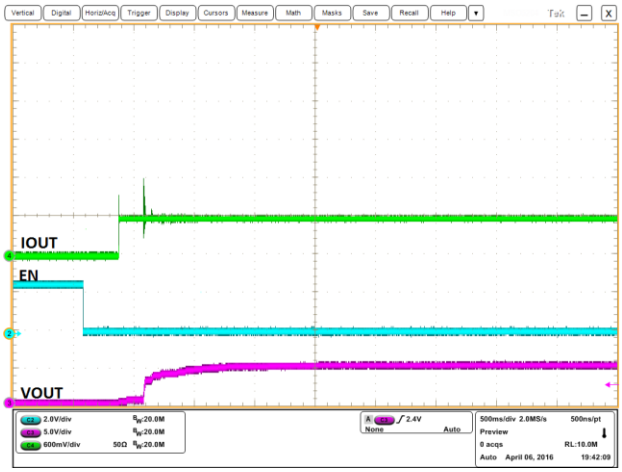
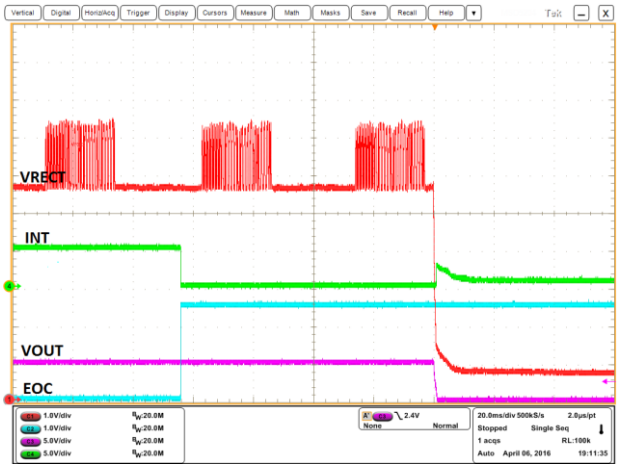


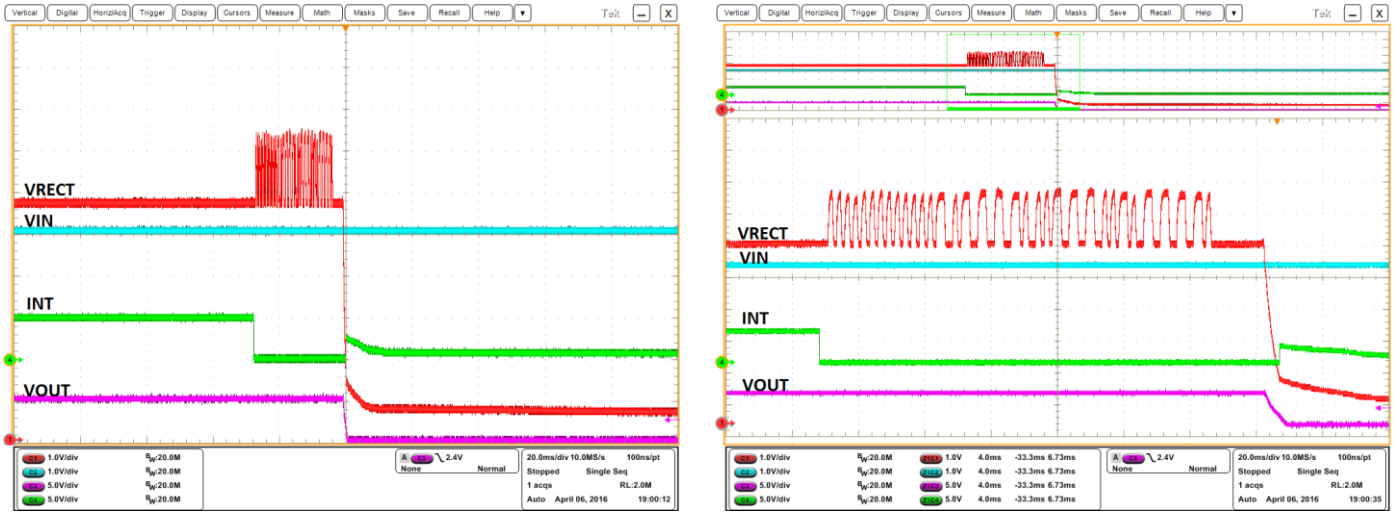
Figure 7. EOC and OC1





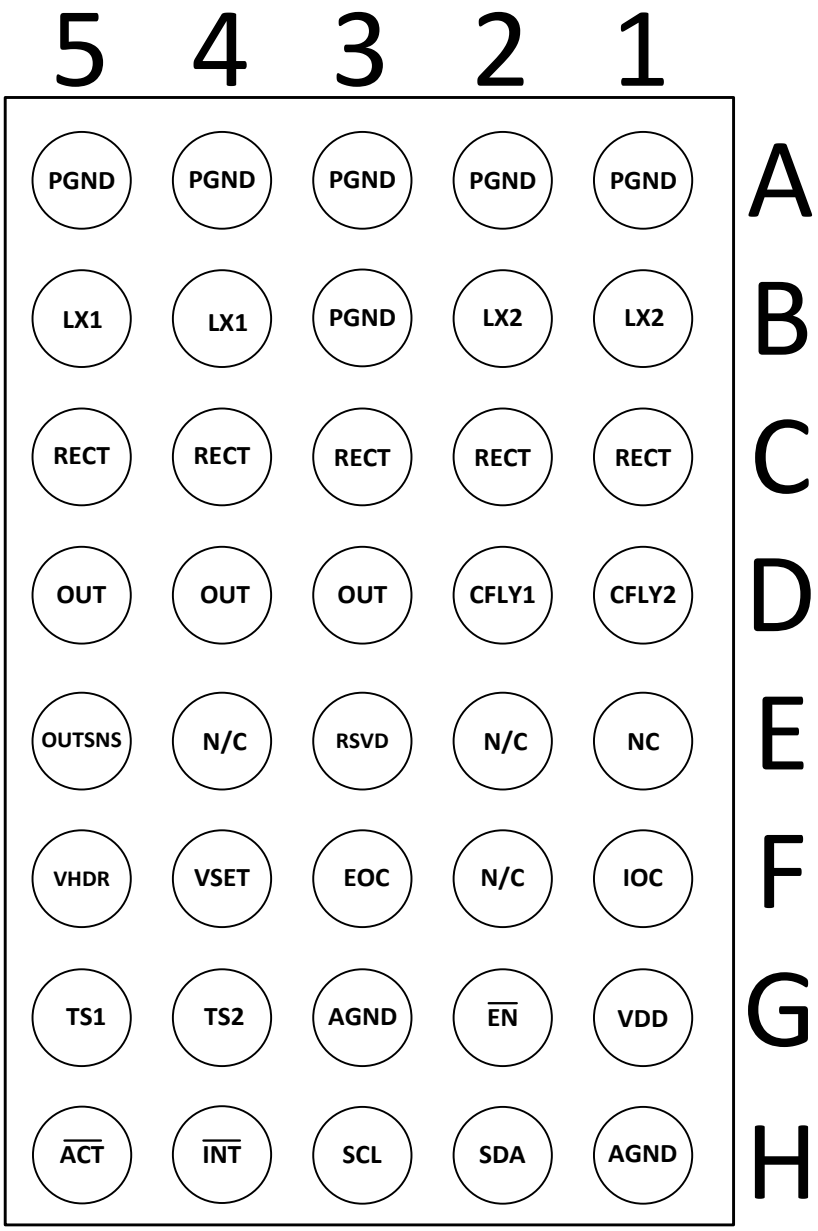
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Figure 8. TSI and TS1 EPTTS1 EPT



Pin Configuration

Figure 9. Pin Configuration



Bottom View

Pin Description

Table 5. Pin Description

Pins	Name	Typical	Description
PGND	A1, A2, A3, A4, A5, B3	GND	Power ground.
LX2	B1, B2	I	Connect the Rx coil to this pin.
LX1	B4, B5	I	Connect the other side of Rx coil to this pin.
RECT	C1, C2, C3, C4, C5	O	Output voltage of the synchronous rectifier bridge. Connect at least two 10 µF capacitors from this pin to PGND. The rectifier voltage dynamically changes as the load changes. See typical curves.
CFLY2	D1	O	Positive and negative terminals of the internal charge pump. Connect a 47 nF capacitor between these two pins.
CFLY1	D2	O	
OUT	D3, D4, D5	O	Regulated output voltage pin. Connect at least two 10 µF capacitors from this pin to PGND. The default voltage is set to 5V when VSET is directly shorted to GND. For more information see VSET application section.
NC	E1, E2, E4, F2	NC	Do not connect.
RSVD	E3	I	This pin is reserved for internal use. Connect a 1.69 KΩ resistor from this pin to GND for 1 W coil. For 2 W and 3 W's coils, use a 1.13 KΩ resistor.
OUTSNS	E5	I	Feedback input pin. This pin must be connected directly to OUT pin to provide a regulated voltage.
IOC	F1	I	Programmable over-current limit pin. Connect a resistor from this pin to GND to set the current-limit threshold. To disable the current-limit, connect the pin directly to GND. For more information see current limit application section.
EOC	F3	I	Active high end of charge input pin. When connected to logic high, the device sends end of power transfer packet (charge complete) to the transmitter to terminate power transfer and shuts down. The OUT pin is high impedance after P9027LP-R is shutdown
VSET	F4	I	Programming pin to set the output voltage. Connect a resistor from the pin to GND to set the output voltage. Shorting the pin to GND sets the output voltage to 5 V. For more information refer to the application section VSET for different output voltage settings.
VHDR	F5	I	Programming pin to set the rectifier voltage. Connect a resistor from the pin to ground. Refer to the application section for appropriate resistor selection.
VDD	G1	O	Charge pumps regulated 5 V supply to power the internal circuitry. Connect a 1 µF capacitor as close as possible from this pin to GND. Do not load the pin.
$\overline{EN}$	G2	I	Active low enable pin. Pulling this pin to logic high forces the device into shutdown mode. When connected to logic low, the device is enabled. Do not leave the pin floating.
AGND	G3, H1	GND	Analog ground.
TS2	G4		Remote temperature sensor 2. If not used, connect to AGND.

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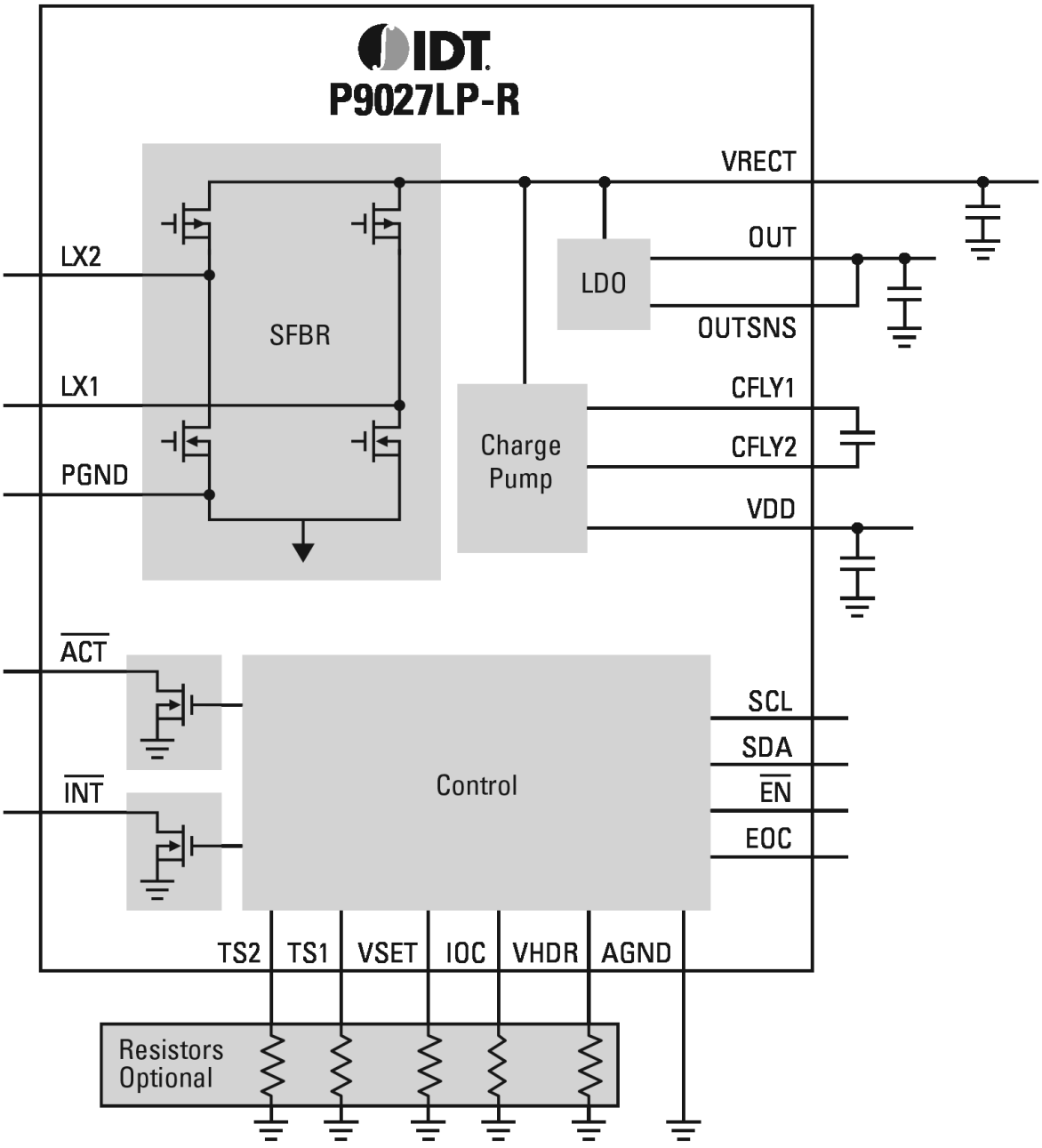
Table 5. Pin Description (Continued)

Pins	Name	Typical	Description
TS1	G5		Remote temperature sensor 1. If not used, connect to AGND.
SDA	H2	I/O	I²C data pin. Open drain output. Connect a 5.1 K resistor from this pin to VDD.
SCL	H3	I	I²C clock pin. Open drain output. Connect a 5.1 K resistor from this pin to VDD.
$\overline{\text{INT}}$	H4	O	Fault interrupt flag pin. It is an open-drain output that signals fault interrupts. It pulls low when EN is high, EOC is high, die temperature reaches 130°C, TS1, or TS2 are triggered.
$\overline{\text{ACT}}$	H5	O	Active flag pin. Open drain output. Connect the cathode of the LED to this pin. When pulled low, it indicates connection between receiver and transmitter is established.

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Functional Block Diagram

Figure 10. Functional Block Diagram



Description of the Wireless Power System

Inductive wireless power transfer involves transmission of energy by changing the magnetic field from a power source to an electrical load, without any connector, across an air gap. The DC power applied to the transmitter (Tx) creates an AC magnetic field in the transmitter coil. Once the receiver (Rx) coil is placed near the magnetic field, the field will induce an AC current through the receiving coil where it is converted into a DC current.

The communication between receiver and the transmitter is accomplished by modulating the load seen by the receiver's inductor. To the transmitter, this appears as an impedance change, which results in measurable variations of the transmitter's output waveform. Modulation is accomplished with AC Modulation, using internal switches from LX1 and LX2 to ground.

The amount of power transferred is controlled by the receiver. The receiver sends communication packets to the transmitter to increase power, decrease power, maintain the power level, or terminate the power transfer. The bit rate for Rx-to-Tx communication link is 2 Kbps. The communication is digital and communication of 1's and 0's is achieved by the Rx modulating the amount of load on the receiver coil.

Theory of Operation

The P9027LP-R wireless power receiver works according to the magnetic induction (MI) principle. The Tx and Rx coils are coupled with a coupling factor between 0.1 and 0.9, and power is transferred through an AC magnetic field.

The P9027LP-R is a highly-integrated wireless power receiver with a maximum output power of 3 Watts. It is designed to convert an AC power signal from a resonant tank into a regulated output voltage. The device includes a high-efficiency synchronous full-bridge rectifier with ultra-low $R_{DS(ON)}$, NMOS LDO, and a charge pump for quick startup under very weak coupling or poor coil alignment. The output voltage is programmable w from 4.5 to 6.0 V. Programming is accomplished with a single external resistor on the VSET pin to ground.

The receiver utilizes IDT's proprietary voltage clamping scheme which limits the maximum voltage at the rectifier pin to 9 V, reducing the voltage rating on the output capacitors while eliminating the need for OVP and communication capacitors. As a result, it provides an extremely small application area, making it an industry-leading wireless power receiver for high power density applications. Together with P9235A-R transmitter, the P9027LP-R is a complete wireless power system solution.

The end of charge (EOC) pin is a logic input, which can be used with application processor or charger IC in battery management applications. When asserted, it sends an end of charge packet to the transmitter, terminating the power transfer and shutting down the device. The electrical on/off of the device is controlled through $\overline{EN}$ pin. When connected to logic high, the device shuts down and consumes minimum current.

Communication Between the P9027LP-R and P9235A-R

When the P9027LP-R is placed on P9235A-R Tx coil, it responds to the transmitter's "ping" signal by rectifying the AC power from the transmitter and storing it on capacitors connected to V_{RECT}. During the "ping" phase, the rectifier provides voltage to the charge pump to supply VDD, and thus, power up the internal control circuitry and logic inside the receiver. To increase the reliability of communication, an internal load of approximately 20 mA is connected to VRECT until the external load is large enough to support communication.

During power up, the P9027LP-R communicates Signal Strength, Identification and Configuration packets to the transmitter, respectively. Once the handshake between Rx and Tx has been established, the wireless power system is in the Power Transfer phase. The control loop of the P9027LP-R then adjusts the rectifier voltage (based on load condition) by sending Control Error Packets instruction to the transmitter. During power delivery to the load, the P9027LP-R control circuit continues to send Control Error Packets to the transmitter to adjust the operating frequency, and thus rectifier voltage, to the level required to maximize the efficiency of the linear regulator.

Over-Voltage Protection

One of the common issues with wireless power receivers is the potential that the transmitter (TX) will transmit more power than the receiver needs or can handle. This can happen when the coupling between the Tx and Rx increases due to a sudden move of the receiver. Because of the slow communication, it may take up to a few seconds before the Tx can adapt its transmitting power, and this may be long enough for the voltage on the LX and RECT pins to increase above the maximum ratings and damage the receiver.

For this reason, the P9027LP-R has over-voltage protection. In most wireless receiver chips, this is implemented by external clamping capacitors. However, the P9027LP-R has implemented this feature internally to save board space and reduce the BOM cost. Furthermore, since the clamping is activated around 8.5 V, the bulk capacitors can have a low voltage rating.

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Charge Pump for Internal Power Supply - VDD

The power supply for the control circuitry in the P9027LP-R is generated by a charge pump. This charge pump requires a 0.47 µF flying capacitor connected between the CFLY1 and CFLY2 terminals. A 1 µF capacitor with a recommended voltage rating of 25 V must be connected from VDD to GND. Adding any external loads to this pin is prohibited as the charge pump output current is limited to 5 mA.

Rectifier Voltage Headroom Setting – VHDR

The rectifier voltage dynamically changes as a function of load when the VHDR resistor is fixed. The reason is to balance power dissipation and dynamic load response. Under the condition of a step load, the wireless power system may not have enough power to respond. This is due to the communication of the Rx-to-Tx feedback loop being relatively slow – where it can take up to several tens of milliseconds for the power required by the receiver to be delivered. Thus, a higher rectifier voltage is preferred to mitigate the step load transient response. On the other hand, a high rectifier voltage will generate more power loss on the LDO. Thus, to meet the requirements of both power dissipation and transient response, the rectifier voltage typically starts at around 6.5V at no load, and it is adjusted to the appropriate value based on the output load once the communication is complete. Figure 11 shows how the rectifier voltage changes with load.

The rectifier voltage is set by connecting a 1% resistor from the VHDR pin to GND. The table below recommends the appropriate resistor value based on system efficiency and transient response when using P9235A-R and P9027LP-R.

Table 6. Resistor Value and Output Current

Resistor Value (KΩ)	Output Current
1.13	0 – 400mA
1.69	400 – 600mA

Rectifier Voltage - RECT

The rectifier output (RECT pin) requires at least a 20 µF ceramic capacitor from the pin to GND to minimize the ripple voltage. It is recommended to use at least either two 10 µF or four 4.7 µF capacitors to reduce the total capacitor ESR.

When selecting a ceramic capacitor, only X5R and X7R dielectric types should be used. Other types such as Z5U and Y5F have such severe loss of capacitance due to effects of temperature variation and applied voltage, they may provide as little as 20% of rated capacitance in many typical applications. Always consult the capacitor manufacturer's data curves before selecting a capacitor.

Setting the Output Voltage - VSET

The P9027LP-R output voltage can be programmed from 4.5 to 6.0 V by connecting a resistor from the VSET pin to GNDx allowing selection from pre-programmed voltages. See the table below for the desired output voltage with an appropriate resistor value.

Table 7. Resistor Value and Output Voltage

Resistor Value (KΩ)	Output Voltage
3.40	4.50
4.22	4.75
GND	5.00
5.36	5.25
6.49	5.50
7.68	5.75
9.09	6.00

Over-Current Limit – IOC

The output over-current (OC) protection mechanism relies on the comparison between the sensed current and the programmed over-current threshold. The over-current threshold is set through a single external resistor, connected between the IOC pin and GND. A pulse 100 µA of current is sourced from the IOC pin to GND. If IOC pin is shorted to GND, the protection is disabled. The LDO output current sensing is

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accomplished internally through sensing circuitry and then digitized by ADC. The current sensing does not vary with the temperature. Refer to the Electrical Characteristic Table for current sense accuracy. The internal current sensing accuracy degrades during light-load conditions.

When the over-current limit is tripped, the P9027LP-R sends End of Power Transfer Over-Current packet (EPT: OC) to the P9235A-R, shutting down the entire system. In the event the transmitter fails to recognize the packet, the receiver will continue sending the EPT: OC packet up to 12 times.

The OC limit is typically set to ~24% higher than maximum load. Please refer to

Table 8 below for different current protection thresholds.

Table 8. Resistor Value, Over-current Setting

Resistor (KΩ)	IOC Limit	Max. Output Current
GND	Disabled	-
2.26	260mA	200mA
6.19	540mA	400mA
9.53	780mA	600mA

Enable pin - $\overline{EN}$

The enable pin ($\overline{EN}$) is an active low logic. When connected to logic high, the receiver shuts down by sending an End of Power Transfer (EPT) packet to P9235A-R and forces the OUT pin to high impedance state. When connected to a logic low, the device operates in normal mode.

Active Flag pin - $\overline{ACT}$

The $\overline{ACT}$ pin is an open drain output indicator. Connect a LED from this pin to OUT to indicate connection between the receiver and the transmitter has been established and the power is being transferred.

Interrupt pin - $\overline{INT}$

The P9027LP-R provides an open-drain, active low interrupt output pin. It is asserted high when $\overline{EN}$ is high, EOC is logic high, die temperature reaches 130°C, TS1 or TS2 and thermal shutdown have been triggered. During normal operation, the $\overline{INT}$ pin is pulled high. This pin can be connected to the interrupt input of a microcontroller. The source of what triggered the interrupt is available in I2 C register.

End of Charge - EOC

The End of Charge feature is a dedicated pin that forces the P9235A-R to terminate power transfer when the EOC is logic high. When EOC is asserted, the device issues an End Power Transfer (EPT) packet to the transmitter terminating all activities by placing P9235A-R into standby mode. The P9235A-R will start digital ping after five minutes or if the P9027LP-R is removed.

Remote Temperature Sensing

The P9027LP has two temperature sensor inputs, TS1 and TS2 that can be used to monitor two remote locations such as the battery and the Rx coil. It is recommended to use an NTC thermistor typical 10 kΩ, depending on the temperature range of interest (0 kΩ – 18 kΩ). The basic characteristic of an NTC thermistor is given below for reference.

$$R = R_0 \exp\left\{B \times \left(\frac{1}{T} - \frac{1}{T_0}\right)\right\}$$

Where:

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T is the temperature in Kelvin.
R_0 is the known resistance at calibration temperature T_0.
B (beta) is the material constant.

The ADC reading of thermistors TS1 and TS2 can be monitored by the I²C interface. The ADC value can be calculated using the thermistor resistance formula and the following:

$$ADC_{TS} = \frac{R \times 100 \times 10^{-6} A}{1.8V} \times 255$$

Recommended Coils

The following coils are recommended with P9027LP-R receiver for 1, 2 and 3 W applications for optimum performance. The recommended vendors have been tested and verified.

Table 9. Coils Recommended with Receiver for 1, 2 and 3 W Applications.

Output Power	Vendor	Part Number	Inductance	DCR	Dimension
1 W	TDK	WR121220-27M8-ID	8.32 uH	0.98 Ω	Ø12 mm
	SunLord	SWA12R12H08C01B	8.50 uH	0.38 Ω	Ø12 mm
2 W	TDK	WR202010-18M8-ID3	11.0 µH	0.40 Ω	Ø20 mm
	Wurth Electronics	760308101220	12.60 µH	0.27 Ω	Ø17 mm
	SunLord	SWA20R20H08C01B	12.0 µH	0.29 Ω	20 mm x 20 mm
3 W	TDK	WR303050-12F5-ID1	8.20 µH	0.30 Ω	30 mm x 30 mm
	Wurth Electronics	760308102213	7.90 µH	0.26 Ω	29 mm x 29 mm
	SunLord	SWA30R30H08C01B	8.20 uH	0.33 Ω	30 mm x 30 mm

PCB Layout Consideration

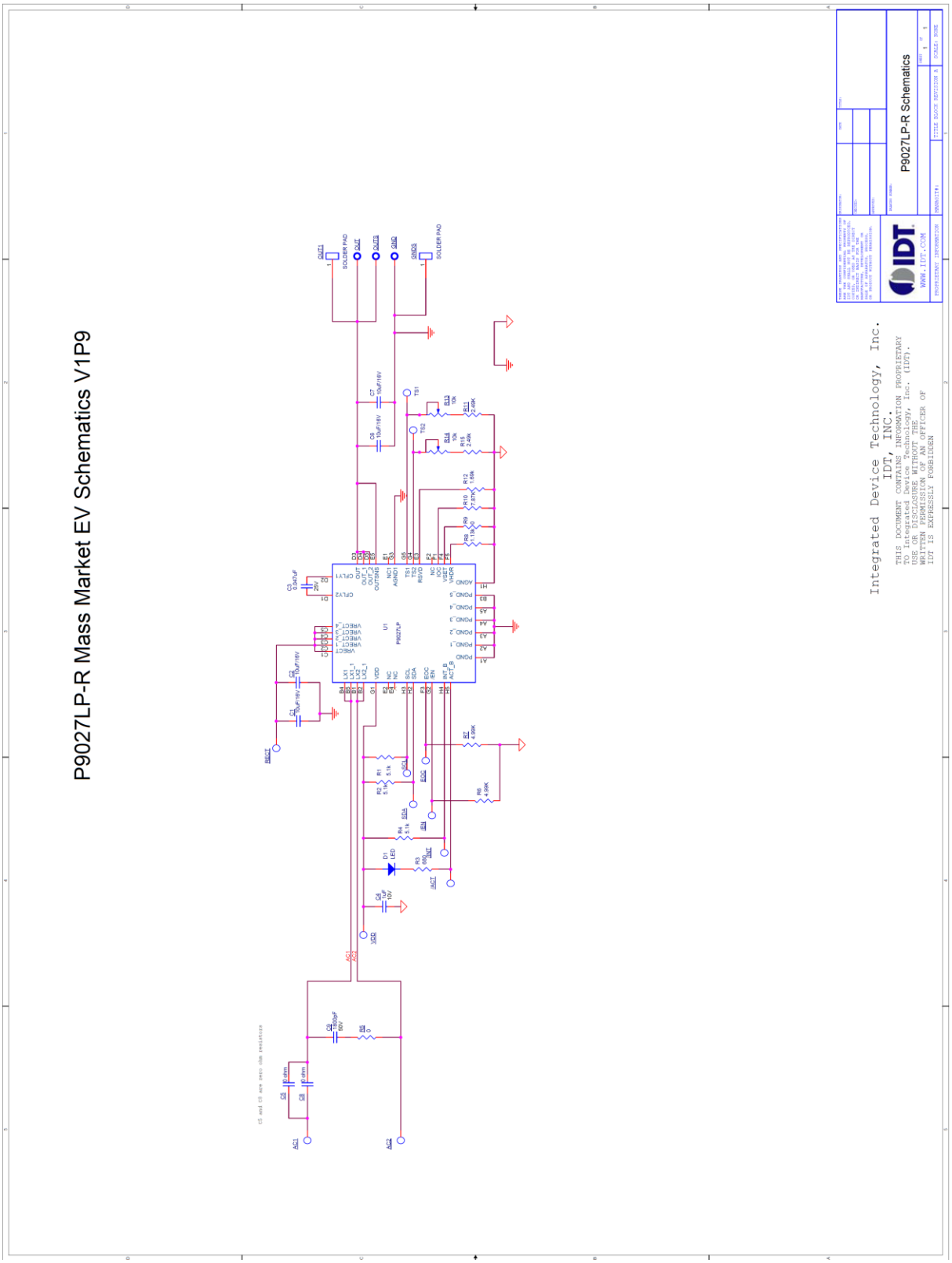
For optimum device performance and lowest output phase noise, IDT recommends that customers copy the reference layout used in the P9027LP-R-EVK reference kit. More information and layout files can be found at http://www.idt.com/WP3W-RK.

Additional layout guidelines can be found in application note AN-933. Users are encouraged to read this document prior to starting a board design.

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Reference Schematic (P9027LP-R-EVK)

Figure 11. P9027LP-R Mass Market EV Schematics



Component Selections

Table 10. Component Selections

Item	Qty	Reference	Description	PCB Footprint	MFG Part Number
1	4	C1, C2, C6, C7	CAP 10 uF/10 V	402	CL05A106MP5NUNC
2	2	C5, C8	RES 0.0 OHM	402	ERJ-2GE0R00X
3	1	C4	CAP 1 UF/25 V	402	C1005X5R1E105M050BC
4	1	C3	CAP 0.047 UF/25 V	402	C1005X7R1E473M050BC
5	1	C9	CAP 1800 PF/50 V	402	GRM155R71H182KA01D
6	2	R1, R2	RES 5.11 k	201	ERJ-1GEF5111C
7	1	R3	RES 680	402	ERJ-2GEJ681X
8	1	R4	RES 5.1 k	402	ERJ-2GEJ512X
9	2	R5, R9	RES 0.0 OHM	201	ERJ-1GE0R00C
10	2	R6, R7	RES 4.99 K	201	ERJ-1GEF4991C
11	1	R8	RES 1.13 K	201	ERJ-1GEF1131C
12	1	R10	RES 7.87 K	201	ERJ-1GEF7871C
13	2	R11, R15	RES 2.49 K	402	ERJ-2RKF2491X
14	1	R12	RES 1.69 K	201	ERJ-1GEF1691C
15	2	R13, R14	Potential meter 10 k	2.2 mm x 2.1 mmx 0.8 mm	PVA2A103A01R00
16	1	D1	LED Indicator	402	LED RED 0402 SMD
17	1	U1	Wireless Power Rx IC	2.24 x 3.62 mm WLCSP, 0.4 mm pitch size	P9027LP-R
18	1	L1	Rx coil	See Table 9	

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I²C Register map

The default I²C slave address is 0x68.

The intent of this register is to identify the device is P9027LP-R.

Table 11. Device Identification

Byte Address	Byte Name	Bit Field	Typical	Default Value	Description
0xFC	Part_number_H	7:0	R/W	0x90	High byte of part number
0xFD	Part_number_L	7:0	R/W	0x27	Low byte of device naming code

This register will provides information about firmware version programmed into the IC.

Table 12. Firmware Version ID

Byte Address	Byte Name	Bit Field	Typical	Default Value	Description
0xFF	CHIP_ID_L	7:0	R	0xAB	Firmware version

All the faults can cause P9027LP-R send EPT (End of Power Transfer) package with different values or pull INT pin high. The faults can be enabled by setting Masked Fault Enable Register. Bit of FLT_RAW will be set if corresponding fault condition is trigged.

Table 13. Masked Fault Enable Register

Byte Address	Byte Name	Bit Field	Typical	Default Value	Description
0xD4	FLT_RAW_15	7	R	0	Reserved.
0xD4	FLT_RAW_14	6	R	0	Reserved.
0xD4	FLT_RAW_13	5	R	0	Reserved
0xD4	FLT_RAW_12	4	R	0	Reserved.
0xD4	FLT_RAW_11	3	R	0	Reserved
0xD4	FLT_RAW_10	2	R	0	Reserved.
0xD4	FLT_RAW_9	1	R	0	Reserved
0xD4	FLT_RAW_8	0	R	0	Reserved
0xD5	FLT_RAW_7	7	R	0	TS2 voltage is above programmed voltage.
0xD5	FLT_RAW_6	6	R	0	TS1 voltage is above programmed voltage.
0xD5	FLT_RAW_5	5	R	0	“1” when die temperature is greater than Tdie_shutdown.
0xD5	FLT_RAW_4	4	R	0	Reserved
0xD5	FLT_RAW_3	3	R	0	Reserved

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0xD5	FLT_RAW_2	2	R	0	“1” when End Of Charge (EOC) pin is set.
0xD5	FLT_RAW_1	1	R	0	Reserved
0xD5	FLT_RAW_0	0	R	0	“1” when enable ($\overline{EN}$) pin is set high.

Enabled fault flag. If the fault condition exists and this fault is enabled in Masked Fault Enable Register, the bit for the fault in FLT_MSKD will be set.

Table 14. Masked Fault Condition

Byte Address	Byte Name	Bit Field	Typical	Default Value	Description
0xD6	FLT_MSKD	7:5	R	0	Reserved.
0xD6	FLT_MSKD	4	R	0	Reserved.
0xD6	FLT_MSKD	3:0	R	0	Reserved
0xD7	FLT_MSKD	7	R	0	TS2 voltage is above programmed voltage. End of power transfer packet sent (0x03) if triggered.
0xD7	FLT_MSKD	6	R	0	TS1 voltage is above programmed voltage. End of power transfer packet sent (0x03) if triggered.
0xD7	FLT_MSKD	5	R	0	“1” when die temperature is greater than Tdie_shutdown. End of power transfer packet sent (0x02) if triggered.
0xD7	FLT_MSKD	4	R	0	Reserved
0xD7	FLT_MSKD	3	R	0	Reserved
0xD7	FLT_MSKD	2	R	0	“1” when End of Charge (EOC) pin is set. End of power transfer packet sent (0x01) if triggered.
0xD7	FLT_MSKD	1	R	0	Reserved
0xD7	FLT_MSKD	0	R	0	“1” when enable ($\overline{EN}$) pin is set high. End of power transfer packet sent (0x02) if triggered.

Enabled fault flag. If the fault condition exists and this fault is enabled in Masked Interrupt Enable Register, the bit for the fault in INTR_MSKD will be set.

Table 15. Masked Interrupt Register

Byte Address	Byte Name	Bit Field	Typical	Default Value	Description
0xD8	INTR_MSKD	7:5	R	0	Reserved.
0xD8	INTR_MSKD	4	R	0	Reserved.
0xD8	INTR_MSKD	3:0	R	0	Reserved
0xD9	INTR_MSKD	7	R	0	TS2 voltage is above programmed voltage, INT pin will be toggled.

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Byte Address	Byte Name	Bit Field	Typical	Default Value	Description
0xD9	INTR_MSKD	6	R	0	TS1 voltage is above programmed voltage, INT pin will be toggled.
0xD9	INTR_MSKD	5	R	0	"1" when die temperature is greater than Tdie_shutdown, INT pin will be toggled.
0xD9	INTR_MSKD	4:3	R	0	Reserved
0xD9	INTR_MSKD	2	R	0	"1" when End Of Charge (EOC) pin is set $\overline{INT}$ pin will be toggled.
0xD9	INTR_MSKD	1	R	0	Reserved
0xD9	INTR_MSKD	0	R	0	"1" when enable ($\overline{EN}$) pin is set high, $\overline{INT}$ pin will be toggled.

Setting 1s in the register enable co-responding fault to send End of Power Transfer.

Table 16. Masked Fault Enable Register

Byte Address	Byte Name	Bit Field	Typical	Default Value	Description
0x00	FLT_MSKD_EN	7:5	R/W	0	Reserved.
0x00	FLT_MSKD_EN	4	R/W	0	Thermal regulation loop is fault enabled send End of Power Packet.
0x00	FLT_MSKD_EN	3:0	R/W	1	Reserved.
0x01	FLT_MSKD_EN	7	R/W	1	TS2 fault is enabled to send End of Power Packet.
0x01	FLT_MSKD_EN	6	R/W	1	TS1 fault is enabled to send End of Power Packet.
0x01	FLT_MSKD_EN	5	R/W	1	Die temperature shutdown is enabled to send End of Power Packet.
0x01	FLT_MSKD_EN	4:3	R/W	1	Reserved.
0x01	FLT_MSKD_EN	2	R/W	1	End of Charge is enabled to send End of Power Packet.
0x01	FLT_MSKD_EN	1	R/W	1	Reserved.
0x01	FLT_MSKD_EN	0	R/W	1	Function to use EN pin to send End of Power Transfer is enabled.

Setting 1s in the register enable co-responding fault to pull high $\overline{INT}$ pin.

Table 17. Masked Interrupt Enable

Byte Address	Byte Name	Bit Field	Typical	Default Value	Description
0x02	INTR_MSKD_EN	7:5	R/W	1	Reserved.
0x02	INTR_MSKD_EN	4	R/W	1	Thermal regulation interrupt is enabled to toggle $\overline{INT}$ pin.

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Byte Address	Byte Name	Bit Field	Typical	Default Value	Description
0x02	INTR_MSKD_EN	3:0	R/W	1	Reserved.
0x03	INTR_MSKD_EN	7	R/W	1	TS2 interrupt is enabled to toggle $\overline{INT}$ pin.
0x03	INTR_MSKD_EN	6	R/W	1	TS1 interrupt is enabled to toggle $\overline{INT}$ pin.
0x03	INTR_MSKD_EN	5	R/W	1	Die temperature Interrupt is enabled to toggle $\overline{INT}$ pin.
0x03	INTR_MSKD_EN	4:3	R/W	1	Reserved.
0x03	INTR_MSKD_EN	2	R/W	1	End of Charge interrupt is enabled to toggle $\overline{INT}$ pin.
0x03	INTR_MSKD_EN	1	R/W	1	Reserved.
0x03	INTR_MSKD_EN	0	R/W	1	Function to use EN pin to pull high $\overline{INT}$ pin is enabled.

When Tdie >= tdie_shdn_off + tdie_shdn_hys , 9027LP-R will shut down.

When Tdie < tdie_shdn_off, die temperature shutdown function is OFF; however 9027LP-R may send EPT to shut down P9235A-R.

If tdie_shdn_off > Tdie > tdie_shdn_off - 10°C , 9027LP-R will send EPT because of die temperature.

If Tdie < tdie_shdn_off - 20°C, no EPT will be sent because of die temperature.

Table 18. Die Temperature Shutdown Register

Byte Address	Byte Name	Bit Field	Typical	Default Value	Description
0x08	TDIE_SHDN_OFF	7	R/W	0	Die temperature shutdown select. "0" : Die temperature shutdown off "1" : 130^{0}C "2" : 140^{0}C "3" : 150^{0}C
0x08	TDIE_SHDN_OFF	6	R/W	1	
0x08	TDIE_SHDN_HYS	5	R/W	1	Die temperature shutdown hysteresis select (Thermal control start temperature = hysteresis + thermal control off temperature) "0" : 10^{0}C "1" : 20^{0}C
0x08	INTR_MSKD_EN	4:0	R/W	0	Reserved.

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Table 19. Output Voltage Setting (VSET)

Byte Address	Byte Name	Bit Field	Typical	Default Value	Description
0x33	VSET_EN	7	R/W	0	VSET (OUT Voltage) set enable "0" : OUT voltage set was disabled, VSET will be set from external resistance on VSET pad. "1": OUT voltage set was enabled, VSET_VALUE will be used for OUT voltage.
0x33	Reserved	6:5	-	-	Reserved.
0x33	VSET_VALUE	4:0	R/W	0	0 : OUT voltage value = 5.00 V 1:5 : Reserved 6 : OUT voltage value = 4.50 V 7, 8 : OUT voltage value = 4.75 V 9, 10 : OUT voltage value = 5.25 V 11, 12 : OUT voltage value = 5.50 V 13, 14 : OUT voltage value = 5.75 V 15, 16, 17 : OUT voltage value = 6.00 V

To have correct temperature information from ADC_TS1 and/or ADC_TS2, the correct value sensing resistor needs to be connected onto TS1 to GND and/or TS2 to GND.

Table 20. Thermistor TS1 and TS2 Register ADC Reading

Address	Register Name	R/W	Default	Function and Description
0x69 [7:0]	TS1 [7:0]	R	-	TS1 (external temperature sensor1) value read (0 ~ 255)
0x6B[7:0]	TS2 [7:0]	R	-	TS2 (external temperature sensor2) value read (0 ~ 255)

Table 21. Operating Frequency Register ADC Reading

Byte Address	Byte Name	Bit Field	Typical	Default Value	Description
0x7 E	Reserved	7:4	X	X	Reserved.
0x7 E	LX_FSW	3:0	R	-	Operating frequency = 1 / (LX_FSW * 3.125 ns)
0x7 F	LX_FSW	7:0	R	-	Operating frequency = 1 / (LX_FSW * 3.125 ns)

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Table 22. Communication Packet Register ADC Reading

Byte Address	Byte Name	Bit Field	Typical	Default Value	Description
0x81	EPT	7:0	R	1	End of Power Transfer Packet parameter value read: 01: Charge Complete. 02: Internal Fault. 03: Over Temperature. 05: Over Current. FF: No fault.
0x82	Reserved	7:0	-	-	Reserved.
0x83	SIGSTR	7:0	R	-	Signal Strength Packet parameter value read.
0x84	Reserved	7:0	-	-	Reserved.
0x85	CTRLERR	7	R	-	Control Error Packet parameter value read.
0x86	Reserved	7:0	-	-	Reserved.
0x87	CHGSTS	7:0	R	1	Charge Status Packet parameter value read.
0x88	Reserved	7:4	-	-	Reserved.
0x88	RCVDPWR	4:0	R	-	Received Power Packet parameter value read (12-bit) : 2.44 mW unit @5W system. Normally only MSB 8-bits [11:4] are used for this parameter: 39.04 mW unit.
0x89	RCVDPWR	7:0	R	-	

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Package Information

Figure 12. WLCSP Landing Pattern (AWG40)

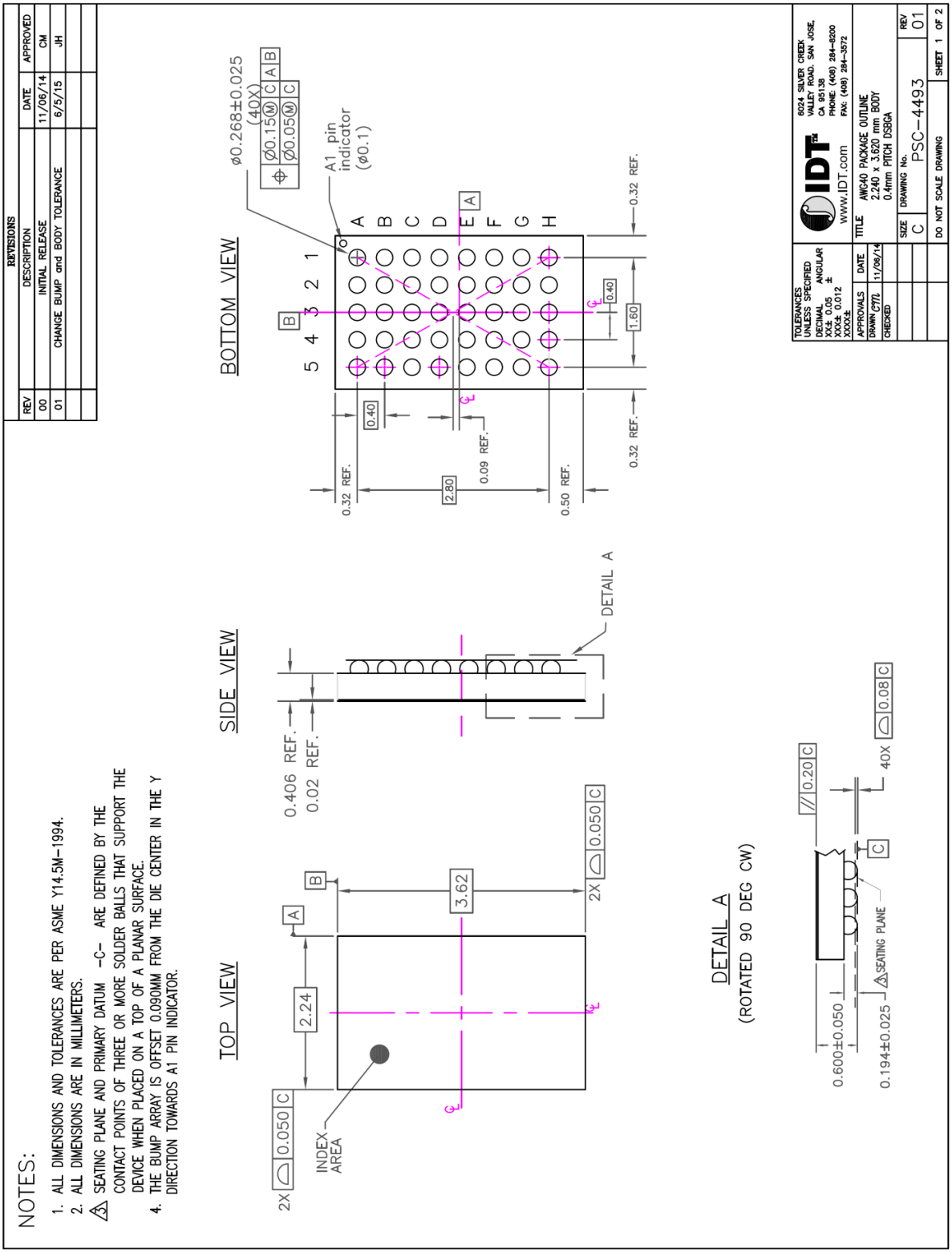
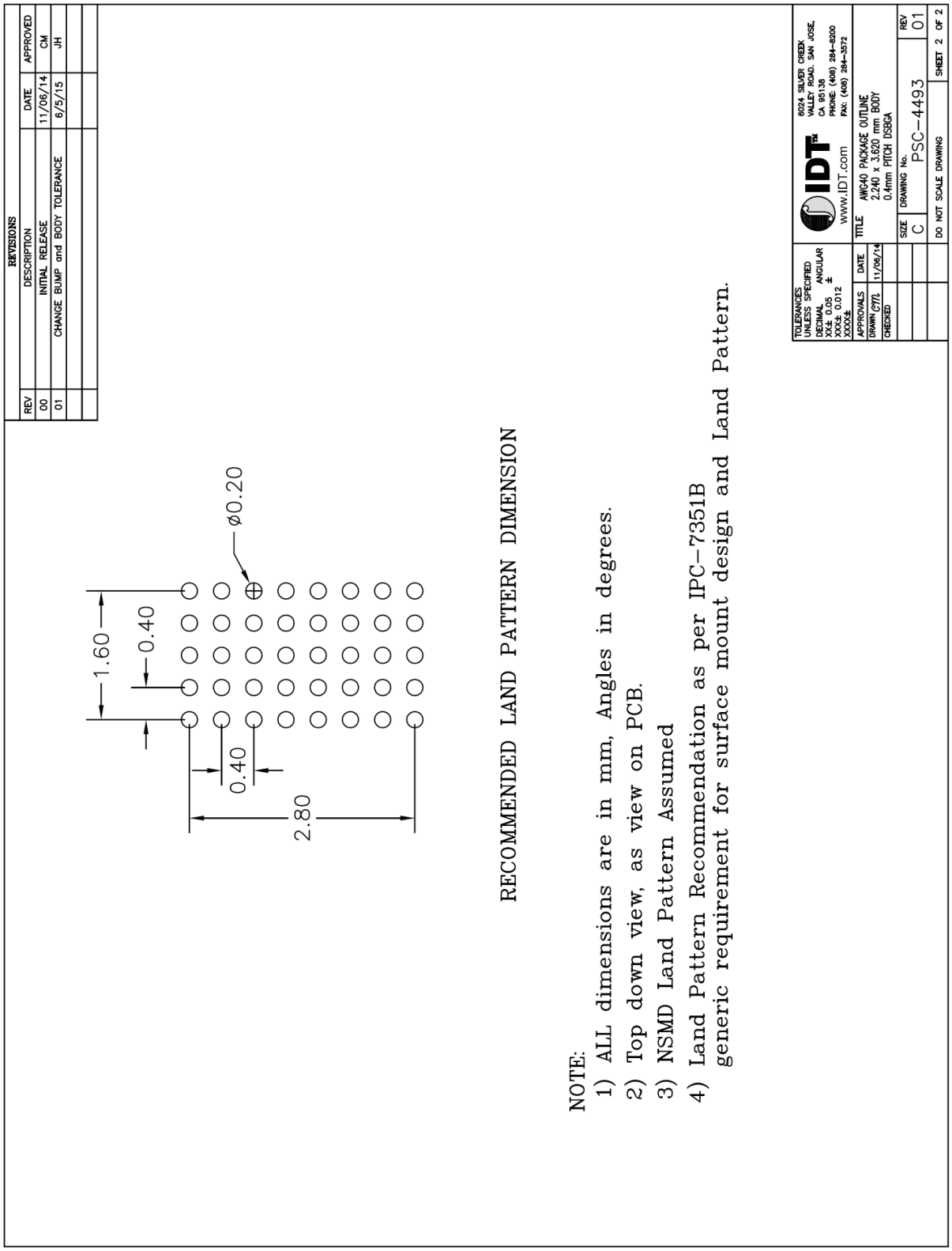


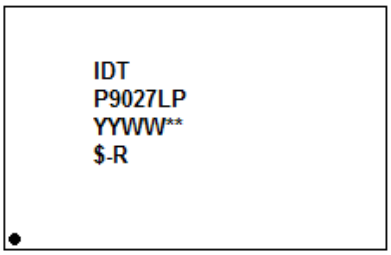
Figure 13. WLCSP Package Outline Drawing (AWG40)



Ordering Information

Orderable Part Number	Package	MSL Rating	Shipping Packaging	Temperature
P9027LP-RAWGI8	WLCSP-40	1	Tape and Reel	0°C to +85°C

Marking Diagram



1. Company name
2. Truncated part number
3. “YWW” is the year and week that the part was assembled.
4. $ is mark code, -R is part of the device part number

Revision History

Revision Date	Description of Change
April 28, 2016	Original release of the P9027LP-R datasheet.

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