Dual Channel Synchronous Step-Down Switcher with Integrated FET

Advanced Datasheet

IDTP9122

Features

- **Input Voltage Range: 2.7V to 5.5V**
- **Two step-down converters with integrated FETs**
  - **Buck1: 2A**
  - **Buck2: 3A**
- **Buck 2 to operate in Buck or Switch mode**
- **Factory Programmable Output Voltage: 0.8 - 3.4V**
- **Automatic PFM/PWM or forced PWM mode**
- **Switching frequency 2MHz**
- **Optional Programmable Sequence Mode**
- **Power Good and/or Power On Reset Output**
- **-40°C to +85°C operating temperature range**
- **Package: QFN 24-ld 4 x 4mm x 0.8mm**

Applications

Point of Load Regulation in a variety of low power applications:

- **Solid State Disk Drive (SSD) Power Management**
- **Low Power USB powered applications**
- **Set Top Box / TV Power Supply**
- **Portable Gaming**

Description

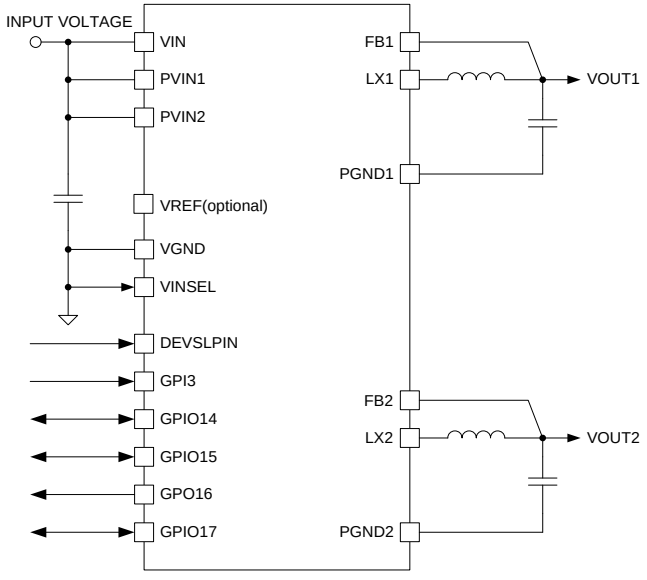
IDTP9122 is a fully integrated power management IC designed to provide 2 factory programmable voltage rails from a single 5V or 3.3V input rail with high efficiency and low quiescent currents in sleep mode or no-load condition.

The device offers selectable direct buck enable inputs or a factory programmable sequencing with power good and power on reset generation.

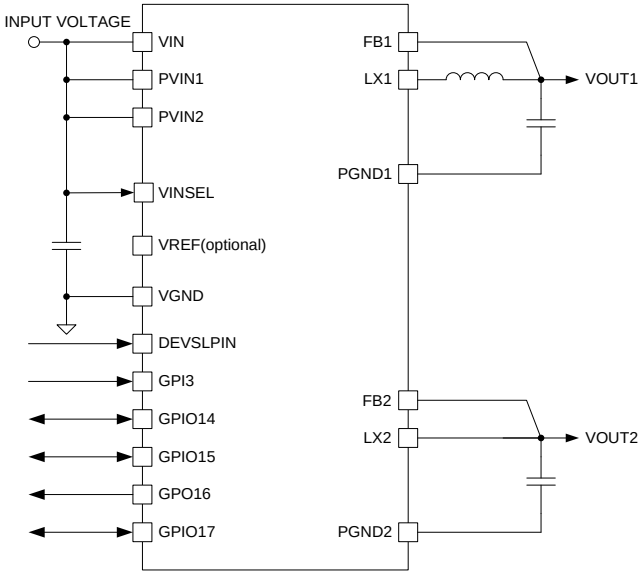
To support low power standby operation, the IDTP9122 supports a configurable sleep mode.

The IDTP9122 is available in a 4mm x 4mm, 24-ld, QFN package and guaranteed to operate over the ambient temperature range -40°C to +85°C.

Simplified Application Diagram



IDTP9122 with VINSEL (pin 4) in Buck Configuration for VOUT2



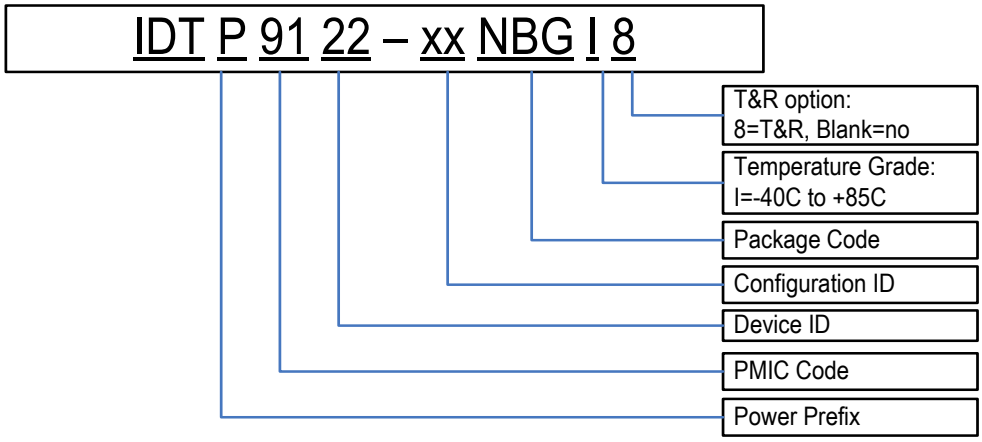
IDTP9122 with VINSEL (pin 4) in Switch Configuration for VOUT2

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ORDERING GUIDE

Table 1 – Ordering Summary

PART NUMBER	MARKING	PACKAGE	AMBIENT TEMP. RANGE	SHIPPING CARRIER	QUANTITY
P9122-00NBGI	P9122-00NBGI	QFN-24 4x4x0.75mm 24-ld	-40°C to +85°C	Tape or Canister	490
P9122-xxNBGI	P9122-xxNBGI	QFN-24 4x4x0.75mm 24-ld	-40°C to +85°C	Tape or Canister	490
P9122-xxNBGI8	P9122-xxNBGI	QFN-24 4x4x0.75mm 24-ld	-40°C to +85°C	Tape and Reel	4000



Additional Ordering Information:

The IDTP9122 will be sampled in "-00" configuration, with all user configurable OTP registers at default state (0). Once a final customer configuration has been defined, a configuration specific "-xx" ID will be assigned and used for order and marking.

ABSOLUTE MAXIMUM RATINGS

Stresses above the ratings listed below can cause permanent damage to the IDTP9122. These ratings are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Table 2 – Absolute Maximum Ratings

SYMBOL	PARAMETER	MIN	MAX	UNIT
PVIN1, PVIN2 to PGND	Regulator input voltage	-0.3	6.0	V
VIN to GND	Supply for device	-0.3	6.0	V
LX1, LX2	Regulator Switch Nodes	-0.3	6.0	V
FB1, FB2	Regulator Feedback pins	-0.3	3.6	V
All other pins		-0.3	6.0	V
T_J	Operating Junction Temperature		125	°C
T_S	Storage Temperature		150	°C
T_{SOLDER}	Soldering Temperature (10 seconds)		260	°C
P_D	Power Dissipation (T_A = 25°C)		2.5	W

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Table 3- Package Thermal Resistivity

SYMBOL	DESCRIPTION	CONDITIONS	Value	Units
θ_{JA}	Thermal Resistance (QFN-24)	Junction to Ambient	40	°C/W
Ψ_{JB}	Thermal Characterization Parameter (QFN-24)	Junction to Board	23	°C/W
P_D	Maximum Package Power Dissipation		1	W
ESD Rating	(HBM) Human Body Model (all pins except 20, 21)	±2000V		
	(HBM) Human Body Model (only pins 20, 21)	± 500V		
	(CDM) Charged Device Model (all pins)	± 500V		

Per JEDEC spec, the QFN-24 package is rated at MSL3. This thermal rating was calculated based on a JEDEC standard 4-layer board with dimensions 3in x 4.5in in still air conditions. Actual thermal resistance will be affected by PCB size, solder joint quality, PCB layer count, copper thickness, air flow, altitude, and other unlisted variables. For the QFN-24 package, the 2.8mm X 2.8mm EP is connected to ground plane with a matrix of 3x3 PCB thermal VIAs plated through from Top to Bottom layers. Actual thermal resistance will be affected by PCB size, solder joint quality, PCB layer count, copper thickness, air flow, altitude, and other unlisted variables.

ELECTRICAL CHARACTERISTICS

Table 4 – General Electrical Characteristics

Typical values at 25°C, unless noted. V_{PVIN1} = V_{PVIN2} = Vin= 5V. $C_{O(BUCK1)}$ = 10uF, $C_{O(BUCK2)}$ = 20µF, L1 = L2 = 1.0µH.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{VIN}	Input voltage range		2.7		5.5	V
	UVLO threshold, VIN rising	VINSEL>1V, Buck2 in Switch (3.3V) Mode	2.95	3	3.05	V
	UVLO threshold, VIN falling		2.65	2.7	2.75	V
	UVLO threshold, VIN rising	VINSEL=0V, Buck2 in Buck (5V) Mode	4.35	4.4	4.45	V
	UVLO threshold, VIN falling		3.95	4.0	4.05	V
$I_{Q(VIN)}$	VIN quiescent current	Device in sleep mode		<1		µA
		Device in active mode, all Bucks = OFF		100		µA
V_{IL}	Low Level Input Voltage	All inputs	0.65	0.85		V
V_{IH}	High Level Input Voltage	All inputs		1.25	1.45	V
I_{PD}	Pull Down Current	GPIO14,15,17, and GPI3		1		µA
I_{PU}	Pull Up Current	DEVSLPIN @ VIN=5V	5	8	10	µA
R_{PU}	Selectable Pull Up Resistor	Optional for GPIO14,15,16,17 and GPI3		50		kΩ
T_{SD}	Thermal Shutdown			135		°C
V_{PG}	PG Detection Threshold	% of selected output voltage in Buck Mode, % of V_{PVIN2} in Switch mode		10		%
I_{OD}	Max Drive Output	In push-pull configuration, V_{OL}=0.4V, V_{FBx} ≥ 1.8V	4			mA
		In open drain configuration, V_{OL}=0.4V	12			mA
V_{REF}	Reference Voltage Output Voltage			$V_{FB(BUCK1)}$/2		V
C_{VREF}	Output Capacitor V_{REF}			0.1		µF
I_{VREF}	Reference Voltage Output Current				1.0	mA

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ELECTRICAL CHARACTERISTICS

Table 5 – Buck1 Electrical Characteristics

$V_{O(BUCK1)}$ = 1.8V.

Typical values at 25°C, unless noted. V_{PVIN1} = V_{PVIN2} = Vin= 5V. $C_{O(BUCK1)}$ = 10uF, $C_{O(BUCK2)}$ = 20µF, L1 = L2 = 1.0µH.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{PVIN1}	Input voltage range		2.7		5.5	V
$V_{O(BUCK1)}$	Output voltage range		0.8		3.4	V
	Regulation voltage accuracy		-2		2	%
	Line Regulation	V_{PVIN1} = 3.0V to 5V		0.01	0.04	%/V
	Load Regulation	I_{OUT1} = 0.2A to 2A, PWM mode			0.5	mV/A
	Offset voltage in PFM mode $V_{O(PFM)} = V_{O(PWM)} + V_{offset}$	PFM mode		15		mV
$I_{SHDN(BUCK1)}$	Shutdown current	GBD		1		µA
$I_{Q(BUCK1)}$	Quiescent Current	No load, PFM mode		25		µA
$I_{OP(BUCK1)}$	Continuous operating DC current	T_J < 115°C			1.8	A
$I_{LIM(BUCK1)}$	Current Limitation		2	2.5		A
$R_{(on)}$	High side switch			110	153	mΩ
	Low side switch			56	78	mΩ
$R_{DIS(BUCK1)}$	Output discharge resistance		500	650	900	Ω
$f_{SW(BUCK1)}$	Switching frequency	PWM mode	1.89	2	2.1	MHz
$T_{ssr(BUCK1)}$	Soft-start ramp rate		4	8	12	mV/µs
I_{FB1}	FB1 input bias current			6	8	µA
$C_{O(BUCK1)}$	Output Capacitor			10		µF
$L_{O(BUCK1)}$	Output Inductor			1		µH

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ELECTRICAL CHARACTERISTICS

Table 6– Buck2 –Electrical Characteristics

$V_{O(BUCK2)}$ = 3.3V

Typical values at 25°C, unless noted. V_{PVIN1} = V_{PVIN2} = Vin= 5V. $C_{O(BUCK1)}$ = 10uF, $C_{O(BUCK2)}$ = 20µF, L1 = L2 = 1.0µH.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
In Buck Mode (VINSEL=LOW)						
V_{PVIN2}	Input voltage range		2.7		5.5	V
$V_{O(BUCK2)}$	Output voltage range		0.8		3.4	V
	Regulation voltage accuracy		-2		2	%
	Line Regulation	V_{PVIN2} = 3.6V to 5V		0.01	0.15	%/V
	Load Regulation	I_{OUT2} = 0.2A to 2.4A, PWM mode		0.4	0.5	mV/A
	Offset voltage in PFM mode $V_{O(PFM)} = V_{O(PWM)} + V_{offset}$	PFM mode		15		mV
$I_{SHDN(BUCK2)}$	Shutdown current			1		µA
$I_{Q(BUCK2)}$	Quiescent Current	No load, PFM mode		28		µA
$I_{OP(BUCK2)}$	Continuous operating DC current	T_J < 115°C			2.3	A
$I_{LIM(BUCK2)}$	Peak Inductor Current		2.6	3		A
$R_{(on)}$	High side switch			64	93	mΩ
	Low side switch			45	61	mΩ
$R_{DIS(BUCK2)}$	Output discharge resistance		500	650	900	Ω
$f_{SW(BUCK2)}$	Switching frequency	PWM mode	1.89	2	2.1	MHz
$T_{ssr(BUCK2)}$	Soft-start ramp rate			8	12	mV/µs
I_{FB2}	FB2 input bias current			9	11	µA
$C_{O(BUCK2)}$	Output Capacitor			20		µF
$L_{O(BUCK2)}$	Output Inductor			1		µH
In Switch Mode (VINSEL=HIGH), $C_{O(BUCK2)}$ = 10µF, V_{PVIN2} = 3.3V						
V_{PVIN2}	Input voltage range		2.7		3.6	V
$I_{SHDN(BUCK2)}$	Shutdown current			1		µA
$I_{Q(BUCK2)}$	Quiescent Current	No load		10		µA
$I_{OP(BUCK2)}$	Continuous operating DC current	T_J < 115°C			2.4	A
$I_{LIM(BUCK2)}$	Current Limitation		2.8	3		A
$R_{(on)}$	High side switch			64	93	mΩ
$R_{DIS(BUCK2)}$	Output discharge resistance		300		800	Ω
$T_{ssr(BUCK2)}$	Soft-start ramp rate			16		mV/µs
$C_{O(BUCK2)}$	Output Capacitor			2		µF

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PIN CONFIGURATION AND DESCRIPTION

Table 7 – Pin Functions by Pin Number

#	Label	Type	Description
1	VGND	GND	Device ground connection
2	VREF	A	Reference output [VREF=VOUT(Buck 1)/2]
3	GPI3	DI	General Purpose Input (see Modes of Operation, page 7, Master Enable Pin when configured.)
4	VINSEL	DI	Logic input to select function of Buck 2. Logic Low = Buck operation, High = Switch operation.
5	DEVSLPIN	DI	Logic input to activate sleep mode. Logic Low = Normal “on” operation, High = Sleep operation.
6	FB1	A	Feedback connection for Buck 1
7	LX1	A	Inductor connection for Buck 1
8	PGND1	GND	Power ground for Buck 1
9	PVIN1	PWR	Power supply input for Buck 1
10	VIN	PWR	Device supply input
11	VGND	VGND	Device ground connection
12	N/C	N/C	Pin must be left floating/open
13	VGND	VGND	Device ground connection
14	GPIO14	DIO	General Purpose Input / Output (see Modes of Operation, page 7).
15	GPIO15	DIO	General Purpose Input / Output (see Modes of Operation, page 7).
16	GPO16	DO	General Purpose Output (see Modes of Operation, page 7).
17	GPIO17	DIO	General Purpose Input / Output (see Modes of Operation, page 7).
18	FB2	A	Feedback connection for Buck 2 (Buck Mode) or Output (Switch Mode)
19	PGND2	GND	Power ground Buck 2
20	LX2	A	Inductor connection Buck 2 (Buck Mode) or Output (Switch Mode)
21	LX2	A	
22	PVIN2	PWR	Power supply input for Buck 2
23	PVIN2	PWR	
24	VIN	PWR	Device supply input
EP	EP	GND	Exposed pad, connect to heat sink ground plane

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FUNCTIONAL DESCRIPTION:

Overview

The IDTP9122 support several modes to control the 2 Buck regulators and to generate status information like PG (power good) or POR (power on reset).

Various device features can be configured during production using one time programmable fuse memory (OTP). During evaluation, the options can be evaluated using the IDTP9122 Evaluation Kit (IDTP9122-EVAL).

The IDTP9122 OTP memory is organized into four fuse banks with 34 bits each. Bank0 and 1 are used for IDT internal trimming and calibration. Bank2 and 3 are used for customer specific device configuration.

Modes of Operation

Device Power States

Device operates in three basic power states controlled by the DEVSLPIN pin and one optional state (standby) when in Mode 3.

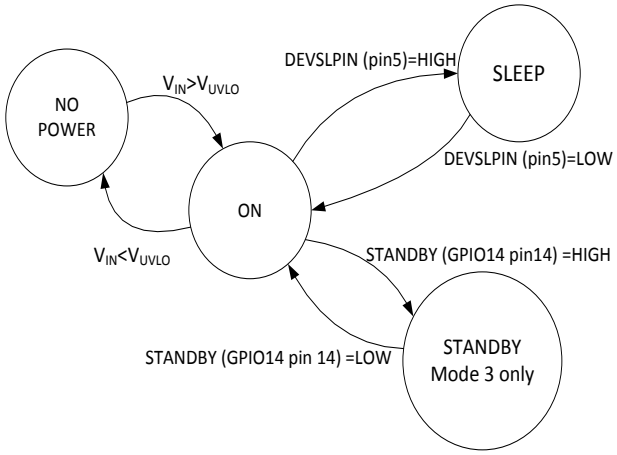


Figure 1. Device Power States

Regulator Control Options (Mode 0..3)

The IDTP9122 supports four different control options for the Buck regulator. The functionality of GPI3, GPIO14,15,16, and 17, and is different for each of the options. (MODE[1:0] = OTP Bank3[1:0])

Table 8 – Buck Control Options

MODE[1:0]	DESCRIPTION	GPI3	GPIO14	GPIO15	GPO16	GPIO17
0 (Default)	Buck regulators controlled by individual enable pins (EN1, EN2)	NC	EN1	GND	PORB	EN2
1	Do not use - reserved					
2	Buck regulators controlled by master enable pin (MEN) w/ sequence	MEN	PORB	PG1	NC	PG2
3	Buck regulators controlled by master enable pin (MEN) w/ sequence and standby mode support	MEN	STANDBY	PG1	NC	PG2/PORB

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Mode0 – Individual Buck control

With IDTP9122 configured for mode0, both regulators are individually controlled via ENx input pin. The PORB output can be configured to indicate various power up conditions.

Mode1 – Do not use - reserved

Mode2 – Master Enable pin (MEN) with sequence

With IDTP9122 configured for mode2, a configurable state machine will ramp up/down both regulators controlled by the MEN pin. The PORB output can be configured to indicate various power up conditions. Individual Power Good output pins indicate the regulator output being established.

Mode3 – Master Enable pin (MEN) with sequence and Standby Mode

With IDTP9122 configured for mode3, a configurable state machine will ramp up/down both regulators controlled by the MEN pin. The PORB output can be configured to indicate various power up conditions. Individual Power Good output pins indicate the regulator output being established.

In addition to mode2, mode3 supports the STANDBY mode entered by asserting the STANDBY pin. During standby, Buck1 and/or 2 will be turned off without sequencing. The configuration is configurable via OTP.

Pin Description

DEVSLPIN

This pin allows the IC to enter and exit SLEEP mode. Sleep mode is the lowest power state of the device and is activated when DEVSLPIN is logic HIGH. The device will be on “normal operation” when DEVSLPIN is logic LOW. See figure 2 – Device Power States.

VINSEL

This pin allows the function of Buck 2 to be changed to a Switch function. Logic LOW on this pin puts the channel into Buck configuration, and a Logic HIGH on this pin puts the channel into Switch configuration.

PVIN1, PVIN2

PVINx is each buck converters’ respective power supply input. They provide power to the internal MOSFETs for the switch mode regulator. Their operating range is 2.7V to 5.5V, and a 10uF capacitor is be placed as close as possible to each of the respective pins. An second 10uF capacitor should be used with PVIN2 because of the greater current sourcing capability of this channel. Because capacitance derates with voltage, a 10V rated X7R ceramic capacitors be used. X7R is preferred over X5R because the derating with X7R is less. For best performance, each of these power supply inputs are to be connected together on a dedicated circuit board power plane, and that the trace going from these pins to the dedicated power plane be made as short as possible. Y5V capacitors are not recommended because of their general low performance with respect to temperature, voltage derating, and higher resistance at high frequency’s minimizing their ability to filter out high frequency noise.

VIN

VIN is the power supply input for the rest of the integrated circuit. It too has an operating range of 2.7V to 5.5V, and a 2.2uF 10V rated X7R capacitor should be placed as close as possible to its’ pin. VIN should also be tied to the same power plane that the PVINx pins are tied to with as short a trace as possible. Y5V capacitors are highly not recommended.

PGND1, PGND2

These are the dedicated ground pins for each of the respective power supply’s. The traces from these pins, to a dedicated ground plane, should be made as short as possible.

VGND

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VGND is the ground pin for the rest of the integrated circuit. The trace from this pin, to a dedicated ground plane, should be made as short as possible.

EP

This is the exposed pad on the bottom side of the IC. It needs to be connected to a circuit board ground plane to maximize the heat dissipation performance of the IC.

VREF

The Vref pin is an internal voltage reference of the IC. It tracks the output voltage of Buck 1, at half its' value. This voltage could be used to interface to the negative input of a comparator as in Li-Ion low battery indicator applications, when the positive input of the comparator is a voltage divided level from the battery's positive node. At the moment of low battery indication, the comparator's output changes state from high to low, thereby, indicating a low battery state, and in turn, for example, then allows an electronic system to begin power down operations. A 2.2uF 6.3V rated X7R capacitor is recommended at this pin.

FB1, FB2

FB1 and FB2 are the respective feedback pins of the output voltage for each buck converter. It is the control input for programming the output voltage of each buck converter. Because of the IDTP9122's output voltage programmability, the classical resistor divider network is no longer needed, thereby saving six resistor components. The granularity of programmability of the outputs for each channel is 25mV all the way from 0.8000V to 3.3375V. During layout, the feedback traces should be kept as short as possible and should never run parallel to the inductors and the inductor trace leading to the inductor switching pin. Feedback traces should always cross inductor's and inductor traces on separate planes and at right angles.

LX1, LX2

LX1, LX2 are the switching pins of the respective buck converters. Small footprint chip inductors of 1uH in value have been optimized for use with the IDTP9122, and connect to the switching pings. The inductors should be placed as close as possible to the LX pins themselves.

GPIO14, GPIO15, GPIO17

These three pins have multiple function, but in the default state they serve as enable pins for each of the three buck converters accordingly:

GPIO14 enables Buck 1. Logic High enables Buck 1. Logic Low disables Buck 1. See Table 9 for alternate mode function.
GPIO15 See Table 9 for alternate mode function.
GPIO16 enables Buck 2. Logic High enables Buck 2. Logic Low disables Buck 2. See Table 9 for alternate mode function.

GPI3

This pin serves no function in default configuration, but when in Mode 2 or Mode 3 configuration, it serves as a master enable pin. I.e., this pin alone will enable all bucks by the change in logic state on its' pin. Logic High enables all the bucks with sequencing of all the bucks, and Logic Low disables all the Bucks with sequencing of all the bucks. See Table 9 for details of GPIO14, GPIO15, GPO16, GOIO17 functionality when the GPI3 pin is configured.

GPO16

This pin serves as a Power on Reset pin or as a Buck 2 Power Good pin depending up whether the device is in Mode 0 or Mode 2 and mode 3 respectively. See Table 9 for alternate mode function.

Component Selection

The IDTP9122 is a high performance dual DC-DC step down convertor that minimizes the solution size demands of miniature portable electronic devices. It supports 2 outputs with currents up to 3A inside a 4mm x 4mm QFN package, and only requires 3 external components per channel (Cin, Cout, L). Because it is designed to automatically switch to a pulse frequency modulation scheme at light loads, the IDTP9122 is able to maintain high efficiency across the entire load range while providing ultra-fast load transient response.

Input Capacitor

A 10uF ceramic capacitor or greater should be placed close to each PVIN pin for each channel for bypassing. Its' voltage rating should be 10V to accommodate any high frequency noise coming from 5V power supply source. The Kemet 0805C106K8RACTU is ideal based

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upon performance, cost, and size. For the VIN pin, a 2.2uF 10V capacitor is sufficient because the VIN pin is powering the low power internal circuitry of the IC.

Output Capacitor

A 10uF or greater ceramic capacitor should be placed close to each output inductor. Increasing the output capacitance will lower output ripple and improve load transient response but could also increase solution size or cost. The voltage rating of the output capacitor should be 6.3V and the C1206C106K9RACTU is recommended, but for more demanding space constrained designs, the Samsung CL10B106MQ8NRNC is a good alternative.

Inductor Selection

The IDTP9122 has been designed for use with a 1.0uH inductor. A larger inductor will produce lower output voltage ripple, but a slightly smaller inductor will produce faster transient response. The best compromise is a 1.0uH inductor. Selection of the inductor needs to ensure maximum operating current not just the DC current, and can be rated for a 40°C temperature rise. This maximum operating current or peak current for a buck converter can be calculated using equation 1

Ipeak = Iout [1 + r/2] eq (1); where r is the inductor current ripple ratio and equal to
r = [Vout (1 – Vout/Vin)] / [Iout * L * f] eq (2); where L and f are the inductor and switching frequency. Simplifying gives equation 3:
Ipeak = Iout + Vout [(1-Vout/Vin) / 2Lf)] eq (3).

Equation 3 shows that the peak inductor current is inversely related to the switching frequency and inductance. In other words, the lower the switching frequency or inductance, the higher the peak current. Peak current also increases as input voltage increases. The size of the inductor depends on the application, and the recommended inductor is the Toko 1239AS-H-1R0M for best performance, size, and cost.

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OTP Register Mapping (Bank T2)

The following table lists all configurable OTP registers available in the IDTP9122. Bank0 and Bank1 are IDT internal use only trimming and calibration registers and not listed.

The registers can be programmed for evaluation purpose using the IDTP9122 Evaluation Kit (IDTP9122-EVAL) with the included GUI software. The final production configuration will be programmed by IDT during final test.

Trim Bits	Parametric Trim
T2[0]	Buck1 Transconductance Selection: Relevant for all modes 0 : Nominal 1 : 3x transconductance
T2[1]	Buck1 Bandwidth Selection: Relevant for all modes 0 : Nominal 1 : 2x bandwidth
T2[2]	Buck1 Forced PWM Mode: Relevant for all modes 0 : Auto-switching between PWM & PFM modes 1 : Forced PWM mode
T2[5:3]	reserved
T2[6]	Buck2 Transconductance Selection: 0 : Nominal 1 : 3x transconductance
T2[7]	Buck2 Bandwidth Selection: 0 : Nominal 1 : 2x bandwidth
T2[8]	Buck2 Forced PWM Mode: 0 : Auto-switching between PWM & PFM modes 1 : Forced PWM mode
T2[10:9]	Power-Off Sequencer Delay 1: Relevant only when mode[1:0]≠'00' 00 : 0.5ms 01 : 1ms 10 : 2ms 11 : 4ms
T2[12:11]	Power-Off Sequencer Delay 2: Relevant only when mode[1:0]≠'00' 00 : 0.5ms 01 : 1ms 10 : 2ms 11 : 4ms

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Trim Bits	Parametric Trim
T2[15:13]	Buck Power-Off Sequence Selection: Relevant only when mode[1:0]≠'00' 000 : wait → Buck2 → Buck1 001 : wait → Buck1 → Buck2 010 : Buck1 → wait → Buck2 011 : Buck1 → Buck2 → wait 100 : Buck2 → Buck1 → wait 101 : Buck2 → wait → Buck1 110 : Buck1 → Buck2 111 : wait → Buck1 & Buck2
T2[18:16]	PORB Output Boolean Operator Selection: PG=Power Good 000 : reserved 001 : PG1 010 : reserved 011 : PG2 100 : reserved 101 : PG1 & PG2 110 : reserved 111 : reserved
T2[19]	GPI3 Internal Pull-up Enable: 0 : Disable (1μA pull-down to VGND) 1 : Enable (100kΩ pull-up to VIN)
T2[20]	Unused
T2[21]	GPIO14 Internal Pull-up Enable: 0 : Disable (1μA pull-down to VGND when pin configured as input) 1 : Enable (50kΩ pull-up to supply voltage selected by gpio14_vio)
T2[22]	GPIO14 Open-Drain Output Select: Relevant only when pin configured as output. 0 : Push-pull output 1 : Open-drain output
T2[23]	GPIO14 I/O Voltage Select: For both input buffer and push-pull output driver. 0 : VOUT2 (FB2) 1 : VOUT1 (FB1)
T2[24]	GPIO15 Internal Pull-up Enable: 0 : Disable (1μA pull-down to VGND when pin configured as input) 1 : Enable (50kΩ pull-up to supply voltage selected by gpio15_vio)
T2[25]	GPIO15 Open-Drain Output Select: Relevant only when pin configured as output. 0 : Push-pull output 1 : Open-drain output
T2[26]	GPIO15 I/O Voltage Select: For both input buffer and push-pull output driver. 0 : VOUT2 (FB2) 1 : VOUT1 (FB1)
T2[27]	GPO16 Internal Pull-up Enable: 0 : Disable 1 : Enable (50kΩ pull-up to supply voltage selected by gpo16_vo)

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T2[28]	GPO16 Open-Drain Output Select: 0 : Push-pull output 1 : Open-drain output
T2[29]	GPO16 Output Voltage Select: For push-pull output driver. 0 : VOUT2 (FB2) 1 : VOUT1 (FB1)
T2[30]	GPIO17 Internal Pull-up Enable: 0 : Disable (1μA pull-down to VGND when pin configured as input) 1 : Enable (50kΩ pull-up to supply voltage selected by gpio17_vio)
T2[31]	GPIO17 Open-Drain Output Select: Relevant only when pin configured as output. 0 : Push-pull output 1 : Open-drain output
T2[32]	GPIO17 I/O Voltage Select: For both input buffer and push-pull output driver. 0 : VOUT2 (FB2) 1 : VOUT1 (FB1)
T2[33]	VREF Output Disable: 0 : VREF = 0.5 x VOUT1(FB1) 1 : VREF output disabled

OTP Register Mapping (Bank T3)

Trim Bits	Parametric Trim
T3[1:0]	Device I/O Configuration and Control: 00 : Individual regulator enable via pins 01 : reserved 10 : Master enable control with programmable sequencing 11 : Master enable control with programmable sequencing + SLEEP mode support
T3[2]	TSD & UVLO Fault Disable: Used for device characterization and burn-in only. 0 : Fault event shuts down all Buck regulators (programmed sequence) 1 : Fault ignored
T3[5:3]	Buck Power-On Sequence Selection: Relevant only when mode[1:0]≠'00' 000 : wait → Buck2 → Buck1 001 : Buck2 → Buck1 → wait 010 : Buck2 → wait → Buck1 011 : Buck1 → Buck2 → wait 100 : wait → Buck1 → Buck2 101 : Buck1 → wait → Buck2 110 : Buck2 → Buck1 111 : Buck1 & Buck2 → wait
T3[6]	Buck1 SLEEP Mode Support: Relevant only when mode[1:0]='11' 0 : Buck1 not affected by SLEEP mode 1 : Buck1 supports SLEEP mode control

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T3[7]	reserved
T3[8]	Buck2 SLEEP Mode Support: Relevant only when mode[1:0]='11' 0 : Buck2 not affected by SLEEP mode 1 : Buck2 supports SLEEP mode control

Trim Bits	Parametric Trim	
T3[10:9]	Power-On Sequencer Delay 1: Relevant only when mode[1:0]≠'00' 00 : 0.5ms 01 : 1ms 10 : 2ms 11 : 4ms	
T3[12:11]	Power-On Sequencer Delay 2: Relevant only when mode[1:0]≠'00' 00 : 0.5ms 01 : 1ms 10 : 2ms 11 : 4ms	
T3[19:13]	Vout1	000d : 1.800V(vout1) / 3.300V(vout2) 001d : 0.800V 002d : 0.825V 003d : 0.850V : : : : 100d : 3.275V 101d : 3.300V 102d : 3.325V ≥103d : 3.3375V
T3[26:20]	reserved	
T3[33:27]	Vout2	

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APPLICATION INFORMATION

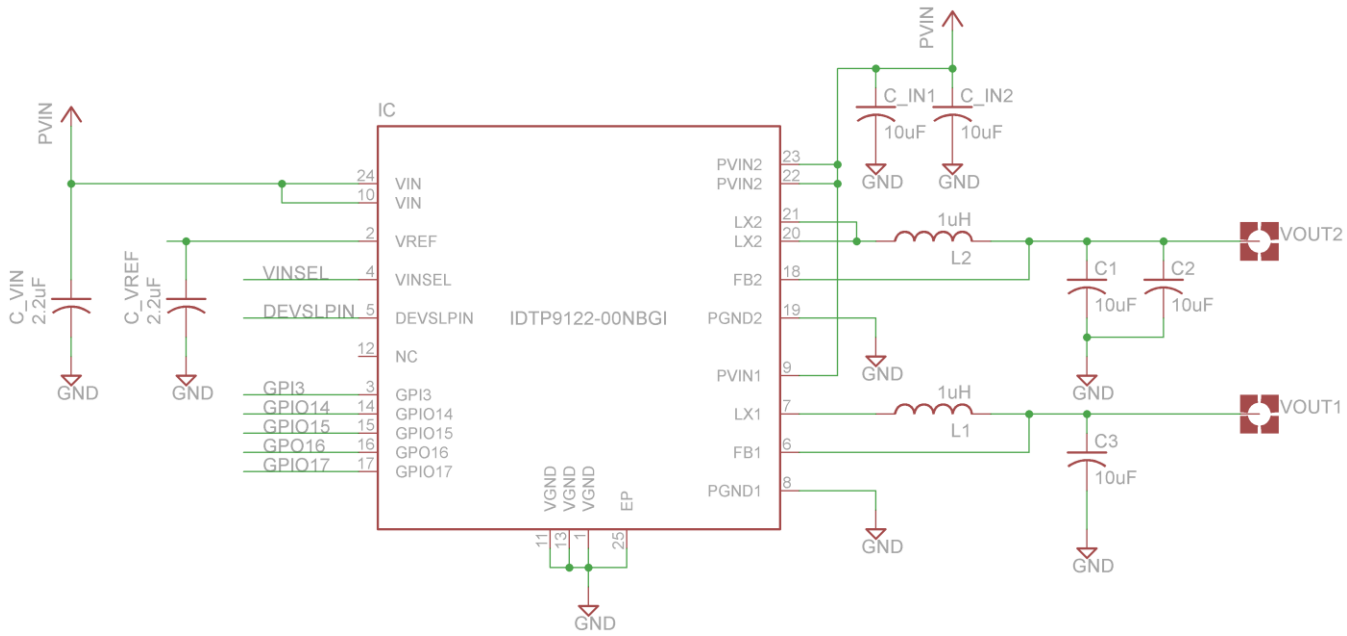


Figure 7. Minimum component schematic of IDTP9122.

Package Information

Please refer to the documents located under http://www.idt.com/package/nbg24 for detailed package outline, recommended footprint, carrier and RoHS information. IDTP9120 is using the P1-NBG24 package option (EP size: 2.8mm)

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