5.5A Distributed Power Unit (DPU)

Advanced Datasheet

IDTP9167

Features

- **Dual supply input:**
  PVIN = 5.6V to 12.6V (main power supply)
  VSYS = 5V (10mA system supply)
- **Output voltage compliance:**
  0.75V to 1.55V
  0.75V to 3.6V (for PVIN = 12V only)
- **Peak output current up to 5.5A**
- **Switching frequency: 2MHz**
- **Support for up to 4 DPUs supplying the same rail**
- **Multiphase output: up to 5 phases configured automatically depending on number of devices**
- **2-wire digital bus interface for device configuration, control and status exchange with host PMIC**
- **-40°C to +85°C operating temperature range**
- **12-ld 4mm x 3mm x 0.85mm DFN package**

Applications

- **Tablet PCs, Notebooks, Embedded systems**

Description

IDTP9167 is a power management device used in conjunction with the IDTP9165 PMIC to either increase the output current capability of existing Buck regulator rails, or implement extra output rails when connected to the PMIC's controller interface. The device works as a controlled current source that supplies current to the load above what the host PMIC can deliver on its own. Up to four IDTP9167s may be used in parallel to provide an additional 22A of peak load current capability.

A high-speed 2-wire digital bus connects the IDTP9165 to the IDTP9167 DPUs to provide control and exchange status information. The device seamlessly integrates into the PMIC eco-system and is transparent from a user point of view.

The IDTP9167 comes in a 4mm x 3mm, 12-ld DFN package. It is guaranteed to operate over the industrial temperature range of -40°C to +85°C.

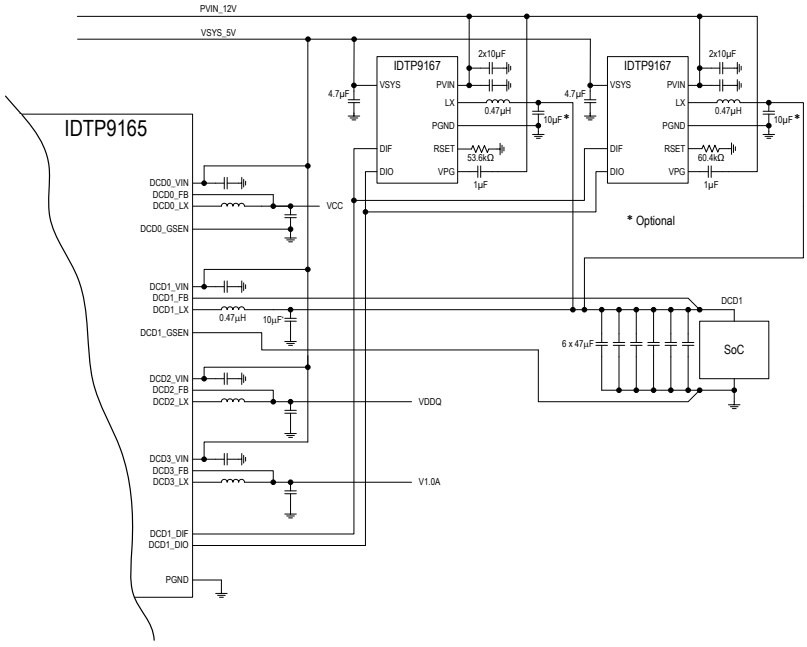


Figure 1 – Typical application circuit including connection to IDTP9165 host PMIC

© 2019 Renesas Electronics Corporation

ABSOLUTE MAXIMUM RATINGS

These absolute maximum ratings are stress ratings only. Stress greater than those listed below may cause permanent damage to the device. Functional operation of the IDTP9167 at absolute maximum ratings is not implied. Exposure to absolute maximum rating conditions for extended periods may affect long-term reliability.

Table 1 – Absolute Maximum Ratings. All voltages are referred to ground, unless otherwise noted.

PINS	MAXIMUM RATING	UNITS
PVIN	-0.3 to 13.2	V
VSYS	-0.3 to 6.0	V
DIF, DIO	-0.3 to 2.2	V
RSET	-0.3 to 6.0	V
VPG	-0.3 < PVIN-VPG < 6.0	V

Table 2 - Package Thermal Information

SYMBOL	DESCRIPTION	RATING	UNITS
θ_{JA}	Thermal Resistance Junction to Ambient	36	°C/W
θ_{JC}	Thermal Resistance Junction to EPAD	7	°C/W
Ψ_{JT}	Junction to Top of Case	10	°C/W
T_J	Junction Temperature	-40 to +125	°C
T_A	Ambient Operating Temperature	-40 to +85	°C
T_{STG}	Storage Temperature	-55 to +150	°C
T_{LEAD}	Lead Temperature (soldering, 10s)	+300	°C

Note 1: The maximum power dissipation is $P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$ where $T_{J(MAX)}$ is 125°C. Exceeding the maximum allowable power dissipation will result in excessive die temperature, and the device will enter thermal shutdown.

Note 2: The thermal rating is calculated based on a JEDEC standard 4-layer board with dimensions 101 mm x 101 mm in still air conditions with 2 oz. copper on the all four layers, 10 thermal Vias at 889 µm pitch, 508 µm drills connecting the EPAD, and an extended PCB pad of 760 µm.

Note 3: Actual thermal resistance is affected by PCB size, solder joint quality, layer count, copper thickness, air flow, altitude, and other unlisted variables.

Table 3 – Absolute Maximum Ratings

SYMBOL	PARAMETER	RATING	UNIT
ESD Rating	(HBM) Human Body Model	±2000	V
	(CDM) Charge Device Model (all pins)	±500	

© 2019 Renesas Electronics Corporation

ELECTRICAL CHARACTERISTICS

V_{PVIN} = 8V, V_{SYS} = 5V, V_O = 1V, L = 0.47µH, C_{OUT} = 2 x 47µF, C_{PVIN} = 2 x 10µF, C_{VSYS} = 4.7µF, C_{VPG} = 1.0µF, T_A = 25°C, unless otherwise noted.

Table 4 – Electrical Characteristics

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{PVIN}	PVIN supply voltage range	PVIN must be greater than VSYS by 0.6V at all times, including during start-up and shut-down supply sequencing	5.6		12.6	V
V_{SYS}	VSYS supply input		4.5		5.5	V
V_{PG}	High-side LDO output voltage	PVIN ≥ VSYS + 0.5V		PVIN - VSYS		V
$I_{SHDN(PVIN)}$	PVIN shutdown current	VSYS = 0V or DIO = 0V		1	2	µA
$I_{SHDN(VSYS)}$	VSYS shutdown current	DIO = 0V			1	µA
$I_{Q(PVIN)}$	PVIN quiescent current	Standby mode: DIO = high, DIF = low		3	5	µA
		Idle mode: DIO = high, DIF = active LX not switching		200	275	µA
$I_{Q(VSYS)}$	VSYS quiescent current	Standby mode: DIO = high, DIF = low		100	150	µA
		Idle mode: DIO = high, DIF = active LX not switching		300	375	µA
$I_{OP(PVIN)}$	PVIN operating supply current	Active mode, switching, no load		8	18	mA
$I_{OP(VSYS)}$	VSYS operating supply current	Active mode, switching, no load		6	10	mA
I_{OUT}	Continuous output current	T_J < 115°C, Efficiency = 80% (GBD)			3.5	A
I_{PULSE}	Maximum pulse load current	Pulse duration < 1ms Pulse duty-cycle < 0.1%		5.5		A
$R_{(on)}$	High side switch			100	150	mΩ
	Low side switch			35	55	mΩ
f_{SW}	Switching frequency	Set by half of DIF input frequency		0.5 x f_{DIF}		MHz
I_{LIM}	LX peak current limit	Occurs at max DIF duty-cycle of 83%		5.9		A
T_{SD}	Thermal shutdown temperature	(GBD)	127	135		°C

© 2019 Renesas Electronics Corporation

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Digital I/O Characteristics (Informative)						
V_{IL}	Low level input voltage			0.65		V
V_{IH}	High level input voltage			1.15		V
V_{OL}	DIO output low voltage	At I_{OL} = 12mA (open-drain output)			0.3	V
t_{DG}	Input deglitch time			4		ns
f_{DIF}	DIF input frequency range		3.7	4.0	4.2	MHz
dt_{DIF}	DIF duty-cycle range	Internally limited	17		83	%
t_{ST}	Device start-up time	From DIO assertion			200	µs
D_{MAX}	Maximum distance from host to furthest DPU device	C_{TRACE} < 80pF		2		ft

© 2019 Renesas Electronics Corporation

PIN CONFIGURATION

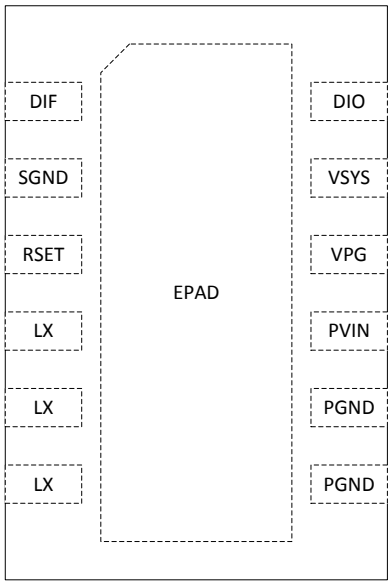


Figure 2 – IDTP9167 DFN-12 Pinout (top view; 4mm x 3mm x 0.85mm; 0.5mm pitch)

© 2019 Renesas Electronics Corporation

PIN DESCRIPTION

Table 5 – 12-Id DFN Pin Functions by Pin Number

NUMBER	LABEL	TYPE	DESCRIPTION
1	DIF	I	Digital interface to the host PMIC: 1.8V logic input
2	SGND	A	DIF/DIO signal ground reference: Connect directly to ground plane
3	RSET	A	RSET resistor connection: Connect to device identification resistor
4	LX	A	Switching node inductor connection: Connect to either 0.47µH or 1µH inductor depending on application
5			
6			
7	PGND	A	Device ground: Connect pins to EPAD ground connection directly below the device
8			
9	PVIN	A	Main supply input: Connect 2x10µF capacitors directly between PVIN & PGND pins (no Via) Capacitor may be connected to ground plane instead when PVIN supply plane is stacked adjacent to the ground plane. Use at least 4 Vias for each capacitor connection.
10	VPG	A	High-side Regulator output capacitor connection: Connect 1.0µF capacitor directly between VPG & PVIN pin (no Via)
11	VSYS	A	5V system supply input: Connect 4.7µF capacitor directly between VSYS & PGND pins (no Via)
12	DIO	IO	Digital interface to the host PMIC: Bi-directional 1.8V logic input & open-drain output
13	EPAD	A	Thermal ground: At least 10 Vias should be used to connect the EPAD to the ground plane directly below the device

© 2019 Renesas Electronics Corporation

THEORY OF OPERATION

OVERVIEW

The IDTP9167 is a 2MHz switching regulator operating as a controlled current-source. The IDTP9167 is used to increase the output current capability of the host PMIC's integrated Buck regulator rails. It is also used by the host PMIC to implement additional Buck outputs when connected to the PMIC's integrated controllers. The device communicates with the host PMIC via a proprietary 2-wire digital bus composed of the DIO and DIF signals. Up to four devices can be connected to the bus to provide an additional 22A of output current capability to the voltage rail. A device identification resistor connected to the RSET pin is used by each DPU to set the device ID which determines the switching phase of the particular device. During device start-up, a 12µA current source is applied to the RSET pin. The voltage generated by the resistor is measured by the DPU and decoded to extract the ID information. For the case when the DPUs are connected to the host PMIC's integrated controller, the same ID setting must be used for all devices in order to support PFM mode operation. In this configuration, multi-phase operation is not available since all DPUs switch at the same time.

Multiple DPUs combined with the host PMIC have the ability to activate and shed phases seamlessly while continuously supplying the desired current to the load. Phase-shedding is not supported when the DPUs are connected to the PMIC's integrated controller.

Other abilities of the IDTP9167 include current limit control and thermal shutdown.

DIO/DIF INTERFACE DESCRIPTION

General

The DIO and DIF bus attaches the host PMIC to up to four IDTP9167 DPUs to provide control and exchange status information. A dedicated DIO/DIF pair is utilized for each output rail. The DIO signal is primarily used to convey configuration information and provide handshake between the host and the DPUs. It also serves as the device master enable as well as the ON/OFF control for individual phases. The DIF signal provides timing and synchronization for DIO data as well as controls the output current of the DPUs through duty-cycle modulation. The LX switching frequency is derived from the DIF clock frequency. When the voltage rail is switched-off, the DIF signal is low and inactive. When the rail is switched-on and one or more DPUs are active and switching, the DIF clock runs at 4MHz. In idle condition, when the voltage rail is still enabled but all DPUs have been phase-shed, the DIF clock lowers to 1MHz frequency to save power while maintaining synchronization which is required to support immediate phase activation during a load step. To ensure robust operation in the presence of noise, interference and ground bounce, error correction circuitry is employed to ignore glitches, runt pulses, and invalid phase and duty-cycle presented at the DIF input.

Initialization

During initialization, the host first asserts the DIO signal to enable the DPUs. The individual DPUs then starts up and immediately reads the connected R_{SET} resistor value to determine its phase ID. The host PMIC then queries the bus to determine the number of DPUs attached, and individual DPUs respond with their respective IDs. For robustness, the query process is repeated to confirm consistent response from all DPUs. Once the host has determined the number of DPUs present, the information is broadcast to all DPUs so individual DPUs can configure their phasing appropriately. The phases are distributed evenly across the entire switching period. If more than one DPU have the same phase ID, then the host will treat them as a single DPU, and those phases will be synchronous.

© 2019 Renesas Electronics Corporation

DIF Signal Integrity Calibration

Depending on the number of DPUs attached, the host automatically configures its DIO and DIF I/O drivers to provide the best signal quality. Varying line capacitance can change the rise and fall times of the DIF clock pulses and distort the perceived duty-cycle of the signal, which represents the output current. To minimize this distortion, the DIF channel is calibrated at start-up and re-calibrated whenever possible to ensure the control transfer function is maintained in each of the DPUs across all bus loading conditions. As a result, the individual DPUs could be located away from the host PMIC, virtually anywhere on the board where space and thermal dissipation allows.

PHASE ACTIVATION AND PHASE SHEDDING CONTROL

Individual DPU phases are automatically shut off sequentially, starting with the highest ID first, as load current demand decreases. When load demand returns, all phases will be switched-on at the same time to minimize the output voltage droop due to the load step. Both current and time hysteresis are built into the phase activation/shedding decision circuitry in the host PMIC to ensure stable operation. Phase activation and phase shedding control is achieved by specific pulse detection on the DIO line. Phase-shedding is not supported when the DPUs are connected to the host PMIC's integrated controller.

PFM MODE SUPPORT

When the IDTP9167 DPUs are connected to an existing Buck regulator rail of the IDTP9165, PFM mode operation is provided by the power stage on board the IDTP9165, and occurs at light load after all DPU phases have been shed.

When the DPUs are used in conjunction with the IDTP9165 PMIC's integrated controller, PFM mode operation is serviced by the DPUs themselves. During PFM operation, the DPUs burst on and off concurrently at intervals controlled by the host PMIC's controller to maintain output voltage level.

THERMAL SHUTDOWN

Thermal shutdown occurs when die temperature exceeds 135°C. Once Thermal Shutdown occurs, the particular DPU will permanently be disabled until the output voltage rail is power-cycled. Until then, the host PMIC's integrated power stage and remaining DPUs will have to absorb the extra load current. Thermal Shutdown on an individual DPU will not affect the output voltage rail unless the host PMIC over-heats and shuts down as well, or if only one DPU is used in conjunction with the PMIC's integrated controller.

© 2019 Renesas Electronics Corporation

TYPICAL PERFORMANCE CHARACTERISTICS

V_{PVIN} = 8V, V_{SYS} = 5V, V_{OUT} = 1V, C_{OUT} = 3 x 47µF per phase, L = 0.47µH, T_A = 25°C.

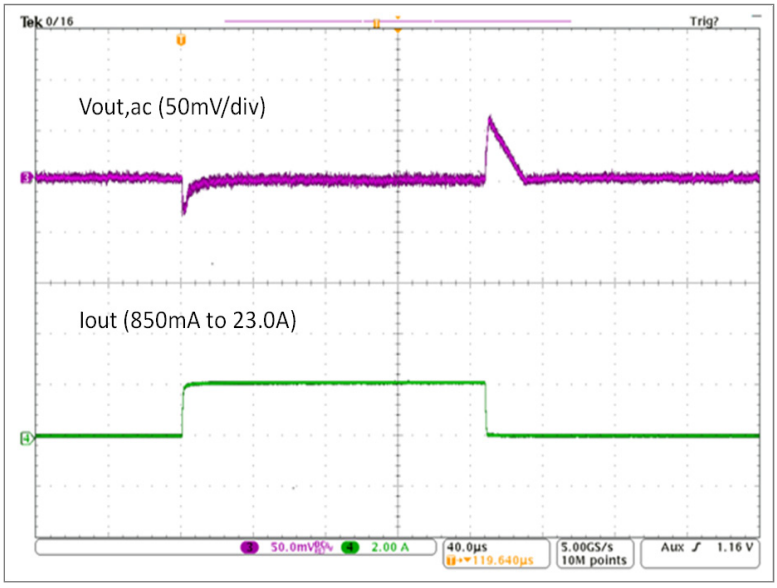


Figure 3 – 4 x IDTP9167 load step: 850mA to 23A transient, 3% undershoot

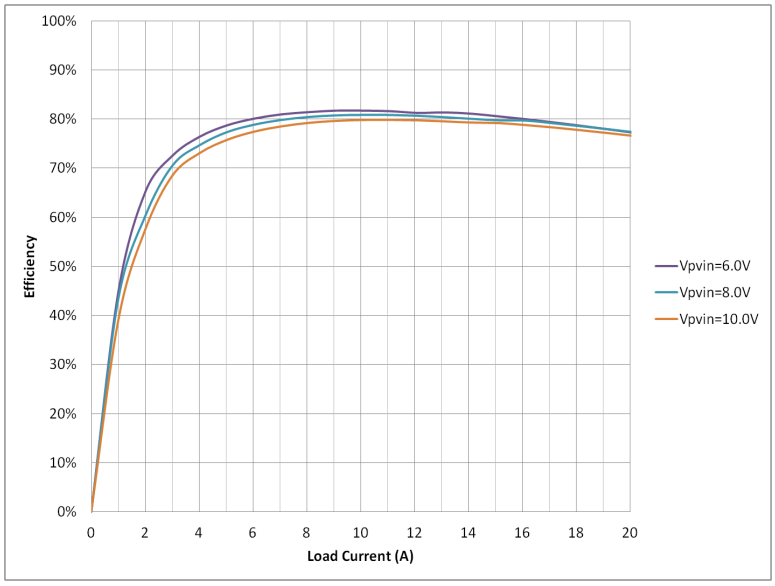


Figure 4 – 3 x IDTP9167 Efficiency: I_{LOAD} = 1A to 20A

© 2019 Renesas Electronics Corporation

APPLICATION

Typical Application Diagram

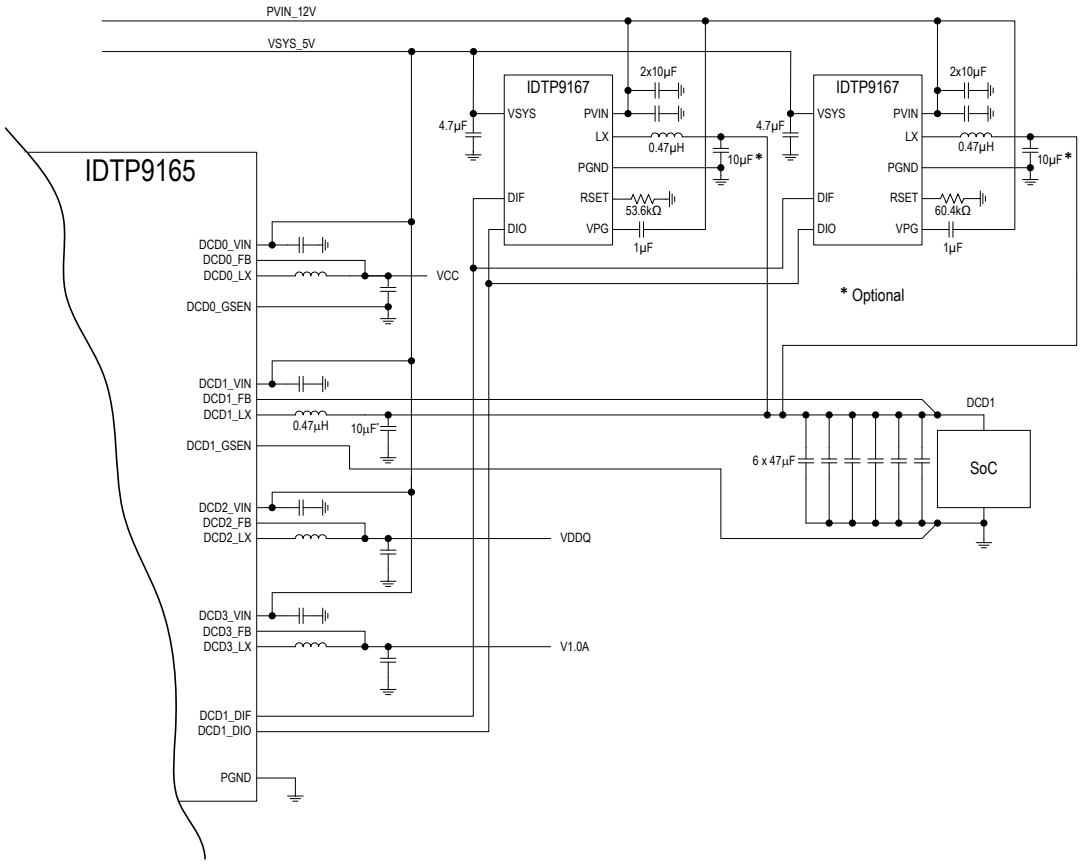
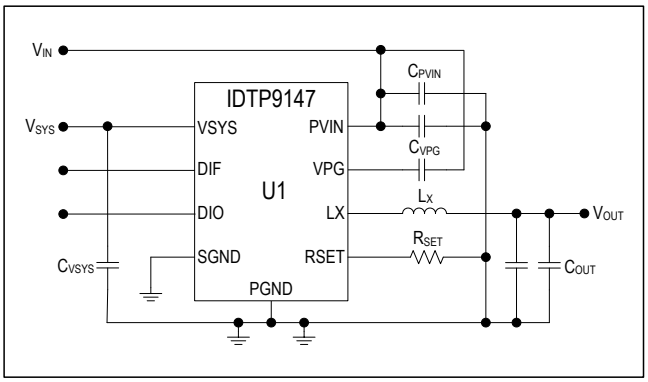


Figure 5 – Typical application diagram showing two IDTP9167s connected as DPUs to augment the output current capability of the IDTP9165 PMIC's VNN rail.

In Figure 5, the 10µF capacitor placed next to the inductor of each DPU may be omitted if board space is limited, and the main output capacitor cluster is within approximately 2 inches away. The inductance value of the LX inductor connected to the DPUs may need to be 1µH in some applications as listed in Table 7. The R_{SET} resistor value of each DPU is dependent on the phase of the particular DPU, and whether the DPU is connected to a controller on the host PMIC, as shown in Table 8.

© 2019 Renesas Electronics Corporation

Bill of Material



Item #	Qty	Ref Design	Value	Description	Manufacturer	Part #
1	2	C_{PVIN}	10µF	CAP: 10µF, ±10%, 25V, X7R,1206, 3.2x1.6x1.6mm	TDK	C3216X7R1E106K
2	1	C_{VPG}	1µF	CAP: 1µF, ±10%, 10V, X7R, 0603, 1.6x0.8x0.8mm	TDK	C1608X7R1A105K
3	1	C_{VSYS}	4.7µF	CAP: 4.7µF, ±10%, 10V, X7R, 0805, 2.00x1.25x0.85mm	TDK	C2012X7R1A475K
4	2	C_{OUT}	47µF	CAP: 47µF, ±10%, 6.3V, X7R, 1210, 3.2x2.5x2.5mm	Murata	GRM32ER70J476KE20
5	1	L_X (A)	0.47µH	INDUCTOR: 0.47µH, ±20%, 6.5A, SMD, 4.0X4.0X1.2mm	Toko	FDSD0412-H-R47M
		L_X (B)	1µH	INDUCTOR: 1µH, ±20%, 5.3A, SMD, 4.0X4.0X1.5mm	Toko	FDSD0415-H-1R0M
6	1	R_{SET}	Varies	RES: ±1%, 0.1W, SMD	Any	
7	1	U1	IDTP9147	IDTP9147	IDT	IDTP9147NRGI

Table 6 – Bill of Material

© 2019 Renesas Electronics Corporation

DESIGN OF COMPONENTS

Suggested Components

Depending on the expected input and output voltage requirement for the application, the recommended inductor and output capacitor values are provided in Table 7. These component values will nominally provide the best stability and transient response. It is recommended that the 47μF output capacitors for all DPUs be clustered together at the point-of-load where the feedback connection is, with the optional 10μF capacitor placed next to the DPU's inductor to absorb ripple current.

V_O (V)	PVIN (V)	L (μH)	C_O (μF)
3.3	12 ± 10%	1.0	10 + 2 x 47
< 2V	5.6 to 12.6	0.47	10 + 2 x 47

Table 7 – Recommended component values

Component Selection

If deviation from the recommended components is desired to further optimize the regulator response for a specific application, guidelines are provided in the following section to aid in the component selection process.

Inductor – L

L is the inductor connected to the switch node of the IDTP9167. The inductor physical size selection should consider its temperature rise and current saturation for the expected operating conditions. The maximum current through the inductor is typically 5.9A. The inductor value chosen should take into account ripple current consideration which can affect peak current handling capability, efficiency and board EMI performance.

The inductor ripple current can be calculated from the following equation:

$$\Delta I_L = 0.5 \times \frac{V_{IN} - V_{OUT}}{L} \times \frac{V_{OUT}}{V_{IN}}$$

where: L (μH) = Inductor value
V_{IN} (V) = Input voltage
V_{OUT} (V) = Output voltage
ΔI_L (A) = Inductor current ripple

For typical application as described in the EC table, the ripple current equates to 931mA(pp).
For an inductor current limit specification of 5.9A, this translates to a maximum load current capability of 5.44A.

© 2019 Renesas Electronics Corporation

Power input capacitor – C_{PVIN}

C_{PVIN} is the power input bypass capacitor. As with any switching regulator, this capacitor can supply high transient currents. The ripple current and ripple voltage can be calculated for the appropriate capacitor using the following approximate equation:

$$I_{RMS} = I_{OUT} \times \sqrt{Vout/Vin}$$

The voltage ripple across the input capacitor is given by:

$$V_{PP} = Vout/Vin \times I_{OUT} \times \left(R_{ESR} + \frac{1 - Vout/Vin}{C_{PVIN} \times F_{SW}}\right)$$

For typical application as described in the EC table, assuming maximum load current of 5.5A, the ripple current through the capacitor equates to I_{RMS} = 1.95A. When the recommended 2 x 10μF PVIN capacitor is used, the voltage ripple is calculated to be 22mV_{PP} assuming effective capacitor ESR of 10mΩ. This calculation excludes the effect of series inductance in the capacitor and the PCB trace leading to it. In actual application, the PVIN voltage spikes caused by this inductance way exceed the calculated ripple voltage. Therefore, it is recommended that two 10μF capacitors be used instead of a single 22μF. Additionally, it is recommended that 25V capacitors be used for reliability.

Output capacitor – C_{OUT}

The output capacitor temporarily supplies the transient load current as well as provides regulator stability. For stability, the minimum C_{OUT} should be around 100uF per phase, and this should provide reasonable load step response. This value can be increased to reduce the voltage droop due to load transients but with diminishing effect. The capacitance may be provided from the load device's supply bypass capacitor bank, depending upon a few considerations. In general, for regulator stability, the feedback should be taken across the output capacitor C_{OUT}. For most systems, the host PMIC's Buck regulator feedback and ground-sense signals will be connected at the load device's power supply pins and ground connections points respectively, where usually the supply capacitor bank is also placed. As long as there is at least 94μF per DPU of total capacitance in the bank, the local C_{OUT} at each DPU may be removed. In the case of a distributed power system where individual DPUs are widely separated on the PCB or far away from the load device, it is recommended to have an additional 10μF ceramic capacitor placed locally at the V_{OUT} side of the inductor connection of each DPU. This local capacitor will absorb some of the inductor ripple current, reducing EMI effects in the PCB trace connecting V_{OUT} to the load device.

VPG bypass capacitor – C_{VPG}

This is the decoupling capacitor for the internal 5V VSYS-tracking high-side LDO which supplies the high-side switch driving circuitry, and is connected between the PVIN and VPG pins. A 10V 1μF ceramic capacitor should be used. The voltage dependency of the capacitor, which can vary with case size, should be such that the de-rated capacitance should be at least 0.8μF when 5V is across it.

VSYS bypass capacitor – C_{VSYS}

This is the input bypass capacitor for the 5V VSYS supply input which powers the low-side switch driving circuitry as well as all biasing and control circuitry in the device. It is connected between the VSYS and PGND pins. A 10V 4.7μF ceramic capacitor is recommended.

© 2019 Renesas Electronics Corporation

ID setting resistor – R_{SET}

The R_{SET} resistor is used to configure the IDTP9167 with an individual identifier (ID). The identifier makes sure each device can be correctly addressed by the host PMIC. Except for the case when the DPUs are connected to the host PMIC's controller, the device ID should be assigned in an ascending order starting with ID0. This ID assignment determines the switching phase position of the particular DPU and, when set appropriately, ensures the output ripple is minimized as the switching phases of all attached DPUs are automatically distributed uniformly in time. With respect to the output ripple, this effectively scales up the equivalent switching frequency by the number of DPUs present.

When the DPUs are connected to the host PMIC's controller, all DPUs must be assigned the same ID value for PFM mode to operate. When one to three DPUs are used, ID0 should be selected as the common ID. When four DPUs are used, ID3 should be selected. It should be noted that when one or more DPUs are set to an identical ID using the same R_{SET} resistor value, the advantage of phase spreading (multi-phase) is lost since DPUs with identical ID will switch at the same time.

The R_{SET} resistor value to device ID mapping is shown in Table 8.

R_{SET} [kΩ]	ID
53.6	0
60.4	1
66.5	2
73.2	3

Table 8 – Recommended R_{SET} values

© 2019 Renesas Electronics Corporation

PCB LAYOUT CONSIDERATIONS

DIO, DIF Communication lines

The DIO and DIF signals transition at a controlled edge rate of typically 8ns with a driving impedance of 70Ω. In most applications, these lines do not need to be treated as transmissions lines, but it is recommended to use trace widths for Z_0 of around 70Ω for optimum signal integrity. In the case when DPUs are widely distributed (e.g. at the 4 corners of the load device), avoid branching or using star-connection on DIO & DIF lines as this may cause signal degradation due to unnecessary reflections at branch points.

C_{OUT} Placement

All C_{OUT} capacitors should be clustered together and placed as close to the load device as possible. The feedback voltage and ground sense lines of the host PMIC should be connected across the load capacitor bank.

For optimum device performance, the following guidelines should be observed. Please contact IDT for Gerber files that contain the recommended board layout.

- The C_{VSYS} & C_{VPG} decoupling capacitors should be mounted on the component side of the board, close to their respective pins. It is recommended not to use Vias between the decoupling capacitors and their pins and to keep their PCB traces as short as possible. Due to the high switching currents possible and the high input voltage range, the C_{PVIN} mounting inductance should be less than the C_{PVIN} capacitor's ESL, which is around 1nH. This can be accomplished by placing C_{PVIN} as shown in the ***Recommended Board Layout***, using only top layer route to connect to the PVIN and PGND pins, minimizing inductance in the PVIN-PGND loop.
- If the PVIN plane or the ground plane is not the top layer, then Vias can be used outside of the PVIN-PGND loop to connect the IDPT9167 to those planes. For the PVIN connection, the average input current for typical operating conditions is:

  $$\boldsymbol{Iin_{avg}} < 0.85A$$

  Since the C_{PVIN} capacitor case size can easily allow a 4-Via connection, this should be used. For the PGND connection, the average input current for the typical conditions is:

  $$\boldsymbol{Iin_{avg}} < 4.76A$$

  This requires more Vias. The number of Vias connecting the PGND and EPAD to the ground plane should be maximized for thermal consideration. It is recommended that at least 10 Vias are used for this connection for typical application.
- The DFN-12 package has an inner thermal pad which requires blind assembly. It is recommended that a more active flux solder paste be used such as the Alpha OM-350 solder paste from Cookson Electronics (http://www.cooksonsemi.com). Please contact IDT for Gerber files that contain recommended solder stencil design.
- The package center exposed pad (EPAD) must be reliably soldered directly to the PCB. The center land pad on the PCB (set 1:1 with EPAD) must also be tied to the board ground plane, primarily to maximize thermal performance in the application. The ground connection is best achieved using a matrix of plated-through-hole (PTH) Vias embedded in the PCB center land pad. The PTH Vias perform as thermal conduits to the ground plane (thermally, a heat spreader) as well as to the solder side of the board. Recommendations for the Via finished hole-size and array pitch are 0.3mm to 0.33mm and 1.3mm, respectively.

© 2019 Renesas Electronics Corporation

- The PCB design and layout can have a significant influence on the power dissipation capabilities of power management ICs. This is due to the fact that the surface mount packages used with these devices rely heavily on thermally conductive traces and planes to transfer heat away from the package. The following general guidelines will be helpful in designing a board layout for low thermal resistance:

    1. PC board traces with large cross sectional areas have higher thermal conductivity. If possible, a 2 oz copper ground plane with ample thermal Vias connecting to the EPAD of the IDTP9167 is recommended.
    2. Do not use solder mask or place silkscreen on the heat-dissipating traces/pads, as they increase the net thermal resistance of the mounted IC package.

Recommended Board Layout

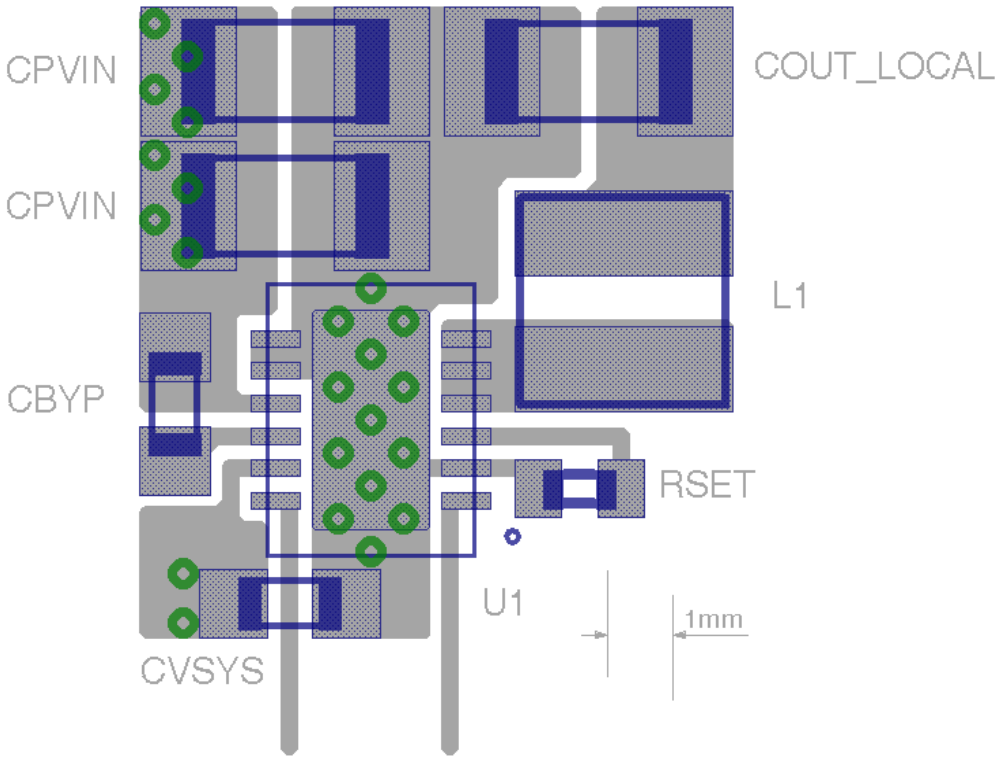


Figure 6 – Recommended board layout of one DPU

© 2019 Renesas Electronics Corporation

Power Dissipation/Thermal Requirements

In addition to layout techniques described in the previous section, placement of the IDTP9167 DPUs with respect to proximity to other heat generating devices should be considered as well. System dependent considerations such as thermal mounting, airflow, heat sinking and convection surfaces will affect the final power dissipation limit of the IDTP9167 in application. The main PCB factors influencing θ_{JA} (in the order of decreasing influence) are the number of copper layers, the number of thermal Vias connecting the device EPAD to the ground plane, and the ground plane thickness.

The maximum power dissipation for a given situation can be calculated from:

$$P_{D(MAX)} = \frac{(T_{J(MAX)} - T_A)}{\theta_{JA}}$$

where: $P_{D(MAX)}$ = Maximum Power Dissipation (W)
θ_{JA} = Package Thermal Resistance (°C/W)
$T_{J(MAX)}$ = Maximum Device Junction Temperature (°C)
T_A = Ambient Temperature (°C)

The maximum operating junction temperature ($T_{J(MAX)}$) of the IDTP9167 device is 125°C. The thermal resistance of the DFN-12 package is optimally θ_{JA}=36°C/W. Operation is specified for maximum ambient temperature (T_A) of 85°C. Therefore, the maximum power dissipation is:

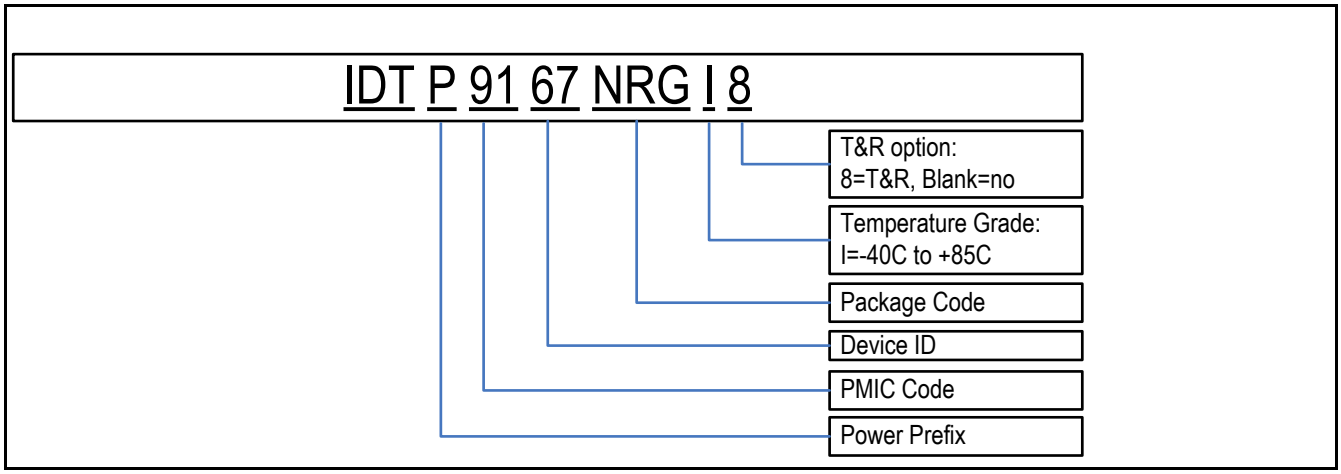
$$\boldsymbol{P_{D(MAX)} = \frac{(125°C - 85°C)}{36°C/W} = 1.1W}$$

© 2019 Renesas Electronics Corporation

ORDERING GUIDE

Table 9 – Ordering Summary

PART NUMBER	MARKING	PACKAGE[1]	AMBIENT TEMP. RANGE	SHIPPING CARRIER	QUANTITY
P9167NRGI8	P9167NRGI	NRG12, T&R	-40°C to +85°C	Tape and Reel	4000



[1] NRG12: 12ld-4x3 DFN, Please refer to http://www.idt.com/package/nrg12 for detailed package information.

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers skilled in the art designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only for development of an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising out of your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Rev.1.0 Mar 2020)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:
www.renesas.com/contact/

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.

© 2020 Renesas Electronics Corporation. All rights reserved.