Description

The P9235A-RB is a highly integrated, magnetic induction, wireless power transmitter supporting up to 5W of total wireless system power with in-band, bi-directional data communication requiring no additional circuitry. The P9235A-RB offers a pre-programmed bootloader that must be used in conjunction with an external flash memory that contains control firmware. This architecture allows the user to change the firmware in the external flash to meet application-specific requirements. Renesas also provides firmware to implement standard WPC coil configurations, such as the A11a addendum.

The P9235A-RB includes an industry-leading 32-bit ARM® Cortex®-M0 processor offering a high level of programmability while consuming extremely low standby power. The transmitter features two open-drain LED outputs with pre-defined blinking patterns and five general-purpose input/output (GPIO) pins. The GPIOs can be firmware-defined for functions such as setting the current limit, setting FOD limits, driving additional coils, or sounding a buzzer, which supports a wide range of applications. The I2C serial communication allows the user to read information such as voltage, current, frequency, and fault conditions.

The P9235A-RB includes an under-voltage lockout and thermal management circuit to safeguard the device under fault conditions. Together with the P9225-R receiver (R_X), the P9235A-RB forms a complete 5W wireless power system solution with bi-directional data communication.

The P9235A-RB is available in a Pb-free, space-saving 5 × 5 mm 40-VFQFPN package. The product is rated over an operating temperature range of -40ºC to +85ºC.

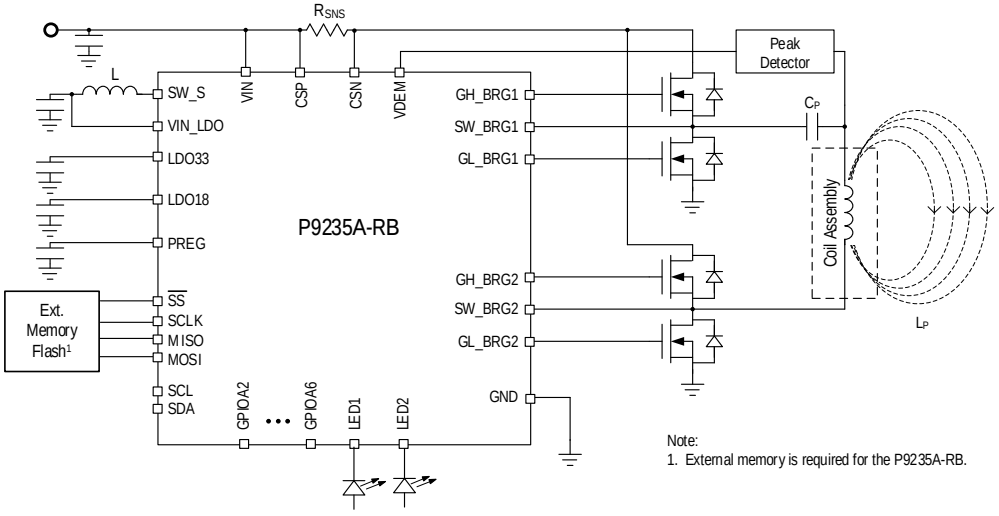
Features

- Power transfer up to 5W
- Wide input voltage range: 4.25V to 21V
- WPC compatible
- Integrated step-down switching regulator
- Embedded 32-bit ARM® Cortex®-M0 processor (trademark of ARM, Ltd.)
- Integrated drivers for external power FETs
- Supports bi-directional data communication
- Simultaneous voltage and current demodulation scheme for robust communication
- Integrated current sense amplifier
- Low standby power
- Dedicated remote temperature sensing
- Two LED outputs that can indicate power transfer and fault conditions
- Foreign object detection (FOD)
- Active-low enable pin for electrical on/off
- Over-current and over-temperature protection
- Supports I2C interface
- SPI interface to access external flash memory
- -40 to +85°C ambient operating temperature range
- 40-VFQFPN, 5 × 5 mm RoHS-compliant package

Typical Applications

- Smart Watches
- Headsets
- Health and Fitness Monitors
- Portable Medical Applications

Application Diagram



Note:
1. External memory is required for the P9235A-RB.

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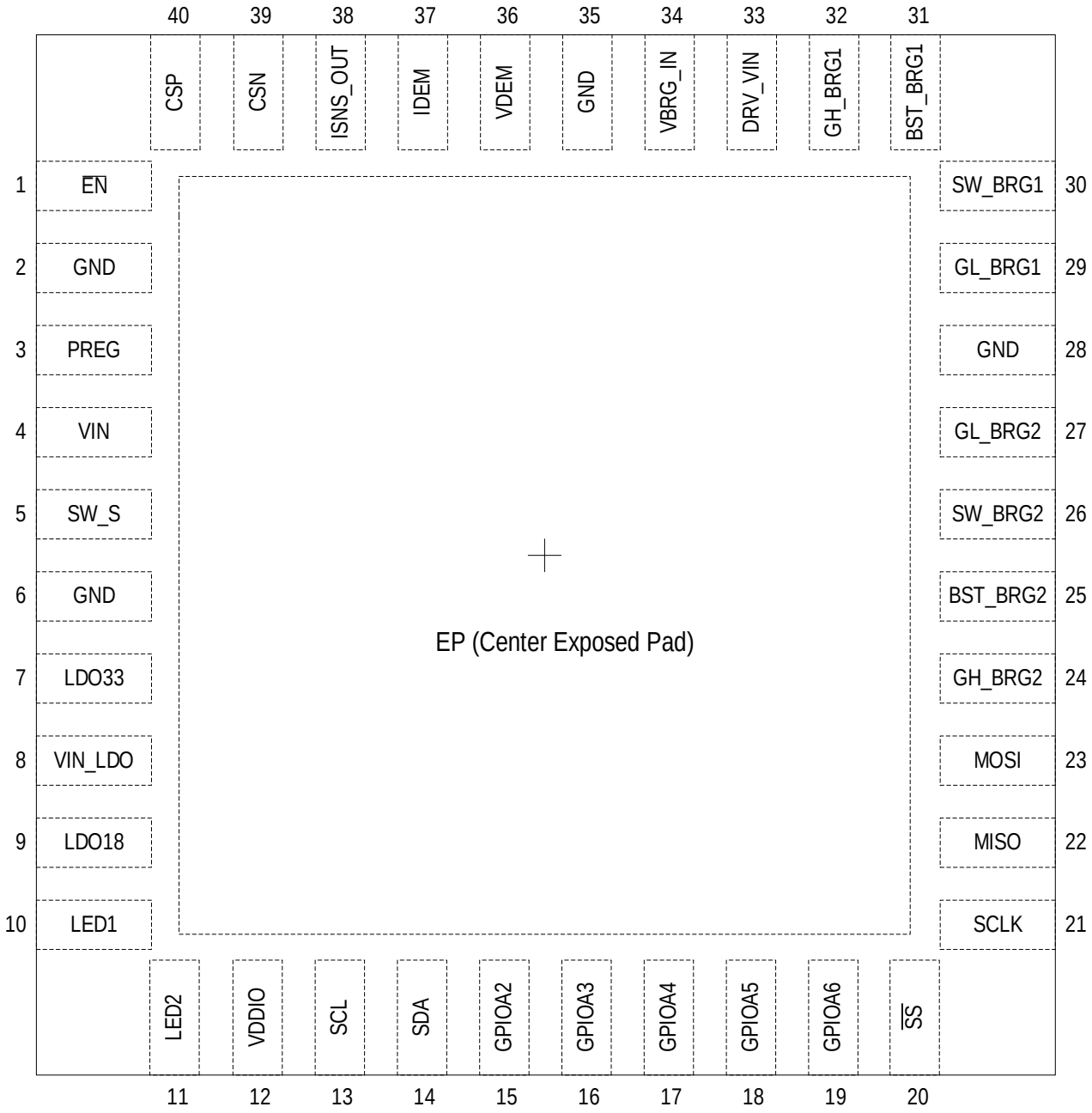
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1. Pin Information

1.1 Pin Assignments

Figure 1. Pin Assignments – Top View



1.2 Pin Descriptions

Table 1. Pin Descriptions

Pin Number	Name	Type	Description
1	$\overline{EN}$	Input	Active low enable pin. When connected to logic high, the device shuts down and consumes less than 25µA of current. When connected to logic low, the device is in normal operation.
2	GND	–	Ground connection.
3	PREG	Output	Regulated output voltage used for the internal device biasing. Connect a 1µF capacitor from this pin to ground. This pin should not be externally loaded.
4	VIN	Input	Input power supply. Connect a 10µF capacitor in parallel with a 0.1µF capacitor from this pin to ground.
5	SW_S	Output	Step-down regulator switch node. Connect one of the terminals of a 4.7µH inductor to this pin and connect the other inductor terminal to the output capacitors and the VIN_LDO pin 8.
6	GND	–	Ground connection.
7	LDO33	Output	Regulated 3.3V output voltage used for internal device biasing. Connect a 1µF capacitor from this pin to ground. This pin should not be externally loaded.
8	VIN_LDO	Input	Low dropout input power supply. Connect this pin to a 5V source, either to the output of the 5V output step-down regulator or to the input power supply pin, VIN.
9	LDO18	Output	Regulated 1.8V output voltage used for internal device biasing. Connect a 1µF capacitor from this pin to ground. This pin should not be externally loaded.
10	LED1	Output	Open-drain output pin. Connect an LED to this pin.
11	LED2	Output	Open-drain output pin. Connect an LED to this pin.
12	VDDIO	Input	Input power supply for internal biasing. This pin must be connected to LDO33.
13	SCL	Input	Serial clock line; open-drain pin. Connect a 5.1kΩ pull-up resistor to the LDO33 rail.
14	SDA	Input/Output	Serial data line; open-drain pin. Connect a 5.1kΩ pull-up resistor to the LDO33 rail.
15	GPIOA2	Input/Output	General purpose input and output pin.
16	GPIOA3	Input/Output	General purpose input and output pin.
17	GPIOA4	Input/Output	General purpose input and output pin.
18	GPIOA5	Input/Output	General purpose input and output pin.
19	GPIOA6	Input/Output	General purpose input and output pin.
20	$\overline{SS}$	Output	Slave select (active-low, output from master). This pin and the SCLK, MISO, and MOSI pins are used by the master P9235A-RB to access the slave external memory via the SPI interface; see section 5.7.
21	SCLK	Output	Serial clock (output from master).
22	MISO	Input	Master input, slave output (output from slave).
23	MOSI	Output	Master output, slave input (output from master).
24	GH_BRG2	Output	Gate driver output for the high-side half bridge 2.

Pin Number	Name	Type	Description
25	BST_BRG2	Input	Bootstrap pin for the half bridge 2. Connect an external capacitor from this pin to the SW_BRG2 pin to generate a drive voltage, which is higher than the input voltage.
26	SW_BRG2	Output	Switch node for half bridge 2.
27	GL_BRG2	Output	Gate driver output for the low-side half bridge 2.
28	GND	–	Ground return connection for half bridge 1 and half bridge 2 external FETs and associated components.
29	GL_BRG1	Output	Gate driver output for the low-side half bridge 1.
30	SW_BRG1	Output	Switch node for half bridge 1.
31	BST_BRG1	Input	Bootstrap pin for half bridge 1. Connect an external capacitor from this pin to the SW_BRG1 pin to generate a drive voltage higher than the input voltage.
32	GH_BRG1	Output	Gate driver output for the high-side half bridge 1.
33	DRV_VIN	Input	Input power supply for the internal gate drivers. Connect a 10µF capacitor from this pin to ground.
34	VBRG_IN	Input	Bridge voltage input voltage sense.
35	GND	–	Ground connection.
36	VDEM	Input	High-pass filter input. Voltage demodulation pin for data packets based on coil voltage variation; transmitted by power receiver.
37	IDEM	Input	High-pass input filter. Current demodulation pin for data packets based on coil current variation; transmitted by power receiver.
38	ISNS_OUT	Output	Differential (CSP - CSN) current-sense buffered output.
39	CSN	Input	Low-side input current sense (V_{BRIDGE}).
40	CSP	Input	High-side input current sense (V_{IN}).
	EP	–	Exposed pad. Thermal pad for heat sinking purposes. Connect EP to GND plane.

2. Specifications

2.1 Absolute Maximum Ratings

The absolute maximum ratings are stress ratings only. Stresses greater than those listed below can cause permanent damage to the device. Functional operation of the device at absolute maximum ratings is not implied. Exposure to absolute maximum rating conditions might affect device reliability.

Table 2. Absolute Maximum Ratings Summary[a]

Pins	Rating	Unit
$\overline{EN}$, VIN, SW_S, VBRG_IN, SW_BRG1, SW_BRG2, CSP, CSN, BST_BRG1, BST_BRG2, GH_BRG1, GH_BRG2	-0.3 to 28	V
PREG, LDO33, VIN_LDO, LED1, LED2, VDDIO, SCL, SDA, GL_BRG1, GL_BRG2, VDEM, IDEM, ISNS_OUT, DRV_VIN, $\overline{SS}$, SCLK, MISO, MOSI, GPIOA2, GPIOA3, GPIOA4, GPIOA5, GPIOA6	-0.3 to 6	V
LDO18	-0.3 to 2	V

[a] All voltages are referred to ground.

2.2 Thermal Characteristics

Table 3. Package Thermal Characteristics

Symbol	Description	QFN Rating	Unit
θ_{JA}	Thermal Resistance Junction to Ambient [a][b][c]	28.5	°C/W
θ_{JC}	Thermal Resistance Junction to Case [b][c]	21.87	°C/W
θ_{JB}	Thermal Resistance Junction to Board [b][c]	1.27	°C/W
T_J	Operating Junction Temperature [a][b]	-40 to +125	°C
T_A	Ambient Operating Temperature [a][b]	-40 to +85	°C
T_{STG}	Storage Temperature	-55 to +150	°C
T_{LEAD}	Lead Temperature (soldering, 10s)	+300	°C

[a] The maximum power dissipation is $P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$ where $T_{J(MAX)}$ is 85°C. Exceeding the maximum allowable power dissipation will result in excessive die temperature, and the device will enter thermal shutdown.

[b] This thermal rating was calculated on JEDEC 51 standard 4-layer board with dimensions 3" x 4.5" in still air conditions.

[c] Actual thermal resistance is affected by PCB size, solder joint quality, layer count, copper thickness, air flow, altitude, and other unlisted variables.

Table 4. ESD Information

Test Model	Pins	Ratings	Unit
HBM	All pins.	±2000	V
CDM	All pins.	±500	V

2.3 Electrical Characteristics

Table 5. Electrical Characteristics

Note: V_{IN} = 5V, $\overline{EN}$ = LOW, T_{AMB} = -40°C to +85°C, unless otherwise noted. Typical values are at 25°C.

Symbol	Description	Conditions	Minimum	Typical	Maximum	Unit
Input Supplies and UVLO						
V_{IN}	Input Operating Range[a]		4.25		21	V
V_{IN_UVLO}	Under-Voltage Lockout	V_{IN} rising		4.0		V
V_{IN_UVHYS}	Under-Voltage Hysteresis	V_{IN} falling		0.5		V
I_{IN}	Operating Mode Input Current	Power-transfer phase, Vin = 12V		10		mA
I_{STD_BY}	Standby Mode Current	Periodic ping		1		mA
I_{SHD}	Shut-Down Current	$\overline{EN}$ = V_{IN} = 21V		25	80	µA
Enable Pin Threshold ($\overline{EN}$)						
V_{IH}	Input Threshold HIGH		2.5			V
V_{IL}	Input Threshold LOW				0.5	V
I_{EN_LKG}	$\overline{EN}$ Pin Input Leakage Current	V_{EN} = 0V	-1		1	µA
		V_{EN} = 5V		2.5		µA
Step-Down Regulator[b] with C_{OUT} = 33µF; L = 4.7µH						
V_{OUT}	Step-Down Output Voltage	Vin = 12V	4.5	5	5.5	V
N-Channel MOSFET Drivers						
$t_{LS_ON_OFF}$	Low-Side Gate Driver Rise and Fall Times	C_{LOAD}= 3nF; 10% to 90%, 90% to 10%		50	150	ns
$t_{HS_ON_OFF}$	High-Side Gate Driver Rise and Fall Times	C_{LOAD} = 3nF; 10% to 90%, 90% to 10%		150	300	ns
Input Current Sense						
V_{SEN_OFST}	Amplifier Output Offset Voltage	Measured at the ISNS_OUT pin; V_{CSP} = V_{CSN}		0.6		V
$ISEN_{ACC_TYP}$	Measured Current Sense Accuracy[c]	V_{R_ISEN} = 25mV, I = 1.25A		±3.5		%
Analog to Digital Converter						
N	Resolution			12		Bit
Channel	Number of Channels			10		
$V_{IN,FS}$	Full Scale Input Voltage			2.4		V

Symbol	Description	Conditions	Minimum	Typical	Maximum	Unit
LDO18[b]						
V_{LDO18}	1.8V LDO Regulator	C_{OUT} = 1µF, V_{VIN_LDO} = 5.5V	1.71	1.8	1.89	V
LDO33[b]						
V_{LDO33}	3.3V LDO Regulator	C_{OUT} = 1µF, V_{VIN_LDO} = 5.5V	3.15	3.3	3.45	V
PREG						
V_{PREG}	5V LDO Regulator			5		V
Thermal Shutdown						
T_{SD}	Thermal Shutdown	Threshold rising		140		˚C
		Threshold falling		120		˚C
General Purpose Input/Output (GPIO), $\overline{SS}$, SCLK, MISO, and MOSI Current Leakage						
I_{LKG}	Leakage Current		-1		1	µA
Output Logic Levels for Open-Drain Pins (LED1, LED2, SCL, SDA)						
V_{OH}	Output Logic HIGH		4			V
V_{OL}	Output Logic LOW	I = 8mA			0.5	V
General Purpose Input/Output (GPIO), $\overline{SS}$, SCLK, MISO, and MOSI Logic Levels						
V_{IH}	Input Voltage HIGH Level		0.7 × V_{DDIO}			V
V_{IL}	Input Voltage LOW Level				0.3 × V_{DDIO}	V
I_{LKG}	Leakage Current				1	µA
V_{OH}	Output Logic HIGH	I = 8mA, V_{DDIO} = 3.3V	2.4			V
V_{OL}	Output Logic LOW	I = 8mA, V_{DDIO} = 3.3V			0.5	V
I2C Interface (SCL, SDA)						
f_{SCL_SLV}	Clock Frequency	As I2C slave			400	kHz
C_B	Capacitive Load	For each bus line			100	pF
C_{BIN}	SCL, SDA Input Capacitance			5		pF
I_{LKG}	Input Leakage Current	V = GND and 3.3V	-1		1	µA

[a] The input voltage operating range is dependent upon the type of transmitter power stage (full-bridge, half-bridge) and transmitting coil inductance. WPC specifications should be consulted for appropriate input voltage ranges by end-product type.

[b] Do not externally load. For internal biasing only.

[c] A 20mΩ, 1% or better sense resistor and a 4.7Ω, 1% input filter resistor are required to meet the FOD specification.

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3. Typical Performance Characteristics

Figure 2. P9235A-RB TX with 5V Input Supply and P9225-R RX Total System Efficiency Characteristics

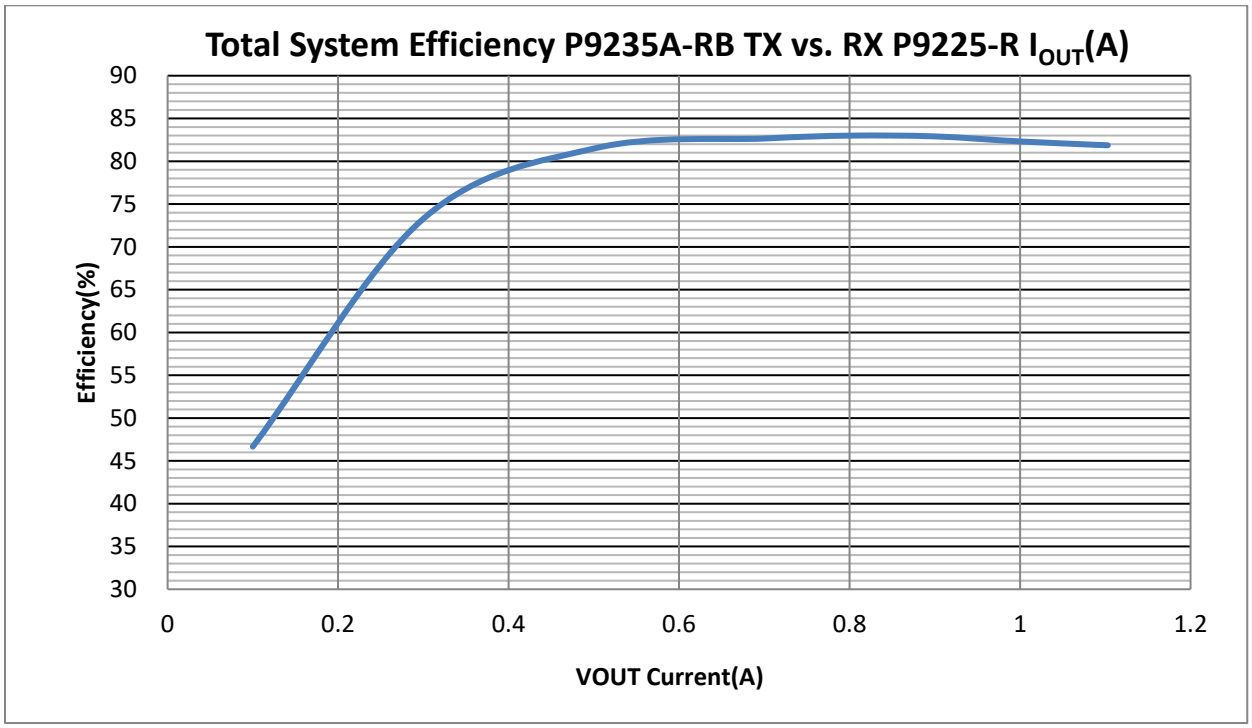
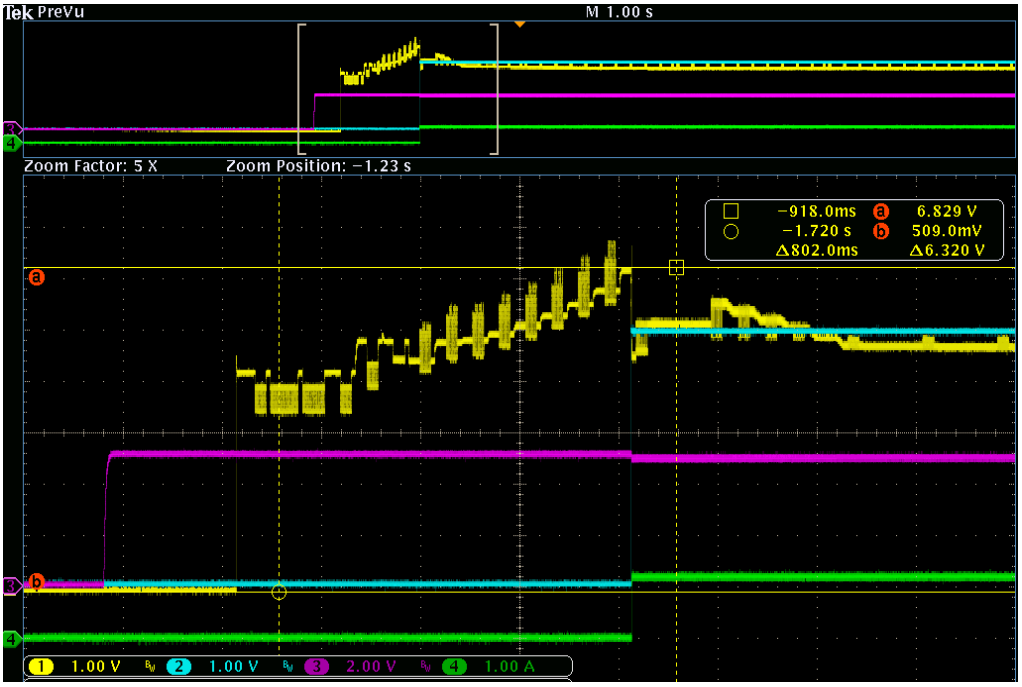
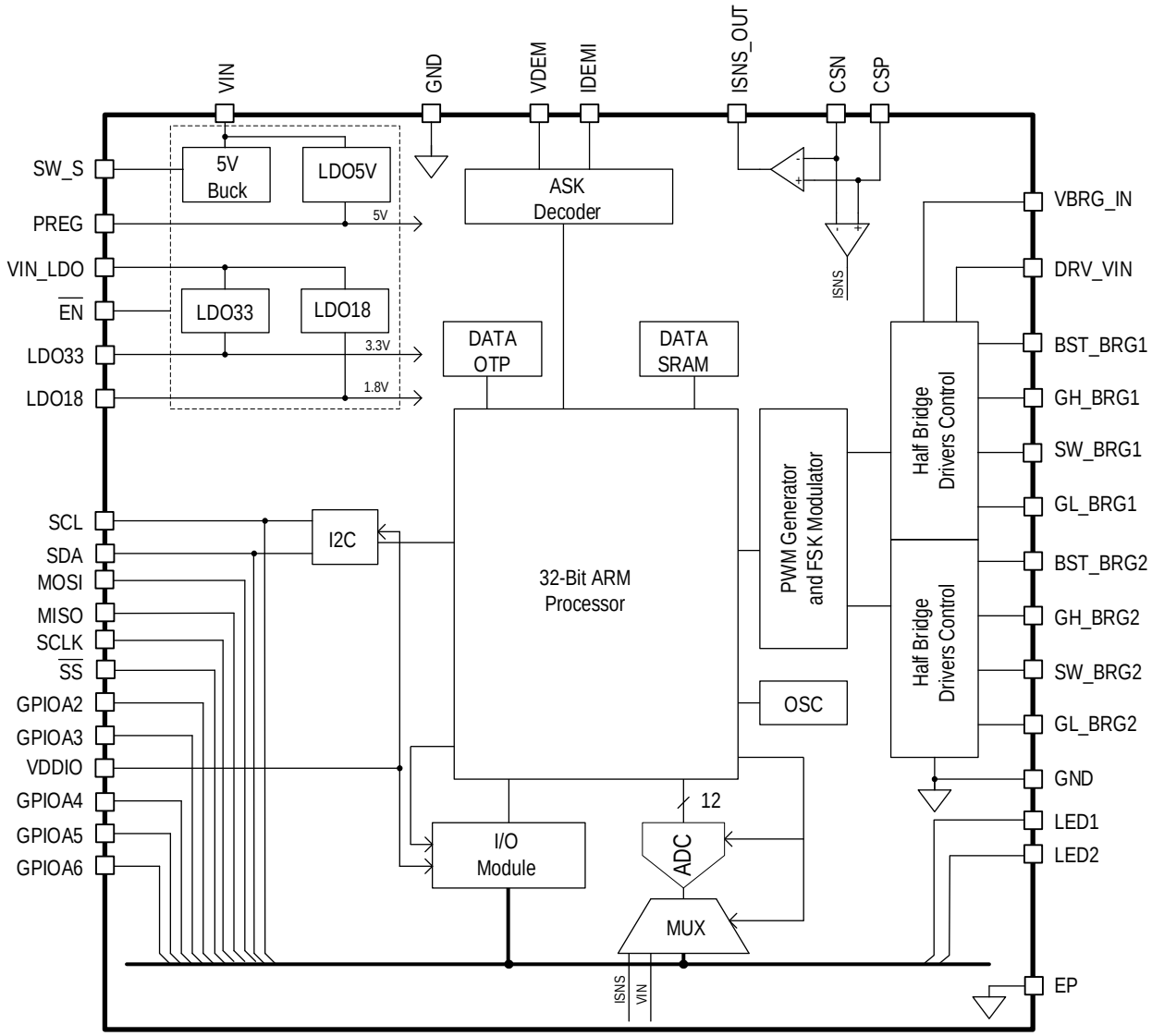


Figure 3. P9235A-RB TX and P9225-R RX Startup Waveform into 1.2A Load Current (IOUT) with 5V Input & 1.2A Load Current (IOUT)



4. Block Diagram



5. Theory of Operation

A wireless power charging system has a base station with one or more transmitters that make power available via DC-to-AC inverter(s) and transmit the power over a strongly-coupled inductor pair to a receiver in a mobile device. The amount of power transferred to the mobile device is controlled by the wireless power receiver by sending communication packets to the transmitter to increase, decrease, or maintain the power level. The communication from receiver to transmitter is purely digital and consists of logic 1's and 0's that ride on top of the power link that exists between the transmitter (TX) and receiver (RX) coil. Communication from transmitter to receiver is achieved by frequency shift keying (FSK) modulation over the power signal frequency, and amplitude shift keying (ASK) is used for the communication protocol from receiver to transmitter.

A feature of the wireless charging system is the fact that when it is not delivering power, the transmitter is in Standby Mode. The transmitter remains in Standby Mode and periodically pings until it detects the presence of a receiver. Once a Baseline Power Profile (BPP) receiver is detected, such as the P9222-R, P9225-R, or equivalent, the transmitter will provide up to 5W of output power.

The P9235A-RB contains features that ensure a high level of functionality and compliance with the WPC requirements, such as a power path that efficiently achieves power transfer, a simple and robust communication demodulation circuit, safety and protection circuits, configuration, and status indication circuits.

5.1 Foreign Object Detection

When metallic objects, such as coins, keys, and paperclips, are exposed to alternating magnetic fields, the eddy current flowing through the object will heat it. The amount of heat generated is a function of the amplitude and frequency of the magnetic field, as well as the characteristics of the object, such as resistivity, size, and shape. In any wireless power system, the heat generated by the eddy current manifests itself as a power loss, reducing the overall system efficiency. If appropriate measures are not taken, the heating could lead to unsafe situations.

The foreign object detection is performed during power transfer where the power-loss difference between the received power and transmitted power is constantly measured and compared to the WPC-specified threshold. If the difference is higher than the threshold set by the WPC specification, the P9235A-RB will identify it as an FOD and the system will shut down to avoid over-heating.

5.2 Input Voltage

The P9235A-RB can support an input voltage from 4.5 to 21V. Depending on the reference design and the WPC coil configuration selection, the input voltage will be limited to a range of operating voltages defined by the WPC specification.

5.3 General Purpose Input/Output – GPIO Pins

The P9235A-RB has 5 GPIOs, which can be repurposed in the firmware to do specific functions, such as setting the current limit or FOD limits, driving the additional coils, or sounding a buzzer.

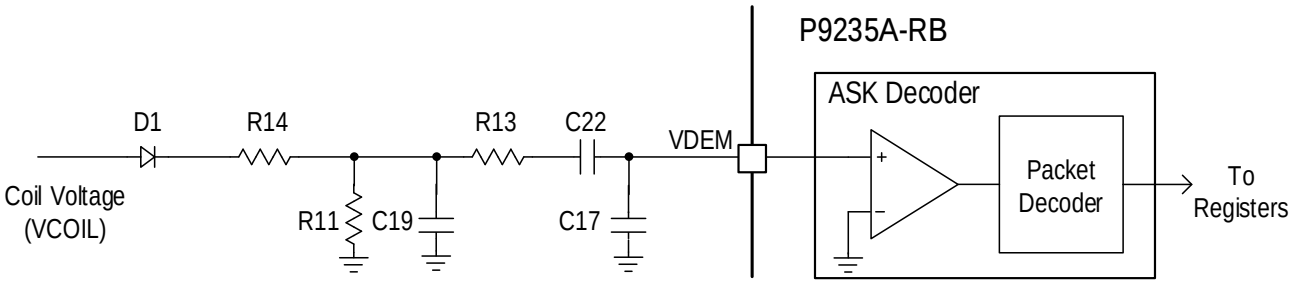
5.4 Enable Pin

The P9235A-RB can be disabled by applying a logic HIGH to the $\overline{EN}$ pin. When the voltage on the $\overline{EN}$ pin is pulled HIGH, operation is suspended and the P9235A-RB is placed in the low-current Shut-Down Mode. If pulled LOW, the P9235A-RB is enabled and active.

5.5 Voltage Demodulation – VDEM

In order to increase the communication reliability in any load condition, the P9235A-RB has integrated two demodulation schemes, one based on coil current information and the other based on coil voltage modulation. The voltage mode envelope detector is implemented using a discrete solution as depicted on Figure 4. This simple implementation achieves the envelope detector function low-pass filter as well as the DC filter function.

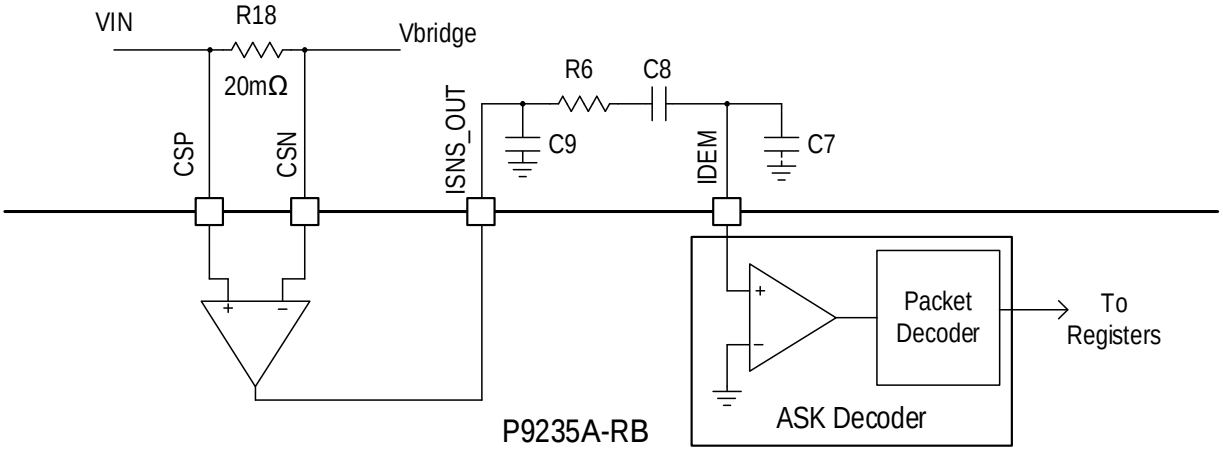
Figure 4. Voltage Mode Envelope Detector



5.6 Current Demodulation – IDEM Pin

The current-mode detector takes the modulation information from the current sense resistor, which carries the coil current modulation information in addition to the averaged input current. An external discrete low-pass filter and DC filter between the ISNS_OUT and IDEM pins provide additional filtering. The packet decoder block is shared between the voltage-mode and current-mode detectors. The packet decoder selects either voltage-mode or current-mode signals depending upon which produces the best demodulated signal.

Figure 5. Current Mode Envelope Detector



5.7 External Memory

The P9235A-RB requires an external flash memory in which firmware must be programmed. Control firmware is programmed into the external flash memory to set operation, control, and FOD parameters. The master P9235A-RB accesses the slave external memory using a standard SPI interface (SCLK, MISO, MOSI, and $\overline{SS}$ pins) to upload the firmware from the flash memory into the P9235A-RB internal SRAM. The W25X20CLUXIG is the recommended external flash memory. Smaller memory sizes can be used depending on the total firmware size.

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5.8 Thermal Protection

The P9235A-RB integrates thermal shutdown circuitry to prevent damage resulting from excessive thermal stress that might be encountered under fault conditions. This circuitry will shut down or reset the P9235A-RB if the die temperature exceeds a threshold to prevent damage resulting from excessive thermal stress that might be encountered under fault conditions. An internal temperature protection block is enabled in the P9235A-RB that monitors the temperature inside the chip. If the die temperature exceeds 140°C, the P9235A-RB shuts down and resumes when the internal temperature drops below 120°C.

5.9 Integrated Step-Down Regulator

The input capacitors must be connected as close as possible between the VIN pin and GND pin. Similarly, the output capacitors must be placed close to the inductor and GND. The output voltage is sensed by the VIN_LDO pin; therefore, the connection from the step-down output (VCC_5V) to the VIN_LDO pin should be made as wide and short as possible to minimize output voltage errors. The step-down regulator is the input voltage to the LDO18 and LDO33 linear regulators and is not recommended for powering an external load.

5.10 Linear Regulators – PREG, LDO33, and LDO18 Pins

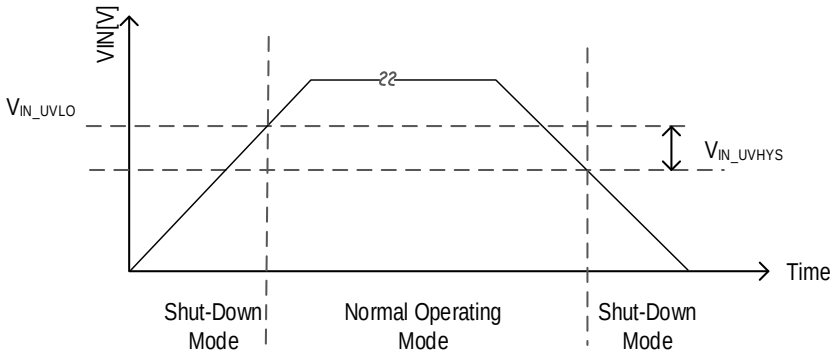
The P9235A-RB has three low-dropout (LDO) regulators used to bias the internal circuitry. The 5V pre-regulator (PREG) provides bias for the entire internal power management. The PREG requires a 1µF ceramic bypass capacitor connected from the PREG pin to GND. This capacitor must be placed very close to the PREG pin. The voltage regulator must not be externally loaded.

The LDO33 and LDO18 are used to bias the internal digital circuit. The regulator's input voltage is supplied through the VIN_LDO pin. Both regulators require a 1µF ceramic capacitor from the pin to GND. The voltage regulators must not be externally loaded.

5.11 Under-Voltage Lock-Out (UVLO) Protection

The P9235A-RB has a 4V (typical, rising) under-voltage lockout circuit on the VIN pin. To guarantee proper functionality, the voltage on the VIN pin must rise above the UVLO threshold. If the input voltage stays below the UVLO threshold, the P9235A-RB is in Shut-Down Mode.

Figure 6. UVLO Threshold Definition



5.12 LC Resonant Circuit

The LC resonant circuit comprises the series primary resonant coil (L_P) and series capacitance (C_P) in the application circuit on page 1. The transmitter coil assembly is vendor specific, and it must comply with the WPC recommendation. The WPC specifications include the self-inductance value, DC resistance (DCR), Q-factor, size, and number of turns.

The P9235A-RB is designed to support various Baseline Power Profile (BPP) coil configurations using half-bridge and full-bridge inverter topologies to drive the primary coil (L_P) and a series capacitance (C_P). Depending on the WPC coil configuration selection, the coil inductance and series capacitance will change. Near resonance, the voltage developed across the C_P series capacitance could reach 70V peak (voltage will change depending on the coil configuration). High-voltage COG-type ceramic capacitors are highly recommended for their AC and DC characteristics and temperature stability. Film-type capacitors can also be used as recommended by Renesas.

6. Communication Interface

6.1 Modulation/Communication

The WPC specification uses two-way communication for power transfer: receiver-to-transmitter and transmitter-to receiver.

Receiver-to-transmitter communication is accomplished by the receiver modulating the load seen by the receiver's coil; the communication is purely digital and logic 1's and 0's carried on the power signal. Modulation is done with amplitude-shift keying (ASK) modulation using with a bit-rate of 2Kbps. To the P9235A-RB transmitter, this appears as an impedance change, which results in measurable variations of the transmitter's coil. The P9235A-RB power transmitter demodulates this variation of the coil current or voltage to receive the packets.

Transmitter-to-receiver communication is accomplished by frequency-shift keying (FSK) modulation over the power signal frequency. The P9235A-RB power transmitter has the capability to modulate FSK data from the power signal frequency and use it in order to establish the handshaking protocol with the power receiver.

The P9235A-RB implements FSK communication when used in conjunction with WPC-compliant receivers, such as the Renesas P9222-R. The FSK communication protocol allows the transmitter to send data to the receiver using the power transfer link in the form of modulating the power transfer signal. This modulation appears in the form of a change in the base operating frequency (f_{OP}) to the modulated operating frequency (f_{MOD}) in periods of 256 consecutive cycles. Equation 1 is used to compute the modulated frequency based on any given operating frequency.

Communication packets are transmitted from transmitter to receiver with less than 1% positive frequency deviation following any receiver-to-transmitter communication packet. The frequency deviation is calculated using Equation 1.

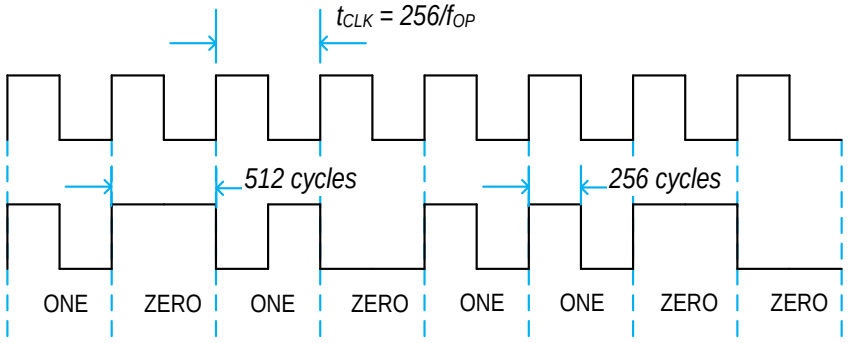
$$f_{MOD} = \frac{60000}{\frac{60000}{f_{OP}} - 3} \text{ [kHz]}$$

Equation 1

Where f_{MOD} is the change in frequency in the power signal frequency; f_{OP} is the base operating frequency of power transfer; and 60000kHz is the frequency of the internal oscillator responsible for counting the period of the power transfer signal.

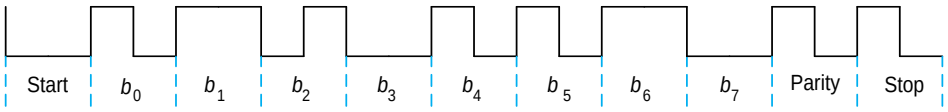
The FSK byte-encoding scheme and packet structure complies with the WPC specification. The FSK communication uses a bi-phase encoding scheme to modulate data bits into the power transfer signal. The start bit will consist of 512 consecutive f_{MOD} cycles (or logic '0'). A logic '1' value will be sent by sending 256 consecutive f_{OP} cycles followed by 256 f_{MOD} cycles or vice versa, and a logic '0' is sent by sending 512 consecutive f_{MOD} or f_{OP} cycles.

Figure 7. Example of Differential Bi-phase Encoding for FSK



Each byte will comply with the start, data, parity, and stop asynchronous serial format structure shown in Figure 8:

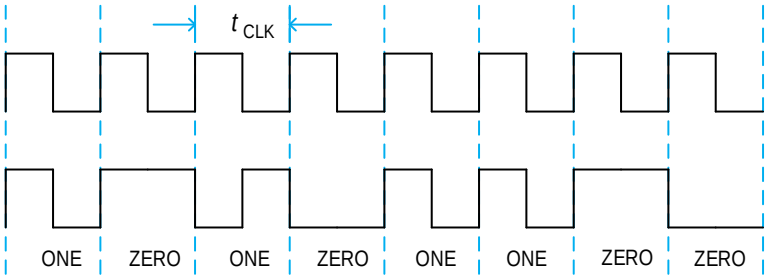
Figure 8. Example of Asynchronous Serial Byte Format for FSK



6.2 Bit Decoding Scheme for ASK

As required by the WPC, the P9235A-RB uses a differential bi-phase coding scheme to demodulate data bits onto the power signal. A clock frequency of 2kHz is used for this purpose. A logic ONE bit is coded using two narrow transitions, whereas a logic ZERO bit is encoded using one wider transition as shown in Figure 9:

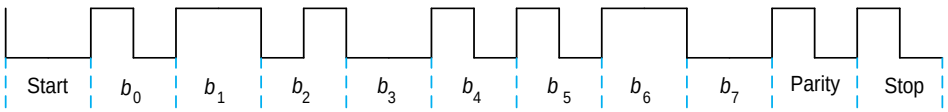
Figure 9. Bit Decoding Scheme



6.3 Byte Decoding for ASK

Each byte in the communication packet comprises 11 bits in an asynchronous serial format, as shown in Figure 10.

Figure 10. Byte Decoding Scheme



Each byte has a start bit, 8 data bits, a parity bit, and a single stop bit.

6.4 Packet Structure

The P9235A-RB communicates with the base station via communication packets. Each communication packet has the following structure:

Figure 11. Communication Packet Structure

Preamble	Header	Message	Checksum

7. Bi-Directional User Data Communication

Note: Only application firmware version 2.17, and higher, will allow Bi-Directional User Data Communication. To download the latest firmware update, visit the P9235A-RB-EVK reference design page.

In customer-end systems, the transmitter and receiver boards must have an external microcontroller (MCU) or leverage an existing on-board application processor to orchestrate bi-directional communication. Using the I2C communication, the MCU on the transmitter board loads the user data into specific registers and triggers the communication. The P9235A-RB sends the data to the P9222-R using frequency shift keying (FSK) modulation. The P9222-R then receives the data and interrupts the MCU on the receiver when the data is ready to be read. The external MCU on the receiver follows the same procedure to send the data to the P9235A-RB using amplitude-shift keying (ASK) modulation. When new data is available to read, the P9235A-RB interrupts the external MCU on the transmitter board.

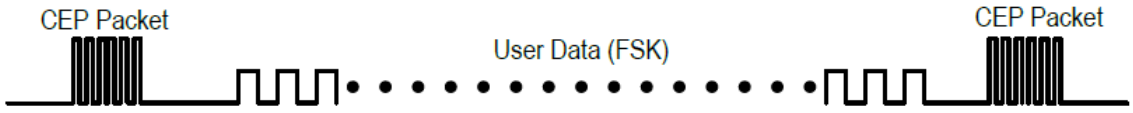
Bi-directional user data communication is enabled only in the power transfer phase. The external MCU on the transmitter board can read the State register to determine whether the P9235A-RB is in the power transfer phase.

7.1 Transferring Data from the P9235A-RB to the P9222-R

The external MCU on the transmitter board should determine the status of the communication channel before initiating a new transfer. The P9235A-RB provides SRAM registers of outgoing user data registers, header register, and communication trigger register (or command register). The external MCU on the transmitter should set communication trigger register after loading the appropriate user data into the header register and outgoing user data register.

The P9235A-RB waits until it receives the Control Error Packet (CEP) from the P9222-R, as the receiver device has the master role within the communication process. Afterwards, the P9235A-RB sends the data into the channel by FSK (Frequency Shift Key) modulation. **Error! Reference source not found.** shows the timing diagram for the user data transfer from the P9235A-RB to the P9222-R.

Figure 12. Timing Diagram for the User Data Transfer from the P9235A-RB to the P9222-R



7.2 Reading Data Sent from the P9222-R

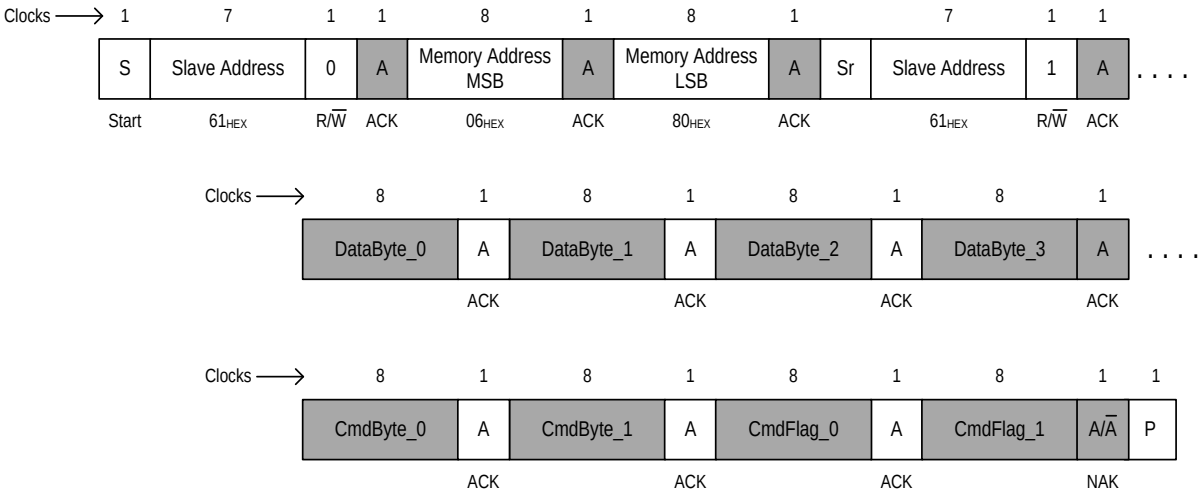
When the P9235A-RB receives data from the P9222-R, the P9235A-RB will generate an interrupt to the external MCU on the transmitter by pulling down the interrupt pin. The MCU can respond to the interrupt and read the received data. After reading the data, the external MCU on the transmitter should clear the interrupt. If the external MCU on the transmitter does not handle interrupts, the MCU should constantly poll the data received flag to check whether there is any new incoming data. If the external MCU on the transmitter does not read data immediately after the interrupt is received, there is a risk that data could become corrupted/overwritten because of next new incoming data. The user can implement a higher-level handshaking protocol between the external MCU on transmitter and receiver to avoid data corruption.

8. I2C Interface

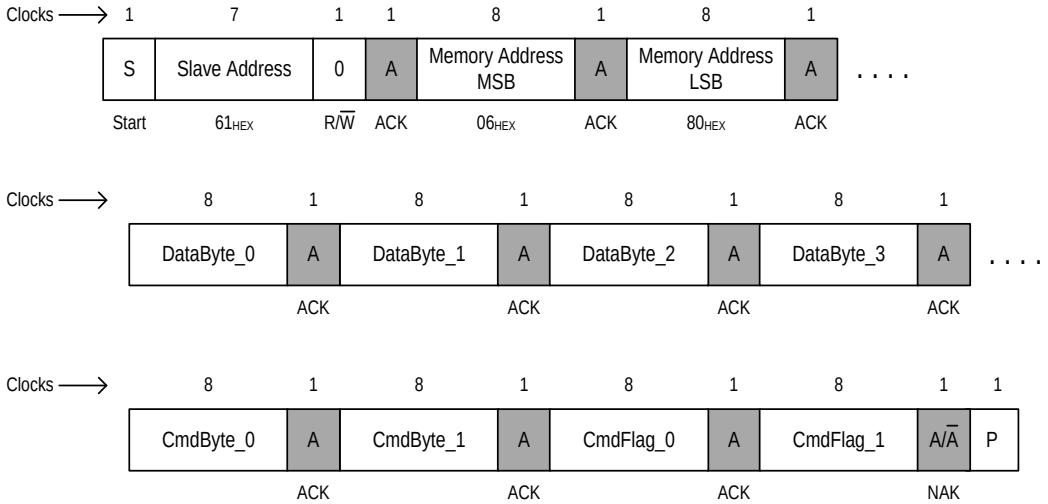
The P9235A-RB supports the standard I2C interface. The default I2C slave address is 0x61. Figure 13 shows the Read and Write protocol structure that the external I2C master must use to communicate with the P9235A-RB.

Figure 13. I2C Access Read Protocol and Write Protocol

Read Protocol



Write Protocol



9. Application Information

9.1 Power Dissipation and Thermal Requirements

The P9235A-RB is offered in a 40-VFQFPN package that has a maximum power dissipation capability of approximately 1.2W. The number of thermal vias between the package and the printed circuit board determines the maximum power dissipation. The maximum power dissipation of the package is limited by the die's specified maximum operating junction temperature, $T_{J(MAX)}$, of 125°C, the maximum ambient operating temperature, T_A, of 85°C, and the package thermal resistance, θ_{JA}. The junction temperature rises when the heat generated by the device's power dissipation flows through the package thermal resistance. The VFQFPN package offers a typical thermal resistance, junction to ambient (θ_{JA}), of 28.5°C/W when the PCB layout guideline and surrounding devices are optimized.

The techniques as noted in the PCB layout section of the *P9235A-RB EVK User Manual* (available on the P9235A-RB-EVK product page) must be followed when designing the printed circuit board layout. Take into consideration possible proximity to other heat-generating devices when placing the P9235A-RB and the bridge FET packages in a given application design. The ambient temperature around the power IC will also have an effect on the thermal limits of an application. The main factors influencing θ_{JA} (in the order of decreasing influence) are PCB characteristics, the size of the thermal pad attached to the die/package (VFQFPN), the thermal vias, and final system hardware construction. Board designers should keep in mind that the package thermal metric θ_{JA} is impacted by the characteristics of the PCB. Changing the design or configuration of the PCB changes the overall thermal resistivity and the board's heat-sinking efficiency.

The use of integrated circuits in low-profile and fine-pitch surface-mount packages requires special attention to power dissipation. Many system-dependent issues, such as thermal coupling, airflow, added heat sinks, convection surfaces, and the presence of other heat-generating components, affect the power-dissipation limits of a given component.

In summary, the three basic approaches for enhancing thermal performance include:

- Improving the power dissipation capability of the PCB design
- Improving the thermal coupling of the component to the PCB
- Introducing airflow into the system

The maximum power dissipation for a given situation should be calculated using Equation 2:

$$P_{D(MAX)} = \frac{(T_{J(MAX)} - T_A)}{\theta_{JA}} \quad \text{Equation 2}$$

Where:

- $P_{D(MAX)}$ = Maximum Power Dissipation
- θ_{JA} = Package Thermal Resistance (°C/W)
- $T_{J(MAX)}$ = Maximum Device Junction Temperature (°C)
- T_A = Ambient Temperature (°C)

The maximum recommended operating junction temperature ($T_{J(MAX)}$) for the P9235A-RB device is 120°C. The thermal resistance of the 40-VFQFPN package is optimally θ_{JA} = 28.5°C/W. Operation is specified to a maximum steady-state ambient temperature (T_A) of 85°C. Therefore, the maximum recommended power dissipation is calculated with Equation 3.

$$P_{D(MAX)} = \frac{(120°C - 85°C)}{28.5°C/W} \cong 1.2W \quad \text{Equation 3}$$

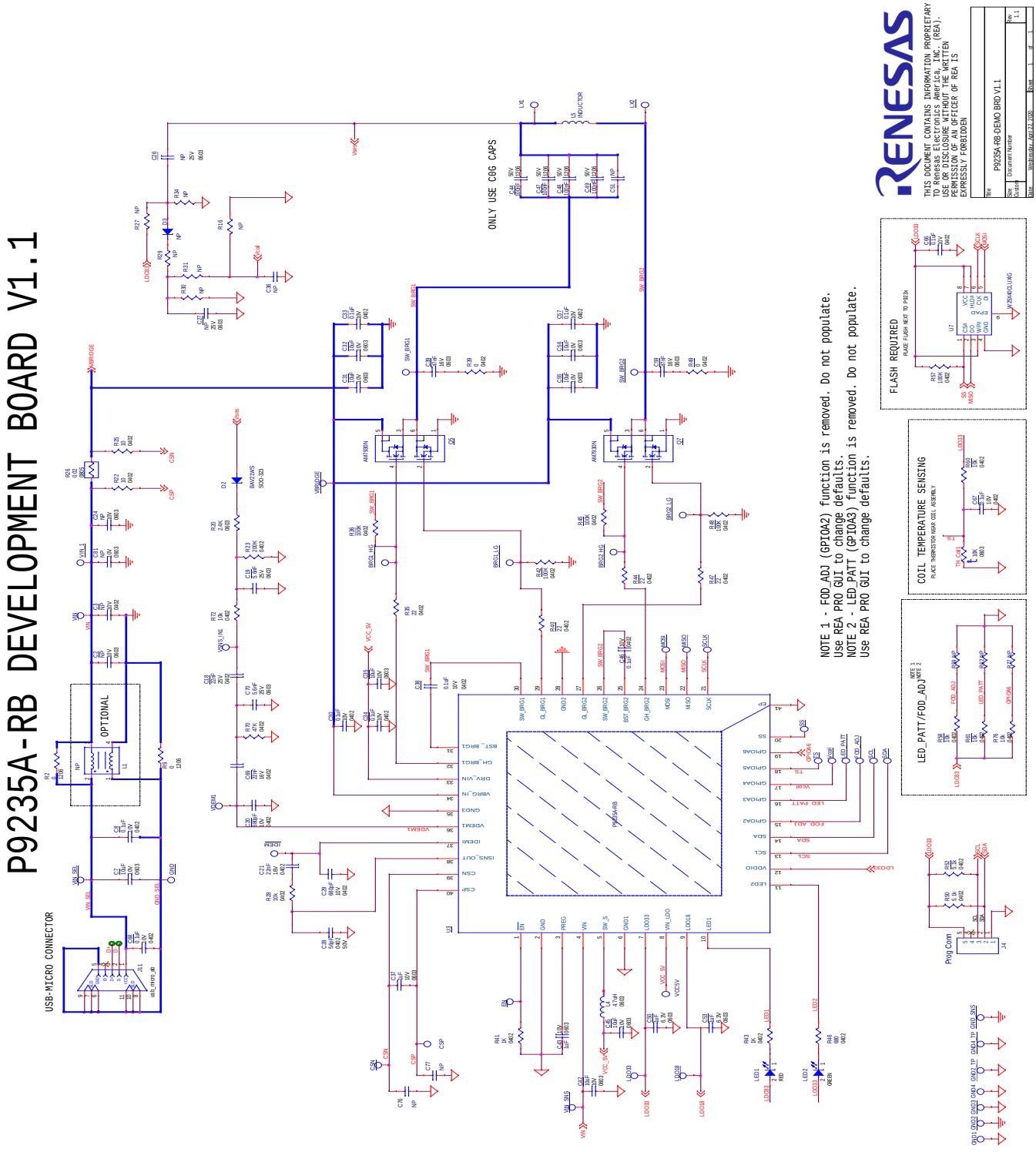
All the previously mentioned thermal resistances are the values found when the P9235A-RB is mounted on a standard board of the dimensions and characteristics specified by the JEDEC 51 standard.

To allow the maximum load current and to prevent thermal overload, the heat generated by the P9235A-RB solution must be dissipated into the PCB. All the available pins must be soldered to the PCB. GND pins (exposed paddle, EP) and bridge FET GND pins should be soldered to the PCB ground plane to improve thermal performance, with multiple vias connected to all layers of the PCB.

9.2 P9235A-RB Evaluation Board v1.1 Schematic

Note: The typical application schematic provides a basic guideline to understanding and building a functional small-power wireless power transmitter type as described in the WPC specifications. Other components not shown on the typical application schematic may be needed in order to comply with other requirements, such as EMC or thermal specifications.

Figure 14. P9235A-RB Typical Application Schematic



10. Package Outline Drawings

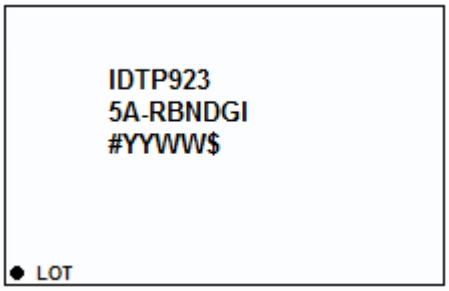
The package outline drawings are located at the end of this document and are accessible from the Renesas website (see package links in Ordering Information). The package information is the most current data available and is subject to change without revision of this document.

11. QFN Package Assembly

Unopened dry packaged parts have a one-year shelf life.

The HIC indicator card for newly opened dry packaged parts should be checked. If there is any moisture content, the parts must be baked for a minimum of 8 hours at 125˚C within 24 hours prior to the assembly reflow process.

12. Marking Diagram



- Line 1: Company name and truncated part number.
- Line 2: 5A-RB is part of the part number indicating a pre-programmed bootloader IC, which is followed by the package code.
- Line 3: “YYWW” is the last two digits of the year and two digits for the work week that the part was assembled. “#” is the device step.“$” denotes the mark code.

13. Ordering Information

Part Number	Description and Package	MSL Rating	Carrier Type	Temp. Range
P9235A-RBNDGI	P9235A-RB Wireless Power Transmitter for 5W Applications with the Programmed Bootloader, 40-VFQFPN, 5 × 5 mm package	MSL1	Tray	-40°C to +85°C
P9235A-RBNDGI8	P9235A-RB Wireless Power Transmitter for 5W Applications with the Programmed Bootloader, 40-VFQFPN, 5 × 5 mm package	MSL1	Reel	-40°C to +85°C

14. Revision History

Revision Date	Description of Change
Nov 9, 2021	▪ Added new sections, “Bi-Directional User Data Communication” and “Application Information” ▪ Updated the package outline drawings; however, no mechanical changes ▪ Completed other minor changes
Mar 8, 2019	Initial release.